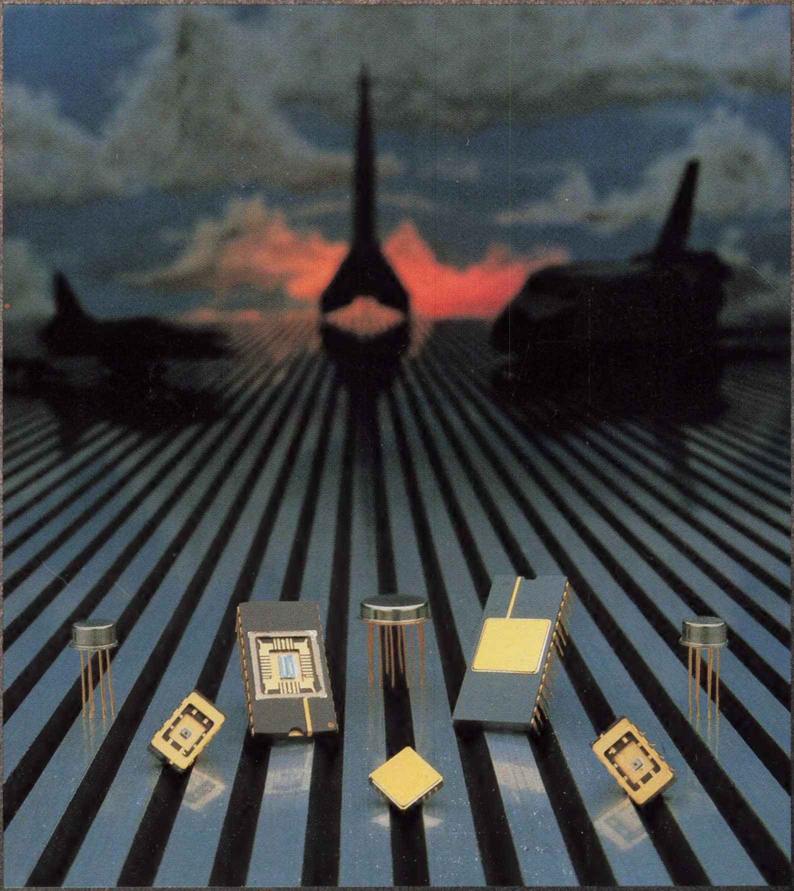

ANALOG
PRODUCT DATA BOOK
MILITARY

HARRIS

Volume 1
$5.00

Harris Semiconductor Military & Aerospace Products

This databook contains detailed technical information on the extensive line of military and aerospace analog products currently available from Harris Semiconductor. Other high reliability products available under the brand names of **GE, RCA** and **Intersil** -- now a part of the **New Harris Semiconductor** -- can be found in the two-volume GE Solid State High-Reliability databook. Volume I contains information on CMOS ICs and Volume II covers Analog ICs and Discrete Devices. In addition, a Harris Semiconductor Digital Military databook will be available Spring 1989.

Harris Linear, Data Acquisition and Telecom Products

Harris Semiconductor's spectrum of analog products meet many specialized requirements ranging from precision to low power to high speed performance. Capitalizing on advanced linear processing technologies developed over the past two decades, Harris Semiconductor offers analog products of high quality and unmatched performance.

This data book describes Harris Semiconductor's military line of Linear, Data Acquisition, and Telecommunication products. In addition, it includes a complete set of data sheets for product specifications; a section of application notes with design details for specific applications of Harris products; and a description of the Harris quality and high reliability program.

If you need more information on these and other Harris products, please contact the nearest Harris sales office listed in the back of this data book, or return the reply card attached inside back cover.

ANALOG

1989 Military Data Book

ALPHA NUMERIC PRODUCT INDEX

ALPHA NUMERIC PRODUCT INDEX (Continued)

Analog Product Listing

Analog-to-Digital Converters

Digital-to Analog Converters

Multiplexers

SINGLE 8/DIFFERENTIAL 4 CHANNEL:

SINGLE 16/DIFFERENTIAL 8 CHANNEL:

4 CHANNEL:

Operational Amplifiers: High Slew Rate

SINGLES:

Analog Product Listing (Continued)

Operational Amplifiers: High Slew-Rate: (Continued)

DUALS:

QUADS:

Operational Amplifiers: Wide Bandwidth

SINGLES:

DUALS:

QUADS:

Operational Amplifiers: Precision

Operational Amplifiers: Low Power

SINGLES:

DUALS:

QUADS:

Analog Product Listing (Continued)

Operational Amplifiers: General Purpose

Operational Amplifiers: High Voltage

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Analog Product Listing (Continued)

Switches (Continued)

2 x SPDT:

DPST:

2 x DPST:

DPDT:

4PST:

Sample and Hold Amplifiers

Telecommunication Circuits

Ordering Information

Harris Semiconductor products are represented by an extensive network of factory sales personnel, sales representatives, and authorized distributors in the United States of America, Europe, and the Far East. Please contact your nearest sales office, representative, or distributor to place an order, obtain price and delivery information, or additional product information. A complete listing of sales offices is available by contacting your nearest sales office headquarters or by contacting the Harris factory at (407) 724-7418. Sales office headquarters are listed at the end of this data book.

Product Code

Harris Semiconductor military product offerings are designated by several nomenclature methods. These methods are based on their method of compliance to the military standards involved. They are:

Harris Product Code:
(Issued by Harris)

Used for all products not subject to government part number assignments such as JAN slash sheet numbers and standard military drawing (SMD). Harris product code example is listed below. Product which is fully compliant to Mil-Std-883 carry a suffix of /883. Suffixes indicating Mil-Std "equivalent" parts are -8 and -Q.

JAN (Joint Army Navy):
(Issued by DESC)

Used for all devices currently on the qualified parts list (QPL) for MIL-M-38510. The part numbers used are "JAN slash sheet numbers". JAN qualified parts are subject to regular audit for compliance to military standards and may not be changed by Harris without government approval and audit.

SMD (Standard Military Drawing)
(Issued by DESC)

Used for all devices specified by DESC by a control document which requires full compliance to Mil-Std-883. Government approval is required before device specifications may be changed by Harris. Although specific device audits are not required, Harris must maintain a JAN facility qualification before SMD's may be issued.

HARRIS PRODUCT CODE EXAMPLE

Harris products are designated by "Harris Product Code". These products will always begin with the letter 'H' and specific device numbers are isolated by hyphens. An example product code is shown below. When ordering, please refer to products by the full code identification.

H A 1 - 2400 /883

PREFIX:
H (Harris)

FAMILY:
- A: Analog
- C: Communications
- F: Filters
- I: Interface
- M: Memory
- V: Analog High Voltage

PACKAGE:
- 1-: Ceramic Dual-In-Line (DIP)
- 2-: Metal Can
- 4-: Ceramic Leadless Chip Carriers (LCC)
- 7-: Ceramic Mini-DIP
- 0-: Chip Form

PART NUMBER

TEMPERATURE/GRADE:
- -6: 100% +25^{o}C Probe (Dice Only)
- -8: -55^{o}C to +125^{o}C Harris Class B Equivalent Devices for Use in Military and Flight Systems.
- -Q: -55^{o}C to +125^{o}C Harris Class S Equivalent Devices for Use in Spacecraft or High Rel Applications.
- /883: Full Compliance to Mil-Std-883
- -BXXX: Altered to Customer Requirements. B Number is Uniquely Assigned to Specific Customer Requirements.

Chip Information

Harris Standard Flows

Harris Semiconductor offers two standard integrated circuit dice product flows which cover the application environments our customers experience. These flows range from low cost commercial dice to military temperature range dice with sample electrical performance data. These product grades have one thing in common. They result from meticulous attention to quality, starting with design decisions made during product development and ending with the labeling of shipping containers for delivery to our customers.

Most of the dice offered by Harris are available in the two standard grades. Consult the Die Product Data Sheets or contact your Harris representative to determine which grades are available for a particular circuit. The standard flows offered are:

DASH 6 - Commercial Grade Dice

DASH 6 dice are 100% probe tested at +25°C to assure the maximum/mimimum DC characteristics listed in the DASH 6 Die Product Data Sheet. DASH 6 dice are intended for use in non-military applications. DASH 6 dice are 100% visually inspected to Harris Semiconductor's commercial grade criteria.

DASH 3 - Military Grade Dice

DASH 3 dice are 100% probe tested at +25°C to assure the maximum/minimum DC characteristics listed in the DASH 3 Die Product Data Sheet. DASH 3 dice are intended for use in military applications. DASH 3 dice are 100% visually inspected to Harris Semiconductor's MIL-STD-883, Method 2010, Condition B (Class B) criteria.

To assure that the electrical specifications will be met, a sample of the DASH 3 dice are pulled. The dice are assembled into standard packages and tested at +25°C, -55°C and +125°C to an LTPD of 15/2. The dice and test data are supplied to the customer. DASH 3 dice are 100% visually inspected to Harris Semiconductor's MIL-STD-883, Method 2010, Condition B (Class B) criteria.

Mechanical Information

Dimensions:

All dimensions given in the die layout section of the Die Product Data Sheet are nominal with tolerance of ± 0.003 inches (± 0.08mm) Die thicknesses are 0.018 inches ± 0.003 inches (0.46mm ± 0.08mm).

Bonding Pads:

Minimum bonding pad size is 0.004 x 0.004 inches (0.10mm x 0.10mm).

Die Product Data Sheets

To enable hybid manufacturers to understand the characteristics of the products which Harris Semiconductor offers in die form, Die Product Data Sheets have been created for selected products and product grades.

Included on each Die Product Data Sheet is a general description of circuit function, die dimensions and layout for hybrid design, backside metallization, substrate voltage bias conditions, passivation materials and a table of electrical performance characteristics.

Dice are placed in conductive waffle carriers, sealed in an antistatic bag, and packaged in a suitable shipping container. The Die Data Sheet for each product will specify the number of dice which will be packed in each individual tray.

Harris Franchised Die Processors

Harris Semiconductor also provides dice to customers through Harris Franchised Die Processors, who provide a line of hybrid-related products which may include semiconductor dice, discrete transistors, resistors and other components.

Services not offered by Harris, but often provided by Die Processors include non-standard inspection and electrical screening, multi-chip lot kitting, inventory management and custom packaging. These features, often requested by some Harris Semiconductor die product users, are best handled through these Die Processors.

Ordering Information

Harris products are designated by Product Code and dice products will always begin with H. Consult your Harris Sales Representative or the factory for Part Number and grade availability, Die Product Data Sheets and General Die Product Information.

HARRIS PART NUMBER EXAMPLE

H A 0 - 2425 - 6

PREFIX:
H (Harris)

FAMILY:
A - Analog
C - Communications
D - Digital
I - Interface
V - High Voltage

PACKAGE:
0 - Dice

PART NUMBER

GRADE:
6 - Commercial
3 - Military

IC Handling Procedures

Harris Analog IC processes are designed to produce the most rugged products on the market. However, no semiconductor is immune from damage resulting from the sudden application of many thousands of volts of static electricity. While the phenomenon of catastrophic failure of devices containing MOS transistors or capacitors is well known, even bipolar circuits can be damaged by static discharge, with altered electrical properties and diminished reliability. None of the common IC internal protection networks operate quickly enough to positively prevent damage.

It is suggested that all semiconductors be handled, tested, and installed using standard "MOS handling techniques" of proper grounding of personnel and equipment. Parts and subassemblies should not be in contact with untreated plastic bags or wrapping material. High impedance IC inputs wired to a P.C. connector should have a path to ground on the card.

HANDLING RULES

Since the introduction of integrated circuits with MOS structures and high quality junctions, a safe and effective means of handling these devices has been of primary importance. One method employed to protect gate oxide structures is to incorporate input protection diodes directly on the monolithic chip. However, there is no completely foolproof system of chip input protection in existence in the industry. In addition, most compensation networks in linear circuits are located at high impedance nodes, where protection networks would disturb normal circuit operation. If static discharge occurs at sufficient magnitude (2kV or more), some damage or degradation will usually occur. It has been found that handling equipment and personnel can generate static potentials in excess of 10kV in a low humidity environment. Thus it becomes necessary for additional measures to be implemented to eliminate or reduce static charge. It is evident, therefore, that proper handling procedures or rules should be adopted.

Elimination or reduction of static charge can be accomplished as follows:

- Use static-free work stations. Static-dissipative mats on work benches and floor, connected to common point ground through a 1MΩ resistor, help eliminate static build-up and discharge. Do not use metallic surfaces.
- Ground all handling equipment.
- Ground all handling personnel with a conductive bracelet through 1MΩ to ground (the 1MΩ resistor will prevent electroshock injury to personnel). Transient product personnel should wear grounding heel straps when conductive flooring is present.
- Smocks and clothing of certain insulating materials (notably nylon) should not be worn in areas where devices are handled. These materials, highly dielectric in nature, will hold, or aid in the generation of a static charge. Where they cannot be eliminated, natural materials such as cotton should be used to minimize charge generation capacity. Conductive smocks are also available as an alternative.
- Control relative humidity to as high a level as practical. 50% is generally considered sufficient. (Operations should cease if R.H. falls below 25%).
- Ionized air blowers reduce charge build-up in areas where grounding is not possible or practical.
- Devices should be in conductive static-shielded containers during all phases of transport. Leads may be shorted by tubular metallic carriers, conductive foam, or foil.
- In automated handling equipment, the belts, chutes, or other surfaces should be of conducting non-metal material. If this is not possible, ionized air blowers or ionizing bars may be a good alternative.

JUNCTION ISOLATION (JI)

Although it is the most common integrated circuit process, Harris offers only a limited number of products, such as the HA-4741, using JI technology. Latchup and other problems have made the Harris Dielectric Isolation (DI) process, described below, more reliable.

Bipolar ICs using the JI process generally begin with a p-type wafer into which a buried layer pattern can be first implanted and diffused. Next the n-type epitaxial layer is grown, and p-type isolation walls are diffused around each area to be electrically isolated from the other circuitry. These isolation walls must be diffused deeply into the wafer in order to contact the original p-substrate. In operation, the p-substrate and isolation walls are connected to the most negative circuit potential, so that each active area is surrounded on the sides and bottom by a reverse biased junction through which a small current flows (Figure 1). This current may not be negligible at operating temperatures higher than +100°C.

To complete the IC, base and emitter diffusions are performed, the wafer is coated with aluminum, and the conductor pattern is etched.

DIELECTRIC ISOLATION (DI)

Harris has developed a different process which has many advantages over JI for fabricating high performance analog ICs. With Dielectric Isolation (DI), each active area is surrounded on the sides and bottom by an insulating layer of silicon dioxide and embedded in polycrystalline silicon for mechanical strength.

For bipolar ICs, the process begins with a wafer of n-type silicon. The side of the wafer which will eventually be the bottom is deeply etched to form the sidewall pattern. Silicon dioxide is then grown and polycrystalline silicon deposited to fill the etched "moats." The opposite side of the wafer is then polished until the insulating sidewalls appear at the wafer surface (Figure 2). Conventional diffusion and metallization processes follow to complete the IC.

ICs fabricated under the DI process are superior in the following ways.

1. Almost all op amp designs require at least one PNP transistor in the signal path. Typical JI op amps must use a lateral PNP with its inherently poor frequency response, which limits typical compensated bandwidth to 1MHz.

   The DI process makes it practical to build a vertical PNP, allowing compensated op amp bandwidths of 50MHz, or higher (Figure 3). Also, transistor collector to substrate capacitance is significantly reduced DI, further enhancing high frequency performance.

2. Other devices, such as optimally specified MOS or JFET transistors may be fabricated on the same chip. Diffused and thin film resistors are implemented routinely.

3. The isolation removes the possibility of parasitic SCRs which might create latchup under certain sequences of power and signal application.

4. Leakage currents to the substrate under high temperature conditions are greatly reduced.

DIELECTRICALLY ISOLATED CMOS

JI processed CMOS analog ICs, which are generally used in conjunction with several power supplies, are particularly prone to parasitic SCR latchup failures as well as failures due to input voltage spikes. The DI CMOS process (described in detail in Harris Application Note 521) has proven to be the best solution.

Since analog multiplexers are often used at the input of a data acquisition system, particular attention must be paid to the possibility of damaging input overvoltage conditions. Harris has provided an effective answer in the HI-546 through HI-549 multiplexers with built-in overvoltage protection.

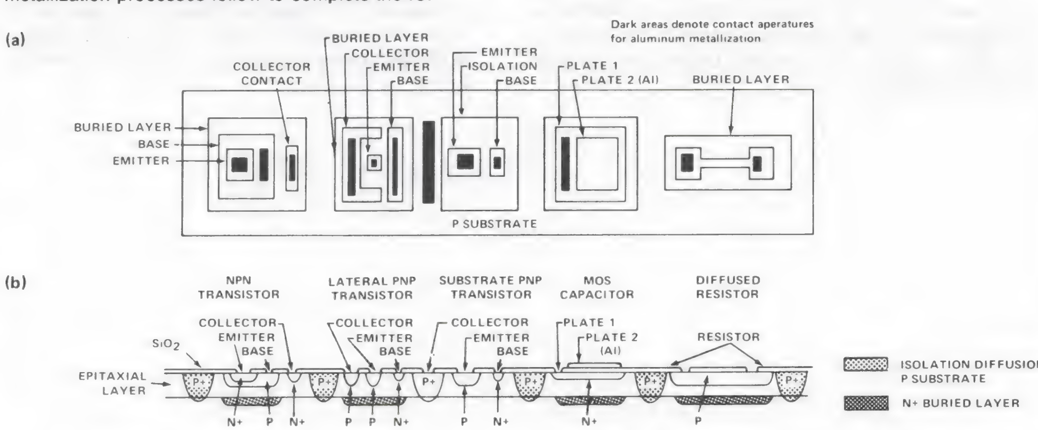


FIGURE 1. STRUCTURES OF VARIOUS COMPONENTS FORMED IN THE JUNCTION-ISOLATION PROCESS. (a) TOPOLOGICAL VIEW. (b) CROSS-SECTIONAL VIEW.

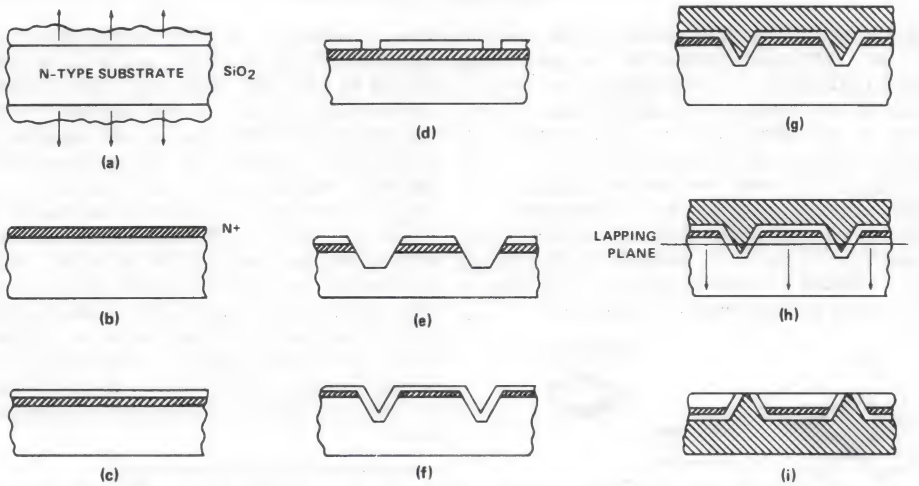


FIGURE 2. PROCESS STEPS FOR DIELECTRIC ISOLATION. (a) SURFACE PREPARATION, (b) N-BURIED LAYER DIFFUSION, (c) MASKING OXIDE, (d) ISOLATION PATTERN, (e) SILICON ETCH, (f) DIELECTRIC OXIDE, (g) POLYCRYSTALLINE DEPOSITION, (h) BACKLAP AND POLISH, (i) FINISHED SLICE.

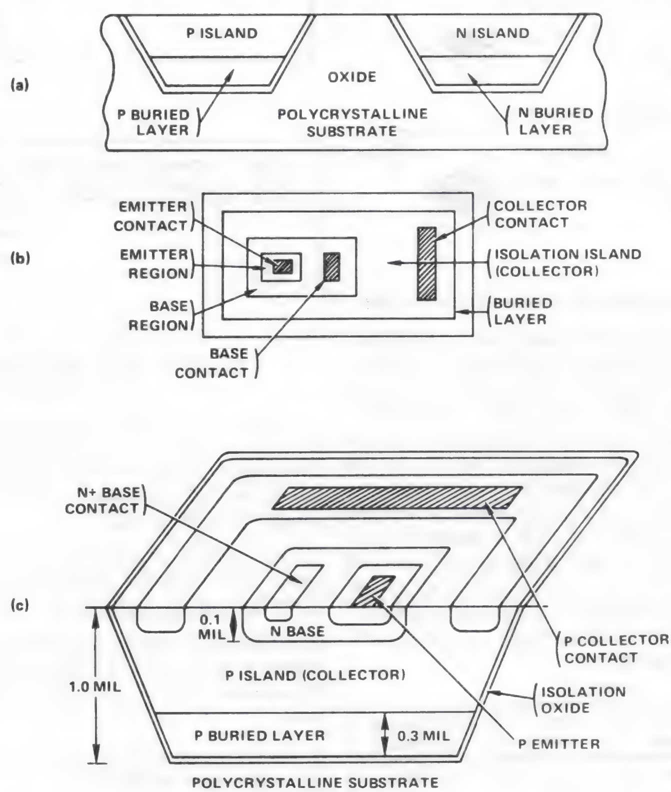


FIGURE 3. THE HIGH-FREQUENCY PROCESS. (a) CROSS-SECTIONAL VIEW OF P AND N ISLANDS FOR PNP AND NPN TRANSISTORS. (b) TOPOLOGICAL VIEW SHOWING RELATIVE PLACEMENT OF TRANSISTOR REGIONS. (c) CROSS-SECTIONAL VIEW OF HIGH- FREQUENCY PNP DEVICE FORMATION IN THE D.I. PROCESS.

Packaging Techniques

Harris Semiconductor offers Leadless Chip Carriers (LCC) as a packaging option on various Analog integrated circuits. An LCC is a square or rectangular package for an Integrated Circuit (IC) that is manufactured in the same manner as a conventional side-braze dual-in-line package (DIP). The LCC is comprised of the cavity and seal ring section of a standard DIP and offers the user a means of achieving high density system configurations while retaining the reliability benefits of hermetic IC Packaging. Figure 1 provides a comparison of the construction of an LCC and a conventional side-braze DIP.

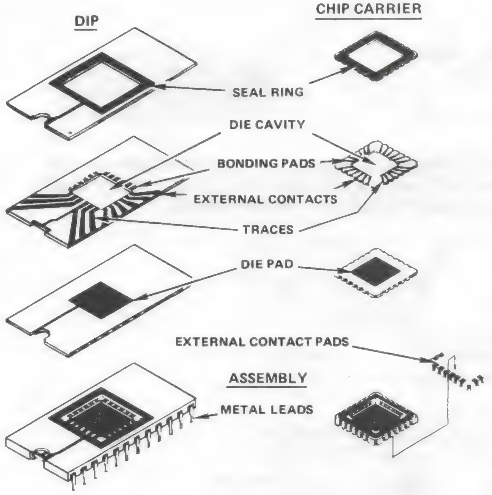


FIGURE 1. EXPLODED VIEW OF CHIP CARRIER AND DIP

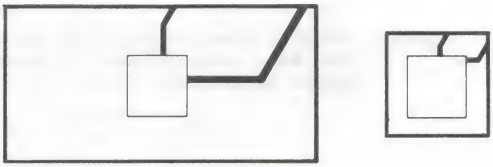
The LCC's two principle advantages over conventional side-braze DIPs are packaging density and electrical performance. Packaging density is the number one advantage to an LCC over a side-braze DIP. The size of a DIP is governed primarily by the number of leads required and not by the size of the IC. As pin count increases, more and more of the DIP package is used only to provide an electrical trace path to the external leads. The size of an LCC is dependent on the size of the die not on the number of leads. As pin count increases, overall size increases but at a much slower rate. Table 1 provides a comparison between the areas of 18, 28 and 48 lead LCCs to 18, 28 and 48 lead side-braze DIPs.

TABLE 1.

LEAD COUNT	LCC AREA	DIP AREA	DIP AREA vs. LCC AREA
18	0.10	0.22	220%
28	0.20	0.84	420%
48	0.31	1.68	542%

(All Units in Square Inches)

The chart indicates a 220% improvement in packaging area for the 18 lead LCC, and 542% improvement for the 48 lead LCC. Obviously, sizeable savings in circuit board area can be achieved with this packaging option. The second major advantage of the LCC is in electrical performance. The package size and geometry also dictates trace length and uniformity. Figure 2 provides a comparison between the trace lengths for various LCCs and side-braze DIPs. As pin count goes up, trace lengths get longer, adding resistance and capacitance unequally around the package. As ICs get faster and more complex these factors start to become a limiting factor on performance. LCCs minimize this effect by maintaining, as close as possible, uniform trace length so that the package is a significantly smaller determinant of system performance.



LEAD COUNT	LONGEST TRACE DIP / LONGEST TRACE LCC	LONGEST TRACE / SHORTEST TRACE	
		LCC	DIP
18	2:1	1.5:1	6:1
24	4:1	1.5:1	3:1
40	5:1	1.5:1	6:1
54	6:1	1.5:1	7:1

FIGURE 2. ELECTRICAL PERFORMANCE (RESISTANCE AND SPEED)

The LCC also offers environmental advantages over "chip-and-wire" manufacturing techniques used in high density hybrid circuits. An IC can be fully tested, burned-in and processed in an LCC, thereby guaranteeing its performance.

The IC is further protected by a small hermetic package in which internal vapor content can be carefully controlled during production.

Harris Semiconductor Leadless Chip Carriers in both Ceramic and Epoxy provide reliable, high density, high performance packaging options for today's systems.

Consult the factory or your Harris sales representative for pricing and availability.

Competitive Cross Reference Chart

Manufacturer	Part Number	Harris Pin-for-Pin Replacement	Harris Closest Replacement	Harris Advantages
AMD	AM118		HA-2510	Unity gain stable
	AM1408		HI-5618-5	Faster, application resistors
	AM1508		HI-5618-2	Faster, application resistors
	AM318		HA-2515	Unity gain stable
	AM6012		HI-562A	Faster, application resistors, int. linearity
			HI-5660	Int. linearity, application resistors
	AM6420		HA-5320	
			HA-5330	
	LF198		HA-2420	Improved performance
	LF398		HA-2425	Improved performance
	SSS1408		HI-5618-5	Faster, application resistors
	SSS1508		HI-5618-2	Faster, application resistors
ANALOG DEV	52		HA-5180	Monolithic
	AD1408		HI-5618-5	Faster, application resistors
	AD1508		HI-5618-2	Faster, application resistors
	AD380,AD382		HA-2542	Monolithic
	AD381		HA-2541	Monolithic
	AD389		HA-5320	Faster, monolithic
	AD507	HA-2620		Identical
	AD509	HA-2520	HA-2529	Identical
	AD515		HA-5180	Monolithic
	AD518	HA-2510		
	AD542L		HA-5170	Better AC
	AD545		HA-5180	Monolithic
	AD547J		HA-5170	Better AC
	AD562		HI-562A	Faster
			HI-5660	Faster
	AD563		HI-565A	Faster
	AD565	HI-565A		Faster
	AD565A	HI-565A		
	AD566		HI-5660	
			HI-562	
	AD566A		HI-5660	
			HI-562A	
	AD574A	HI-574A,HI-674A		Digital timing, 674A is 2.3 times faster
	AD582		HA-2425	Acquisition time
	AD583K	HA-2425-5		Identical
	AD611		HA-5320	Faster, better accuracy
	AD667		HI-5811	
	AD7501		HI-508	DI process
	AD7502	HI-1828A		DI process
	AD7503	HI-1818A		DI process
	AD7506	HI-506		DI process
	AD7507	HI-507		DI process
	AD7511		HI-201	
	AD7512		HI-5043	
	ADADC80		HI-574A	Power, smaller pkg.
			HI-674A	Faster, power, smaller pkg.
	ADADC84/85		HI-674A	Power, smaller pkg.
	ADDAC 08		HI-5618	Faster, application resistors
	DAC 80	HI-5680,HI-5690		5690 is 2.67 times faster
	DAC 85	HI-5685,HI-5695		5695 is 2.67 times faster
	DAC 87	HI-5687,HI-5697		5697 is 2.67 times faster
	ADG200		HI-200	
	ADLH0032		HA-5190,HA-2542	Monolithic
	HOS050		HA-2542	Monolithic
	HOS100		HA-5033	Monolithic
ANALOGIC	MN4708		HI-508	
			HI-1818A	
	MP1812A		HI-5680V	Faster, monolithic, power, smaller pkg.
	MP250M		HA-2420/25	Faster, monolithic, smaller
	MP260		HA-2420/25	Monolithic, smaller pkg.
	MP261		HA-2420	Monolithic, smaller pkg.
	MP270/271		HA-5320	Monolithic, smaller pkg.
BECKMAN	7556		HI-574A	Faster, smaller pkg.
	7580	HI-5690	HI-5680	Faster, monolithic
BURR-BROWN	3500		HA-2600	Better AC
	3503	HA-2505		Identical
	3506	HA-2605		Identical
	3507	HA-2525	HA-2529	Identical
	3508	HA-2625		Identical

Competitive Cross Reference Chart (Continued)

Manufacturer	Part Number	Harris Pin-for-Pin Replacement	Harris Closest Replacement	Harris Advantages
BURR-BROWN (cont.)	3521		HA-5170	Better AC
	3523		HA-5180	Better AC
	3527		HA-5180	Better AC and DC
	3528		HA-5180	Better AC
	3550		HA-2541	Monolithic
	3553		HA-5033	Monolithic
	3554		HA-2542	Monolithic
	ADC80		HI-574A	Smaller pkg., power
			HI-674A	Faster, smaller pkg., power
	ADC84/85		HI-674A	Smaller pkg., power
	DAC70		HI-DAC16	Faster, monolithic
	DAC700/701		HI-DAC16	
	DAC702/703		HI-DAC16	
	DAC71/72		HI-DAC16	Monolithic, "I" output
	DAC80	HI-5680, HI-5690		Faster, monolithic, power
	DAC800	HI-5680, HI-5690		5690 is 3.33 times faster, lower power
	DAC811	HI-5811		
	DAC85	HI-5685, HI-5695		Faster, monolithic, power
	DAC850	HI-5685, HI-5695		5695 is 3.33 times faster, lower power
	DAC851	HI-5687, HI-5697		5697 is 3.33 times faster, lower power
	DAC87	HI-5687, HI-5697		Faster, monolithic, power
	MPC16S	HI-546-5		Identical
	MPC4D	HI-549-5		Identical
	MPC800KG	HI-516-5		Identical
	MPC801KG	HI-518-5		Identical
	MPC801SG	HI-518-2		Identical
	MPC8D	HI-547-5		Identical
	MPC8S	HI-548-5		Identical
	OPA103		HA-5180	Better AC
	OPA104		HA-5180	
	OPA11		HA-2600	
	OPA21		HA-5141, HA-5151	
	OPA27		HA-5127	
	OPA37		HA-5137, HA-5147	
	OPA600		HA-2542	
	OPA633		HA-5033	
	SCH298AM		HA-2425	Improved performance
	SCH80/85		HA-2425	Faster, monolithic, power
	SHC85ET		HA-2420	Faster, monolithic, power
	SHM60		HA-5320	Monolithic, smaller pkg.
	ADC574A	HI-574A		Identical
	ADC674A	HI-674A		Identical
	SHC5320	HA-5320		Identical
DATA DEVICE CORP.	ADH051		HA-5330	Monolithic, smaller pkg., power
	ADH8585		HI-674A	Smaller pkg., power
	DDC5200		HI-574A	Faster
	DDC5210/11		HI-674A	
	DDC5212/16		HI-674A	
	DDCADC85		HI-674A	Smaller pkg., power
	DDCDAC85	HI-5680, HI-5690		Faster, smaller pkg., power
	DDCDAC85LD	HI-5685, HI-5695		Monolithic, power
	DDCDAC87	HI-5687, HI-5697		Monolithic, power, 5697 is 3.33 times faster
	DGL13		HA-5320	Monolithic, smaller pkg., power
	THC4460		HA-5320	Monolithic, smaller pkg.
DATEL	ADC52XX		HI-674A	Lower power
	ADC574A	HI-574A, HI-674A		Identical, 674 is 1.67 times faster
	ADC8412		HI-674A	Smaller pkg. power
	ADC85C12		HI-674A	Smaller pkg., power
	ADC8712		HI-674A	Smaller pkg., power
	ADCHX12B		HI-574A	Smaller pkg., power
			HI-674A	Faster, smaller pkg., power
	ADCL12B2		HI-574A	Smaller pkg.
			HI-674A	Faster, smaller pkg.
	ADCM12B2		HI-674A	Smaller pkg.
	ADCMA12B2A		HI-574A	Faster, smaller pkg.
	ADCMA12B2B		HI574A	Smaller pkg.
			HI-674A	Faster, smaller pkg.
	AM450	HA-2505		
	AM452	HA-2525	HA-2529	
	AM460	HA-2605		
	AM462	HA-2625		
	AM464	HA-2645		
	DAC08B		HI-5618	Faster, application resistors
	DAC562	HI-562A		Identical

Competitive Cross Reference Chart (Continued)

Manufacturer	Part Number	Harris Pin-for-Pin Replacement	Harris Closest Replacement	Harris Advantages
DATEL (cont.)	DAC71/72		HI-DAC16	Monolithic
	DAC85	HI-5685,HI-5695		Faster, monolithic, power
	DAC85C	HI-5680,HI-5690		Monolithic, power, 5690 is 2 times faster
	DAC87	HI-5687,HI-5697		Faster, monolithic, power
	DACHP16B		HI-DAC16	Monolithic
	DACHR16B		HI-DAC16	Monolithic, smaller pkg.
	DACHZ12B	HI-5690/95/97	HI-5680/85/87	Faster, monolithic
	DACIC10B		HI-5610	Faster, application resistors
	DACIC8B		HI-5618	Faster, application resistors
	MV1606	HI-506		Identical
	MV808	HI-1818A		Identical
	MVD409	HI-1828A		Identical
	MVD807	HI-507		Identical
	MX1606	HI-546		Identical
	MX1616	HI-516		Identical
	MX808	HI-548		Identical
	MX818	HI-518		Identical
	MXD409	HI-549		Identical
	MXD807	HI-547		Identical
	SHM1C-1	HA-2425		Identical
	SHM1C-1M	HA-2420		Identical
	SHM20	HA-5320		Identical
	SHM6M		HA-5320	Monolithic, smaller pkg.
			HA-5330	Faster, monolithic, smaller pkg.
	SHM9M		HA-2420	Faster, monolithic, smaller pkg.
	SHMLM-2		HA-2420	Faster
ELANTEC	EHA2500	HA-2500		
	EHA2502	HA-2502		
	EHA2505	HA-2505		
	EHA2510	HA-2510		
	EHA2512	HA-2512		
	EHA2515	HA-2515		
	EHA2520	HA-2520		
	EHA2522	HA-2522		
	EHA2525	HA-2525		
	EHA2600	HA-2600		
	EHA2602	HA-2602		
	EHA2605	HA-2605		
	EHA2620	HA-2620		
	EHA2622	HA-2622		
	EHA2625	HA-2625		
	ELH0002		HA-5002-2	Monolithic
	ELH0002C		HA-5002-5	Monolithic
	ELH0033		HA-5033-2	Monolithic
	ELH0033C		HA-5033-5	Monolithic
	ELH0041		HA-2542-2	Monolithic
	ELH0041C		HA-2542-5	Monolithic
EXAR	XR4212		HA-4741	
	XR3417			Lower power
	XR3418		HC-55536 or	Fewer external components
	XR3517		HC-55564	Military pkg.
	XR3518			
FAIRCHILD	μA0801/02		HI-5618	Faster, application resistors
	μA1458		HA-5102	Better AC, lower noise
	μA1558		HA-5102	Better AC, lower noise
	μA198		HA-2420	Improved performance
	μA398		HA-2425	Improved performance
	μA565	HI-565A		
	μA702		HA-2620	
	μA709		HA-2620	
	μA714		HA-5135	Better DC
	μA715		HA-2520,HA-2529	Better AC
	μA727		HA-5135	Better DC
	μA740		HA-5170	Better AC
	μA741		HA-2600	Better AC
FAIRCHILD	μA747		HA-5102	Lower noise
	μA748		HA-2600	Better AC
	μA776		HA-2720	Better AC, lower noise
HITACHI	HA17408		HI-5618	Faster, application resistors

1 GENERAL INFORMATION

Competitive Cross Reference Chart (Continued)

Manufacturer	Part Number	Harris Pin-for-Pin Replacement	Harris Closest Replacement	Harris Advantages
HYBRID SYSTEM	ADC550		HI-574A	Faster, smaller pkg., power
	ADC581		HI-574A	
			HI-674A	Faster
	DAC3281-16		HI-DAC16	Monolithic, smaller pkg.
	DAC335-12		HI-5687V	Faster, monolithic
	DAC346C-12		HI-5680V	Faster, monolithic
	DAC347LP-12		HI-5687V	Faster, monolithic
	DAC372		HI-5680	Monolithic
	DAC3721-8		HI-5618	Faster, monolithic
	DAC395-8		HI-5618	Monolithic, smaller pkg.
	HS346		HA-5320	Faster, monolithic
	HS5200		HI-674A	
	HS574	HI-574A,HI-674A		Digital timing, 674 is 2 times faster
	HS730		HA-5320	Monolithic, smaller pkg.
			HA-5330	Faster, monolithic, smaller pkg.
	HSDAC80	HI-5680,HI-5690		Faster, monolithic, power, 5690 is 5.56 times faster
	HSDAC87	HI-5687,HI-5697		Faster, monolithic, power
	MUX201	HI-1818A		Lower power, smaller pkg.
	SH725		HA-2420	Faster, monolithic, smaller pkg.
INTECH	1048BIN-P		HI-574A	Smaller pkg., power
			HI-674A	Faster, smaller pkg., power
	416 BIN		HI-DAC16	Smaller pkg.
	A3103		HI-674A	Smaller pkg., power
	A3155		HI-574A	Smaller pkg., power
			HI-674A	Faster, smaller pkg., power
	A880/880-2		HA-5320	Faster, monolithic, power
	A881		HA-5320	Monolithic, smaller pkg., power
	A882/884		HA-2420/25	Faster, monolithic, power
	ADC111		HI-574A	Smaller pkg., power
			HI-674A	Faster, smaller pkg., power
	ADC2812		HI-547A	Smaller pkg., power
			HI-674A	Faster, smaller pkg., power
	ASH240/250		HA-2420/25	Monolithic, smaller pkg., power
	ASH271		HA-5320	Monolithic, smaller pkg., power
	CYAAD12QM		HI-574A	Smaller pkg., power
			HI-674A	Faster, smaller pkg., power
INTEL	D2912	HC-5512		Lower power, lower noise
	D2912A	HC-5512		Lower power, lower noise
		HC-5512A/12D		Lower power, lower noise
	SBC 86/05	HB0-986C05		CMOS micro components. Lower
	NMOS			power 16K static RAM w/full mercury back-up
INTERSIL	DG200	HI-200		Dielectric Isolation
	DG201	HI-201		Dielectric Isolation
	ICL7541			Identical
	ICL7611		HA-5141	Lower noise
	ICL7615		HA-5141	Better AC, lower noise
	ICL7621		HA-5142	Better AC, lower noise
	ICL7642		HA-5144	Better AC, lower noise
	ICL8017		HA-2520,HA-2529	
	ICL8021		HA-5141	Better AC
	ICL8075			
	ICL8211			
	IH201	HI-201		More stable over temp.
	IH5040	HI-5040		More stable over temp.
	IH5041	HI-5041		More stable over temp.
	IH5042	HI-5042		More stable over temp.
	IH5043	HI-5043		More stable over temp.
	IH5044	HI-5044		More stable over temp.
	IH5045	HI-5045		More stable over temp.
	IH5046	HI-5046		More stable over temp.
	IH5047	HI-5047		More stable over temp.
	IH5048	HI-5048		More stable over temp.
	IH5049	HI-5049		More stable over temp.
	IH5050	HI-5050		More stable over temp.
	IH5051	HI-5051		More stable over temp.
	IH5108	HI-548		Signal range, same pinout
	IH5110/11		HA-2420/25	
	IH5112/13		HA-2420/25	
	IH5114/15		HA-2420/25	
	IH5200	HI-200		Constant Ron
	IH5201	HI-201		Constant Ron
	IH5208	HI-509A		Vin range, same pinout
	IH6108	HI-508		Ron, DI, same pinout

Competitive Cross Reference Chart (Continued)

Manufacturer	Part Number	Harris Pin-for-Pin Replacement	Harris Closest Replacement	Harris Advantages
INTERSIL (cont.)	IH6116	HI-506		Ron, DI, same pinout
	IH6208	HI-509		Ron, DI, same pinout
	IH6216	HI-507		Ron, DI, same pinout
	LM4250		HA-2720	Better AC, lower noise
INTRONICS	A-560		HA-2525,HA-2529	
	A-561		HA-2625	
MAXIM	MAX400M		HA-5127-2	
	MAX400C		HA-5127-5	
	MAX460M		HA-5033-2	Lower noise, DI
	MAX460C		HA-5033-5	Lower noise, DI
	BB3553		HA-5033	Monolithic, DI
	BB3554		HA-2542	Monolithic, DI
	LH0033		HA-5033	Monolithic
	OP07		HA-5130	Better AC - DI
	DG201A	HI-201		Dielectric Isolation
	DG211		HI-201	Full Temperature Range Specified
	DG300A	HI-300		Dielectric Isolation
	DG301A	HI-301		Dielectric Isolation
	DG302A	HI-302		Dielectric Isolation
	DG303A	HI-303		Dielectric Isolation
	DG304A	HI-304		Dielectric Isolation
	DG305A	HI-305		Dielectric Isolation
	DG306A	HI-306		Dielectric Isolation
	DG307A	HI-307		Dielectric Isolation
	DG381A	HI-381		Dielectric Isolation
	DG384A	HI-384		Dielectric Isolation
	DG387A	HI-387		Dielectric Isolation
	DG390	HI-390		Dielectric Isolation
	IH5040	HI-5040		Dielectric Isolation
	IH5041	HI-5041		Dielectric Isolation
	IH5042	HI-5042		Dielectric Isolation
	IH5043	HI-5043		Dielectric Isolation
	IH5044	HI-5044		Dielectric Isolation
	IH5045	HI-5045		Dielectric Isolation
	IH5046	HI-5046		Dielectric Isolation
	IH5047	HI-5047		Dielectric Isolation
	IH5048	HI-5048		Dielectric Isolation
	IH5049	HI-5049		Dielectric Isolation
	IH5050	HI-5050		Dielectric Isolation
	IH5051	HI-5051		Dielectric Isolation
MICRO NETWORKS	ADC80		HI-574A	Smaller pkg., power
			HI-674A	Faster, smaller pkg., power
	DAC80	HI-5680,HI-5690		Monolithic, power, 5690 is 5.56 times faster
	DAC85	HI-5685,HI-5695		Monolithic, power, 5695 is 5.56 times faster
	DAC87	HI-5687,HI-5697		Monolithic, power, 5697 is 5.56 times faster
	MN-ADC84/85/87		HI-674A	Smaller pkg., power
	MN3009		HI-5618	Monolithic
	MN3014		HI-5618	Monolithic
	MN3348		HI-5680V/87V	Faster, monolithic, power
	MN3349		HI-5685V/87V	Faster, monolithic
	MN343/344		HA-2420	Faster, monolithic
	MN346/347		HA-5320	Faster, monolithic
	MN370/371		HI-5687V	Monolithic
	MN373	HA-5320		
	MN375		HA-5330	Monolithic, lower power
	MN5200		HI-574A	Faster
	MN5210		HI-674A	Two chip design
	MN565A	HI-565A		
	MN574A	HI-574A,HI-674A		674A is 2.3 times faster
MICRO POWER SYSTEMS	MP200DI	HI-200		Constant Ron
	MP201DI	HI-201		Constant Ron
	MP5527		HA-5127	
	MP5537		HA-5137	
	MP562	HI-562A		Faster
	MP574	HI-574A,HI-674A		Digital timing, 674A is 2 times faster
	MP7501	HI-508		
	MP7503	HI-1818A		
	MP7502	HI-1828A		
	MP7506	HI-506		DI processing
	MP7507	HI-507		DI processing
	MP7508DI	HI-508		
	MP7509DI	HI-509		

Competitive Cross Reference Chart (Continued)

Manufacturer	Part Number	Harris Pin-for-Pin Replacement	Harris Closest Replacement	Harris Advantages
MITEL	MT8912	HC-5512		Lower noise, lower cross talk
MOSTEK	MK5912	HC-5512		Lower noise and power
MOTOROLA	LF155		HA-5170	Better DC
	LF155A		HA-5170	Better DC
	LF156		HA-5170	Better DC
	LF156A		HA-5170	Better DC
	LF157		HA-5160	Better DC
	LF157A		HA-5160	Better DC
	LF355		HA-5170	Better DC
	LF355A		HA-5170	Better DC
	LF356		HA-5170	Better DC
	LF356A		HA-5170	Better DC
	LF357		HA-5160	Better DC
	LF357A		HA-5160	Better DC
	MC1408		HI-5618-5	Faster, application resistors
	MC1430		HA-2600	Better AC
	MC1431		HA-2600	Better AC
	MC1436		HA-2640	Better AC and DC
	MC1458		HA-5102	Better AC, lower noise
	MC1508		HI-5618-2	Faster, application resistors
	MC1558		HA-5102	Better AC, lower noise
	MC1748		HA-2600	Better AC and DC
	MC1776		HA-5141	Better AC, lower noise
	MC34002		HA-5102	Better AC
	MC34004		HA-5104	Better AC
	MC3403		HA-4741	Better AC
	AD562A	HI-562A		
	MC3412	HI-565A		
	MC3417		HC-55564 or	Lower power, few external components, military pkg.
	MC3418		HC-55536	
	MC3517			
	MC3518			
	MC3419		HC-5502A	Better longitudinal balance, transhybrid loss. Fewer external components
			HC-5504	Better longitudinal balance, transhybrid loss Fewer external components
	MC35002		HA-5102	Better AC
	MC35004		HA-5104	Better AC
	MC4741	HA-4741		Better AC
NATIONAL SEMICONDUCTOR	ADC1080/1280		HI-574A	Smaller pkg., lower power
			HI-674A	Faster, smaller pkg. power
	ADC1210/11		HI-574A	Faster, complete A/D
	BLC 86/05	HBO-986C05		CMOS micro components, lower power 16K static ram w/full mercury back-up
	DAC0800/0102		HI-5618	Faster, application resistors
	DAC0806/07/08		HI-5618	Faster, application resistors
	DAC1200/01		HI-5685V/87V	Faster, lower power
	DAC1265	HI-565A		
	DAC1266	HI-5660		
	DAC1280	HI-5680,HI-5690		Monolithic, performance, 5690 is 4.44 times faster
	DAC1285	HI-5685/87 HI-5695/97		Monolithic, performance, 5695/97 is 4.44 times faster
	LF0023/43		HA-2420	Monolithic, performance
	LF0053		HA-2420/25	Monolithic
			HA-5320	Faster, monolithic
	LF11201	HI-201		
	LF11508	HI-508-2		Faster, Ron, power
	LF11509	HI-509-2		Faster, Ron, power
	LF13201	HI-201		CMOS Dielectric Isolation
	LF13508	HI-508-5		Faster, Ron, power
	LF13509	HI-509-5		Faster, Ron, power
	LF147		HA-5104	
	LF151		HA-5170	
	LF153		HA-5102	
	LF155		HA-5170	Better DC
	LF155A		HA-5170	Better DC
	LF156		HA-5170	Better DC
	LF156A		HA-5170	Better DC
	LF157		HA-5170	Better DC
	LF157A		HA-5160	Better DC
	LF198		HA-2420	Improved performance
	LF247			
	LF253			

Competitive Cross Reference Chart (Continued)

Manufacturer	Part Number	Harris Pin-for-Pin Replacement	Harris Closest Replacement	Harris Advantages
NATIONAL SEMICONDUCTOR (cont.)	LF347			
	LF353			
	LF355		HA-5170	Better DC
	LF355A		HA-5170	Better DC
	LF356		HA-5170	Better DC
	LF356A		HA-5170	Better DC
	LF357		HA-5160	Better DC
	LF357A		HA-5160	Better DC
	LF398		HA-2425	Improved performance
	LF412		HA-5102	
	LF412A		HA-5102	
	LF441		HA-5141	Lower noise
	LF442		HA-5142	
	LF444		HA-5144	
	LH0002		HA-5002	Monolithic, better AC and DC
	LH0003		HA-2520,HA-2529	Monolithic
	LH0004		HA-2640	Monolithic
	LH0005		HA-2620	Monolithic
	LH0022		HA-5180	Monolithic, better AC and DC
	LH0032		HA-2542	Monolithic
	LH0033		HA-5033	Monolithic, better DC
	LH0042		HA-5180	Monolithic, better AC and DC
	LH0052		HA-5180	Monolithic, better AC
	LH0062		HA-5160	Monolithic, better AC
	LM108		HA-5135	Better DC and AC
	LM108A		HA-5135	Better DC and AC
	LM118		HA-2510	Unity gain stable
	LM124		HA-4741	Better AC
	LM143		HA-2640	Higher supply voltage
	LM144		HA-2640	
	LM146		HA-2740	Better AC
	LM148		HA-4741	Better AC
	LM208		HA-5135	Better DC and AC
	LM208A		HA-5135	Better DC and AC
	LM308		HA-5135	Better DC and AC
	LM308A		HA-5135	Better DC and AC
	LM308A		HA-5135	Better DC and AC
	LM318		HA-2510	Unity gain stable
	LM324		HA-4741	Better AC
	LM343		HA-2640	Higher supply voltage
	LM344		HA-2640	
	LM348		HA-4741	Better AC
	LM4250		HA-5141	Lower noise
	TP3040	HC-5512		Identical
	TP3040A	HC-5512A		Identical
		HC-5512D		Military spec
PMI	PM-155		HA-5180	
	PM-156		HA-5170	
	PM-157		HA-5160	
	OP-15		HA-5170	
	OP-16		HA-5160	
	OP-17		HA-5160	
	OP-42		HA-5160	
	OP-43		HA-5170	
	OP-77		HA-5177	
	OP-227		HA-5102	
	OP-400		HA-5134	
	OP-470		HA-5104	
PRECISION MONOLITHICS	DAC-08		HI-5618	Faster, application resistors
	DAC-1408		HI-5618-5	Faster, application resistors
	DAC-1508		HI-5618-2	Faster, application resistors
	DAC-312		HI-562A	Int. linearity, application resistors
	DMX-88	HI-508		V_{IN} range, lower power
	GAP01		HA-2400	4 channels
	MUX-08	HA-508		IN range, lower power
	MUX-16	HI-506		V_{IN} range, lower power
	MUX-24	HI-509		V_{IN} range, lower power
	MUX-28	HI-507		V_{IN} range, lower power
	MUX-88	HI-508		V_{IN} range, lower power
	OP01		HA-2500	Better AC
	OP05		HA-5135	Better AC and DC
	OP11		HA-4741	
	OP20		HA-5141	Better AC
	OP220		HA-5142	Better AC

Competitive Cross Reference Chart (Continued)

Manufacturer	Part Number	Harris Pin-for-Pin Replacement	Harris Closest Replacement	Harris Advantages
PRECISION MONOLITHICS (cont.)	OP27		HA-5127	
	OP37		HA-5137,HA-5147	HA-5147 Superior performance
	OP420		HA-5144	Better AC
	PM-562		HI-562A	Faster
	SMP-10/11	HA-2425		Lower power
			HA-5320	Faster, improved accuracy
	SMP-81		HA-2420/25	Lower power
			HA-5320	Faster, improved accuracy
	SSS1458		HA-5102	Better AC, lower noise
	SS1558		HA-5102	Better AC, lower noise
RAYTHEON	LF155		HA-5170	Better DC
	LF155A		HA-5170	Better DC
	LF156		HA-5170	Better DC
	LF156A		HA-5170	Better DC
	LF157		HA-5160	Better DC
	LF157A		HA-5160	Better DC
	LF355		HA-5170	Better DC
	LF355A		HA-5170	Better DC
	LF356		HA-5170	Better DC
	LF356A		HA-5170	Better DC
	LF357		HA-5160	Better DC
	LF357A		HA-5160	Better DC
	LM108		HA-5135	Better AC and DC
	LM108A		HA-5135	Better AC and DC
	LM118		HA-2510	Unity gain stable
	LM124		HA-4741,HA-5154	Better AC
	LM148		HA-4741,HA-5154	Better AC
	LM208		HA-5135	Better AC and DC
	LM208A		HA-5135	Better AC and DC
	LM308		HA-5135	Better AC and DC
	LM308A		HA-5135	Better AC and DC
	LM318		HA-2515	Unity gain stable
	LM324		HA-4741,HA-5154	Better AC
	LM348		HA-4741,HA-5154	Better AC
	RC1556		HA-2605	Better AC and DC
	RC4131		HA-2605	Better AC
	RC4136		HA-4741	
	RC4531		HA-2505	Dielectric Isolation
	RC4741	HA-4741		Better AC
	RM1556		HA-2600	Better AC and DC
	RM4131		HA-2600	Better AC
	RM4136		HA-4741,HA-5154	
	RM4156		HA-4741,HA-5154	
	RM4531		HA-2500	Dielectric Isolation, Better AC
	RM4741	HA-4741		Better AC
RCA	CA3020			
	CA3100		HA-2620	
	CA6078		HA-5141	
	CD4016		HI-201	Better AC and DC
SIGNETICS	AM6012		HI-562A	Int. linearity, application resistors
			HI-5660	Int. linearity, application resistors
	DAC08		HI-5618	Faster, application resistors
	LF198		HA-2420	Improved performance
	LF398		HA-2425	Improved performance
	MC1408		HI-5618-5	Faster, application resistors
	MC1508		HI-5618-2	Faster, application resistors
	NE531		HA-2515	
	NE5532		HA-5102	Lower noise
	NE5533		HA-5112	Lower noise
	NE5534		HA-5135	
	NE5537		HA-2425-5	Lower power
			HA-5320-5	Faster
	NE5539		HA-2539	Better AC
	SE531		HA-2510	
	SE5532		HA-5102	Lower noise
	SE5533		HA-5112	Lower noise
	SE5534		HA-5135	
	SE5539		HA-2539	Better AC
SILICON-GENERAL	SG741		HA-2500	
SILICONIX	DG181		HI-381	Dielectric Isolation

Competitive Cross Reference Chart (Continued)

Manufacturer	Part Number	Harris Pin-for-Pin Replacement	Harris Closest Replacement	Harris Advantages
SILICONIX (cont.)	DG182		HI-381	Dielectric Isolation
	DG184		HI-384	Dielectric Isolation
	DG185		HI-384	Dielectric Isolation
	DG187		HI-387	Dielectric Isolation
	DG188		HI-387	Dielectric Isolation
	DG190		HI-390	Dielectric Isolation
	DG191		HI-390	Dielectric Isolation
	DG200A	HI-200		Dielectric Isolation
	DG201A	HI-201		Dielectric Isolation
	DG211		HI-201	Full temp range specified
	DG271		HI-201HS	Faster
	DG300A	HI-300		Dielectric Isolation
	DG301A	HI-301		Dielectric Isolation
	DG302A	HI-302		Dielectric Isolation
	DG303A	HI-303		Dielectric Isolation
	DG304A	HI-304		Dielectric Isolation
	DG305A	HI-305		Dielectric Isolation
	DG306A	HI-306		Dielectric Isolation
	DG307A	HI-307		Dielectric Isolation
	DG381A	HI-381		Dielectric Isolation
	DG384A	HI-384		Dielectric Isolation
	DG387A	HI-387		Dielectric Isolation
	DG390A	HI-390		Dielectric Isolation
	DG5040	HI-5040		Dielectric Isolation
	DG5041	HI-5041		Dielectric Isolation
	DG5042	HI-5042		Dielectric Isolation
	DG5043	HI-5043		Dielectric Isolation
	DG5044	HI-5044		Dielectric Isolation
	DG5045	HI-5045		Dielectric Isolation
	DG506A	HI-506		Lower power, DI processing
	DG506AA	HI-506-2		Lower power, DI processing
	DG507A	HI-507		Lower power, DI processing
	DG507AA	HI-507-2		Lower power, DI processing
	DG508A	HI-508		Lower power, DI processing
	DG508AA	HI-508-2		Lower power, DI processing
	DG509A	HI-509		Lower power, DI processing
	DG509AA	HI-509-2		Lower power, DI processing
	SD5200		HI-201HS	Dielectric Isolation
SOLITRON	CM4016A		HI-201	Better AC and DC
	UC4000		HA-2600	
	UC4002		HA-2605	
SPRAGUE	ULN2139		HA-2600	
	ULN2151		HA-2600	
	ULN2156		HA-2600	
	ULN2157		HA-2650	
	ULN2158		HA-2650	
	ULN2171		HA-2600	
	ULN2172		HA-2620	
	ULN2173		HA-2600	
	ULN2174		HA-2620	
	ULN2175		HA-2600	
	ULN2176		HA-2600	
TELEDYNE PHILBRICK	1321	HA-2620		Identical
	1322	HA-2620		Identical
	1332	HA-2645		Identical
	1339		HA-2625	
	1341	HA-2540		Identical
	1342	HA-2539		Identical
	1343	HA-5190		Identical
	1344	HA-5160		Identical
	1345	HA-5162		Identical
	1346	HA-5180		Identical
	1347	HA-5180A		Identical
	1437		HA-2541	Monolithic
	1438		HA-2541	Monolithic
	1460		HA-2542	Monolithic
	1466		HA-2542	Monolithic
	4058		HI-5680	Monolithic
	4058-83		HI-5687	Monolithic
	4068A	HI-562A		Identical
	4084	HI-5618		Identical
	4088	HI-DAC16		Identical

Competitive Cross Reference Chart (Continued)

Manufacturer	Part Number	Harris Pin-for-Pin Replacement	Harris Closest Replacement	Harris Advantages
TELEDYNE PHILBRICK (cont.)	4189			
	4551	HI-547		Identical
	4552	HI-546		Identical
	4553	HI-549		Identical
	4554	HI-548		Identical
	4853		HA-5320	Monolithic, smaller pkg.
	4854		HA-2420	Faster, monolithic, smaller pkg.
	4856	HA-2420/25		Identical
	4857		HA-5320	Monolithic, smaller pkg., power
	4866	HA-5320		Identical
	DAC80I/V	HI-5680I/V		Identical
	TP5210		HI-674A	
	TP565A	HI-565A		Identical
	TP574A	HI-574A,HI-674A		Identical, 674A is 1.67 times faster
	TPADC85/87			
TEXAS INSTRUMENTS	MC1458		HA-5102	Lower noise
	MC1558		HA-5102	Lower noise
	TCM2912A	HC-5512		Lower noise, lower cross talk, lower power
	TCM4212+		HC-5502A or	Fewer external components
	TCM4201+		HC-5504	
	TCM4208= 3 chip set			
	TL022		HA-5142	Better DC
	TL044		HA-5144	Better DC
	TL061		HA-5141,HA-5151	Better DC, lower noise
	TL062		HA-5142,HA-5152	MIL range available
	TL064		HA-5144,HA-5154	MIL range available
	TL072		HA-5102	MIL range available
	TL074		HA-5104	MIL range available
	TL082		HA-5102	MIL range available
	TL084		HA-5104	MIL range available
TRANSITRON	TOA7709	HA-2600		
	TOA8709	HA-2605		

ANALOG

Military Programs

2

Harris Military Grade Levels

Mil-Std-883 describes several levels or "grades" of screening for microcircuits. Although basic circuit design and manufacturing process technology may be identical, differences in testing, documentation, and product assurance criteria are designed to guarantee the needed reliability levels for a particular application. Harris offers two basic levels of standard products.

MILITARY GRADE	APPLICATION
Class S	Spacecraft and other "Hi-Rel" systems which require long term reliability in a harsh environment. Applications are frequently life-critical and component replacement is costly or impossible. Harris class S or equivalent product is used in military, commercial, and scientific satellite systems as well as medical implantible and nuclear powerplant applications.
Class B	Military Systems for harsh applications requiring performance over an extended temperature range. Harris class B and equivalent product is used in aerospace, strategic, tactical, and secure communications systems as well as low priority space and commercial aircraft applications.

2

MILITARY PROGRAMS

Military Grade Product Offerings

Harris military grade product is offered in the following levels. For detailed process flows and specific quality and reliability information, refer to section 9.

- **JAN - JOINT ARMY NAVY**
  (Indicated by DESC Issued "Slash Sheet" Number)

  Fully compliant to Mil-Std-883. Changes must be approved by DESC who also maintains a continuing audit of manufacturing compliance. (class S and class B).

- **SMD - STANDARD MILITARY DRAWING**
  (Indicated by DESC Part Number)

  Fully compliant to Mil-Std-883. Changes must be approved by DESC (currently applies to class B only).

- **HARRIS CLASS B COMPLIANT**
  (Indicated by /883 Suffix on Harris Part Number)

  Fully compliant to Mil-Std-883.

- **HARRIS CLASS B "EQUIVALENT"**
  (Indicated by -8 Suffix on Harris Part Number)

  Exceptions to Mil-Std-883 per individual data sheet.

- **HARRIS CLASS S "EQUIVALENT"**
  (Indicated by -Q Suffix on Harris Part Number)

  Exceptions to Mil-Std-883 per individual data sheet.

Non-Standard Product Offerings

Harris understands the need for customer generated Source Control Drawings with non-standard parameter and/or screening requirements. A Customer Engineering Department is responsibile for efficiently expediting your SCDs through a comprehensive review process. The Customer Engineering Group compares your SCD to its closest equivalent grade device type and works closely with the Product Engineer, Manufacturing Engineer, Design Engineer, or applicable individual to compare Harris' screening ability against your non-standard requirement(s). For product processed to non-standard requirements, a unique part number suffix is assigned.

Harris shares the military's objective to utilize standards wherever possible. We recommend using our /883 data sheet as the guideline for your SCD's. In instances where an available military specification or Harris /883 datasheet is inappropriate, it is Harris' sincerest wish to work closely with the buyer in establishing an acceptable procurement document. For this reason, the customer is requested to contact the nearest Harris Sales Office or Representative before finalizing the Source Control Drawing. Harris looks forward to working with the customer prior to implementation of the formal drawing so that both parties may create a mutually acceptable procurement document.

Harris/883/JAN/DESC Part Number Listing

ANALOG PRODUCTS					
MARKETING PART #	**MIL-STD-883 †**	**JAN DRAWING #**	**JAN STATUS**	**DESC DRAWING**	**DESC STATUS**
OPERATIONAL AMPLIFIERS					
HA-2400	Yes			5962-87783	Pending
HA-2500	Yes	12204BGC	Approved		N/A
HA-2502	Yes				N/A
HA-2510	Yes	12205BGC	Approved		N/A
HA-2512	Yes				N/A
HA-2520	Yes	12206BGC	Approved		N/A
HA-2522	Yes				N/A
HA-2529	Yes	Preparing JAN			TBD
HA-2539	Yes			5962-87787	Pending
HA-2540	Yes			Preparing SMD	Pending
HA-2541	Yes			5962-87785	Pending
HA-2542	Yes			Preparing SMD	Pending
HA-2544	Yes			5962-89502	Pending
HA-2600	Yes	12202BGC	Approved		N/A
HA-2602	Yes				N/A
HA-2620	Yes	12203BGC	Approved		N/A
HA-2622	Yes				N/A
HA-2640	Yes			7800302	Approved
HA-4741	Yes			Preparing SMD	Pending
HA-5101	Yes			Preparing SMD	Pending
HA-5102	Yes			Preparing SMD	Pending
HA-5104	Yes			5962-88502	Pending
HA-5111	Yes			Preparing SMD	Pending
HA-5112	Yes			Preparing SMD	Pending
HA-5114	Yes			Preparing SMD	Pending
HA-5127	Yes			Preparing SMD	Pending
HA-5134	Yes			Preparing SMD	Pending
HA-5135	Yes			Preparing SMD	Pending
HA-5137	Yes			Preparing SMD	Pending
HA-5141	Yes			Preparing SMD	Pending
HA-5142	Yes			Preparing SMD	Pending
HA-5144	Yes			Preparing SMD	Pending
HA-5147	Yes			Preparing SMD	Pending
HA-5151	Yes			Preparing SMD	Pending
HA-5152	Yes			Preparing SMD	Pending
HA-5154	Yes			Preparing SMD	Pending
HA-5160	CY'89				N/A
HA-5162	CY'89				N/A
HA-5170	CY'89				N/A
HA-5177	Yes			Preparing SMD	Pending
HA-5180	CY'89				N/A
HA-5190	Yes			5962-87784	Pending
COMPARATOR					
HA-4902	Yes			5962-86860	Pending

† -8 is available in support of programs with part requirements dated prior to Dec. 31, 1984 in accordance with paragraph 1.2. of MIL-STD-883 or where 883 is not currently available.

Harris/883/JAN/DESC Part Number Listing

MARKETING PART #	MIL-STD-883 †	JAN DRAWING #	JAN STATUS	DESC DRAWING	DESC STATUS
ANALOG PRODUCTS (CONTINUED)					
SAMPLE AND HOLD					
HA-2420	Yes			8001601CA	Approved
HA-5330	Yes			5962-87677	In Process
BUFFERS					
HA-5033	Yes			Preparing SMD	Pending
HA-5002	Yes			Preparing SMD	Pending
TELECOMMUNICATIONS					
HC-55564	Yes				N/A
SWITCHES					
HI-200	Yes				N/A
HI-201	Yes	12302BEA	Approved		N/A
HI-201HS	Yes			5962-8671601EA	Approved
HI-222	Yes			Preparing SMD	Pending
HI-300	Yes				N/A
HI-301	Yes				N/A
HI-302	Yes				N/A
HI-303	Yes				N/A
HI-304	Yes				N/A
HI-305	Yes				N/A
HI-306	Yes				N/A
HI-307	Yes				N/A
HI-381	Yes				N/A
HI-384	Yes				N/A
HI-387	Yes				N/A
HI-390	Yes				N/A
HI-5040	Yes			8100609EA	Approved
HI-5041	Yes			8100610EA	Approved
HI-5042	Yes			8100611EA	Approved
HI-5043	Yes			8100612EA	Approved
HI-5044	Yes			8100613EA	Approved
HI-5045	Yes			8100614EA	Approved
HI-5046	Yes			8100615EA	Approved
HI-5046A	Yes			8100617EA	Approved
HI-5047	Yes			8100616EA	Approved
HI-5047A	Yes			8100618EA	Approved
HI-5048	Yes			8100619EA	Approved
HI-5049	Yes			8100620EA	Approved
HI-5050	Yes			8100621EA	Approved
HI-5051	Yes			8100622EA	Approved

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Harris/883/JAN/DESC Part Number Listing

MARKETING PART #	MIL-STD-883 †	JAN DRAWING #	JAN STATUS	DESC DRAWING	DESC STATUS
ANALOG PRODUCTS (CONTINUED)					
MULTIPLEXERS					
HI-1818A	Yes				N/A
HI-1828A	Yes				N/A
HI-506	Yes	19001B	Pending		N/A
HI-506A	See HI-546	19002B	Pending		N/A
HI-507	Yes	19003B	Pending		N/A
HI-507A	See HI-547	19004B	Pending		N/A
HI-508	Yes	19007B	Pending	7705201	Approved
HI-508A	See HI-548	19005B	Pending	7705202	Approved
HI-509	Yes	19008B	Pending		N/A
HI-509A	See HI-549	19006B	Pending		N/A
HI-516	Yes				N/A
HI-518	Yes				N/A
HI-524	Yes				N/A
HI-546	Yes			5962-8513101	Pending
HI-547	Yes			5962-8513102	Pending
HI-548	Yes			7705202	Pending
HI-549	Yes			5962-8513103	Pending
DIGITAL TO ANALOG CONVERTERS					
HI-562A	Yes				N/A
HI-565ATD	Yes				N/A
HI-565ASD	Yes				N/A
HI-5687V	Yes				N/A
HI-5697V	Yes				N/A
ANALOG TO DIGITAL CONVERTERS					
HI-574ATD	Yes			5962-8512704	In Process
HI-574ATE	Yes			5962-8512703	In Process
HI-574ASD	Yes				N/A
HI-574ASE	Yes				N/A
HI-674ATD	Yes			5962-88615	In Process
HI-674ATE	Yes				N/A
HI-674ASD	Yes				N/A
HI-674ASE	Yes				N/A
HI-774S	Yes				N/A
HI-774T	Yes				N/A
HI-774A	CY'89				N/A

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Military Product Program Controls

	REQUIREMENT	883 REFERENCE	JAN	DESC/SMD	/883	-8
SYSTEM CONTROLS	Product Assurance Plan	1.2.1.B.21	Per Appendix A of MIL M38510			Per Harris R&QA Manual
	Facility Certification	1.2.1.B.28	RADC/DESC	Harris QC	Harris QC	Harris QC
	Product Certification	1.2.1.B.26	RADC/DESC	RADC/DESC	Harris QA	Not Required
	Detail Specifications	1.2.1.A	Slash Sheet	DESC DWG/ SMD	Harris /883 Data Sheet	Harris Catalog
	Qualifying Activity	1.2.1.B.1	RADC/DESC	Harris	Harris	Harris
	Qualification Test GPC	1.2.1.B.17	Required	Per Governing Military Spec	Per Governing Military Spec	Per Harris Spec
	Qualification Test GPD	1.2.1.B.17	Required	Per Governing Military Spec	Per Governing Military Spec	Per Harris Spec
	QPL Listing		MIL M38510	None	None	None
	Change Controls	1.2.1.B.25	MIL M38510 para 3.4.2	DoD 480	DoD 480	Harris Internal ECN Controls
	Change Notification	1.2.1.B.25	DESC	DESC	Data Sheet Registration	Catalog
	Traceability	1.2.1.B.27	Wafer Lot	6 Week Seal	6 Week Seal	6 Week Seal
	Deviations to 883	1.2.1	Per Slash Sheet	Per DESC DWG/SMD	None	Per Harris Spec
	Product Construction	1.2.1.B.2-12	Compliant	Compliant	Compliant	May Be Non-Compliant
LOCATIONS	Fab		USA Only	USA	USA	USA
	Assembly		USA Only	USA/Malaysia	USA/Malaysia	Malaysia
	Screening		USA Only	USA/Malaysia	USA/Malaysia	Malaysia
	Quality Conformance		USA Only	USA	USA	Malaysia

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Harris Product Specification Highlights

Harris Semiconductor is a leading supplier of high reliability integrated circuits to the military and aerospace community and takes pride in offering products tailored to your most demanding applications requirements. Our facility is JAN-Certified to MIL-M-38510 and provides JAN-qualified and MIL-STD-883 products as standard data book items. This Analog Military Product Data Book contains detailed technical information on high-reliability integrated circuits presently available from Harris Semiconductor.

The intent of the /883 data sheet is to provide to our customers a clear understanding of the testing being performed in conformance with MIL-STD-883 requirements. Additionally, it is our intent to provide the most effective and comprehensive testing economically feasible.

This data book is organized by sections, similiar to the 1988 Harris Analog Industrial/Commercial Products Data Book. The darkened tab index distinguishes the major selections and provides a visual guide to the reader. Each section covers specific product line families, such as Operational Amplifiers, Comparators, Switches, Multiplexers, Data Conversion Products, S/H Amplifiers, and ASICs. Special attention should be given to Section 9 which emphasizes Harris committment to ongoing Quality and Reliability improvements used in all levels of production, test and documentation. Section 10 includes the Application Notes for devices that are MIL-STD-883 certified.

Document Control

Internally at Harris, each /883 data sheet has been established as a controlled document. Any revision or modification is signed-off throughout the manufacturing and engineering sections. Harris has made every effort to ensure accuracy of the information in this data book through quality control methods. Harris reserves the right to make changes to the products contained in this data book to improve performance, reliability and producibility. Each data sheet will use the printed date as the control revision means to the user. Harris has also established a Data Sheet Registration Program to inform the user of the most recent data sheet printing. Registration is done through the sign-up card attached to the back of this data book. Otherwise, contact Harris for the latest available specifications and performance data.

/883 Data Sheet Highlights

Each specific /883 data sheet documents the features, description, pinouts, tested electrical parameters, test circuits, burn-in circuits, die characteristics, packaging and design information. The following are notes and clarifications that will help in applying the information provided in the data sheet.

Packaging/Pinout

In addition to the packages offered for military products, Harris offers a complete line of package options for commercial and industrial applications. See our Analog Industrial/Commercial data book for more information. Harris utilizes MIL-M-38510, Appendix C for packages used for /883 product. The mechanical dimensions and material used are shown for each product to complete each data sheet as a self-contained document.

Thermal Information

Each /883 data sheet provides thermal information relating to both package and die. This information is intended for use in system designs to prevent exceeding maximum allowable temperature ratings.

D.C. and A.C. Electrical Parameters

Table 1 and 2 define the D.C. and A.C. Electrical Parameters that are 100% tested in production to guarantee compliance to MIL-STD-883. Subgroups used are defined in MIL-STD-883, Method 5005 and designated under the provisions of Paragraph 1.2.1a. Test Conditions and Test Circuits are provided for specific parameter testing.

Table 3 provides additional device limits that are guaranteed by characterization of the device and are not directly tested in production. Certain parameters such as noise voltage density and video characteristics have a sample plan used during production. Characterization data is on file and available demonstrating the test limits established.

Table 4 provides a summary of test requirements and applicable subgroups.

Burn-In Circuits

Burn-in circuits defined are those used in the actual production process. Burn-In is conducted per MIL-STD-883, Method 1015.

Design Information Sections

Harris provides an additional Design Information Section in each data sheet to assist in system application and design. The information may be provided under a 'Design Limit' column or in the form of performance curves under variable conditions. While this information cannot be guaranteed, it is based on actual characterization of the product and is representative of the data sheet device.

Programs Served By Harris

- Tube-Launched, Optically Tracked, Wire-Guided Missile
- Angle Rate Bombing Set
- Advanced Medium Range Air-To-Air Missile
- Advanced Capability (MK-48 Torpedo)
- Position Location and Reporting System
- Joint Tactical Information Distribution System
- Target Acquisition System (MK-23)
- Miniature Vehicle Sensors
- Driver's Thermal Viewer
- Detecting and Ranging Set
- Fighting Vehicle System (Bradley)
- Helicopter (or Hughes) Night Vision System
- Advanced Optic Adjunct
- Advanced Light Weight Torpedo
- Ground Launched Cruise Missile
- Air Launched Cruise Missile
- Medium Range Air-To-Surface Missile
- Modular Universal Laser Equipment
- Low Altitude Navigation and Targeting Infrared
- Anti-Submarine Warfare
- Multiple Launch Rocket System
- Advanced Self Protection Jammer
- Global Positioning System
- Distant Early Warning
- High Speed Anti-Radar Missile
- Rolling Airframe Missile
- Medium Depth Mine
- Terminal Guidance Small Missile
- Time Division Multiple Access
- Distributed Time Division Multiple Access
- Long Range Search and Track
- Glide Bomb Unit
- Divisional Air Defense
- Field Support Tracked Vehicle
- Integrated Solar Sensor Assembly
- Continuous Motion Gyro for ISSA
- Advanced Warning and Control System
- Forward Looking Infrared
- Ring Laser Gyro Programs
- Tail Warning System
- Space Telescope
- Mariner Series
- MK 46 NEARTIP
- AV8B HARRIER
- F14/A6E SMS
- Bearclaw
- CAINS II
- TAI/MK6
- B1
- F-16
- Phalanx
- Stinger
- Locust
- Sidearm
- Rattler
- Pavetack
- Viking
- Skylab
- Shuttle
- Intelsat
- Spacelab
- Voyager
- Mark 50
- Captor
- Maverick
- Phoenix

ANALOG

Operational Amplifiers & Comparators

3

3

OP AMPs & COMPARATORS

OPERATIONAL AMPLIFIER & COMPARATOR DATA SHEETS **PAGE**

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

HARRIS

HA-2400/883

PRAM Four Channel Programmable Operational Amplifier

January 1989

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Digital Programmability**
- **High Slew Rate (Uncompensated) .... 20V/μs Min**
  (Compensated) .... 6V/μs Min
- **Wide Gain Bandwidth**
  (Uncompensated) .... 20MHz Min
  (Compensated) .... 4MHz Min
- **High Gain .... 50kV/V Min**
- **Low Offset Current .... 50nA Max**
- **Single Capacitor Compensation For Unity Gain**
- **DTL/TTL Compatible Inputs**

Applications

- **Single Selection/Multiplexing**
- **Op Amp Gain Stage**
- **Frequency Oscillator**
- **Filter Characteristics**
- **Add-Subtract Functions**
- **Integrator Characteristics**
- **Comparator Levels**

Description

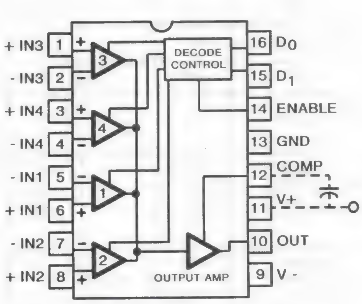
The HA-2400/883 is a four channel programmable amplifier providing a level of versatility unsurpassed by any other monolithic operational amplifier. Versatility is achieved by employing four input amplifier channels, any one (or none) of which may be electronically selected and connected to a single output stage through DTL/TTL compatible address inputs. The device formed by the output and the selected pair of inputs is an op amp which delivers excellent slew rate, gain bandwidth and power bandwidth performance. Other advantages features for these dielectrically isolated amplifiers include high voltage gain and input impedance coupled with low input offset voltage and offset current. External compensation is not required on this device at closed loop gains greater than 10.

Each channel of the HA-2400/883 can be controlled and operated with suitable feedback networks in any of the standard op amp configurations. This specialization makes these amplifiers excellent components for multiplexing, signal selection, and mathematical function designs. With 20V/μs slew rate, 20MHz gain bandwidth, and low input bias currents makes these devices ideal building blocks for signal generators, active filters, and data acquisition designs. Programmability coupled with 9mV maximum offset voltage and 50nA offset current makes these amplifiers outstanding components for the signal conditioning circuits.

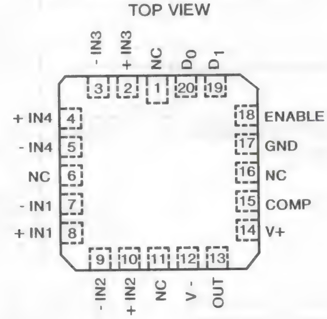
The HA-2400/883 is available in the 16 pin Dual-in-Line Ceramic package and a 20 pin LCC package. The HA-2400/883 is specified from -55°C to +125°C.

Pinouts

HA1-2400/883 (CERAMIC DIP)
TOP VIEW



HA4-2400/883 (CERAMIC LCC)
TOP VIEW



TRUTH TABLE

D_1	D_0	EN	SELECTED CHANNEL
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4
X	X	L	NONE

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 45V
Differential Input Voltage .... $\pm V_{SUPPLY}$
Voltage at Either Input Terminal .... V+ to V-
Digital Input Voltage .... -0.76V to +10V
Peak Output Current (Short Circuit Protected) ...... $I_{SC} < \pm 33mA$
Junction Temperature (T_J) .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... <2000V
Lead Temperature (Soldering 10 sec) .... +275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	91°C/W	25°C/W
Ceramic LCC Package	88°C/W	28°C/W

Internal Power Dissipation
Package Power Dissipation Limit at +75°C for $T_J \leq +175°C$
Ceramic DIP Package 1.11W
Ceramic LCC Package 1.14W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 11.1mW/°C
Ceramic LCC Package .... 11.4mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... +15V
Negative Supply Voltage .... -15V

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: V+ = +15V, V- = -15V, R_S = 100Ω, R_L = 500kΩ, V_O = 0V Unless Otherwise Specified.
Digital Inputs: V_{IL} = +0.5V, V_{IH} = +2.4V, Limits Apply to Each of the Four Channels, When Addressed.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Offset Voltage	V_{IO}	V_{CM} = 0V	1	+25°C	-9	9	mV
			2, 3	+125°C, -55°C	-11	11	mV
Input Bias Current	$+I_B$	V_{CM} = 0V $+R_S$ = 100kΩ $-R_S$ = 100Ω	1	+25°C	-200	200	nA
			2, 3	+125°C, -55°C	-400	400	nA
	$-I_B$	V_{CM} = 0V $+R_S$ = 100Ω $-R_S$ = 100kΩ	1	+25°C	-200	200	nA
			2, 3	+125°C, -55°C	-400	400	nA
Input Offset Current	I_{IO}	V_{CM} = 0V $+R_S$ = 100kΩ $-R_S$ = 100kΩ	1	+25°C	-50	50	nA
			2, 3	+125°C, -55°C	-100	100	nA
Common Mode Range	+CMR	V+ = +6V V- = -24V V_{OUT} = -9V	1	+25°C	9	-	V
			2, 3	+125°C, -55°C	9	-	V
	-CMR	V+ = +24V V- = -6V V_{OUT} = +9V	1	+25°C	-	-9	V
			2, 3	+125°C, -55°C	-	-9	V
Large Signal Voltage Gain	A_V	V_{OUT} = -10V to +10V	4	+25°C	50	-	kV/V
		R_L = 2kΩ	5, 6	+125°C, -55°C	25	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔV_{CM} = +5V +V = +10V -V = -20V V_{OUT} = -5V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	-CMRR	ΔV_{CM} = -5V +V = +20V -V = -10V V_{OUT} = +5V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
Output Voltage Swing	$+V_{OUT}$	R_L = 2kΩ	4	+25°C	+10	-	V
			5, 6	+125°C, -55°C	+10	-	V
	$-V_{OUT}$	R_L = 2kΩ	4	+25°C	-	-10	V
			5, 6	+125°C, -55°C	-	-10	V

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: V+ = +15V, V- = -15V, R_S = 100Ω, R_L = 500kΩ, V_O = 0V Unless Otherwise Specified.
Digital Inputs: V_{IL} = +0.5V, V_{IH} = +2.4V, Limits Apply to Each of the Four Channels, When Addressed

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current	$+I_{OUT}$	V_{OUT} = +10V	4	+25°C	+10	-	mA
	$-I_{OUT}$	V_{OUT} = -10V	4	+25°C	-	-10	mA
Supply Current	$+I_{CC}$	V_{OUT} = 0V	1	+25°C	-	6	mA
			2, 3	+125°C, -55°C	-	7	mA
	$-I_{CC}$	V_{OUT} = 0V	1	+25°C	-6	-	mA
			2, 3	+125°C, -55°C	-7	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = ±5V V+ = +20V, V- = -15V V+ = +10V, V- = -15V	1	+25°C	74	-	dB
			2, 3	+125°C, -55°C	74	-	dB
	-PSRR	ΔV_{SUP} = ±5V V+ = +15V, V- = -20V V+ = +15V, V- = -10V	1	+25°C	74	-	dB
			2, 3	+125°C, -55°C	74	-	dB
Crosstalk	C_T	V_{IN} = ±10V	1	+25°C	-80	-	dB
Digital Logic Current	I_{IL}	V_{IL} = 0V	1	+25°C	-	1.5	mA
			2, 3	+125°C, -55°C	-	1.5	mA
	I_{IH}	V_{IH} = 5.0V	1	+25°C	-	1	µA
			2, 3	+125°C, -55°C	-	1	µA

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: V+ = +15V, V- = -15V, R_L = 2kΩ, C_{LOAD} = 50pF, Unless Otherwise Specified.
Subscript 1 Refers to A_V = +1, C_{COMP} = 15pF
Digital Inputs: V_{IL} = +0.5V, V_{IH} = +2.4V, Limits Apply to Each of the Four Channels, When Addressed.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Slew Rate$_1$	$+SR_1$	V_{OUT} = -5V to +5V	7	+25°C	6	-	V/µs
	$-SR_1$	V_{OUT} = +5V to -5V	7	+25°C	6	-	V/µs
Rise & Fall Time	T_{R1}	V_{OUT} = 0 to +200mV	7	+25°C	-	45	ns
	T_{F1}	V_{OUT} = 0 to -200mV	7	+25°C	-	45	ns
Overshoot	$+OS_1$	V_{OUT} = 0 to +200mV	7	+25°C	-	40	%
	$-OS_1$	V_{OUT} = 0 to -200mV	7	+25°C	-	40	%

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: V+ = +15V, V- = -15V, Unless Otherwise Specified.
Subscript 2 Refers to A_V = +10, C_{COMP} = 0pF

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Unity Gain Bandwidth	$UGBW_1$	A_V = +1, C_{COMP} = 15pF R_L = 2kΩ, C_L = 50pF	1	+25°C	4	-	MHz
Gain Bandwidth Product	$GBWP_2$	A_V = +10, C_{COMP} = 0pF R_L = 2kΩ, C_L = 50pF	1	+25°C	20	-	MHz
Full Power Bandwidth$_1$	$FPBW_1$	R_L = 2kΩ, A_V = +1V, V_O = ±10V, C_L = 50pF, C_{COMP} = 15pF	1, 2	+25°C	95	-	kHz
Full Power Bandwidth$_2$	$FPBW_2$	R_L = 2kΩ, A_V = +10V, V_O = ±10V, C_L = 50pF, C_{COMP} = 0pF	1, 2	+25°C	300	-	kHz
Settling Time	T_{SET1}	A_V = +1, C_{COMP} = 15pF R_L = 2kΩ, C_L = 50pF, V_O = 10V_{p-p}, to 0.1% F.V. Logic Control = +5.0V	1	+25°C	-	2.5	µs
Slew Rate$_2$	$+SR_2$	V_{OUT} = -5V to +5V R_L = 2kΩ, C_L = 50pF, A_V = +10, C_{COMP} = 0pF	1	+25°C	20	-	V/µs
	$-SR_2$	V_{OUT} = +5V to -5V R_L = 2kΩ, C_L = 50pF, A_V = +10, C_{COMP} = 0pF	1	+25°C	20	-	V/µs
Output Delay	T_{DEL}	R_L = 2kΩ, C_L = 50pF, C_{COMP} = 15pF, V_{IN} = +5V	1	+25°C	-	250	ns
Minimum Closed Loop Stability	CLS_1	R_L = 2kΩ, C_L = 50pF, C_{COMP} = 15pF	1	+25°C	1	-	V/V
	CLS_2	R_L = 2kΩ, C_L = 50pF, C_{COMP} = 0pF	1	+25°C	10	-	V/V

NOTES: 1. The parameters listed in this table are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

2. $FPBW = \frac{S.R.}{2\pi \text{ Vpeak}}$

TABLE 4. ELECTRICAL TEST REQUIREMENTS

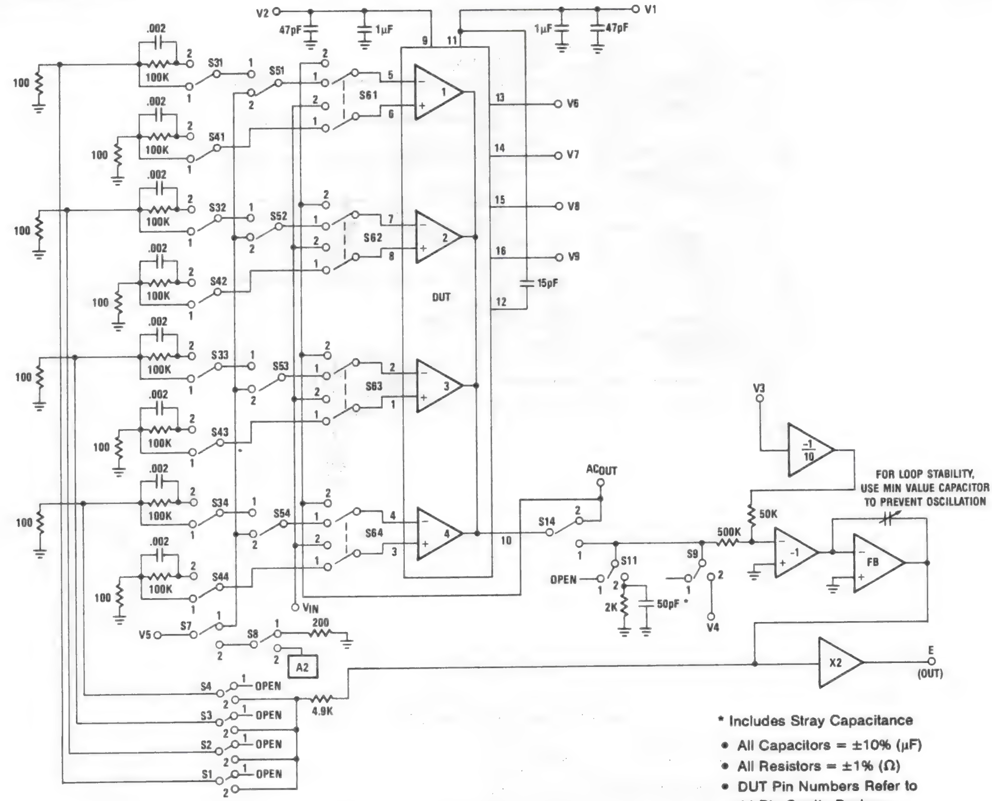
MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6, 7
Group A Test Requirements	1, 2, 3, 4, 5, 6, 7
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

The subgroup assignments of the parameters in these tables were patterned after DESC SMD #5962-87783.

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Test Circuit

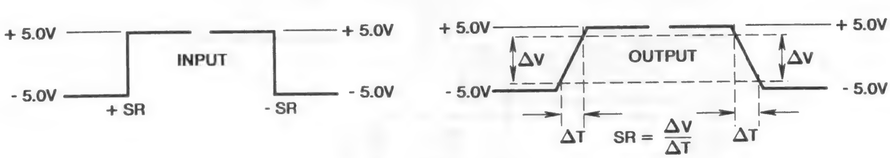


* Includes Stray Capacitance

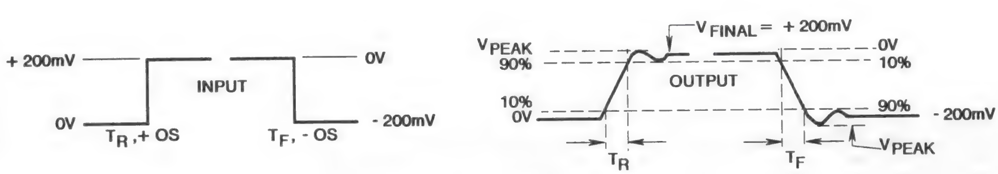
- All Capacitors = ±10% (μF)
- All Resistors = ±1% (Ω)
- DUT Pin Numbers Refer to 14 Pin Cerdip Package

For Detailed Information, Refer to HA-2400/883 Test Tech Brief

Test Waveforms



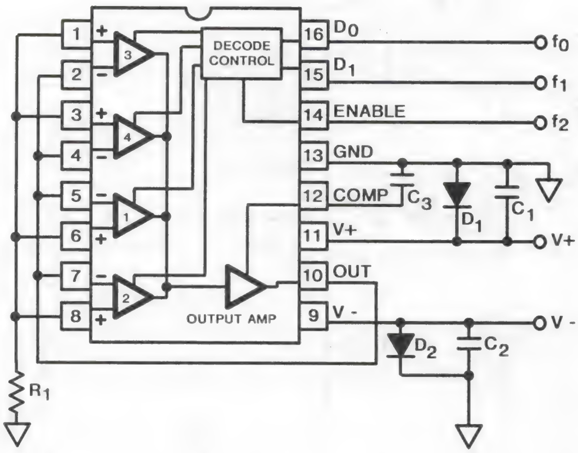
SLEW RATE WAVEFORMS



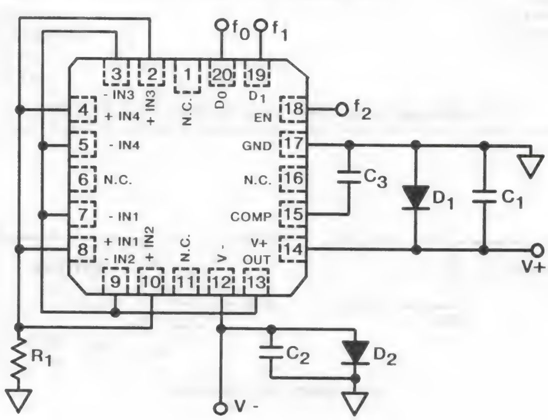
OVERSHOOT, RISE & FALL TIME WAVEFORMS

Burn-In Circuits

HA-2400/883 CERAMIC DIP



HA-2400/883 CERAMIC LCC



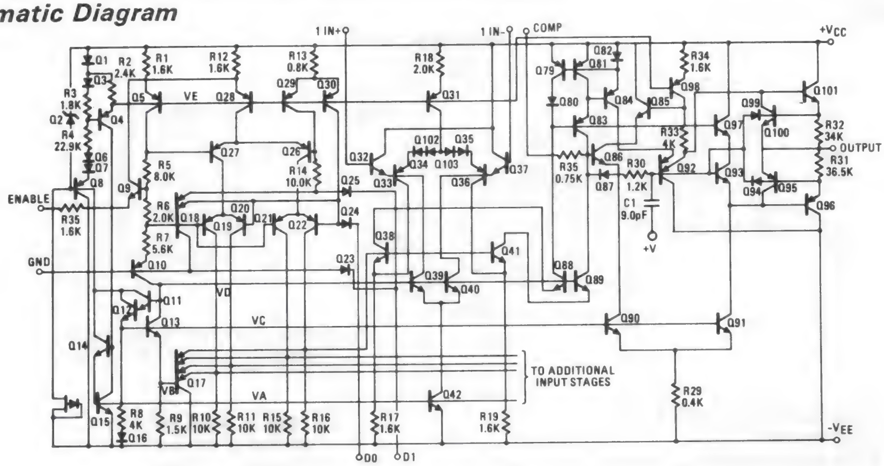
NOTES:

R_1 = 100kΩ/Socket, 5%, 1/4W (Min)
$C_1 = C_2$ = 0.01μF/Socket (Min) or 0.1μF/Row (Min)
C_3 = 0.001μF/Socket, 10%
$D_1 = D_2$ = 1N4002 or Equivalent/Board
$|(V+) - (V-)|$ = 30V

f_0 = 100kHz
f_1 = 50kHz
f_2 = 25kHz

50% Duty Cycle

Schematic Diagram



Die Characteristics

DIE DIMENSIONS:
88 x 67 x 19 mils
(2240 x 1710 x 483μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

SUBSTRATE POTENTIAL (POWERED UP): Unbiased

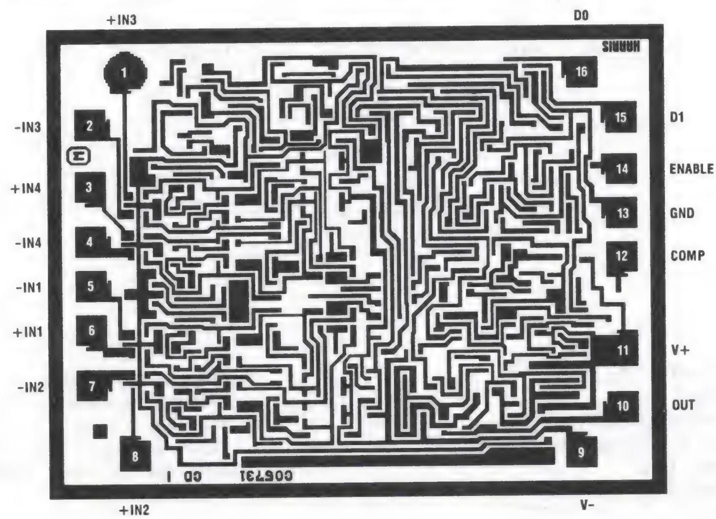
DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:
$0.7 \times 10^5 A/cm^2$

ACTIVE DEVICE COUNT: 251

Metallization Mask Layout

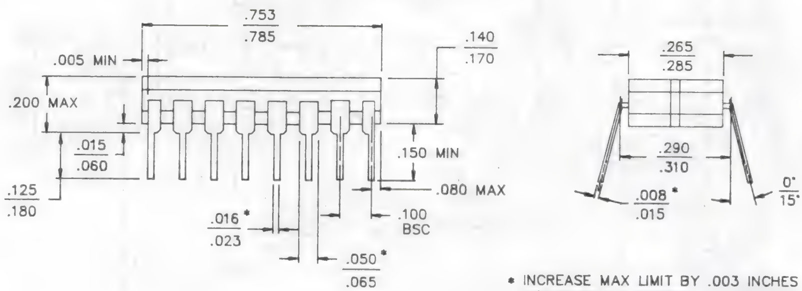
HA-2400/883



NOTE: Pin Numbers Correspond to DIP Package Only.

Packaging†

16 PIN CERAMIC DIP

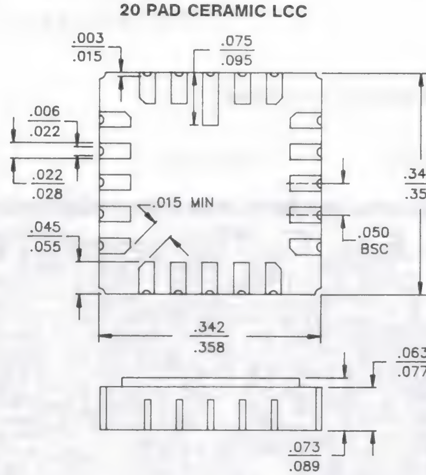


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-2

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

HA-2400

DESIGN INFORMATION

PRAM Four Channel Programmable Operational Amplifier

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Devices Characterized at: $V_S = \pm 15V$, $V_{IL} = +0.5V$, $V_{IH} = +2.4V$. Values Apply to Each of Four Channels When Addressed.

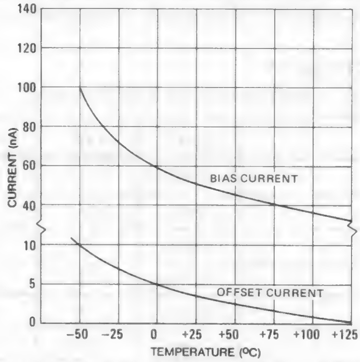
PARAMETERS	CONDITIONS	TEMP	TYP	UNITS
Offset Voltage	$V_{CM} = 0V$	+25°C	4	mV
Bias Current	$V_{CM} = 0V$	+25°C	50	nA
Offset Current	$V_{CM} = 0V$	+25°C	5	nA
Input Resistance		+25°C	30	MΩ
Large Signal Voltage Gain	$R_L = 2k\Omega$, $V_O = 20V_{p-p}$	+25°C	150	kV/V
Common Mode Rejection Ratio	$V_{CM} = \pm 5VDC$	Full	100	dB
Gain Bandwidth Product	$R_L = 2k\Omega$, $C_L = 50pF$, $C_{COMP} = 0pF$, $A_V = +10$	+25°C	40	MHz
Unity Gain Bandwidth	$R_L = 2k\Omega$, $C_L = 50pF$, $C_{COMP} = 15pF$, $A_V = +1$	+25°C	8	MHz
Output Voltage Swing	$R_L = 2k\Omega$	Full	±12	V
Output Current	$V_{OUT} = \pm 10V$	+25°C	20	mA
$FPBW_1$	Note 2, $V_P = 10V$	+25°C	475	kHz
$FPBW_2$	Note 2, $V_P = 10V$	+25°C	125	kHz
Rise Time	$R_L = 2k\Omega$, $C_L = 50pF$, $C_{COMP} = 15pF$, $A_V = +1$	+25°C	20	ns
Overshoot	$R_L = 2k\Omega$, $C_L = 50pF$, $C_{COMP} = 15pF$, $A_V = +1$	+25°C	25	%
Slew $Rate_1$	$A_V = +1V/V$	+25°C	8	V/µs
Slew $Rate_2$	$A_V = +10V/V$	+25°C	30	V/µs
Settling $Time_1$	$V_O = 10V_{p-p}$ to 0.1%	+25°C	1.5	µs
Digital Logic Current	$V_{IN} = +5.0V$	Full	5	nA
	$V_{IN} = 0V$	Full	1	mA
Output Delay	To 10% of Final Value	+25°C	100	ns
Crosstalk	Unselected Input to Output, $V_{IN} = \pm 10VDC$	+25°C	-110	dB
Supply Current	Not Loaded	+25°C	4.8	mA
PSRR	$\Delta V_S = \pm 10V$	Full	90	dB

DESIGN INFORMATION (Continued)

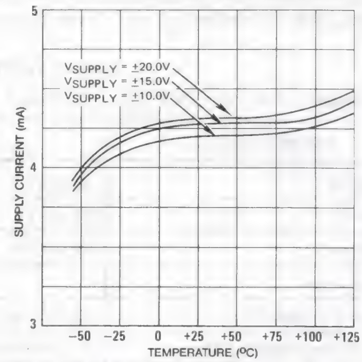
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: V± = ±15V, T_A = +25°C

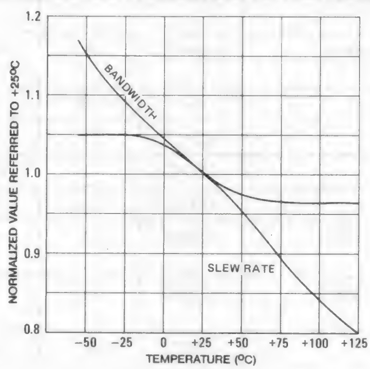
INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



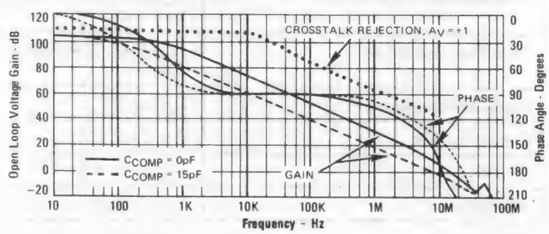
POWER SUPPLY CURRENT DRAIN AS A FUNCTION OF TEMPERATURE



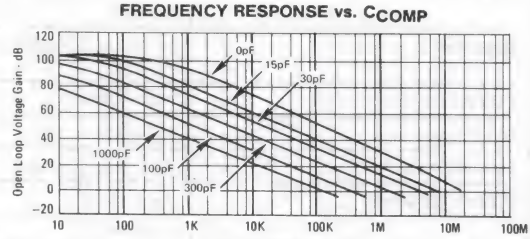
NORMALIZED A.C. PARAMETERS vs. TEMPERATURE



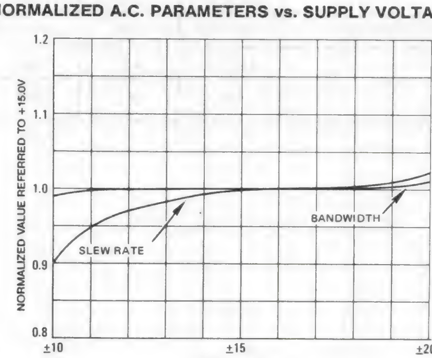
OPEN LOOP FREQUENCY AND PHASE RESPONSE



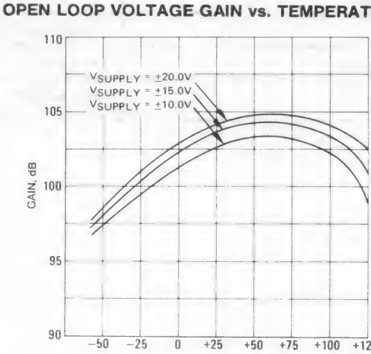
FREQUENCY RESPONSE vs. CCOMP



NORMALIZED A.C. PARAMETERS vs. SUPPLY VOLTAGE



OPEN LOOP VOLTAGE GAIN vs. TEMPERATURE

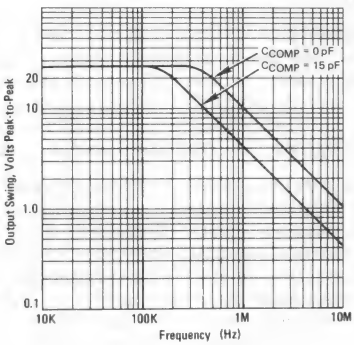


DESIGN INFORMATION (Continued)

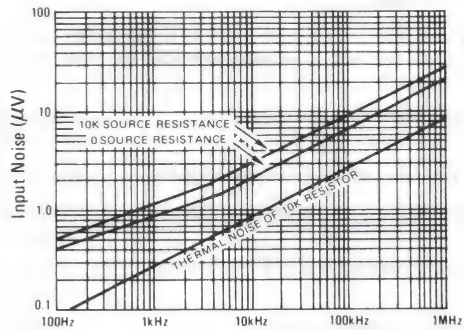
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: V± = ±15V, T_A = +25°C

OUTPUT VOLTAGE SWING



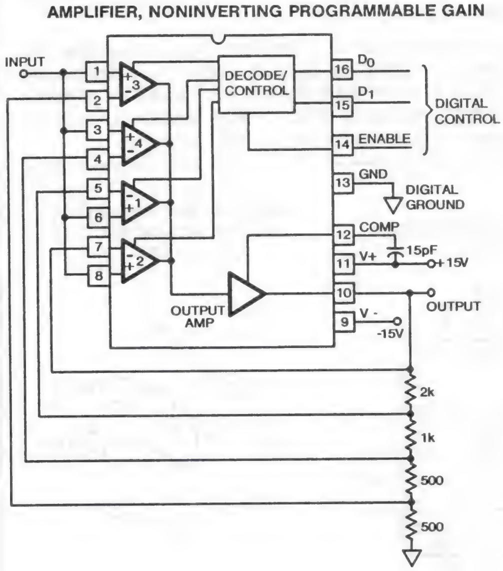
EQUIVALENT INPUT NOISE vs. BANDWIDTH



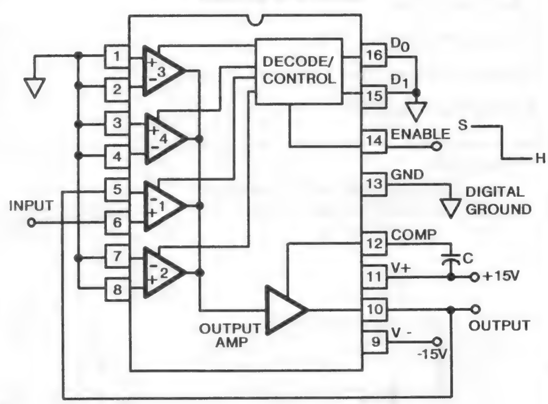
Upper 3dB Frequency
Lower 3dB Frequency - 10Hz
Broadband Noise Characteristics

Typical Applications (Also See Application Note 514 in the Harris Analog Data Book)

AMPLIFIER, NONINVERTING PROGRAMMABLE GAIN



SAMPLE AND HOLD



Sample Charging Rate $\frac{I_1}{C}$ V/sec

Hold Drift Rate $\frac{I_2}{C}$ V/sec

Switch Pedestal Error $\frac{Q}{C}$ Volts

$I_1 \approx 150 \times 10^{-6}$ A
$I_2 \approx 200 \times 10^{-9}$ A @ +25°C
$\approx 600 \times 10^{-9}$ A @ -55°C
$\approx 100 \times 10^{-9}$ A @ +125°C
$Q \approx 2 \times 10^{-12}$ Coulombs

HA-2500/883
HA-2502/883

Precision High Slew Rate Operational Amplifiers

January 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- High Slew Rate (HA-2500/883).......... 25V/μs Min, 30V/μs Typ
- Wide Power Bandwidth (HA-2500/883) .... 350kHz Min
- High Input Impedance (HA-2500/883)...... 25MΩ Min, 50MΩ Typ
- Low Offset Current (HA-2500/883) .... 25nA Max, 10nA Typ
- Low Quiescent Current.................... 6mA Max
- Fast Settling Time (0.1% of 10V Step) ..... 330ns Typ
- High Gain Bandwidth Product ....12MHz Typ
- Internally Compensated For Unity Gain Stability

Applications

- Data Acquisition Systems
- R.F. Amplifiers
- Video Amplifiers
- Signal Generators
- Pulse Amplification

Description

HA-2500/883 and HA-2502/883 comprise a series of monolithic operational amplifiers whose designs are optimized to deliver excellent slew rate, bandwidth, and settling time specifications. The outstanding dynamic features of this internally compensated device are complemented with low offset voltage and offset current.

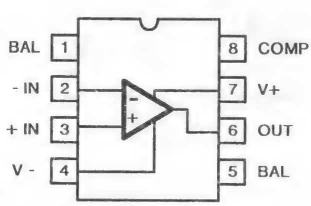
These dielectrically isolated amplifiers are ideally suited for applications such as data acquisition, R.F., video, and pulse conditioning circuits. Guaranteed slew rates of ±25V/μs minimum (HA-2500/883) and ± 20V/μs minimum (HA-2502/883) make these devices excellent components in fast, accurate data acquisition and pulse amplification designs. To insure compliance, all devices are 100% tested for A.C. performance characteristics over the full temperature limits.

A typical 12MHz gain bandwidth product and 500kHz full power bandwidth make these devices well suited to R.F. and video applications. With guaranteed offset voltages of 5mV (HA-2500/883) and 8mV (HA-2502/883) plus external offset trim flexibility and low offset current, these amplifiers are particularly useful components in signal conditioning designs.

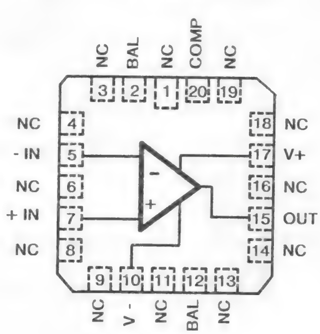
HA-2500/883 and HA-2502/883 are specified over the -55°C to +125°C temperature range. Both devices are available in 8 pin Metal Cans (TO-99) and 8 pin Ceramic Mini-DIP. The HA-2502/883 is also available in a 20 pin Ceramic Leadless Chip Carrier (LCC) package.

Pinouts

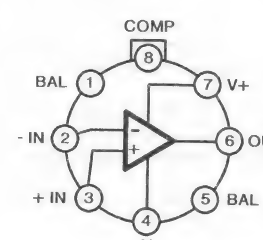
HA7-2500/883 (CERAMIC MINI-DIP)
HA7-2502/883 (CERAMIC MINI-DIP)
TOP VIEW



HA4-2502/883 (CERAMIC LCC)
TOP VIEW



HA2-2500/883 (METAL CAN)
HA2-2502/883 (METAL CAN)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40.0V
Differential Input Voltage 15.0V
Voltage at Either Input Terminal .... V+ to V-
Peak Output Current 50mA
Junction Temperature (T_J) .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... < 2000V
Lead Temperature (Soldering 10 sec) .... 275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	137°C/W	59°C/W
Ceramic LCC Package	74°C/W	24°C/W
Metal Can Package	139°C/W	42°C/W

Package Power Dissipation Limit at +75°C for $T_J \leq$ +175°C
Ceramic DIP Package 730mW
Ceramic LCC Package 1.35W
Metal Can Package 730mW

Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 7.4mW/°C
Ceramic LCC Package .... 13.5mW/°C
Metal Can Package .... 7.3mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±15V

$V_{INcm} \leq 1/2$ (V+ - V-)
$R_L \geq 2k\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	HA-2500/883 MIN	HA-2500/883 MAX	HA-2502/883 MIN	HA-2502/883 MAX	UNITS
Input Offset Voltage	V_{IO}	V_{CM} = 0V	1	+25°C	-5	5	-8	8	mV
			2, 3	+125°C, -55°C	-8	8	-10	10	mV
Input Bias Current	$+I_B$	V_{CM} = 0V $+R_S$ = 100kΩ $-R_S$ = 100Ω	1	+25°C	-200	200	-250	250	nA
			2, 3	+125°C, -55°C	-400	400	-500	500	nA
	$-I_B$	V_{CM} = 0V $+R_S$ = 100Ω $-R_S$ = 100kΩ	1	+25°C	-200	200	-250	250	nA
			2, 3	+125°C, -55°C	-400	400	-500	500	nA
Input Offset Current	I_{IO}	V_{CM} = 0V $+R_S$ = 100kΩ $-R_S$ = 100kΩ	1	+25°C	-25	25	-50	50	nA
			2, 3	+125°C, -55°C	-50	50	-100	100	nA
Common Mode Range	+CMR	V+ = 5V V- = -25V	1	+25°C	+10	-	+10	-	V
			2, 3	+125°C, -55°C	+10	-	+10	-	V
	-CMR	V+ = 25V V- = -5V	1	+25°C	-	-10	-	-10	V
			2, 3	+125°C, -55°C	-	-10	-	-10	V
Large Signal Voltage Gain	$+A_{VOL}$	V_{OUT} = 0V and +10V R_L = 2kΩ	4	+25°C	20	-	15	-	kV/V
			5, 6	+125°C, -55°C	15	-	10	-	kV/V
	$-A_{VOL}$	V_{OUT} = 0V and -10V R_L = 2kΩ	4	+25°C	20	-	15	-	kV/V
			5, 6	+125°C, -55°C	15	-	10	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔV_{CM} = +10V +V = +5V -V = -25V V_{OUT} = -10V	1	+25°C	80	-	74	-	dB
			2, 3	+125°C, -55°C	80	-	74	-	dB
	-CMRR	ΔV_{CM} = -10V +V = +25V -V = -5V V_{OUT} = +10V	1	+25°C	80	-	74	-	dB
			2, 3	+125°C, -55°C	80	-	74	-	dB

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	HA-2500/883		HA-2502/883		UNITS
					MIN	MAX	MIN	MAX	
Output Voltage Swing	$+V_{OUT}$	R_L = 2kΩ	4	+25°C	10	-	10	-	V
			5, 6	+125°C, -55°C	10	-	10	-	V
	$-V_{OUT}$	R_L = 2kΩ	4	+25°C	-	-10	-	-10	V
			5, 6	+125°C, -55°C	-	-10	-	-10	V
Output Current	$+I_{OUT}$	V_{OUT} = -10V	4	+25°C	10	-	10	-	mA
			5, 6	+125°C, -55°C	7.5	-	7.5	-	mA
	$-I_{OUT}$	V_{OUT} = +10V	4	+25°C	-	-10	-	-10	mA
			5, 6	+125°C, -55°C	-	-7.5	-	-7.5	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V	1	+25°C	-	6	-	6	mA
		I_{OUT} = 0mA	2, 3	+125°C, -55°C	-	6.5	-	7	mA
	$-I_{CC}$	V_{OUT} = 0V	1	+25°C	-6	-	-6	-	mA
		I_{OUT} = 0mA	2, 3	+125°C, -55°C	-6.5	-	-7	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = 10V +V = +20V, -V = -15V	1	+25°C	80	-	74	-	dB
		+V = +10V, -V = -15V	2, 3	+125°C, -55°C	80	-	74	-	dB
	-PSRR	ΔV_{SUP} = 10V +V = +15V, -V = -20V	1	+25°C	80	-	74	-	dB
		+V = +15V, -V = -10V	2, 3	+125°C, -55°C	80	-	74	-	dB
Offset Voltage Adjustment	$+V_{IO}Adj$	Note 4	1	+25°C	V_{IO}-1	-	V_{IO}-1	-	mV
			2, 3	+125°C, -55°C	V_{IO}-1	-	V_{IO}-1	-	mV
	$-V_{IO}Adj$	Note 4	1	+25°C	V_{IO}+1	-	V_{IO}+1	-	mV
			2, 3	+125°C, -55°C	V_{IO}+1	-	V_{IO}+1	-	mV

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_{VCL} = +1V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	HA-2500/883		HA-2502/883		UNITS
					MIN	MAX	MIN	MAX	
Slew Rate	+SR	V_{OUT} = -5V to +5V	7	+25°C	25	-	20	-	V/µs
			8A, 8B	+125°C, -55°C	20	-	15	-	V/µs
	-SR	V_{OUT} = +5V to -5V	7	+25°C	25	-	20	-	V/µs
			8A, 8B	+125°C, -55°C	20	-	15	-	V/µs
Rise & Fall Time	T_R	V_{OUT} = 0 to +200mV $10\% \leq T_R \leq 90\%$	7	+25°C	-	50	-	50	ns
			8A, 8B	+125°C, -55°C	-	60	-	60	ns
	T_F	V_{OUT} = 0 to -200mV $10\% \leq T_F \leq 90\%$	7	+25°C	-	50	-	50	ns
			8A, 8B	+125°C, -55°C	-	60	-	60	ns
Overshoot	+OS	V_{OUT} = 0 to +200mV	7	+25°C	-	40	-	50	%
			8A, 8B	+125°C, -55°C	-	50	-	60	%
	-OS	V_{OUT} = 0 to -200mV	7	+25°C	-	40	-	50	%
			8A, 8B	+125°C, -55°C	-	50	-	60	%

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	HA-2500/883		HA-2502/883		UNITS
					MIN	MAX	MIN	MAX	
Differential Input Resistance	R_{IN}	V_{CM} = 0V	1	+25°C	25	-	20	-	MΩ
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	+25°C	350	-	300	-	kHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 2kΩ, C_L = 50pF	1	-55°C to +125°C	1	-	1	-	V/V
Quiescent Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	195	-	210	mW

NOTES: 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).

3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)

4. Offset adjustment range is [$V_{IO(Measured)}$ ± 1mV] minimum referred to output. This test is for functionality only to assure adjustment through 0V.

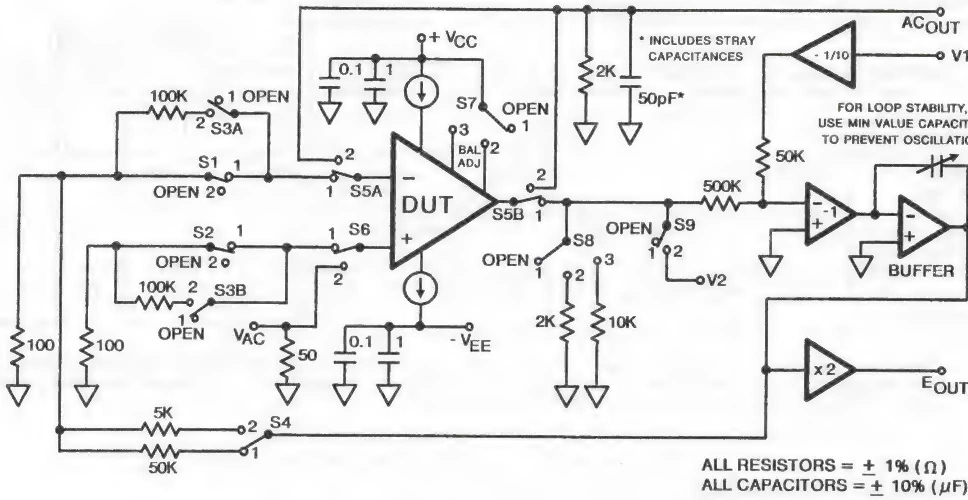
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6, 7, 8A, 8B
Group A Test Requirements	1, 2, 3, 4, 5, 6, 7, 8A, 8B
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

The Subgroup assignments of the parameters in these tables were patterned after Mil-M-38510/122, device type 04.

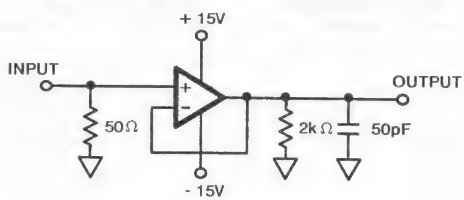
Test Circuit (Applies to Tables 1 and 2)



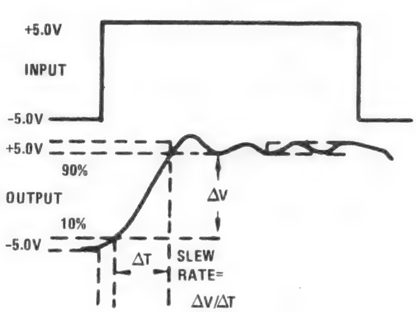
For Detailed Information, Refer to HA-2500/883; HA-2502/883 Test Tech Brief

Test Waveforms

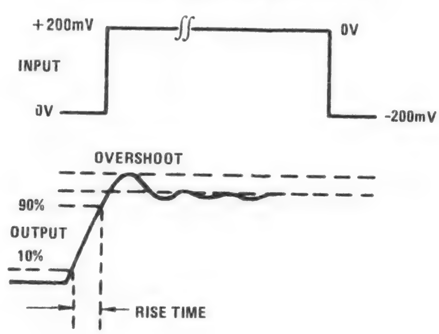
SIMPLIFIED TEST CIRCUIT (Applies to Table 2)



SLEW RATE WAVEFORM



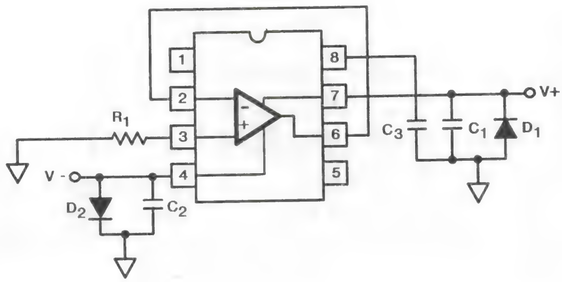
TRANSIENT RESPONSE WAVEFORM



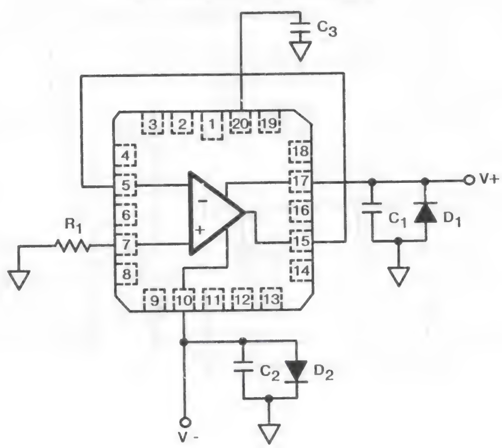
NOTE: Measured on both positive and negative transitions.
Capacitance at Compensation pin should be minimized.

Burn-In Circuits

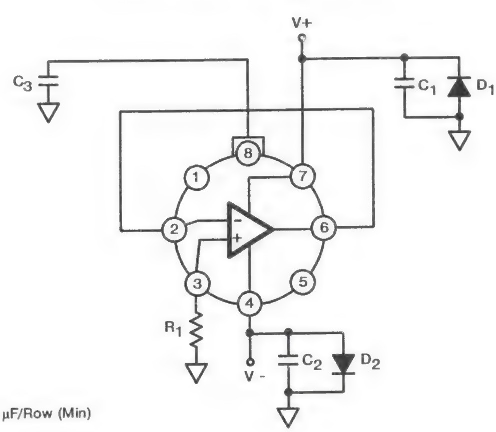
HA7-2500/883 CERAMIC DIP
HA7-2502/883 CERAMIC DIP



HA4-2502/883 CERAMIC LCC

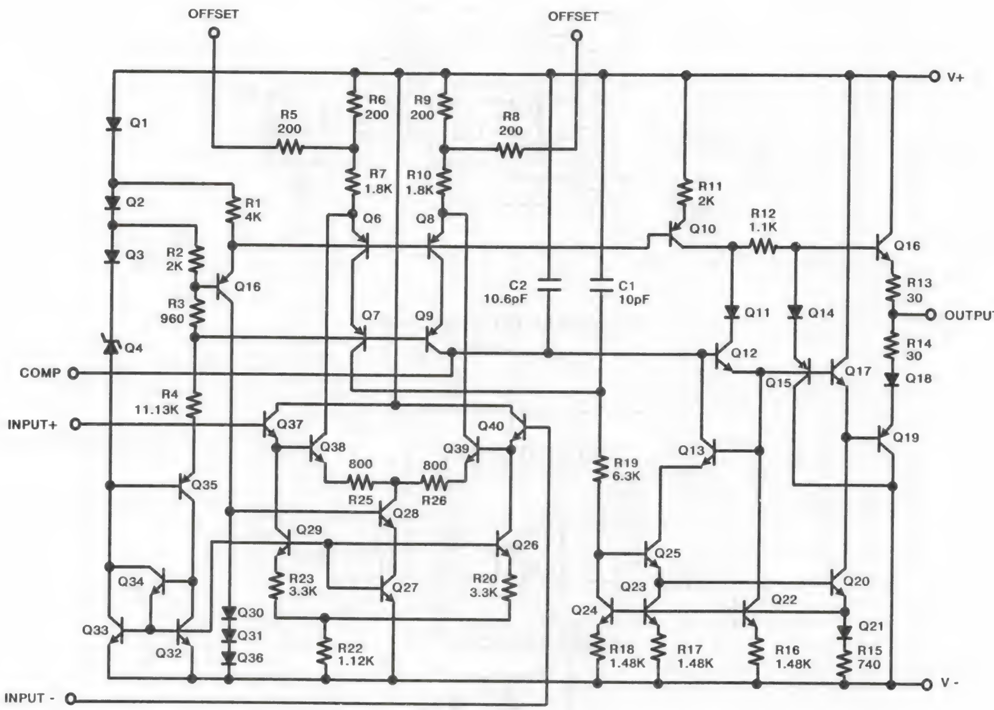


HA2-2500/883 (TO-99) METAL CAN
HA2-2502/883 (TO-99) METAL CAN



NOTES:
R_1 = 1MΩ, ±5%, 1/4W (Min)
$C_1 = C_2$ = 0.01μF/Socket (Min) or 0.1μF/Row (Min)
C_3 = 0.01μF/Socket (10%)
$D_1 = D_2$ = IN4002 or Equivalent/Board
$|(V+) - (V-)| = 30V$

Schematic Diagram



Die Characteristics

DIE DIMENSIONS:
65 x 57 x 19 mils
(1660 x 1950 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$0.3 \times 10^5 A/cm^2$

SUBSTRATE POTENTIAL (Powered Up):
Unbiased

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

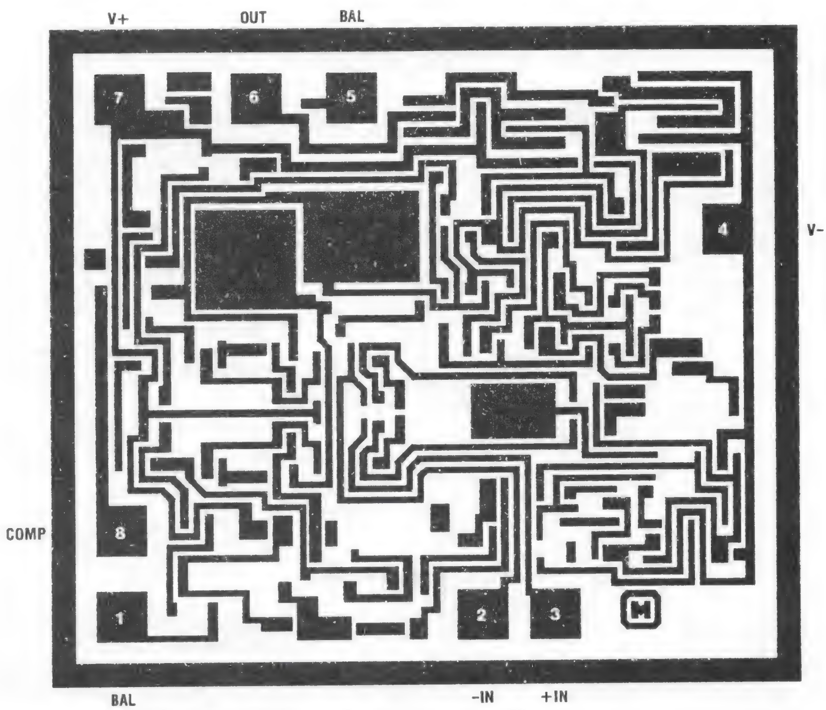
TRANSISTOR COUNT:
HA-2500/883: 40
HA-2502/883: 40

PROCESS: Std. Linear Bipolar Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)
Metal Can — 420°C (Max)

Metallization Mask Layout

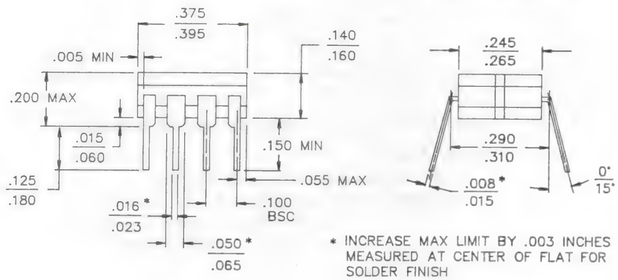
HA-2500/883 HA-2502/883



NOTE: Pad Numbers Correspond to 8 Lead Metal Can and Mini-DIP Packages Only.

Packaging †

8 PIN CERAMIC DIP

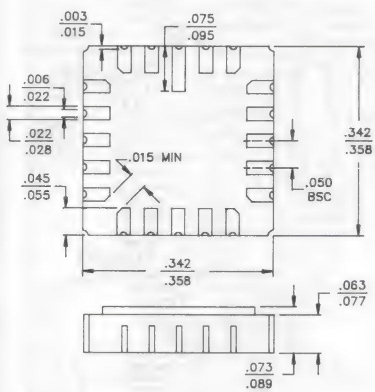


LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
- Material: Glass Frit
- Temperature: 450°C ± 10°C
- Method: Furnace Seal

INTERNAL LEAD WIRE:
- Material: Aluminum
- Diameter: 1.25 Mil
- Bonding Method: Ultrasonic

COMPLIANT OUTLINE: 38510 D-4

20 PAD CERAMIC LCC

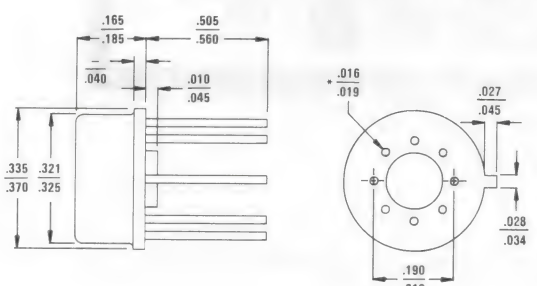


PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Ceramic, 90% Al_2O_3
PACKAGE SEAL:
- Material: Gold/Tin (80/20)
- Temperature: 320°C ± 10°C
- Method: Furnace Braze

INTERNAL LEAD WIRE:
- Material: Aluminum
- Diameter: 1.25 Mil
- Bonding Method: Ultrasonic

COMPLIANT OUTLINE: 38510 C-2

8 PIN TO-99 METAL CAN



LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
- Material: No Seal Material
- Temperature: Room Temperature
- Method: Resistance Weld

INTERNAL LEAD WIRE:
- Material: Aluminum
- Diameter: 1.25 Mil
- Bonding Method: Ultrasonic Bonded

COMPLIANT OUTLINE: 38510 A-1

*Dimension Maximum Limits Are Increased by 0.003 inches for Solder Dip Finish

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

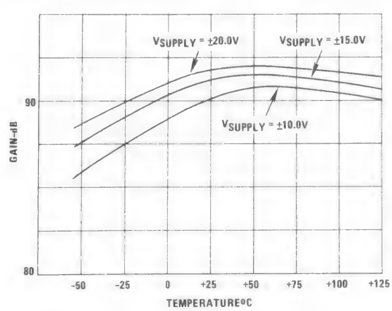
DESIGN INFORMATION

Precision High Slew Rate Operational Amplifiers

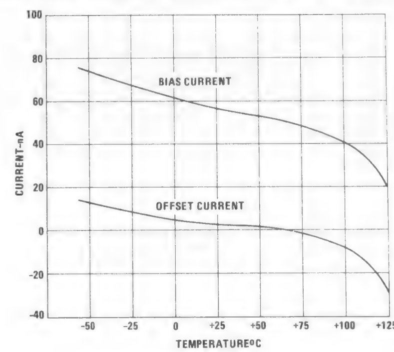
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

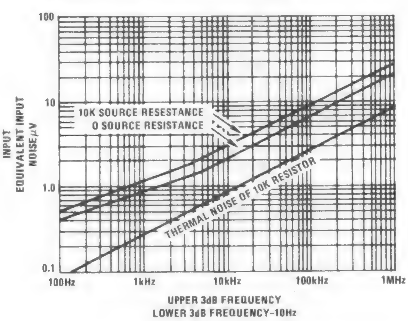
OPEN LOOP VOLTAGE GAIN vs. TEMPERATURE



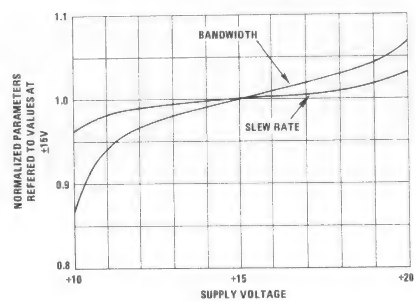
INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



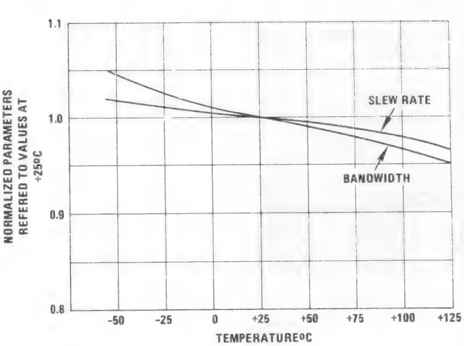
EQUIVALENT INPUT NOISE vs. BANDWIDTH



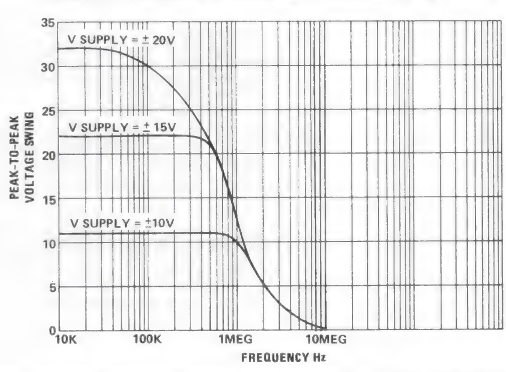
NORMALIZED A.C. PARAMETERS vs. SUPPLY VOLTAGE @ +25°C



NORMALIZED A.C. PARAMETERS vs. TEMPERATURE



OUTPUT VOLTAGE SWING vs. FREQUENCY @ +25°C

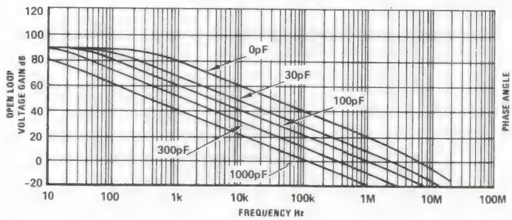


DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

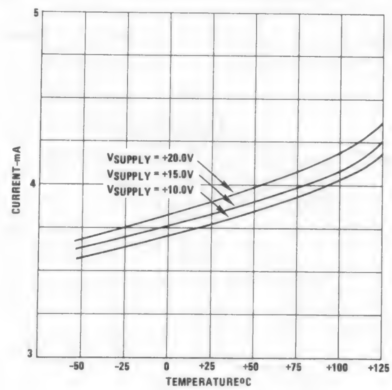
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND

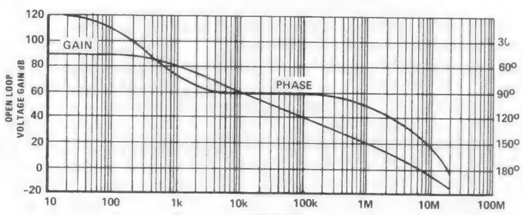


NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired.

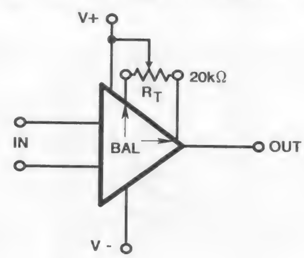
POWER SUPPLY CURRENT vs. TEMPERATURE



OPEN-LOOP FREQUENCY AND PHASE RESPONSE

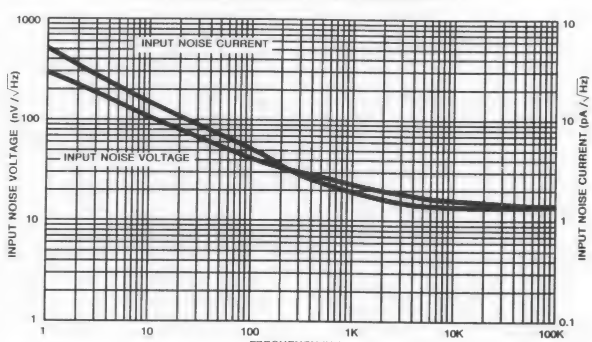


SUGGESTED V_{OS} ADJUSTMENT



Tested Offset Adjustment is $|V_{OS} + 1mV|$ Minimum Referred to Output.
Typical Range is ±8mV for $R_T = 20k\Omega$

INPUT NOISE DENSITY vs. FREQUENCY



DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: $V_S = \pm15V$, $R_L = 2K$, $C_L = 50pF$, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	HA-2500 TYPICAL	HA-2502 TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage	$V_{CM} = 0V$	+25°C	2	4	Table 1	mV
Offset Voltage Average Drift	$V_{CM} = 0V$	Full	20	20	30	μV/°C
Input Impedance		+25°C	50	50	Table 3	MΩ
Large Signal Voltage Gain	$V_{OUT} = \pm10V$	+25°C	30	25	Table 1	kV/V
CMRR	$V_{CM} = \pm10V$	Full	90	90	Table 1	dB
PSRR	$\Delta V_{Supply} = \pm10V$	Full	90	90	Table 1	dB
Gain Bandwidth Product	$A_V = \geq 10$	+25°C	12	12	10	MHz
Unity Gain Bandwidth	Small Signal ($\leq$ 200mV)	Full	8	8	6	MHz
Output Current	$V_O = \pm10V$	+25°C	±20	±20	Table 1	mA
Full Power Bandwidth	$V_O = \pm10V$, (Table 3, Note 2)	+25°C	500	500	Table 3	kHz
Rise/Fall Time	$V_O = \pm200mV$	+25°C	25	25	Table 2	ns
Overshoot	$V_O = \pm200mV$	+25°C	25	25	Table 2	%
Slew Rate	$V_O = \pm5V$	+25°C	±30	±30	Table 2	V/μs
Settling Time	10V Step to 0.1%	+25°C	330	330	500	ns
Output Resistance	Open Loop	+25°C	30	30	50	Ω
Minimum Supply Voltage	Functional Operation Only Other Parameters Will Vary	+25°C	±4	±4	±5	V

HARRIS

HA-2510/883
HA-2512/883

High Slew Rate Operational Amplifiers

January 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- High Slew Rate (HA-2510/883) .... 50V/μs Min, 65V/μs Typ
- Wide Power Bandwidth (HA-2510/883) .... 750kHz Min
- Low Offset Current (HA-2510/883) .... 25nA Min, 10nA Typ
- High Input Impedance (HA-2510/883) ... 50MΩ Min, 100MΩ Typ
- Wide Small Signal Bandwidth .... 12MHz Typ
- Fast Settling Time (0.1% of 10V Step) .... 250ns Typ
- Low Quiescent Supply Current .... 6mA Max
- Internally Compensated For Unity Gain Stability

Applications

- Data Acquisition Systems
- R. F. Amplifiers
- Video Amplifiers
- Signal Generators
- Pulse Amplification

Description

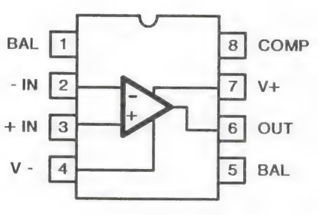
The HA-2510/883 and HA-2512/883 are a series of high performance operational amplifiers which set the standards for maximum slew rate and wide bandwidth operation in moderately powered, internally compensated, monolithic devices. In addition to excellent dynamic characteristics, these dielectrically isolated amplifiers also offer low offset current and high input impedance.

The ± 50V/μs minimum slew rate and fast settling time of the HA-2510/883 are ideally suited for high speed D/A, A/D, and pulse amplification designs. The HA-2510/883 and the HA-2512/883's superior bandwidth and 750KHz (HA-2510/883) minimum full power bandwidth are extremely useful in R. F. and video applications. To insure compliance with slew rate and transient response specifications, all devices are 100% tested for A. C. performance characteristics over full temperature limits. To improve signal conditioning accuracy, the HA-2510/883 provides a maximum offset current of 25nA and a minimum input impedance of 50MΩ, both at +25°C, as well as offset voltage trim capability.

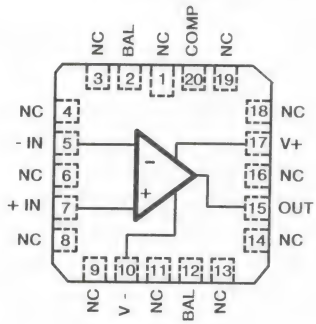
The HA-2510/883 and HA-2512/883 are available as MIL-STD-883 compliant devices screened to Class B level. These devices are sensitive to electrostatic discharge and are in microcircuit group number 49 (see MIL-M-38510, Appendix E). The HA-2510/883 and HA-2512/883 have guaranteed operation over the military temperature range from -55°C to +125°C and are available in TO-99, 8 pin Metal Can and Ceramic Mini-DIP packages. The HA-2512/883 is also available in a 20 pin LCC package.

Pinouts

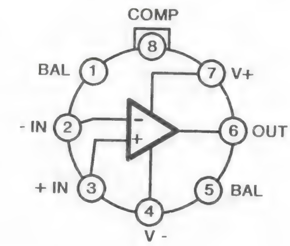
HA7-2510/883 (CERAMIC MINI-DIP)
HA7-2512/883 (CERAMIC MINI-DIP)
TOP VIEW



HA4-2512/883 (CERAMIC LCC)
TOP VIEW



HA2-2510/883 (METAL CAN)
HA2-2512/883 (METAL CAN)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage 15V
Voltage at Either Input Terminal .... V+ to V-
Peak Output Current 50mA
Junction Temperature (T_J) .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... < 2000V
Lead Temperature (Soldering 10 sec) .... 275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	137°C/W	59°C/W
Ceramic LCC Package	74°C/W	24°C/W
Metal Can Package	139°C/W	42°C/W

Package Power Dissipation Limit at +75°C for $T_J \leq$ +175°C
Ceramic DIP Package 730mW
Ceramic LCC Package 1.35W
Metal Can Package 730mW

Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 7.4mW/°C
Ceramic LCC Package .... 13.5mW/°C
Metal Can Package .... 7.3mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±15V
$V_{INcm} \leq$ 1/2 (V+ - V-)
$R_L \geq$ 2kΩ

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	HA-2510/883		HA-2512/883		UNITS
					MIN	MAX	MIN	MAX	
Input Offset Voltage	V_{IO}	V_{CM} = 0V	1	+25°C	-8	8	-10	10	mV
			2, 3	+125°C, -55°C	-10	10	-14	14	mV
Input Bias Current	$+I_B$	V_{CM} = 0V, $+R_S$ = 100kΩ, $-R_S$ = 100Ω	1	+25°C	-200	200	-250	250	nA
			2, 3	+125°C, -55°C	-400	400	-500	500	nA
	$-I_B$	V_{CM} = 0V, $+R_S$ = 100Ω, $-R_S$ = 100kΩ	1	+25°C	-200	200	-250	250	nA
			2, 3	+125°C, -55°C	-400	400	-500	500	nA
Input Offset Current	I_{IO}	V_{CM} = 0V, $+R_S$ = 100kΩ, $-R_S$ = 100kΩ	1	+25°C	-25	25	-50	50	nA
			2, 3	+125°C, -55°C	-50	50	-100	100	nA
Common Mode Range	+CMR	V+ = 5V, V- = -25V	1	+25°C	+10	-	+10	-	V
			2, 3	+125°C, -55°C	+10	-	+10	-	V
	-CMR	V+ = 25V, V- = -5V	1	+25°C	-	-10	-	-10	V
			2, 3	+125°C, -55°C	-	-10	-	-10	V
Large Signal Voltage Gain	$+A_{VOL}$	V_{OUT} = 0V and +10V, R_L = 2kΩ	4	+25°C	20	-	15	-	kV/V
			5, 6	+125°C, -55°C	15	-	10	-	kV/V
	$-A_{VOL}$	V_{OUT} = 0V and -10V, R_L = 2kΩ	4	+25°C	20	-	15	-	kV/V
			5, 6	+125°C, -55°C	15	-	10	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔV_{CM} = +10V, +V = +5V, -V = -25V, V_{OUT} = -10V	1	+25°C	80	-	74	-	dB
			2, 3	+125°C, -55°C	80	-	74	-	dB
	-CMRR	ΔV_{CM} = -10V, +V = +25V, -V = -5V, V_{OUT} = +10V	1	+25°C	80	-	74	-	dB
			2, 3	+125°C, -55°C	80	-	74	-	dB

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

3
OP AMPs & COMPARATORS

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	HA-2510/883 MIN	HA-2510/883 MAX	HA-2512/883 MIN	HA-2512/883 MAX	UNITS
Output Voltage Swing	$+V_{OUT}$	R_L = 2kΩ	4	+25°C	10	-	10	-	V
			5, 6	+125°C, -55°C	10	-	10	-	V
	$-V_{OUT}$	R_L = 2kΩ	4	+25°C	-	-10	-	-10	V
			5, 6	+125°C, -55°C	-	-10	-	-10	V
Output Current	$+I_{OUT}$	V_{OUT} = -10V	4	+25°C	10	-	10	-	mA
			5, 6	+125°C, -55°C	7.5	-	7.5	-	mA
	$-I_{OUT}$	V_{OUT} = +10V	4	+25°C	-	-10	-	-10	mA
			5, 6	+125°C, -55°C	-	-7.5	-	-7.5	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V, I_{OUT} = 0mA	1	+25°C	-	6	-	6	mA
			2, 3	+125°C, -55°C	-	6.5	-	7	mA
	$-I_{CC}$	V_{OUT} = 0V, I_{OUT} = 0mA	1	+25°C	-6	-	-6	-	mA
			2, 3	+125°C, -55°C	-6.5	-	-7	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = 10V, +V = +20V, -V = -15V, +V = +10V, -V = -15V	1	+25°C	80	-	74	-	dB
			2, 3	+125°C, -55°C	80	-	74	-	dB
	-PSRR	ΔV_{SUP} = 10V, +V = +15V, -V = -20V, +V = +15V, -V = -10V	1	+25°C	80	-	74	-	dB
			2, 3	+125°C, -55°C	80	-	74	-	dB
Offset Voltage Adjustment	$+V_{IO}Adj$	Note 4	1	+25°C	$V_{IO}-1$	-	$V_{IO}-1$	-	mV
			2, 3	+125°C, -55°C	$V_{IO}-1$	-	$V_{IO}-1$	-	mV
	$-V_{IO}Adj$	Note 4	1	+25°C	$V_{IO}+1$	-	$V_{IO}+1$	-	mV
			2, 3	+125°C, -55°C	$V_{IO}+1$	-	$V_{IO}+1$	-	mV

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_{VCL} = +1V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	HA-2510/883 MIN	HA-2510/883 MAX	HA-2512/883 MIN	HA-2512/883 MAX	UNITS
Slew Rate	+SR	V_{OUT} = -5V to +5V	7	+25°C	50	-	40	-	V/μs
			8A, 8B	+125°C, -55°C	45	-	35	-	V/μs
	-SR	V_{OUT} = +5V to -5V	7	+25°C	50	-	40	-	V/μs
			8A, 8B	+125°C, -55°C	45	-	35	-	V/μs
Rise & Fall Time	T_R	V_{OUT} = 0 to +200mV, $10\% \leq T_R \leq 90\%$	7	+25°C	-	50	-	50	ns
			8A, 8B	+125°C, -55°C	-	60	-	60	ns
	T_F	V_{OUT} = 0 to -200mV, $10\% \leq T_F \leq 90\%$	7	+25°C	-	50	-	50	ns
			8A, 8B	+125°C, -55°C	-	60	-	60	ns
Overshoot	+OS	V_{OUT} = 0 to +200mV	7	+25°C	-	40	-	50	%
			8A, 8B	+125°C, -55°C	-	50	-	60	%
	-OS	V_{OUT} = 0 to -200mV	7	+25°C	-	40	-	50	%
			8A, 8B	+125°C, -55°C	-	50	-	60	%

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	HA-2510/883		HA-2512/883		UNITS
					MIN	MAX	MIN	MAX	
Differential Input Resistance	R_{IN}	V_{CM} = 0V	1	+25°C	50	-	40	-	MΩ
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	+25°C	750	-	600	-	kHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 2kΩ, C_L = 50pF	1	-55°C to +125°C	1	-	1	-	V/V
Quiescent Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	195	-	210	mW

NOTES: 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).

3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)

4. Offset adjustment range is [$V_{IO(Measured)}$ ± 1mV] minimum referred to output. This test is for functionality only to assure adjustment through 0V.

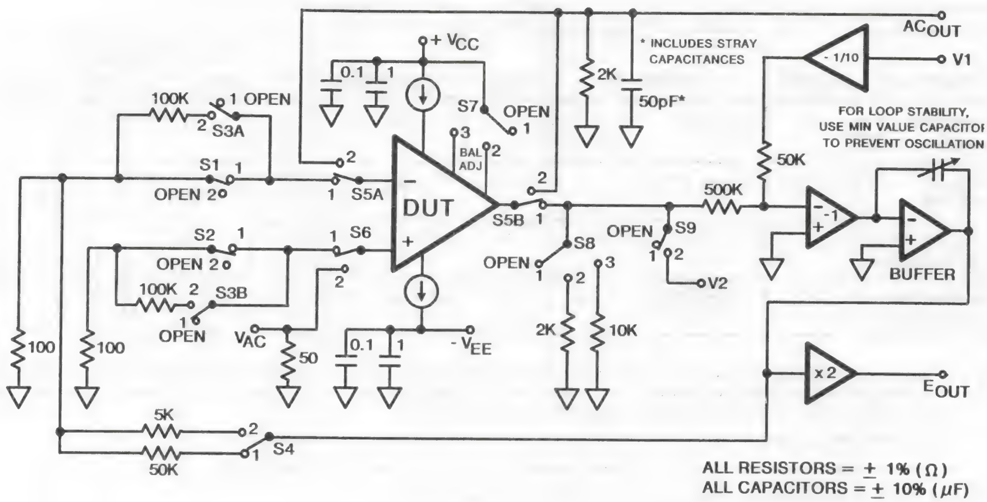
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6, 7, 8A, 8B
Group A Test Requirements	1, 2, 3, 4, 5, 6, 7, 8A, 8B
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

The Subgroup assignments of the parameters in these tables were patterned after Mil-M-38510/122, device type 05.

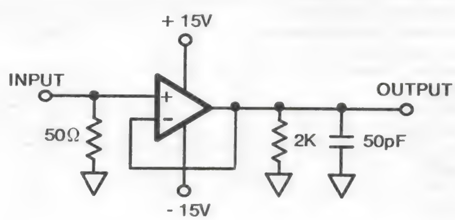
Test Circuit (Applies to Tables 1 and 2)



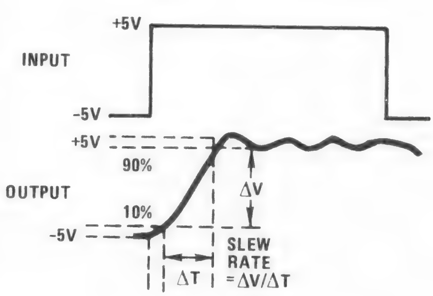
For Detailed Information, Refer to HA-2510/883; HA-2512/883 Test Tech Brief

Test Waveforms

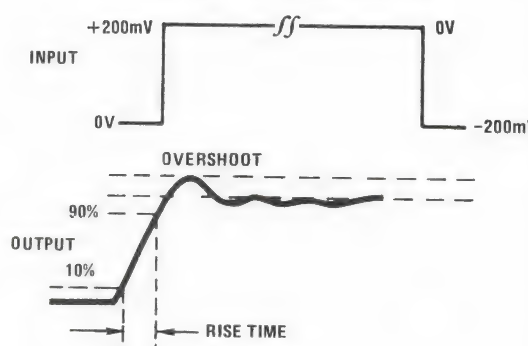
SIMPLIFIED TEST CIRCUIT (Applies to Table 2)



SLEW RATE WAVEFORM



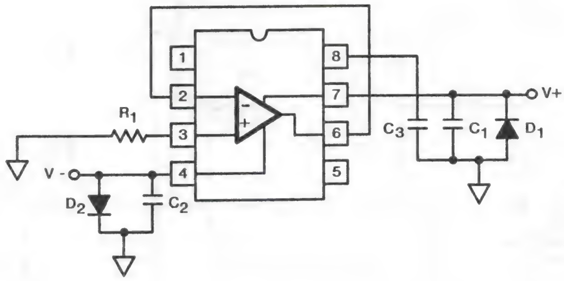
TRANSIENT RESPONSE WAVEFORM



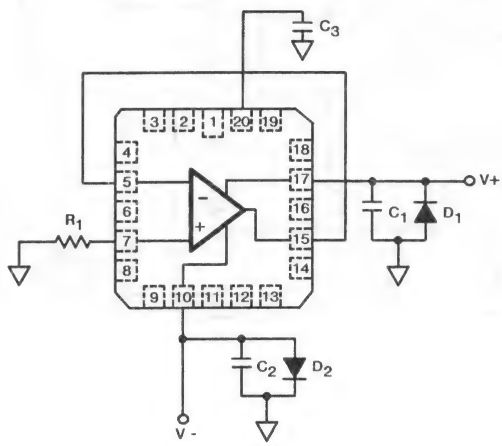
NOTE: Measured on both positive and negative transitions.
Capacitance at Compensation pin should be minimized.

Burn-In Circuits

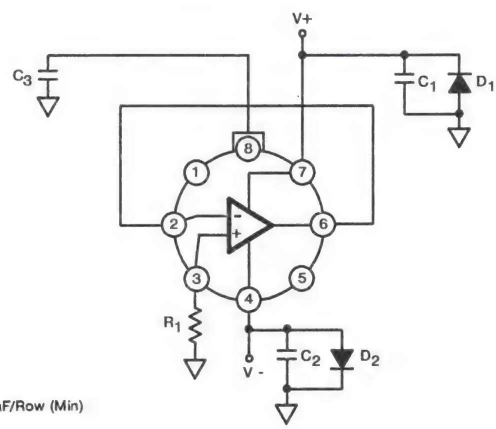
HA7-2510/883 CERAMIC MINI-DIP
HA7-2512/883 CERAMIC MINI-DIP



HA4-2512/883 CERAMIC LCC



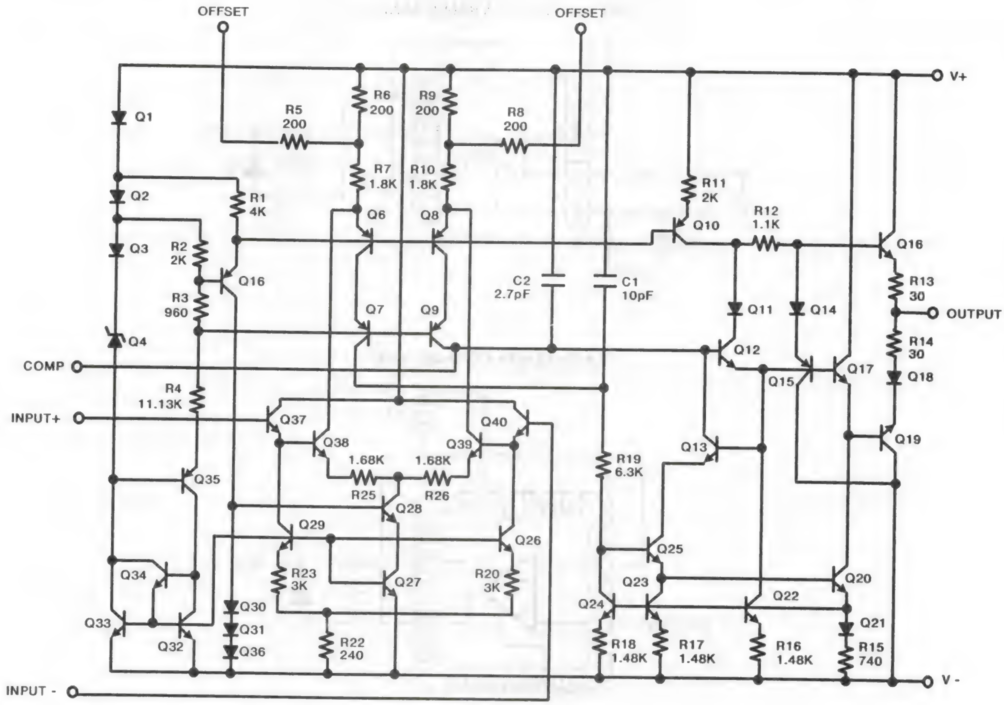
HA2-2510/883 (TO-99) METAL CAN
HA2-2512/883 (TO-99) METAL CAN



NOTES:
$R_1 = 1M\Omega$, ±5%, 1/4W (Min)
$C_1 = C_2 = 0.01\mu F$/Socket (Min) or $0.1\mu F$/Row (Min)
$C_3 = 0.01\mu F$/Socket (10%)
$D_1 = D_2$ = IN4002 or Equivalent/Board
$|(V+) - (V-)| = 30V$

3
OP AMPs & COMPARATORS

Schematic Diagram



Die Characteristics

DIE DIMENSIONS:
65 x 57 x 19 mils
(1660 x 1950 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$0.3 \times 10^5 A/cm^2$

SUBSTRATE POTENTIAL (Powered Up):
Unbiased

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

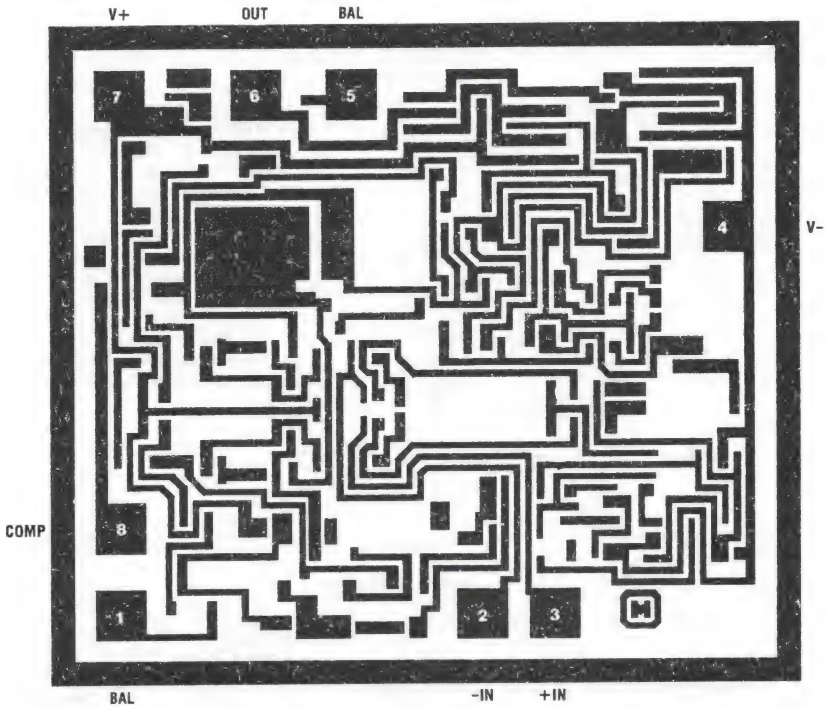
TRANSISTOR COUNT:
HA-2510/883: 40
HA-2512/883: 40

PROCESS: Std. Linear Bipolar Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)
Metal Can — 420°C (Max)

Metallization Mask Layout

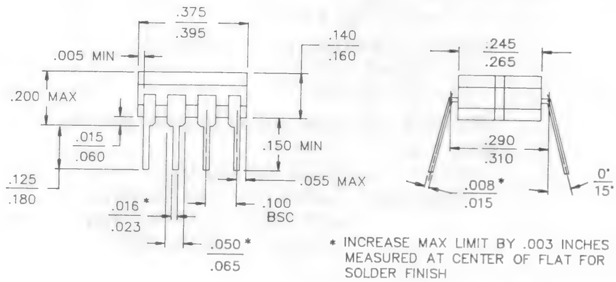
HA-2510/883 HA-2512/883



NOTE: Pin Numbers Correspond to 8 Lead Metal Can and Ceramic Mini-DIP Packages Only.

Packaging †

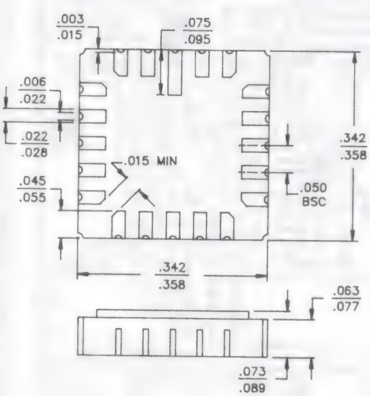
8 PIN CERAMIC DIP



* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

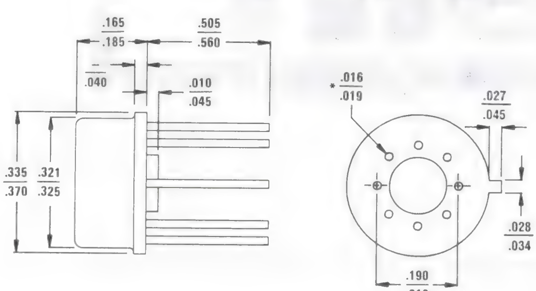
LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-4

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Ceramic, 90% Al_2O_3
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

8 PIN TO-99 METAL CAN



LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
Material: No Seal Material
Temperature: Room Temperature
Method: Resistance Weld
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic Bonded
COMPLIANT OUTLINE: 38510 A-1

*Dimension Maximum Limits Are Increased by 0.003 inches for Solder Dip Finish

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

HA-2510
HA-2512

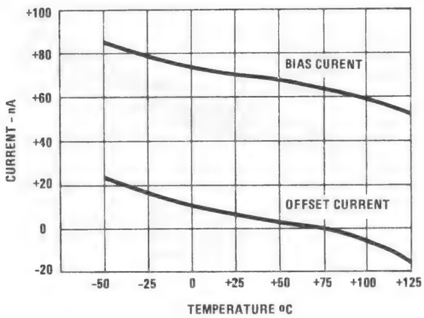
DESIGN INFORMATION

High Slew Rate Operational Amplifiers

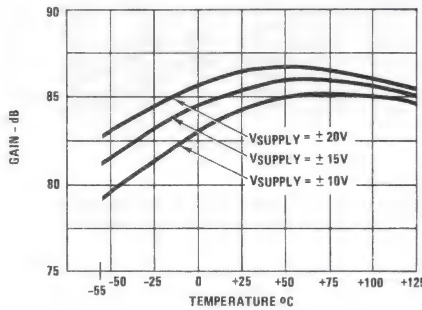
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

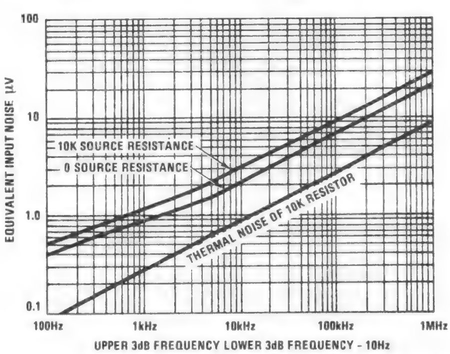
INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



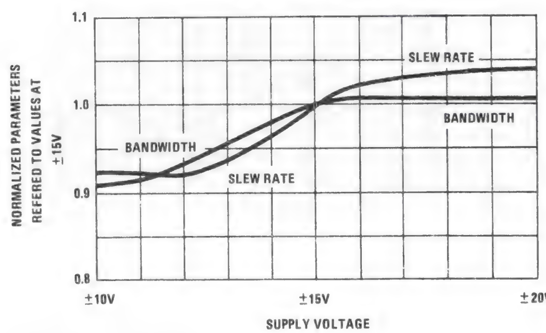
OPEN LOOP VOLTAGE GAIN vs. TEMPERATURE



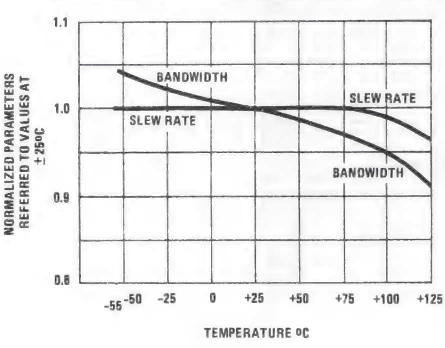
EQUIVALENT INPUT NOISE vs. BANDWIDTH



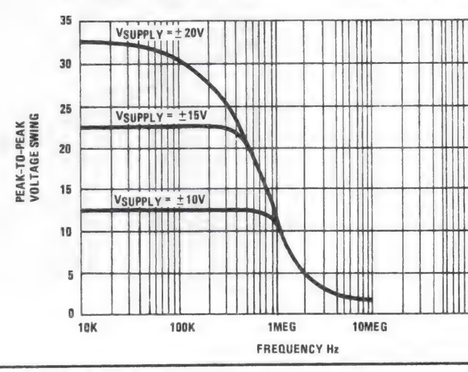
NORMALIZED A.C. PARAMETERS vs. SUPPLY VOLTAGE @ +25°C



NORMALIZED A.C. PARAMETERS vs. TEMPERATURE



OUTPUT VOLTAGE SWING vs. FREQUENCY @ +25°C

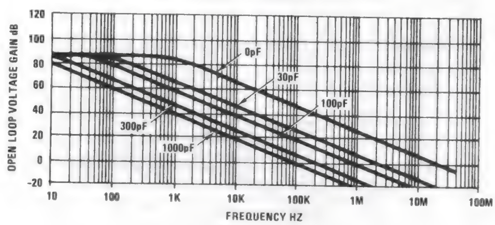


DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

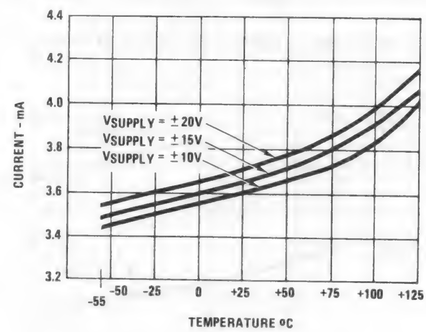
Typical Performance Curves
Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND

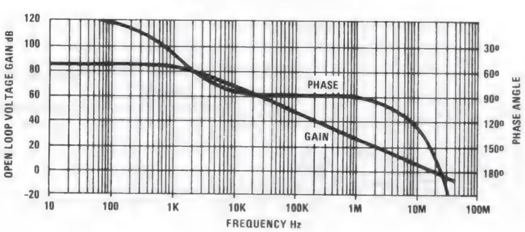


NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired.

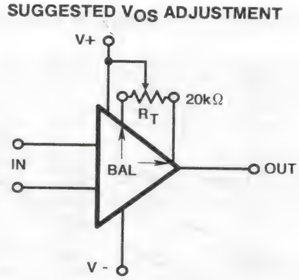
POWER SUPPLY CURRENT vs. TEMPERATURE



OPEN LOOP GAIN AND PHASE RESPONSE vs. FREQUENCY

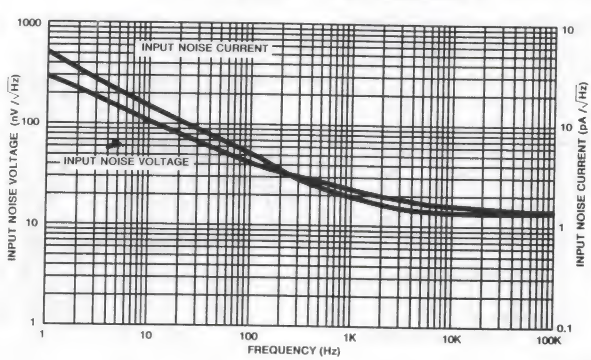


SUGGESTED V_{OS} ADJUSTMENT



Tested Offset Adjustment is $|V_{OS} + 1mV|$
Minimum Referred to Output.
Typical Range is ±8mV for R_T = 20kΩ

INPUT NOISE DENSITY vs. FREQUENCY



DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: $V_S = \pm15V$, $R_L = 2K$, $C_L = 50pF$, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	HA-2510 TYPICAL	HA-2512 TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage	$V_{CM} = 0V$	+25°C	2	4	Table 1	mV
Offset Voltage Average Drift	$V_{CM} = 0V$	Full	20	20	30	μV/°C
Input Impedance		+25°C	50	50	Table 3	MΩ
Large Signal Voltage Gain	$V_{OUT} = \pm10V$	+25°C	30	25	Table 1	kV/V
CMRR	$V_{CM} = \pm10V$	Full	90	90	Table 1	dB
PSRR	$\Delta V_{Supply} = \pm10V$	Full	90	90	Table 1	dB
Gain Bandwidth Product	$A_V = \geq 10$	+25°C	12	12	10	MHz
Unity Gain Bandwidth	Small Signal ($\leq$ 200mV)	Full	8	8	6	MHz
Output Current	$V_O = \pm10V$	+25°C	±20	±20	Table 1	mA
Full Power Bandwidth	$V_O = \pm10V$, (Table 3, Note 2)	+25°C	500	500	Table 3	kHz
Rise/Fall Time	$V_O = \pm200mV$	+25°C	25	25	Table 2	ns
Overshoot	$V_O = \pm200mV$	+25°C	25	25	Table 2	%
Slew Rate	$V_O = \pm5V$	+25°C	±30	±30	Table 2	V/μs
Settling Time	10V Step to 0.1%	+25°C	330	330	500	ns
Output Resistance	Open Loop	+25°C	30	30	50	Ω
Minimum Supply Voltage	Functional Operation Only Other Parameters Will Vary	+25°C	±4	±4	±5	V

HARRIS

HA-2520/883
HA-2522/883

Uncompensated, High Slew Rate Operational Amplifiers

January 1989

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **High Slew Rate (HA-2520/883) .... 100V/μs Min; 120V/μs Typ**
- **Wide Power Bandwidth (HA-2520/883) .... 1.5MHz Min**
- **Wide Gain Bandwidth (HA-2520/883) .... 10MHz Min; 20MHz Typ**
- **High Input Impedance (HA-2520/883) .... 50MΩ Min; 100MΩ Typ**
- **Low Offset Current (HA-2520/883) .... 25nA Min; 10nA Typ**
- **Fast Settling (0.1% of 10V Step) .... 200ns Typ**
- **Low Quiescent Supply Current .... 6mA Max**

Applications

- **Data Acquisition Systems**
- **R. F. Amplifiers**
- **Video Amplifiers**
- **Signal Generators**
- **Pulse Amplifiers**

Description

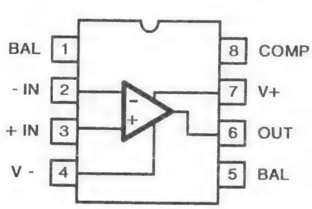
The HA-2520/883 and HA-2522/883 are monolithic operational amplifiers which deliver an unsurpassed combination of specifications for slew rate, bandwidth and settling time. These dielectrically isolated amplifiers are designed for closed loop gains of 3 or greater without external compensation. In addition, these high performance components also provide low offset current and high input impedance.

The 100V/μs (min) slew rate (80V/μs for HA-2522/883) and fast settling time of these amplifiers make them ideal components for pulse amplification and data acquisition designs. To insure compliance with slew rate and transient response specifications, all devices are 100% tested for A.C. performance characteristics over full temperature. These devices are valuable components for R. F. and video circuitry requiring wideband operation. For accurate signal conditioning designs, the HA-2520/883's superior dynamic specifications are complemented by 25nA (max) offset current (50nA for HA-2522/883) and offset voltage trim capability.

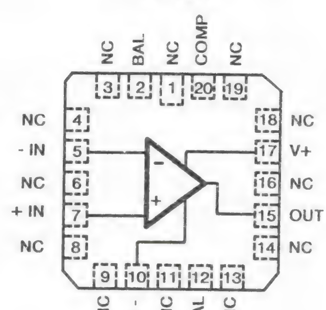
The HA-2520/883 and HA-2522/883 are available as MIL-STD-883 compliant devices screened to class B level. These devices are sensitive to electrostatic discharge and are in microcircuit group number 49 (see MIL-M-38510, Appendix E). The HA-2520/883 and HA-2522/883 have guaranteed operation over the military temperature range from -55°C to +125°C and are available in TO-99 Metal Can and Ceramic Mini-DIP packages. The HA-2522/883 is also available in a 20 pin LCC package.

Pinouts

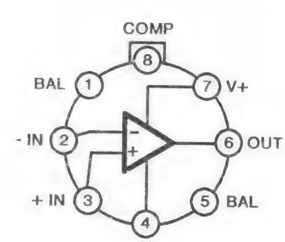
HA7-2520/883 (CERAMIC MINI-DIP)
HA7-2522/883 (CERAMIC MINI-DIP)
TOP VIEW



HA4-2522/883 (CERAMIC LCC)
TOP VIEW



HA2-2520/883 (METAL CAN)
HA2-2522/883 (METAL CAN)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage 15V
Voltage at Either Input Terminal .... V+ to V-
Peak Output Current 50mA
Junction Temperature (T_J) .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... < 2000V
Lead Temperature (Soldering 10 sec) .... 275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	140°C/W	65°C/W
Ceramic LCC Package	76°C/W	26°C/W
Metal Can Package	148°C/W	45°C/W

Package Power Dissipation Limit at +75°C for $T_J \leq$ +175°C
- Ceramic DIP Package 710mW
- Ceramic LCC Package 1.3W
- Metal Can Package 670mW

Package Power Dissipation Derating Factor Above +75°C
- Ceramic DIP Package .... 7.1mW/°C
- Ceramic LCC Package .... 13.1mW/°C
- Metal Can Package .... 6.7mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±15V
$V_{INcm} \leq 1/2$ (V+ - V-)
$R_L \geq 2k\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	HA-2520/883 MIN	HA-2520/883 MAX	HA-2522/883 MIN	HA-2522/883 MAX	UNITS
Input Offset Voltage	V_{IO}	V_{CM} = 0V	1	+25°C	-8	8	-10	10	mV
			2, 3	+125°C, -55°C	-10	10	-14	14	mV
Input Bias Current	$+I_B$	V_{CM} = 0V, $+R_S$ = 100kΩ, $-R_S$ = 100Ω	1	+25°C	-200	200	-250	250	nA
			2, 3	+125°C, -55°C	-400	400	-500	500	nA
	$-I_B$	V_{CM} = 0V, $+R_S$ = 100Ω, $-R_S$ = 100kΩ	1	+25°C	-200	200	-250	250	nA
			2, 3	+125°C, -55°C	-400	400	-500	500	nA
Input Offset Current	I_{IO}	V_{CM} = 0V, $+R_S$ = 100kΩ, $-R_S$ = 100kΩ	1	+25°C	-25	25	-50	50	nA
			2, 3	+125°C, -55°C	-50	50	-100	100	nA
Common Mode Range	+CMR	V+ = 5V, V- = -25V	1	+25°C	+10	-	+10	-	V
			2, 3	+125°C, -55°C	+10	-	+10	-	V
	-CMR	V+ = 25V, V- = -5V	1	+25°C	-	-10	-	-10	V
			2, 3	+125°C, -55°C	-	-10	-	-10	V
Large Signal Voltage Gain	$+A_{VOL}$	V_{OUT} = 0V and +10V, R_L = 2kΩ	4	+25°C	10	-	7.5	-	kV/V
			5, 6	+125°C, -55°C	7.5	-	5	-	kV/V
	$-A_{VOL}$	V_{OUT} = 0V and -10V, R_L = 2kΩ	4	+25°C	10	-	7.5	-	kV/V
			5, 6	+125°C, -55°C	7.5	-	5	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔV_{CM} = +10V, +V = +5V, -V = -25V, V_{OUT} = -10V	1	+25°C	80	-	74	-	dB
			2, 3	+125°C, -55°C	80	-	74	-	dB
	-CMRR	ΔV_{CM} = -10V, +V = +25V, -V = -5V, V_{OUT} = +10V	1	+25°C	80	-	74	-	dB
			2, 3	+125°C, -55°C	80	-	74	-	dB

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	HA-2520/883		HA-2522/883		UNITS
					MIN	MAX	MIN	MAX	
Output Voltage Swing	$+V_{OUT}$	R_L = 2kΩ	4	+25°C	10	-	10	-	V
			5, 6	+125°C, -55°C	10	-	10	-	V
	$-V_{OUT}$	R_L = 2kΩ	4	+25°C	-	-10	-	-10	V
			5, 6	+125°C, -55°C	-	-10	-	-10	V
Output Current	$+I_{OUT}$	V_{OUT} = -10V	4	+25°C	10	-	10	-	mA
			5, 6	+125°C, -55°C	7.5	-	7.5	-	mA
	$-I_{OUT}$	V_{OUT} = +10V	4	+25°C	-	-10	-	-10	mA
			5, 6	+125°C, -55°C	-	-7.5	-	-7.5	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V	1	+25°C	-	6	-	6	mA
		I_{OUT} = 0mA	2, 3	+125°C, -55°C	-	6.5	-	7	mA
	$-I_{CC}$	V_{OUT} = 0V	1	+25°C	-6	-	-6	-	mA
		I_{OUT} = 0mA	2, 3	+125°C, -55°C	-6.5	-	-7	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = 10V +V = +20V, -V = -15V	1	+25°C	80	-	74	-	dB
		+V = +10V, -V = -15V	2, 3	+125°C, -55°C	80	-	74	-	dB
	-PSRR	ΔV_{SUP} = 10V +V = +15V, -V = -20V	1	+25°C	80	-	74	-	dB
		+V = +15V, -V = -10V	2, 3	+125°C, -55°C	80	-	74	-	dB
Offset Voltage Adjustment	$+V_{IO}Adj$	Note 4	1	+25°C	V_{IO}-1	-	V_{IO}-1	-	mV
			2, 3	+125°C, -55°C	V_{IO}-1	-	V_{IO}-1	-	mV
	$-V_{IO}Adj$	Note 4	1	+25°C	V_{IO}+1	-	V_{IO}+1	-	mV
			2, 3	+125°C, -55°C	V_{IO}+1	-	V_{IO}+1	-	mV

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_{VCL} = +3V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	HA-2520/883		HA-2522/883		UNITS
					MIN	MAX	MIN	MAX	
Slew Rate	+SR	V_{OUT} = -5V to +5V	7	+25°C	100	-	80	-	V/µs
			8A, 8B	+125°C, -55°C	84	-	60	-	V/µs
	-SR	V_{OUT} = +5V to -5V	7	+25°C	100	-	80	-	V/µs
			8A, 8B	+125°C, -55°C	84	-	60	-	V/µs
Rise & Fall Time	T_R	V_{OUT} = 0 to +200mV 10% ≤ T_R ≤ 90%	7	+25°C	-	50	-	50	ns
			8A, 8B	+125°C, -55°C	-	55	-	60	ns
	T_F	V_{OUT} = 0 to -200mV 10% ≤ T_F ≤ 90%	7	+25°C	-	50	-	50	ns
			8A, 8B	+125°C, -55°C	-	55	-	60	ns
Overshoot	+OS	V_{OUT} = 0 to +200mV	7	+25°C	-	40	-	50	%
			8A, 8B	+125°C, -55°C	-	45	-	60	%
	-OS	V_{OUT} = 0 to -200mV	7	+25°C	-	40	-	50	%
			8A, 8B	+125°C, -55°C	-	45	-	60	%

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, $A_V \geq 3$, C_{COMP} = 0pF, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	HA-2520/883		HA-2522/883		UNITS
					MIN	MAX	MIN	MAX	
Differential Input Resistance	R_{IN}	V_{CM} = 0V	1	+25°C	50	-	40	-	MΩ
Gain Bandwidth Product	GBWP	V_O = 200mV, f_O = 10kHz	1	+25°C	10	-	10	-	MHz
		V_O = 200mV, f_O = 1MHz	1	+25°C	10		10		MHz
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	+25°C	1.6	-	1.2	-	MHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 2kΩ, C_L = 50pF	1	-55°C to +125°C	+3	-	+3	-	V/V
Quiescent Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	195	-	210	mW

NOTES: 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).

3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)

4. Offset adjustment range is [$V_{IO(Measured)}$ ± 1mV] minimum referred to output. This test is for functionality only to assure adjustment through 0V.

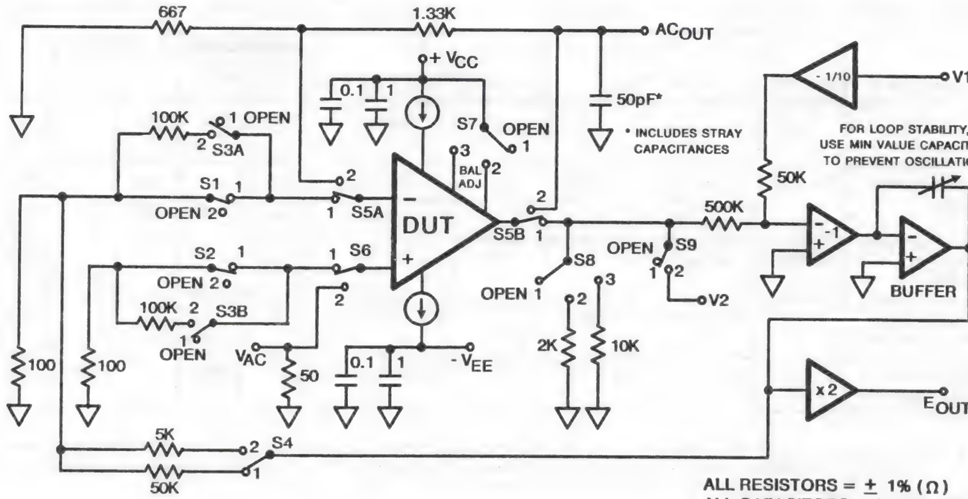
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6, 7, 8A, 8B
Group A Test Requirements	1, 2, 3, 4, 5, 6, 7, 8A, 8B
Groups C & D End Points	1

* PDA applies to Subgroup 1 only.

The Subgroup assignments of the parameters in these tables were patterned after MIL-M-38510/122, device type 06.

Test Circuit (Applies to Tables 1 and 2)

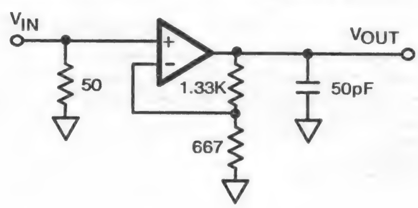


ALL RESISTORS = ± 1% (Ω)
ALL CAPACITORS = ± 10% (μF)

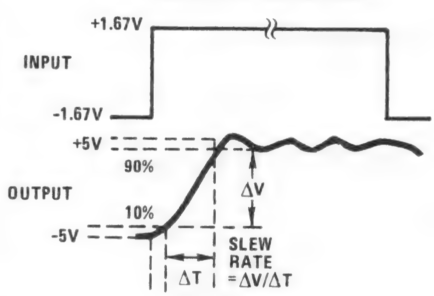
For Detailed Information, Refer to HA-2520/883; HA-2522/883 Test Tech Brief

Test Waveforms

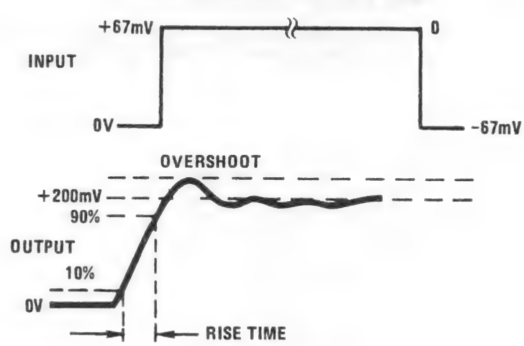
SIMPLIFIED TEST CIRCUIT (Applies to Table 2)



SLEW RATE WAVEFORM



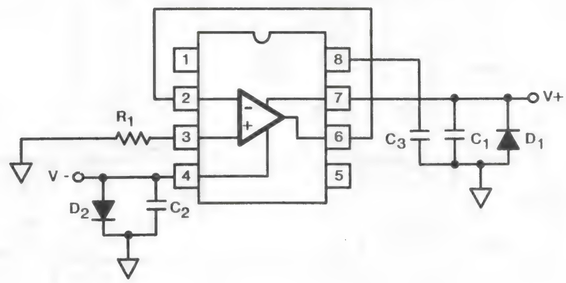
TRANSIENT RESPONSE WAVEFORM



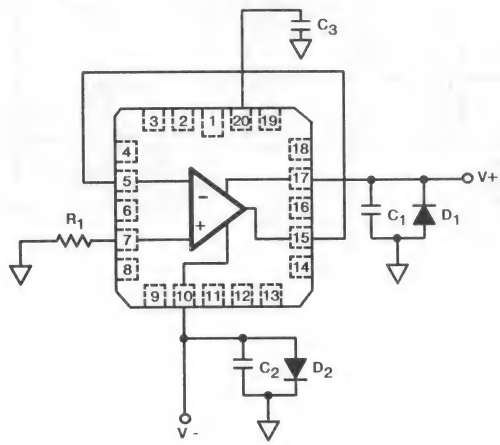
NOTE: Measured on both positive and negative transitions.
Capacitance at Compensation pin should be minimized.

Burn-In Circuits

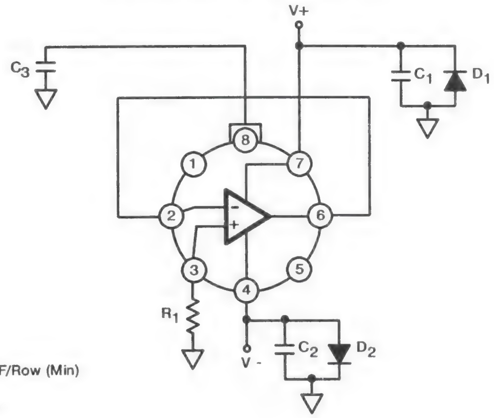
HA7-2520/883 CERAMIC MINI-DIP
HA7-2522/883 CERAMIC MINI-DIP



HA4-2522/883 CERAMIC LCC



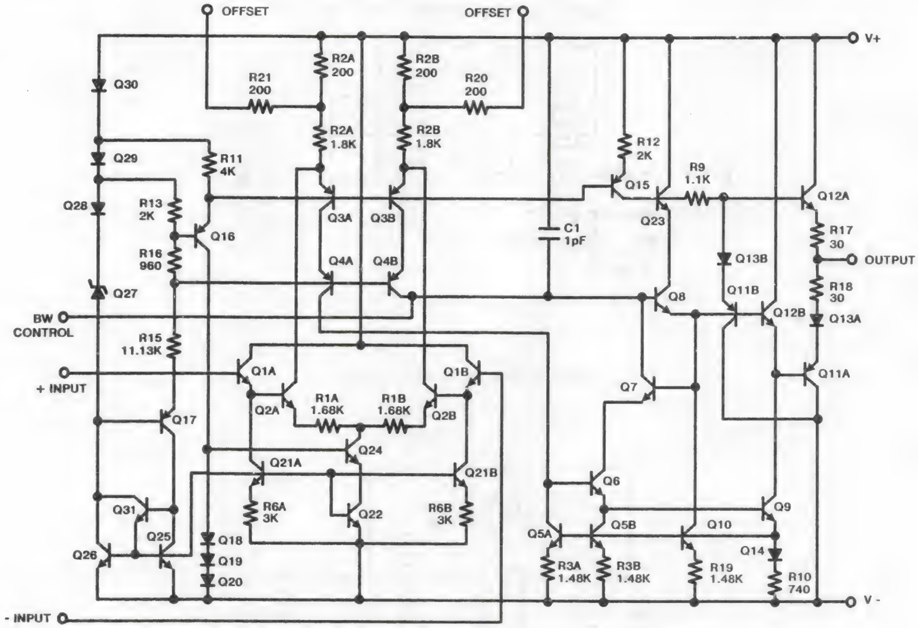
HA2-2520/883 (TO-99) METAL CAN
HA2-2522/883 (TO-99) METAL CAN



NOTES:

R_1 = 1MΩ, ±5%, 1/4W (Min)
$C_1 = C_2$ = 0.01μF/Socket (Min) or 0.1μF/Row (Min)
C_3 = 0.01μF (±10%)/Socket
$D_1 = D_2$ = IN4002 or Equivalent/Board
$|(V+) - (V-)| = 30V$

Schematic Diagram



Die Characteristics

DIE DIMENSIONS:
65 x 50 x 19 mils
(1660 x 1270 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$0.79 \times 10^5 A/cm^2$ @ 10mA

SUBSTRATE POTENTIAL (Powered Up):
Unbiased

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

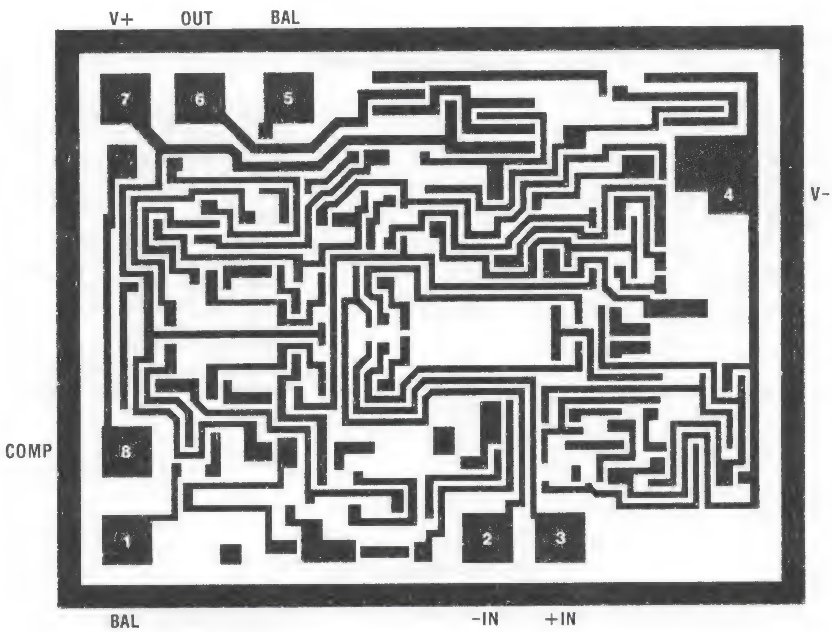
TRANSISTOR COUNT:
HA-2520/883: 40
HA-2522/883: 40

PROCESS: Std. Linear Bipolar Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic Mini-DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)
Metal Can — 420°C (Max)

Metallization Mask Layout

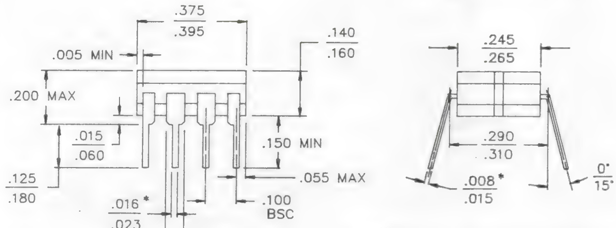
HA-2520/883 HA-2522/883



NOTE: Pin Numbers Correspond to 8 Lead Metal Can and Ceramic Mini-DIP Package Only.

Packaging †

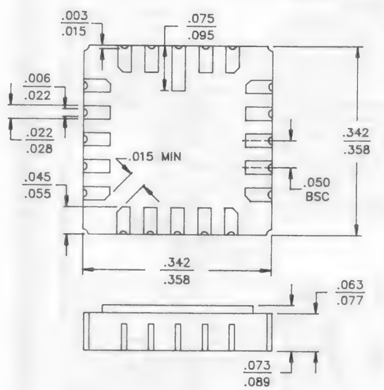
8 PIN CERAMIC DIP



* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

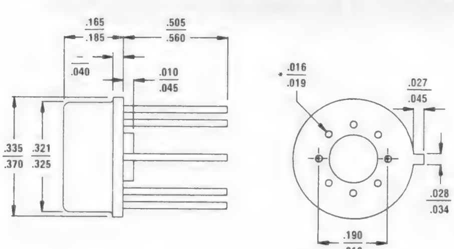
LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-4

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Al_2O_3
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

8 PIN TO-99 METAL CAN



*Dimension Maximum Limits Are Increased by 0.003 inches for Solder Dip Finish

LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
Material: No Seal Material
Temperature: Room Temperature
Method: Resistance Weld
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic Bonded
COMPLIANT OUTLINE: 38510 A-1

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

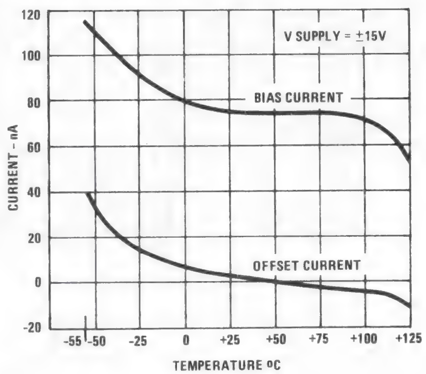
DESIGN INFORMATION

Uncompensated, High Slew Rate Operational Amplifiers

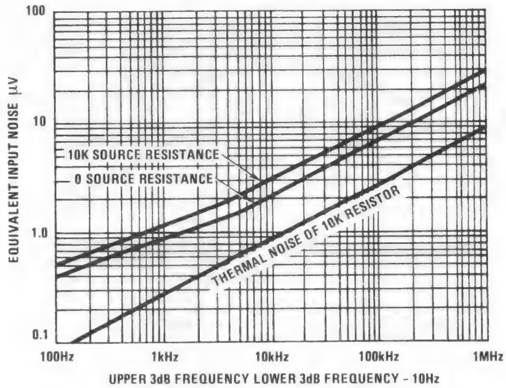
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $\pm V_{SUPPLY} = \pm 15V$

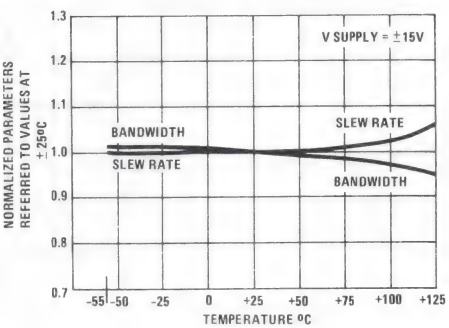
INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



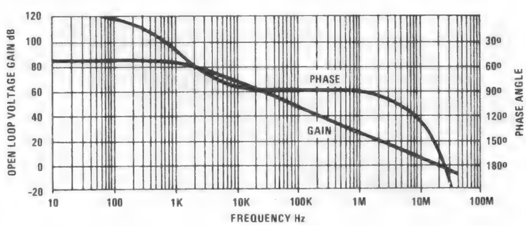
EQUIVALENT INPUT NOISE vs. BANDWIDTH



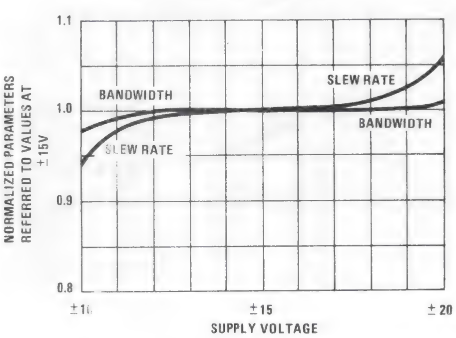
NORMALIZED A.C. PARAMETERS vs. TEMPERATURE



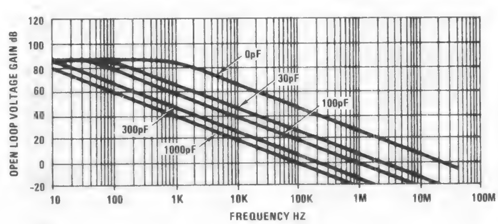
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



NORMALIZED A.C. PARAMETERS vs. SUPPLY VOLTAGE @ +25°C



OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND



3

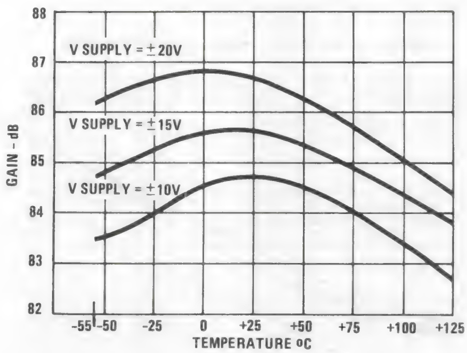
OP AMPs & COMPARATORS

DESIGN INFORMATION (Continued)

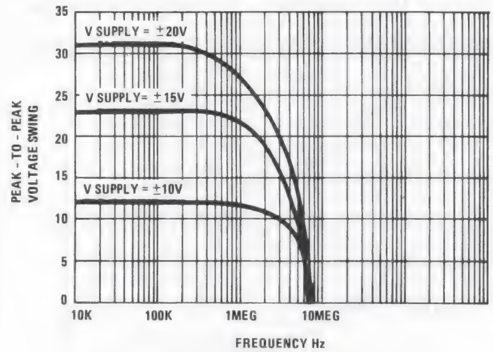
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $\pm V_{SUPPLY} = \pm 15V$

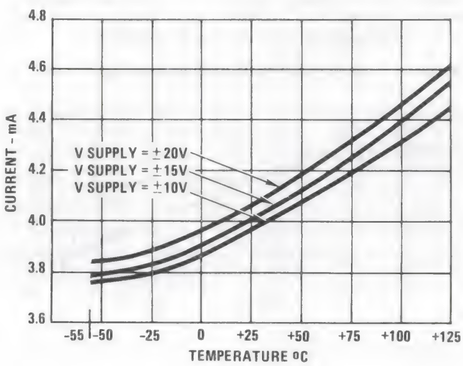
OPEN-LOOP VOLTAGE GAIN vs. TEMPERATURE



OUTPUT VOLTAGE SWING vs. FREQUENCY @ +25°C

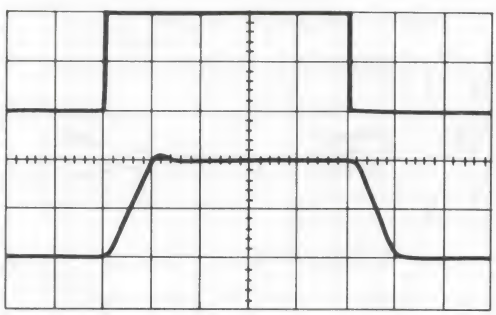


POWER SUPPLY CURRENT vs. TEMPERATURE

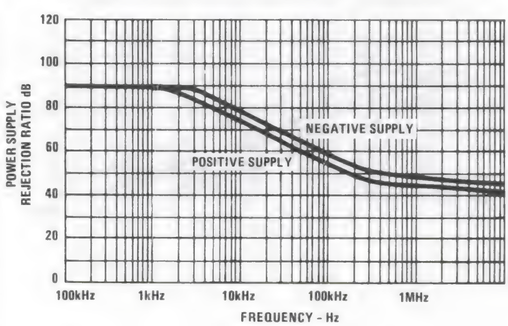


VOLTAGE FOLLOWER PULSE RESPONSE

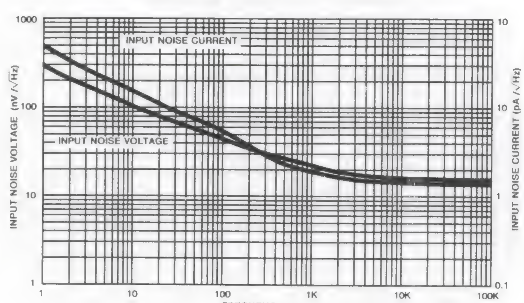
$R_L = 2K\Omega$, $C_L = 50pF$, Horizontal = 100ns/Div.
Upper Trace: Input; 1.67V/Div. $T_A = +25^oC$, $V_S = +15V$
Lower Trace: Output; 5V/Div.



POWER SUPPLY REJECTION RATIO vs. FREQUENCY



INPUT NOISE DENSITY vs. FREQUENCY



DESIGN INFORMATION (Continued)

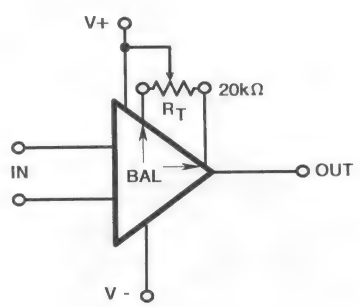
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: $V_S = \pm15V$, $R_L = 2K$, $C_L = 50pF$, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	HA-2520 TYPICAL	HA-2522 TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage	$V_{CM} = 0V$	+25°C	4	5	Table 1	mV
Offset Voltage Average Drift	Versus Temperature	Full	20	25	30	µV/°C
Offset Current Average Drift	Versus Temperature	Full	200	300	500	pA/°C
Differential Input Resistance		+25°C	100	100	Table 3	MΩ
Large Signal Voltage Gain	$V_{OUT} = \pm10V$	+25°C	15	15	Table 1	kV/V
CMRR	$V_{CM} = \pm10V$	Full	90	90	Table 1	dB
PSRR	$\Delta V_{Supply} = \pm10V$	Full	90	90	Table 1	dB
Output Current	$V_{OUT} = \pm10V$	+25°C	±20	±20	Table 1	mA
Gain Bandwidth Product	$A_V = \geq 10$ Small Signal ($\leq$ 200mV)	+25°C	20	20	Table 3	MHz
Rise/Fall Time	$V_O = \pm200mV$	+25°C	25	25	Table 2	ns
Overshoot	$V_O = \pm200mV$	+25°C	25	25	Table 2	%
Slew Rate	$V_O = \pm5V$	+25°C	120	120	Table 2	V/µs
Settling Time	10V Step to 0.1%	+25°C	0.2	0.2	1.1	µs
Output Resistance	Open Loop	+25°C	30	30	50	Ω
Minimum Supply Voltage	Functional Operation Only Other Parameters Will Vary	+25°C	±4	±4	±5	V

Suggested V_{OS} Adjustment



Tested Offset Adjustment Range is $|V_{OS} + 1mV|$ minimum referred to output. Typical range is +20mV to −18mV with R_T = 20kΩ.

HARRIS

HA-2529/883

Uncompensated, High Slew Rate High Output Current, Operational Amplifier

January 1989

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **High Slew Rate .... 135V/μs (Min)** **150V/μs (Typ)**
- **High Output Current.................. ±30mA (Min)**
- **High Gain-Bandwidth Product .... 15MHz (Min)** **20MHz (Typ)**
- **Wide Power Bandwidth .... 2.1MHz (Min)**
- **High Input Impedance .... 50MΩ (Min)** **130MΩ (Typ)**
- **Low Offset Current .... 25nA (Max)** **5nA (Typ)**
- **Fast Settling (10V Step to 0.1 %) .... 200ns (Typ)**
- **Low Quiescent Supply Current .... 6mA (Max)**

Applications

- **Data Acquisition Systems**
- **R.F. Amplifiers**
- **Video Amplifiers**
- **Signal Generators**
- **Pulse Amplification**

Description

The HA-2529/883 is a monolithic operational amplifier which typifies excellence of design. With a design based on years of experience coupled with the reliable dielectric isolation process, these amplifiers provide an outstanding combination of D.C. and A.C. parameters at closed loop gains of 3 or greater without external compensation.

The HA-2529/883 offers 135V/μs (min) slew rate and fast settling time (200ns typ), while consuming a mere 6mA (max) quiescent supply current, making these amplifiers ideal components for video circuitry and data acquisition designs. With 15MHz minimum gain-bandwidth product combined with 7.5kV/V minimum open loop gain, the HA-2529/883 is an ideal component for demanding signal conditioning designs. These devices provide ±30mA (min) output current drive with an output voltage swing of ±10V (min), making then suited for pulse amplifier and R.F. amplifier components.

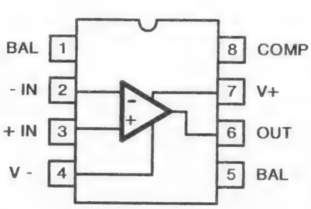
HA-2529/883 will upgrade a system presently using the HA-2520/22/883 or EHA-2520/22/883 in regards to output current, slew rate, offset voltage drift, and offset current drift. To insure compliance with slew rate and transient response specifications, all devices are 100% tested for A.C. performance characteristics over full temperature.

The HA-2529/883 is available as a MIL-STD-883 compliant device screened to class B level. This device is sensitive to electrostatic discharge and is in microciruit group number 49 (see MIL-STD-38510, Appendix E).

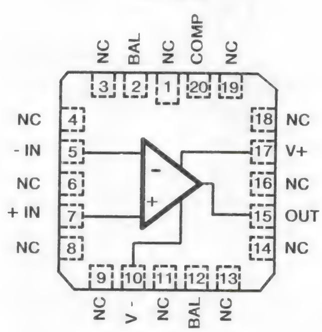
The HA-2529/883 guarantees operation over the military temperature range from -55°C to +125°C and is available in 8 pin Metal Can, Ceramic Mini-DIP or 20 pad Ceramic LCC packages.

Pinouts

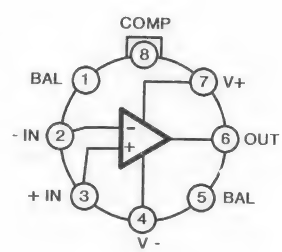
HA7-2529/883 (CERAMIC MINI-DIP)
TOP VIEW



HA4-2529/883 (CERAMIC LCC)
TOP VIEW



HA2-2529/883 (METAL CAN)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage 15V
Voltage at Either Input Terminal .... V+ to V-
Peak Output Current (10% Duty Cycle) 90mA
Junction Temperature (T_J) .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... < 2000V
Lead Temperature (Soldering 10 sec) .... 275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	140°C/W	65°C/W
Ceramic LCC Package	74°C/W	20°C/W
Metal Can Package	148°C/W	45°C/W

Package Power Dissipation Limit at +75°C for $T_J \leq$ +175°C
Ceramic DIP Package 710mW
Ceramic LCC Package 1.35W
Metal Can Package 670mW

Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 7.1mW/°C
Ceramic LCC Package .... 13.4mW/°C
Metal Can Package .... 6.7mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±15V
$V_{INcm} \leq$ 1/2 (V+ - V-)
$R_L \geq 500\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, $R_{SOURCE} = 100\Omega$, $R_{LOAD} = 500k\Omega$, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	V_{CM} = 0V	1	+25°C	-5	5	mV
			2, 3	+125°C, -55°C	-8	8	mV
Input Bias Current	$+I_B$	V_{CM} = 0V $+R_S = 100k\Omega$ $-R_S = 100\Omega$	1	+25°C	-200	200	nA
			2, 3	+125°C, -55°C	-400	400	nA
	$-I_B$	V_{CM} = 0V $+R_S = 100\Omega$ $-R_S = 100k\Omega$	1	+25°C	-200	200	nA
			2, 3	+125°C, -55°C	-400	400	nA
Input Offset Current	I_{IO}	V_{CM} = 0V $+R_S = 100k\Omega$ $-R_S = 100k\Omega$	1	+25°C	-25	25	nA
			2, 3	+125°C, -55°C	-50	50	nA
Common Mode Range	+CMR	V+ = 5V V- = -25V	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	-CMR	V+ = 25V V- = -5V	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
Large Signal Voltage Gain	$+A_{VOL}$	V_{OUT} = 0V and +10V $R_L = 2k\Omega$	4	+25°C	10	-	kV/V
			5, 6	+125°C, -55°C	7.5	-	kV/V
	$-A_{VOL}$	V_{OUT} = 0V and -10V $R_L = 2k\Omega$	4	+25°C	10	-	kV/V
			5, 6	+125°C, -55°C	7.5	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔV_{CM} = +10V +V = +5V -V = -25V V_{OUT} = -10V	1	+25°C	83	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	-CMRR	ΔV_{CM} = -10V +V = +25V -V = -5V V_{OUT} = +10V	1	+25°C	83	-	dB
			2, 3	+125°C, -55°C	80	-	dB

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Voltage Swing	$+V_{OUT}$	$R_L = 2k\Omega$	4	+25°C	10	-	V
			5, 6	+125°C, -55°C	10	-	V
	$-V_{OUT}$	$R_L = 2k\Omega$	4	+25°C	-	-10	V
			5, 6	+125°C, -55°C	-	-10	V
Output Current	$+I_{OUT}$	$V_{OUT} = -10V$	4	+25°C	30	-	mA
			5, 6	+125°C, -55°C	20	-	mA
	$-I_{OUT}$	$V_{OUT} = +10V$	4	+25°C	-	-30	mA
			5, 6	+125°C, -55°C	-	-20	mA
Quiescent Power Supply Current	$+I_{CC}$	$V_{OUT} = 0V$ $I_{OUT} = 0mA$	1	+25°C	-	6	mA
			2, 3	+125°C, -55°C	-	7	mA
	$-I_{CC}$	$V_{OUT} = 0V$ $I_{OUT} = 0mA$	1	+25°C	-6	-	mA
			2, 3	+125°C, -55°C	-7	-	mA
Power Supply Rejection Ratio	+PSRR	$\Delta V_{SUP} = 10V$ +V = +10V, -V = -15V +V = +20V, -V = -15V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	-PSRR	$\Delta V_{SUP} = 10V$ +V = +15V, -V = -10V +V = +15V, -V = -20V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
Offset Voltage Adjustment	$+V_{IO}Adj$	Note 4	1	+25°C	$V_{IO}-1$	-	mV
			2, 3	+125°C, -55°C	$V_{IO}-1$	-	mV
	$-V_{IO}Adj$	Note 4	1	+25°C	$V_{IO}+1$	-	mV
			2, 3	+125°C, -55°C	$V_{IO}+1$	-	mV

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_{VCL} = +3V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Slew Rate	+SR	V_{OUT} = -5V to +5V	7	+25°C	135	-	V/μs
			8A, 8B	+125°C, -55°C	125	-	V/μs
	-SR	V_{OUT} = +5V to -5V	7	+25°C	135	-	V/μs
			8A, 8B	+125°C, -55°C	125	-	V/μs
Rise & Fall Time	T_R	V_{OUT} = 0 to +200mV $10\% \leq T_R \leq 90\%$	7	+25°C	-	45	ns
			8A, 8B	+125°C, -55°C	-	50	ns
	T_F	V_{OUT} = 0 to -200mV $10\% \leq T_F \leq 90\%$	7	+25°C	-	45	ns
			8A, 8B	+125°C, -55°C	-	50	ns
Overshoot	+OS	V_{OUT} = 0 to +200mV	7	+25°C	-	40	%
			8A, 8B	+125°C, -55°C	-	40	%
	-OS	V_{OUT} = 0 to -200mV	7	+25°C	-	40	%
			8A, 8B	+125°C, -55°C	-	40	%

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, C_{COMP} = 0pF, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Differential Input Resistance	R_{IN}	V_{CM} = 0V	1	+25°C	50	-	MΩ
Gain Bandwidth Product	GBWP	V_O = 200mV, $f_O \geq$ 10kHz	1	+25°C	15	-	MHz
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	+25°C	2.1	-	MHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 2kΩ, C_L = 50pF	1	-55°C to +125°C	±3	-	V/V
Output Resistance	R_{OUT}	Open Loop	1	+25°C	-	60	Ω
Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	210	mW

NOTES:
1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).
3. Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)
4. Offset Adjustment Range is [V_{IO} (measured) ±1mV] minimum referred to output. This test is for functionality only to assure adjustment through 0V.

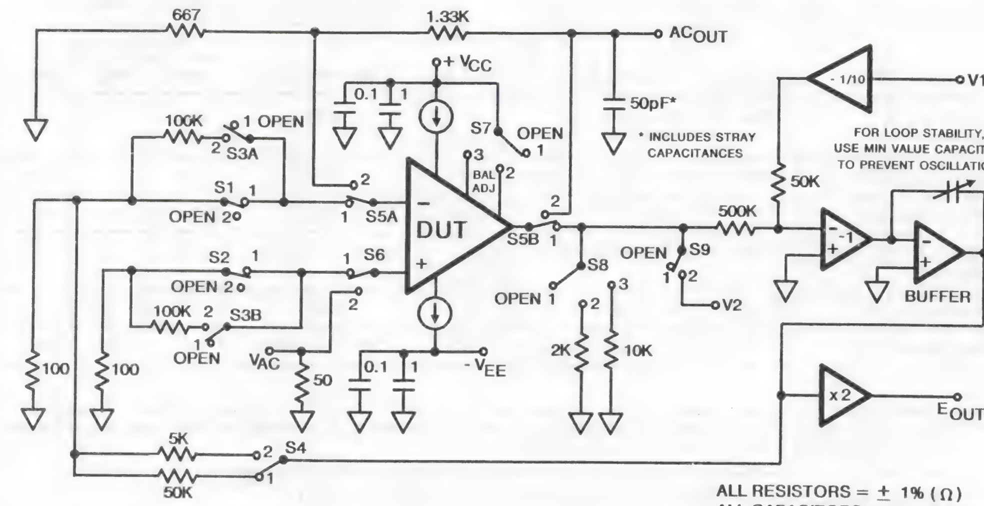
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6, 7, 8A, 8B
Group A Test Requirements	1, 2, 3, 4, 5, 6, 7, 8A, 8B
Groups C & D End Points	1

* PDA applies to Subgroup 1 only.

The Subgroup assignments of the parameters in these tables were patterned after MIL-M-38510/122.

Test Circuit (Applies to Tables 1 and 2)

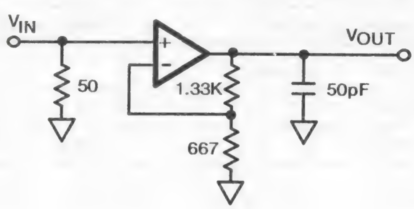


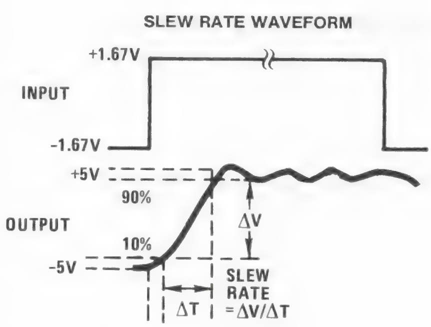
ALL RESISTORS = ± 1% (Ω)
ALL CAPACITORS = ± 10% (μF)

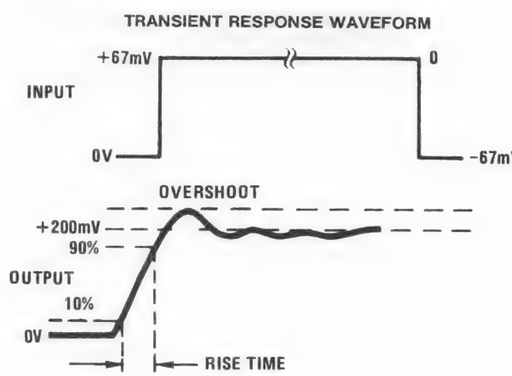
For Detailed Information, Refer to HA-2529/883 Test Tech Brief

Test Waveforms

SIMPLIFIED TEST CIRCUIT (Applies to Table 2)



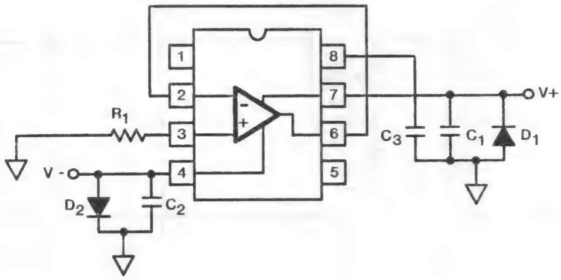




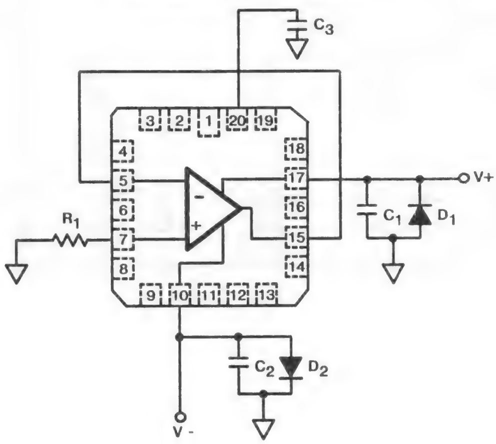
NOTE: Measured on both positive and negative transitions.
Capacitance at Compensation pin should be minimized.

Burn-In Circuits

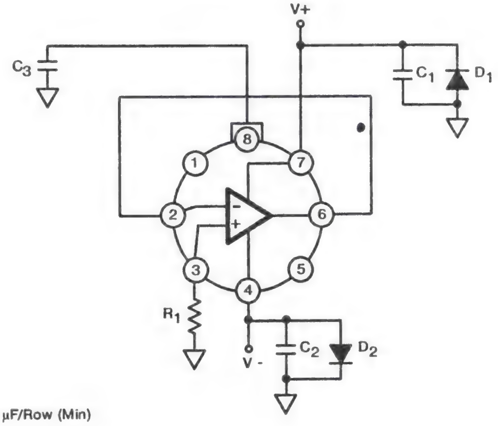
HA7-2529/883 CERAMIC MINI-DIP



HA4-2529/883 CERAMIC LCC



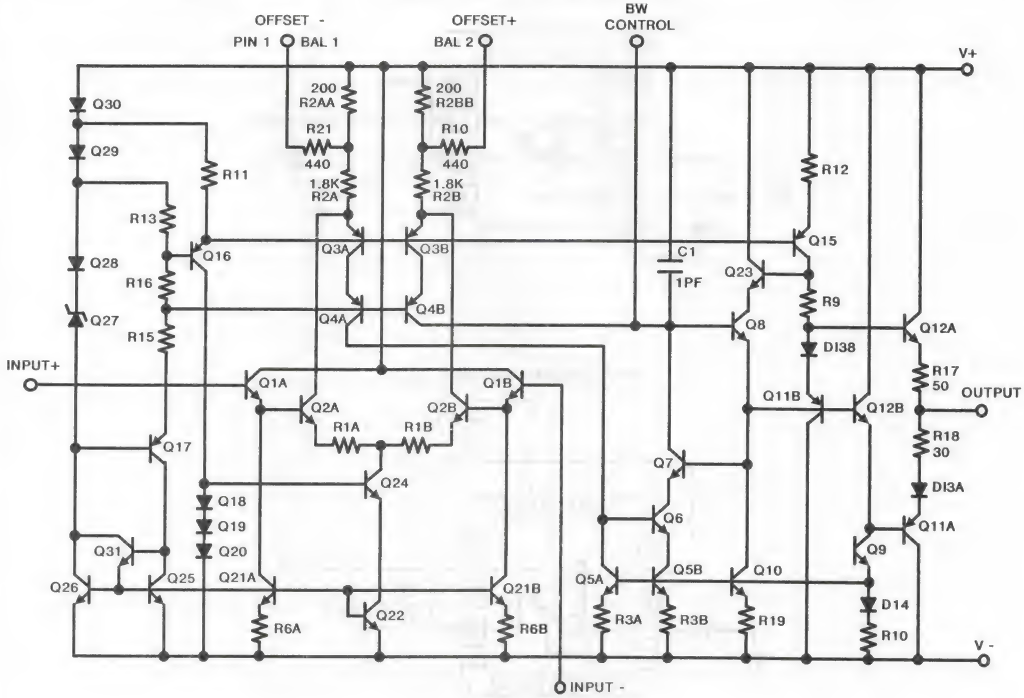
HA2-2529/883 (TO-99) METAL CAN



NOTES:

R_1 = 1MΩ, ±5%, 1/4W (Min)
$C_1 = C_2$ = 0.01μF/Socket (Min) or 0.1μF/Row (Min)
C_3 = 0.01μF (±10%)/Socket
$D_1 = D_2$ = IN4002 or Equivalent/Board
$|(V+) - (V-)| = 30V$

Schematic Diagram



Die Characteristics

DIE DIMENSIONS:
65.4 x 51.2 x 19 mils
(1660 x 1300 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$1.27 \times 10^5 A/cm^2$

SUBSTRATE POTENTIAL (Powered Up):
Unbiased

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

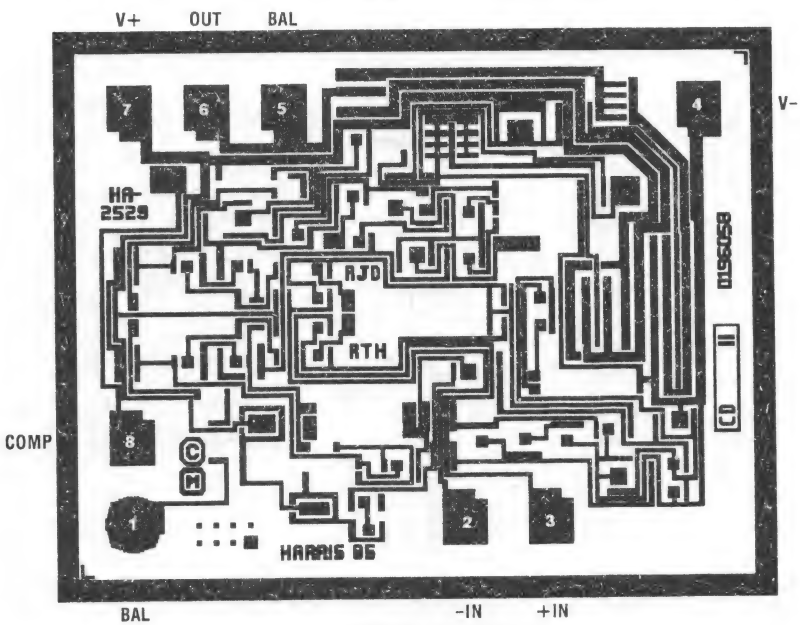
TRANSISTOR COUNT: 40

PROCESS: Std. Linear Bipolar Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic Mini-DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)
Metal Can — 420°C (Max)

Metallization Mask Layout

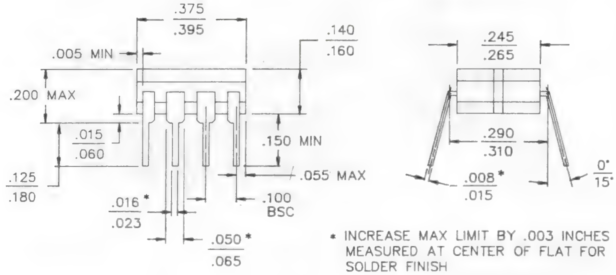
HA-2529/883



NOTE: Pin Numbers Correspond to Can and Mini-DIP Package Only.

Packaging †

8 PIN CERAMIC DIP

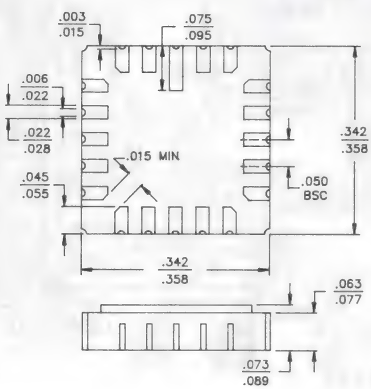


LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
- Material: Glass Frit
- Temperature: 450°C ± 10°C
- Method: Furnace Seal

INTERNAL LEAD WIRE:
- Material: Aluminum
- Diameter: 1.25 Mil
- Bonding Method: Ultrasonic

COMPLIANT OUTLINE: 38510 D-4

20 PAD CERAMIC LCC

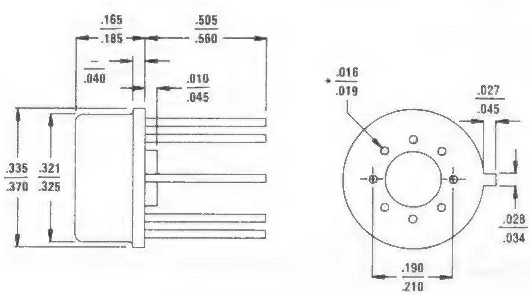


PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Ceramic, 90% Al_2O_3
PACKAGE SEAL:
- Material: Gold/Tin (80/20)
- Temperature: 320°C ± 10°C
- Method: Furnace Braze

INTERNAL LEAD WIRE:
- Material: Aluminum
- Diameter: 1.25 Mil
- Bonding Method: Ultrasonic

COMPLIANT OUTLINE: 38510 C-2

8 PIN TO-99 METAL CAN



LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
- Material: No Seal Material
- Temperature: Room Temperature
- Method: Resistance Weld

INTERNAL LEAD WIRE:
- Material: Aluminum
- Diameter: 1.25 Mil
- Bonding Method: Ultrasonic Bonded

COMPLIANT OUTLINE: 38510 A-1

*Dimension Maximum Limits Are Increased by 0.003 inches for Solder Dip Finish

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

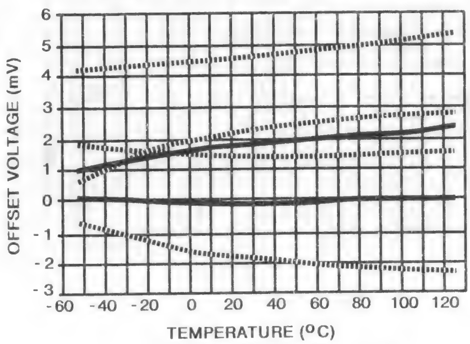
DESIGN INFORMATION

Uncompensated, High Slew Rate High Output Current, Operational Amplifier

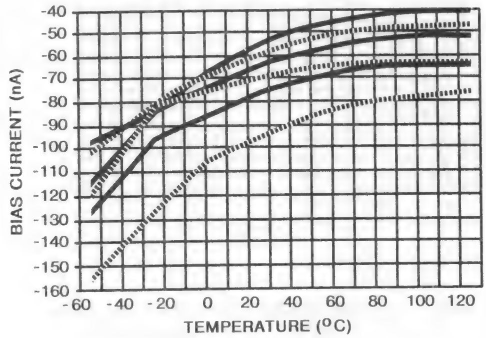
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

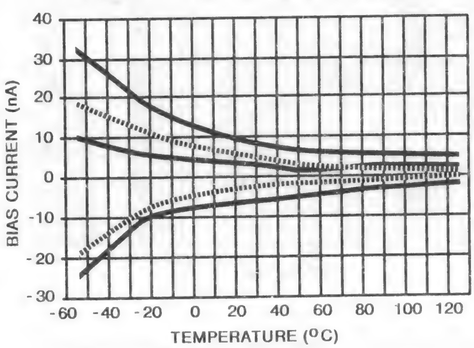
OFFSET VOLTAGE vs. TEMPERATURE
6 Typical Units From 3 Lots @ $V_S = \pm15V$



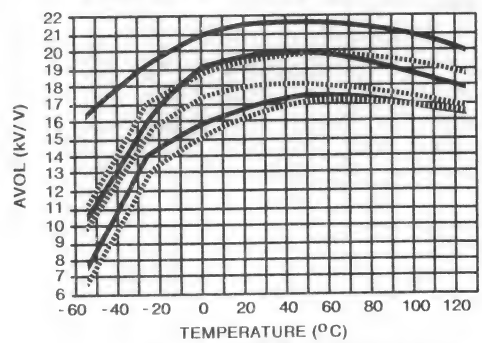
BIAS CURRENT vs. TEMPERATURE
6 Typical Units From 3 Lots @ $V_S = \pm15V$



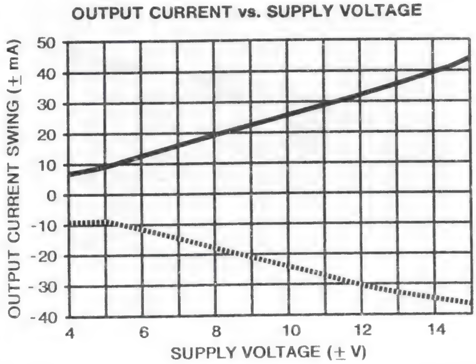
OFFSET CURRENT vs. TEMPERATURE
5 Typical Units From 3 Lots @ $V_S = \pm15V$



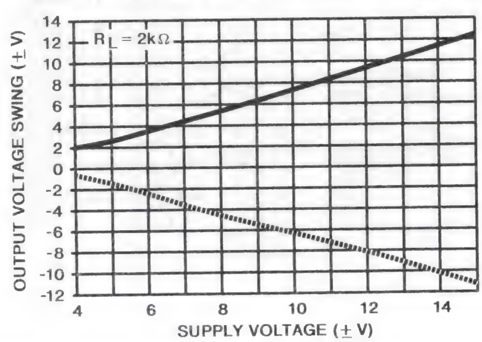
OPEN LOOP GAIN vs. TEMPERATURE
6 Typical Units From 3 Lots @ $V_S = \pm15V$



OUTPUT CURRENT vs. SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE



DESIGN INFORMATION (Continued)

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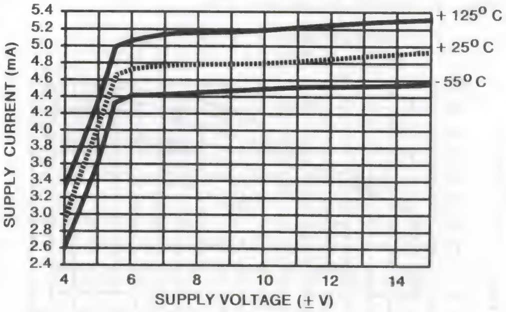
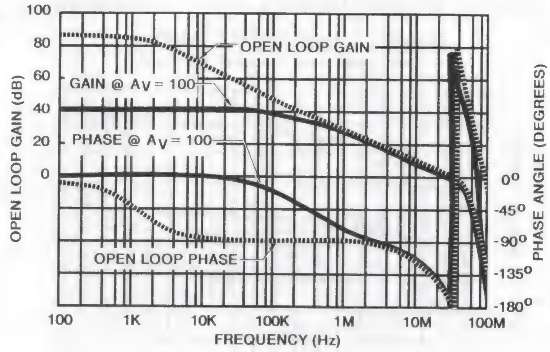
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

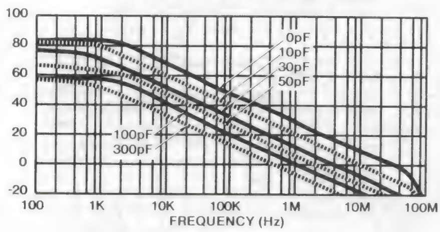
SUPPLY CURRENT vs. SUPPLY VOLTAGE
Over Full Temperature



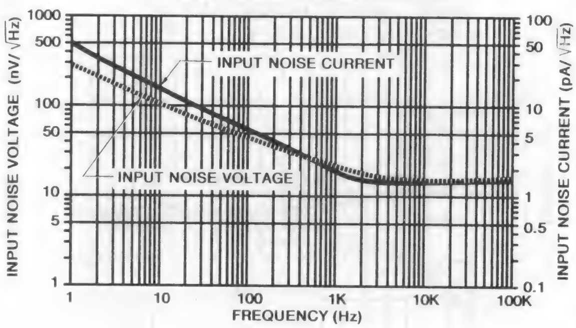
FREQUENCY RESPONSE AT VARIOUS GAINS



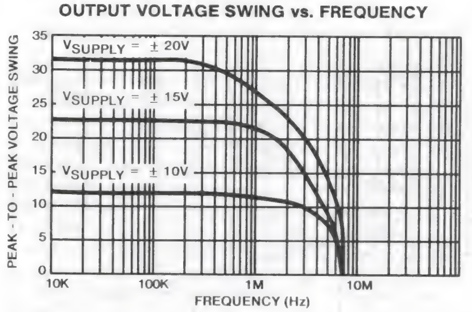
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND



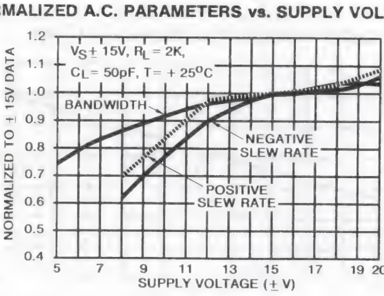
INPUT NOISE CHARACTERISTICS



OUTPUT VOLTAGE SWING vs. FREQUENCY



NORMALIZED A.C. PARAMETERS vs. SUPPLY VOLTAGE

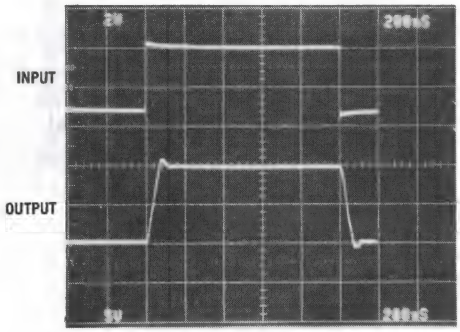


DESIGN INFORMATION (Continued)

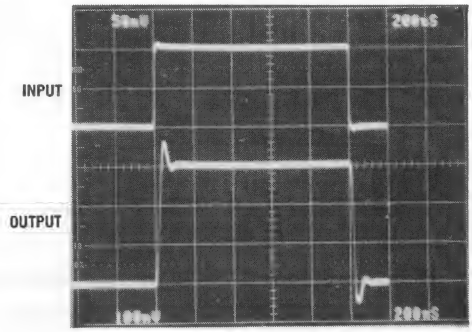
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

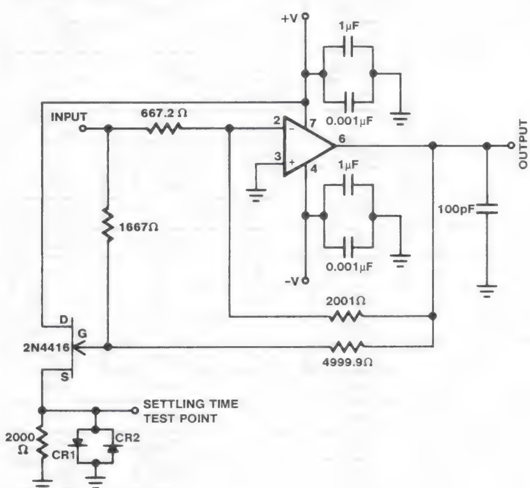
LARGE SIGNAL RESPONSE
Vertical Scale: (200ns/Div.)
Horizontal Scale: (2V/Div. Input)
(5V/Div. Output)



SMALL SIGNAL RESPONSE
Vertical Scale: (200ns/Div.)
Horizontal Scale: (50mV/Div. Input)
(100mV/Div. Output)

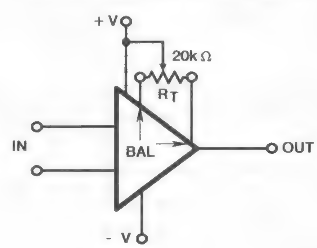


Settling Time Circuit



- $A_V = -3$
- Feedback and summing resistor ratios should be 0.1% matched.
- Clipping diodes CR1 and CR2 are optional. HP5082-2810 recommended.

SUGGESTED V_{OS} ADJUSTMENT

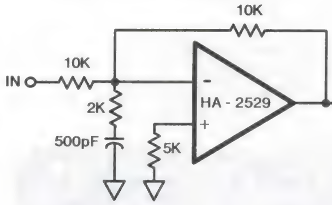


Tested Offset Adjustment is $|V_{OS} + 1mV|$ minimum referred to output. Typical range is +28mV to -18mV with R_T = 20kΩ.

DESIGN INFORMATION (Continued)

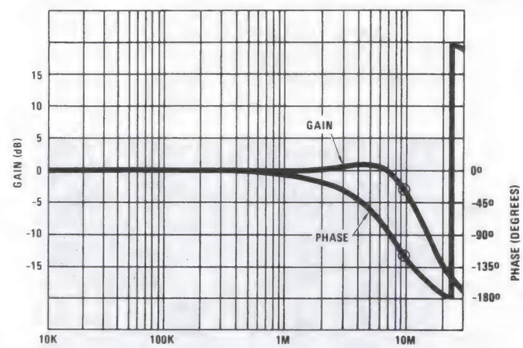
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Applications



NOTE: Compensation Circuit for $A_V = -1$
Slew rate ≈ 120/μs
Bandwidth ≈ 10MHz
Settling Time (0.1%) ≈ 500ns
Capacitance at pin 8 must be minimized for maximum bandwidth.
Tested and functional with supply voltages from ±4V to ±15V.

FREQUENCY RESPONSE FOR INVERTING UNITY GAIN CIRCUIT



TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_L = 2kΩ, C_L = 50pF, A_V = +3V/V, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage	V_{CM} = 0V	+25°C	2	Table 1	mV
Average Offset Voltage Drift	Versus Temperature	Full	10	20	μV/°C
Bias Current	V_{CM} = 0V	+25°C	50	Table 1	nA
		Full	80	Table 1	nA
Average Bias Current Drift	Versus Temperature	Full	0.2	1.2	nA/°C
Offset Current	V_{CM} = 0V	+25°C	5	Table 1	nA
		Full	10	Table 1	nA
Average Offset Current Drift	Versus Temperature	Full	0.02	0.5	nA/°C
Differential Input Resistance		+25°C	130	Table 3	MΩ
Differential Input Capacitance		+25°C	3	5	pF
Input Noise Voltage	$f_O \geq$ 1kHz	+25°C	20	25	nV/$\sqrt{Hz}$
Input Noise Current	$f_O \geq$ 1kHz	+25°C	1.8	3	pA/$\sqrt{Hz}$
Large Signal Voltage Gain	V_O = ±10V	+25°C	20	Table1	kV/V
		Full	15	Table 1	kV/V
CMRR	V_{CM} = ±10V	Full	100	Table 1	dB
PSRR	ΔV_{SUPPLY} = 10V	Full	90	Table 1	dB
Gain Bandwidth Product	Small Signal	+25°C	25	Table 3	MHz
Rise/Fall Time	V_O = +200mV, -200mV	+25°C	20	Table 2	ns
Overshoot	V_O = +200mV, -200mV	+25°C	10	Table 2	%
Slew Rate	V_O = ±5V	+25°C	160	Table 2	V/μs
Settling Time	0.1% of 10V step	+25°C	200	600	ns
Output Resistance	Open Loop	+25°C	30	Table 3	Ω
Saturation Recovery Time	V_O = +12.5V, -11.2V	+25°C	0.92	1.5	μs
Minimum Supply Voltage	Functional Operation Only Other Parameters Will Vary	+25°C	±4	±5	V
Supply Current	No Load	Full	4.5	Table 1	mA

HARRIS

HA-2539/883

Very High Slew Rate Wideband Operational Amplifier

January 1989

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Very High Slew Rate .... 550V/μs (Min)**
  600V/μs (Typ)
- **Open Loop Gain .... 10K V/V (Min)**
  15K V/V (Typ)
- **Wide Gain Bandwidth .... 550MHz (Min)**
  600MHz (Typ)
- **Full Power Bandwidth .... 8.7MHz (Min)**
  9.5MHz (Typ)
- **Low Offset Voltage .... 10mV (Max)**
- **Input Voltage Noise @ 1kHz .... 6nV/$\sqrt{Hz}$ (Typ)**
- **Output Voltage Swing .... ±10V (Min)**

Applications

- **Pulse and Video Amplifiers**
- **Wideband Amplifiers**
- **High Speed Sample and Hold Circuits**
- **RF Oscillators**

Description

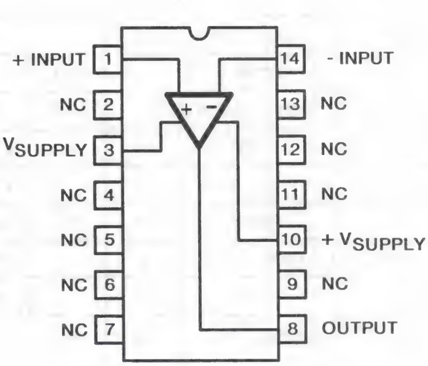
The Harris HA-2539/883 represents the ultimate in high slew rate wideband, monolithic, operational amplifiers. It has been designed and constructed with the Harris high frequency bipolar dielectric isolation process and features dynamic parameters never before available from a truly differential device.

With a 600V/μs slew rate and a 600MHz gain bandwidth product, the HA-2539/883 is ideally suited for use in video and RF amplifier designs, in closed loop gains of 10 or greater. Full ±10V swing coupled with outstanding AC parameters and complemented by high open loop gain makes the device useful in high speed data acquisition systems.

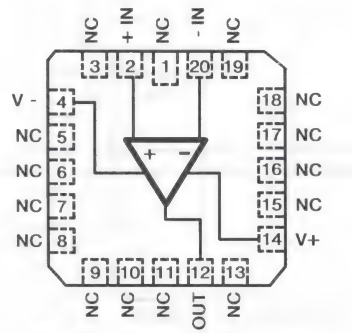
The HA-2539/883 is available in the 14 pin Ceramic DIP and a 20 pin LCC package and is pin-for-pin functional with the Signetics NE5539. The HA-2539/883 operates over the -55°C to +125°C temperature range.

Pinouts

HA1-2539/883 (CERAMIC DIP)
TOP VIEW



HA4-2539/883 (CERAMIC LCC)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage 6V
Voltage at Either Input Terminal .... V+ to V-
Peak Output Current (< 10% Duty Cycle) 50mA
Junction Temperature (T_J) .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... < 2000V
Lead Temperature (Soldering 10 sec) .... +275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	98°C/W	30°C/W
Ceramic LCC Package	95°C/W	35°C/W

Package Power Dissipation Limit at +75°C For $T_J \leq 175°C$
Ceramic DIP Package 1.03W
Ceramic LCC Package 1.06W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 10.2mW/°C
Ceramic LCC Package .... 10.6mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±12V to ±15V
$V_{INcm} \leq 1/2$ (V+ - V-)
$R_L \geq 1k\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, $R_{SOURCE} = 100\Omega$, $R_{LOAD} = 100k\Omega$, $V_{OUT} = 0V$, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	$V_{CM} = 0V$	1	+25°C	-10	10	mV
			2, 3	+125°C, -55°C	-15	15	mV
Input Bias Current	$+I_B$	$V_{CM} = 0V$ $+R_S = 1.1k\Omega$ $-R_S = 100\Omega$	1	+25°C	-20	20	µA
			2, 3	+125°C, -55°C	-25	25	µA
	$-I_B$	$V_{CM} = 0V$ $+R_S = 100\Omega$ $-R_S = 1.1k\Omega$	1	+25°C	-20	20	µA
			2, 3	+125°C, -55°C	-25	25	µA
Input Offset Current	I_{IO}	$V_{CM} = 0V$ $+R_S = 1.1k\Omega$ $-R_S = 1.1k\Omega$	1	+25°C	-6	6	µA
			2, 3	+125°C, -55°C	-8	8	µA
Common Mode Range	+CMR	V+ = 5V V- = -25V	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	-CMR	V+ = 25V V- = -5V	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
Large Signal Voltage Gain	$+A_{VOL}$	V_{OUT} = 0V and +10V $R_L = 1k\Omega$	4	+25°C	10	-	kV/V
			5, 6	+125°C, -55°C	5	-	kV/V
	$-A_{VOL}$	V_{OUT} = 0V and -10V $R_L = 1k\Omega$	4	+25°C	10	-	kV/V
			5, 6	+125°C, -55°C	5	-	kV/V
Common Mode Rejection Ratio	+CMRR	$\Delta V_{CM} = +10V$ +V = +5V -V = -25V $V_{OUT} = -10V$	1	+25°C	60	-	dB
			2, 3	+125°C, -55°C	60	-	dB
	-CMRR	$\Delta V_{CM} = -10V$ +V = +25V -V = -5V $V_{OUT} = +10V$	1	+25°C	60	-	dB
			2, 3	+125°C, -55°C	60	-	dB

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 100kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Voltage Swing	$+V_{OUT}$	R_L = 1kΩ	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	$-V_{OUT}$	R_L = 1kΩ	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
Output Current	$+I_{OUT}$	V_{OUT} = -10V	1	+25°C	10	-	mA
	$-I_{OUT}$	V_{OUT} = +10V	1	+25°C	-	-10	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-	24	mA
			2, 3	+125°C, -55°C	-	24	mA
	$-I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-24	-	mA
			2, 3	+125°C, -55°C	-24	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = 10V +V = +5V, -V = -15V +V = +15V, -V = -15V	1	+25°C	60	-	dB
			2, 3	+125°C, -55°C	60	-	dB
	-PSRR	ΔV_{SUP} = 10V +V = +15V, -V = -5V +V = +15V, -V = -15V	1	+25°C	60	-	dB
			2, 3	+125°C, -55°C	60	-	dB

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Table 2 Intentionally Left Blank. See A.C. Specifications on Table 3.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_{LOAD} = 1kΩ, $C_{LOAD} \leq$ 10pF, A_V = 10V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Gain Bandwidth Product	GBWP	V_O = 100mV, f_O = 1MHz	1	+25°C	550	-	MHz
		V_O = 100mV, f_O = 60MHz	1	+25°C	600	-	MHz
Slew Rate	+SR	V_{OUT} = -5V to +5V	1	+25°C	550	-	V/μs
	-SR	V_{OUT} = +5V to -5V	1	+25°C	550	-	V/μs
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	+25°C	8.7	-	MHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 1kΩ, $C_L \leq$ 10pF	1	-55°C to +125°C	10	-	V/V
Rise & Fall Time	T_R	V_{OUT} = 0V to +200mV	1, 4	+25°C	-	10	ns
	T_F	V_{OUT} = 0V to -200mV	1, 4	+25°C	-	10	ns
Overshoot	+OS	V_{OUT} = 0V to +200mV	1	+25°C	-	45	%
	-OS	V_{OUT} = 0V to -200mV	1	+25°C	-	45	%
Output Resistance	R_{OUT}	Open Loop	1	+25°C	-	60	Ω
Quiescent Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	720	mW

NOTES: 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).

3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)

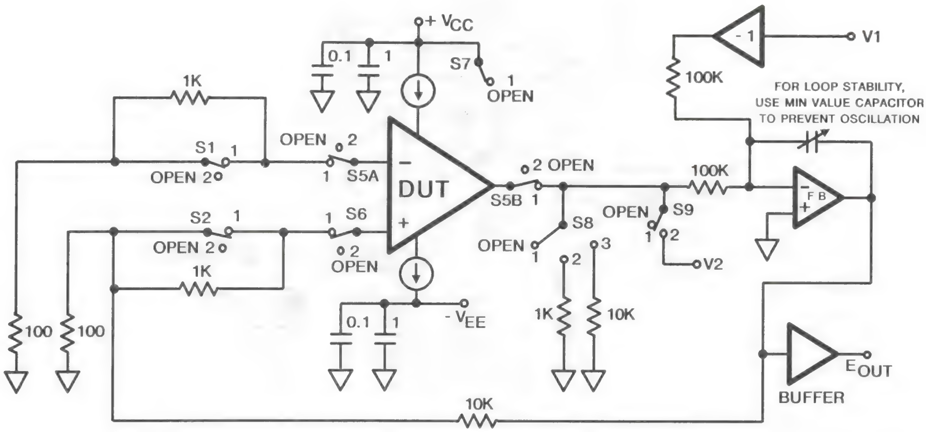
4. Measured between 10% and 90% points.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6
Group A Test Requirements	1, 2, 3, 4, 5, 6
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

Test Circuit (Applies to Table 1)

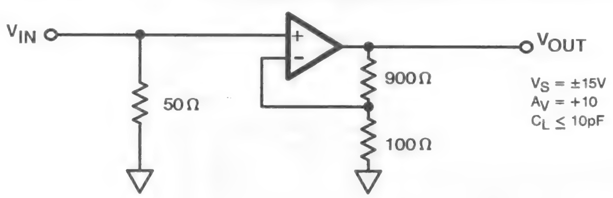


ALL RESISTORS = ± 1% (Ω)
ALL CAPACITORS = ± 10% (μF)

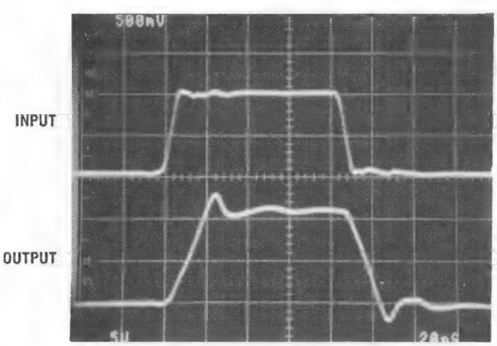
For Detailed Information, Refer to HA-2539/883 Test Tech Brief

Test Waveforms

SIMPLIFIED TEST CIRCUIT FOR LARGE AND SMALL SIGNAL RESPONSE (Applies to Table 3)

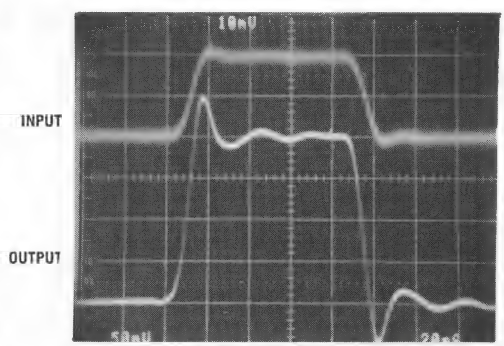


MEASURED LARGE SIGNAL RESPONSE
Vertical Scale: Input = 500mV/Div., Output = 5V/Div.
Horizontal Scale: Time: 20ns/Div.



$A_V = +10V/V$, $R_L = 1k\Omega$

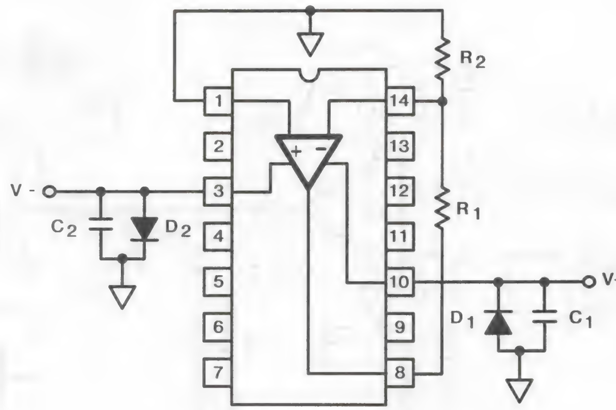
MEASURED SMALL SIGNAL RESPONSE
Vertical Scale: Input = 10mV/Div., Output = 50mV/Div.
Horizontal Scale: 20ns/Div.



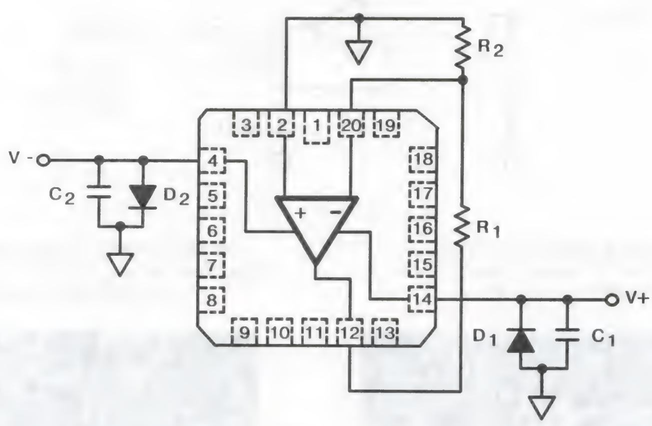
$A_V = +10V/V$, $R_L = 1k\Omega$

Burn-In Circuits

HA1-2539/883 CERAMIC DIP



HA4-2539/883 CERAMIC LCC



NOTES:

$R_1 = 10k\Omega$, ±5%, 1/4W (Min)

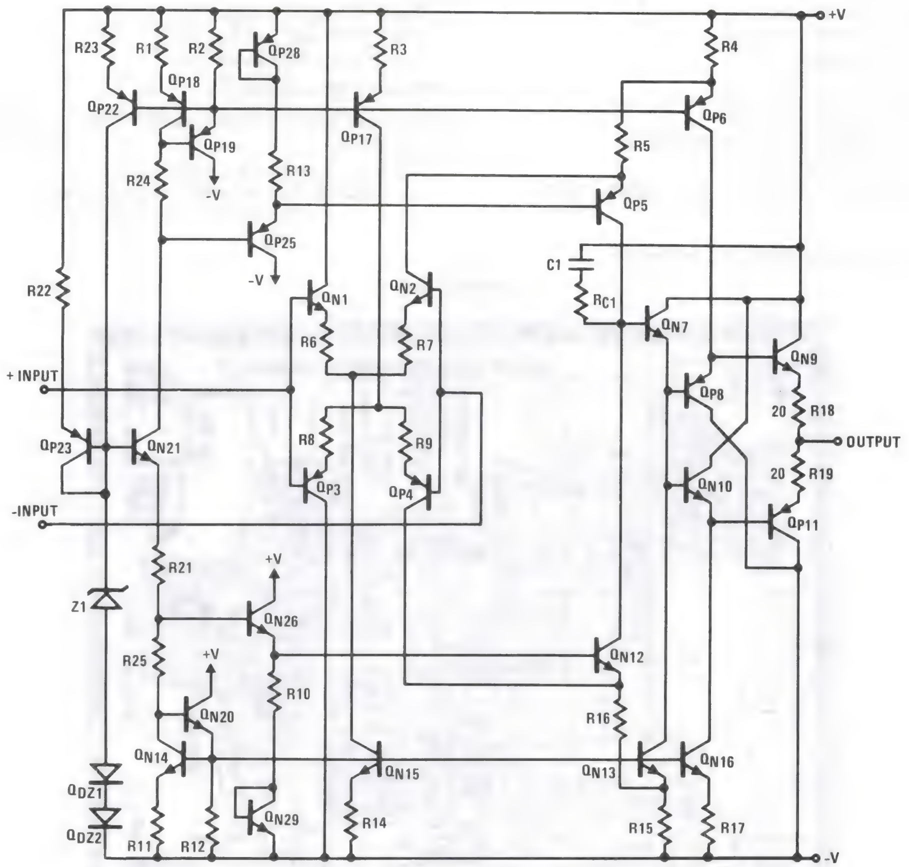
$R_2 = 1k\Omega$, ±5%, 1/4W (Min)

$C_1 = C_2 = 0.01\mu F$/Socket (Min) or $0.1\mu F$/Row, (Min)

$D_1 = D_2$ = IN4002 or Equivalent/Board

$|(V+) - (V-)| = 30V$

Schematic Diagram



Die Characteristics

DIE DIMENSIONS:
75.2 x 61 x 19 mils
(1910 x 1550 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 20kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$2 \times 10^5 A/cm^2$ @ 11mA

SUBSTRATE POTENTIAL (POWERED UP): V-

GLASSIVATION:
Type: Nitride over Silox
Silox Thickness: 12kÅ ± 2kÅ
Nitride Thickness: 3.5kÅ ± 1kÅ

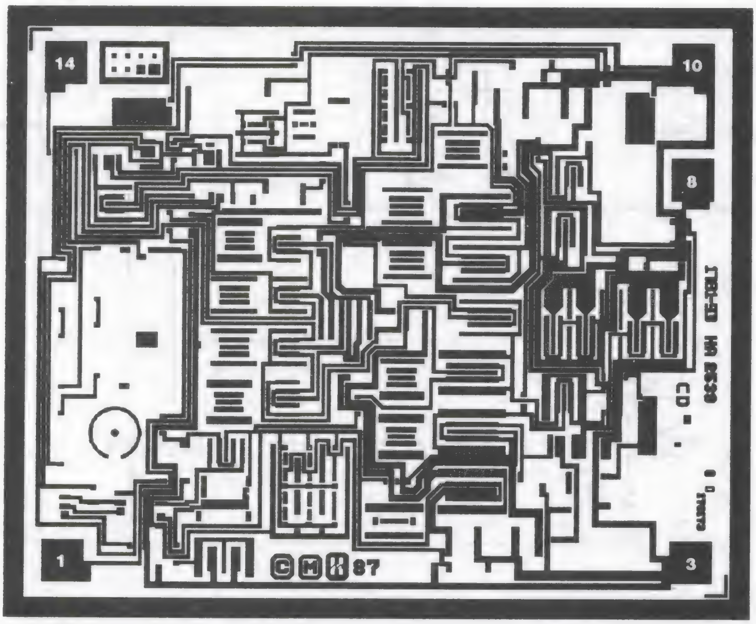
TRANSISTOR COUNT: 30

PROCESS: High Frequency Bipolar Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

Metallization Mask Layout

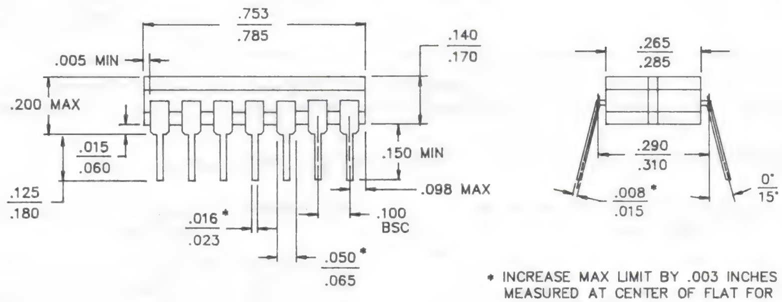
HA-2539/883



NOTE: Pin Numbers Correspond to 14 Pin DIP Package Only.

Packaging†

14 PIN CERAMIC DIP

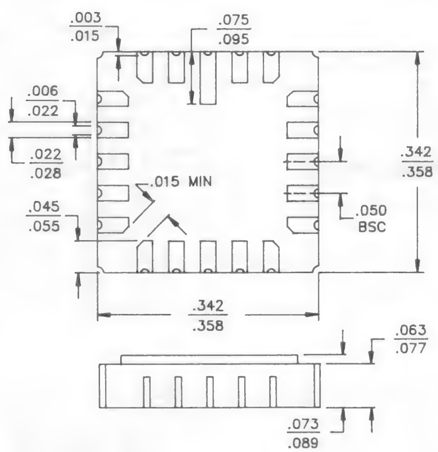


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-1

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

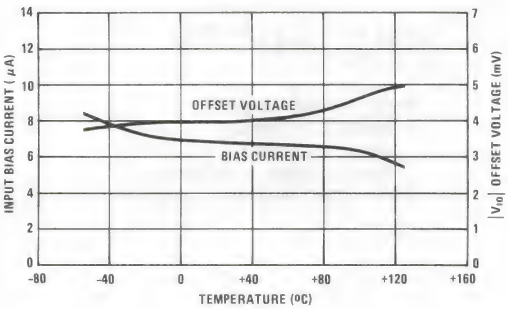
DESIGN INFORMATION

Very High Slew Rate Wideband Operational Amplifier

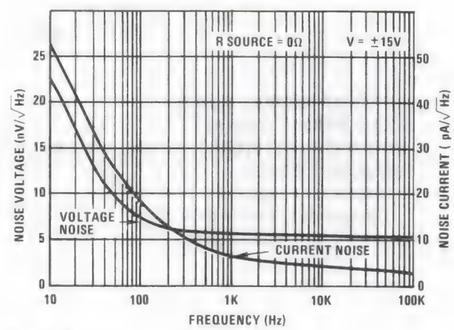
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

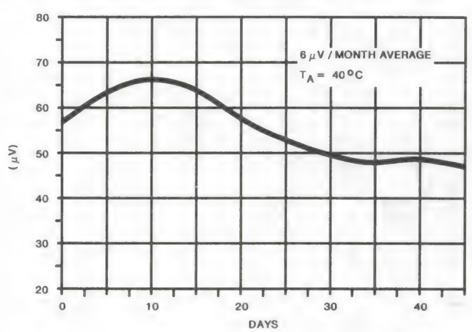
INPUT OFFSET VOLTAGE AND BIAS CURRENT vs. TEMPERATURE



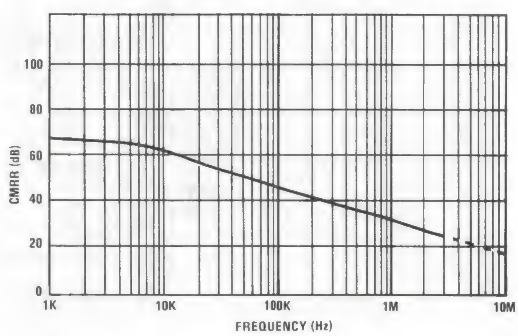
INPUT NOISE VOLTAGE AND NOISE CURRENT vs. FREQUENCY



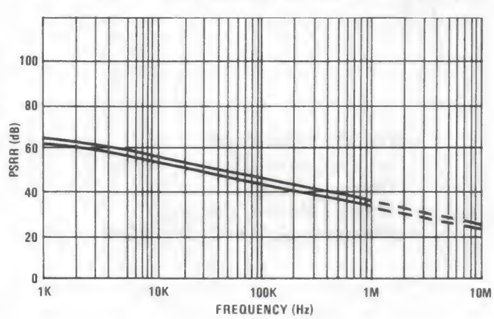
HA-2539 OFFSET VOLTAGE DRIFT vs. TIME



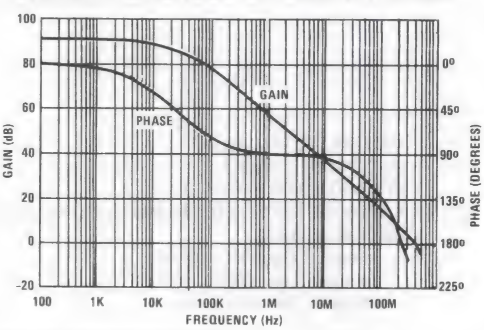
COMMON MODE REJECTION RATIO vs. FREQUENCY



POWER SUPPLY REJECTION RATIO vs. FREQUENCY



OPEN LOOP GAIN/PHASE vs. FREQUENCY HA-2539

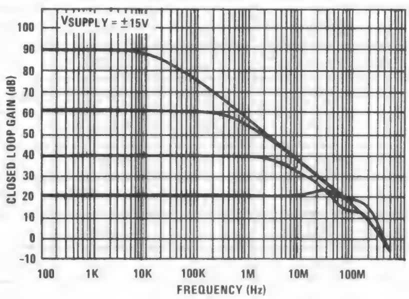


DESIGN INFORMATION (Continued)

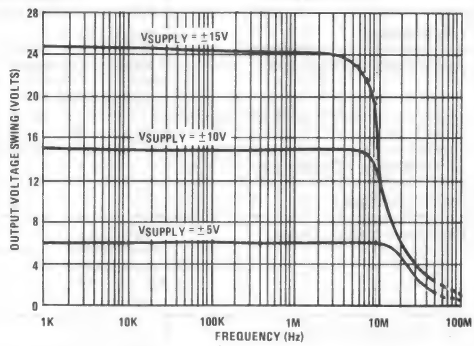
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

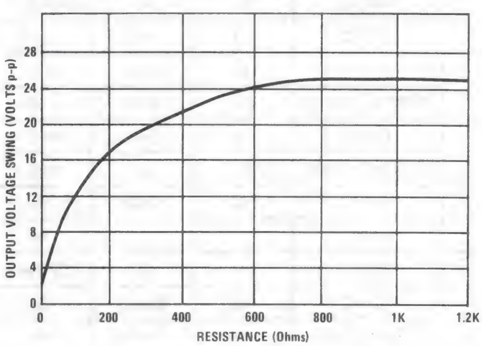
CLOSED LOOP FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS



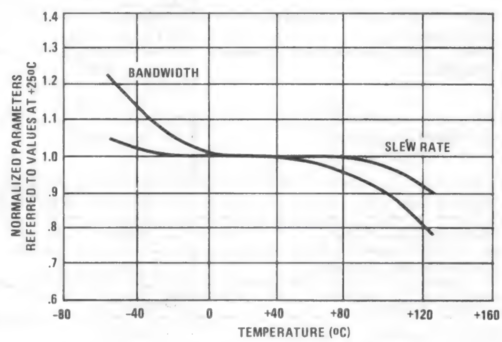
OUTPUT VOLTAGE SWING vs. FREQUENCY



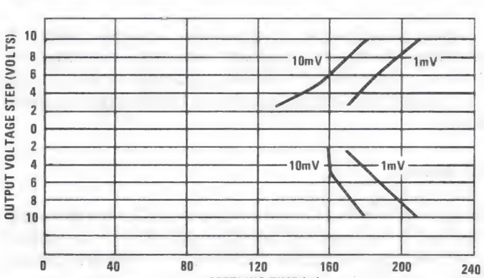
OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



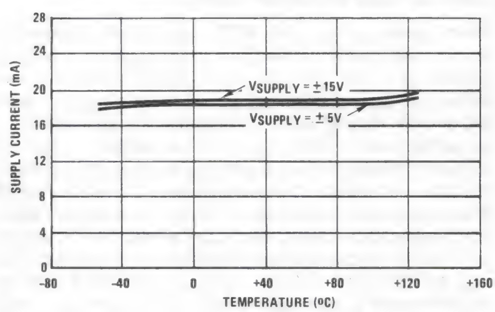
NORMALIZED AC PARAMETERS vs. TEMPERATURE



SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



POWER SUPPLY CURRENT vs. TEMPERATURE AND SUPPLY VOLTAGE



DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_L = 1kΩ, $C_L \leq$ 10pF, A_V = 10V/V, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage	V_{CM} = 0V	+25°C	8	Table 1	mV
Average Offset Voltage Drift	Versus Temperature	-55°C to +125°C	20	30	µV/°C
	Versus Time	+40°C	6	12	µV/Month
Bias Current	V_{CM} = OV	+25°C	6	Table 1	µA
Differential Input Resistance		+25°C	10	5	kΩ
Input Capacitance		+25°C	1	3	pF
Input Noise Voltage Density	f_O = 10Hz	+25°C	22	40	nV/$\sqrt{Hz}$
	f_O = 100Hz	+25°C	8	20	nV/$\sqrt{Hz}$
	f_O = 1kHz	+25°C	6	15	nV/$\sqrt{Hz}$
Input Noise Current Density	f_O = 10Hz	+25°C	50	80	pA/$\sqrt{Hz}$
	f_O = 100Hz	+25°C	20	30	pA/$\sqrt{Hz}$
	f_O = 1kHz	+25°C	6	10	pA/$\sqrt{Hz}$
Broadband Noise	0.1Hz to 1MHz	+25°C	50	75	μV_{p-p}
Slew Rate	V_{OUT} = ±5V	+25°C	600	Table 3	V/µs
		-55°C to +125°C	450	425	V/µs
Full Power Bandwidth	V_{PEAK} = 10V	+25°C	9.5	Table 3	MHz
		-55°C to +125°C	7.2	6.7	MHz
Settling Time	A_V = -10V/V, 10V to 0.1%	+25°C	180	250	ns
Differential Gain Error	$f_O \leq$ 5MHz	+25°C	3	5	%
Differential Phase Error	$f_O \leq$ 5MHz	+25°C	1	2	Degree
Output Resistance	Open Loop	+25°C	30	Table 3	Ω
Supply Current	I_{OUT} = 0mA	-55°C to +125°C	19	Table 1	mA
Minimum Supply Voltage	Functional Operation Only. Other Parameters Will Vary.	+25°C	±5	±7	V

Application Information

When using the HA-2539 for high frequency performance, care must be given in the system's design to optimize this component's use. High frequency layout techniques, ground planning, supply decoupling, and short lead lengths will help eliminate unwanted parasitic effects. A suggested component's choice for the feedback and input resistor is to keep their valve as small as possible, preferably less than 1kΩ. Capacitive loading, which cause a loss of phase margin can be increased by adding series resistance in the output path. Closed loop gain of less than 10 should not be designed due also to a loss of phase margin. If circuits must be designed in lower gains, inverting methods are recommended. Output saturation to the -V rail which may cause regeneration or oscillation during saturation, should also be avoided.

For other application suggestions, please refer to Application Note 541 which includes methods for DC error reductions, frequency compensation, higher output current and voltage circuits and other high frequency circuits.

Heat Sinking

Although not required for compliancy of /883, heat sinking is suggested in high ambient conditions (> 75°C). Suggested models include thermalloy model 6007 or AAVID model 5602B. Junction temperature should be maintained below +175°C. Further information is provided in Application Note 556, and proper thermal resistance values are provided in the thermal information section.

HARRIS

HA-2540/883

Wideband, Fast Settling Operational Amplifier

January 1989

Features

- This Circuit Is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Very High Slew Rate .... 350V/µs (Min) 400V/µs (Typ)
- Fast Settling Time .... 200ns (Typ)
- Wide Gain Bandwidth .... 300MHz (Min) 400MHz (Typ)
- Full Power Bandwidth .... 5.5MHz (Min) 6MHz (Typ)
- Low Offset Voltage .... 10mV (Max)
- Input Voltage Noise @ 1kHz .... 6nV/$\sqrt{Hz}$ (Typ)
- Output Voltage Swing .... ±10V (Min)
- Monolithic Bipolar Construction

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample and Hold Circuits
- Fast, Precise D/A Converters

Description

The Harris HA-2540/883 is a wideband, very high slew rate, monolithic operational amplifier featuring superior speed and bandwidth characteristics. Bipolar construction coupled with dielectric isolation allows this truly differential device to deliver outstanding performance. Additionally, the HA-2540/883 has a drive capability of ±10V into a 1kΩ load. Other desirable characteristics include low input voltage noise, low offset voltage, and fast settling time.

A 350V/µs slew rate ensures high performance in video and pulse amplification circuits, while the 400MHz gain-bandwidth-product is ideally suited for wideband signal amplification. A settling time of 250ns also makes the HA-2540/883 an excellent selection for high speed Data Acquisition Systems.

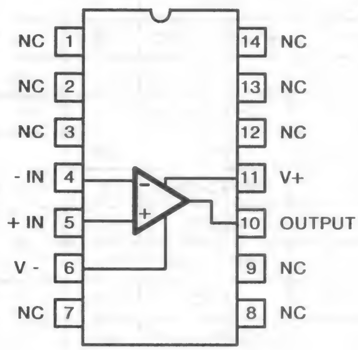
The HA-2540/883 is specified over the -55°C to +125°C temperature range.

3

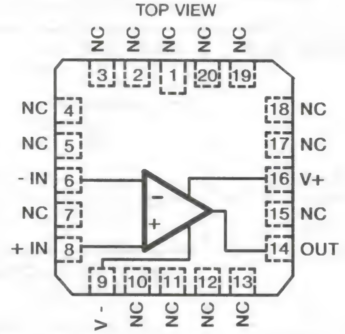
OP AMPs & COMPARATORS

Pinouts

HA1-2540/883 (CERAMIC DIP)
TOP VIEW



HA4-2540/883 (CERAMIC LCC)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage 6V
Voltage at Either Input Terminal .... V+ to V-
Peak Output Current (< 10% Duty Cycle) 50mA
Junction Temperature (T_J) .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... < 2000V
Lead Temperature (Soldering 10 sec) .... +275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	98°C/W	30°C/W
Ceramic LCC Package	95°C/W	35°C/W

Package Power Dissipation Limit at +75°C For $T_J \leq 175°C$
Ceramic DIP Package 1.03W
Ceramic LCC Package 1.06W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 10.2mW/°C
Ceramic LCC Package .... 10.6mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±12V to ±15V
$V_{INcm} \leq 1/2$ (V+ - V-)
$R_L \geq 1k\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, $R_{SOURCE} = 100\Omega$, $R_{LOAD} = 100k\Omega$, $V_{OUT} = 0V$, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	$V_{CM} = 0V$	1	+25°C	-10	10	mV
			2, 3	+125°C, -55°C	-15	15	mV
Input Bias Current	$+I_B$	$V_{CM} = 0V$ $+R_S = 1.1k\Omega$ $-R_S = 100\Omega$	1	+25°C	-20	20	µA
			2, 3	+125°C, -55°C	-25	25	µA
	$-I_B$	$V_{CM} = 0V$ $+R_S = 100\Omega$ $-R_S = 1.1k\Omega$	1	+25°C	-20	20	µA
			2, 3	+125°C, -55°C	-25	25	µA
Input Offset Current	I_{IO}	$V_{CM} = 0V$ $+R_S = 1.1k\Omega$ $-R_S = 1.1k\Omega$	1	+25°C	-6	6	µA
			2, 3	+125°C, -55°C	-8	8	µA
Common Mode Range	+CMR	V+ = 5V V- = -25V	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	-CMR	V+ = 25V V- = -5V	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
Large Signal Voltage Gain	$+A_{VOL}$	V_{OUT} = 0V and +10V $R_L = 1k\Omega$	4	+25°C	10	-	kV/V
			5, 6	+125°C, -55°C	5	-	kV/V
	$-A_{VOL}$	V_{OUT} = 0V and -10V $R_L = 1k\Omega$	4	+25°C	10	-	kV/V
			5, 6	+125°C, -55°C	5	-	kV/V
Common Mode Rejection Ratio	+CMRR	$\Delta V_{CM} = +10V$ +V = +5V -V = -25V $V_{OUT} = -10V$	1	+25°C	60	-	dB
			2, 3	+125°C, -55°C	60	-	dB
	-CMRR	$\Delta V_{CM} = -10V$ +V = +25V -V = -5V $V_{OUT} = +10V$	1	+25°C	60	-	dB
			2, 3	+125°C, -55°C	60	-	dB

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 100kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Voltage Swing	$+V_{OUT}$	R_L = 1kΩ	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	$-V_{OUT}$	R_L = 1kΩ	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
Output Current	$+I_{OUT}$	V_{OUT} = -10V	1	+25°C	10	-	mA
	$-I_{OUT}$	V_{OUT} = +10V	1	+25°C	-	-10	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-	24	mA
			2, 3	+125°C, -55°C	-	24	mA
	$-I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-24	-	mA
			2, 3	+125°C, -55°C	-24	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = 10V +V = +5V, -V = -15V +V = +15V, -V = -15V	1	+25°C	60	-	dB
			2, 3	+125°C, -55°C	60	-	dB
	-PSRR	ΔV_{SUP} = 10V +V = +15V, -V = -5V +V = +15V, -V = -15V	1	+25°C	60	-	dB
			2, 3	+125°C, -55°C	60	-	dB

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Table 2 Intentionally Left Blank. See A.C. Specifications on Table 3.

3

OP AMPs & COMPARATORS

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_{LOAD} = 1kΩ, $C_{LOAD} \leq$ 10pF, A_V = 10V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Gain Bandwidth Product	GBWP	V_O = 100mV, f_O = 1MHz	1	+25°C	300	-	MHz
		V_O = 100mV, f_O = 40MHz	1	+25°C	300	-	MHz
Slew Rate	+SR	V_{OUT} = -5V to +5V	1	+25°C	350	-	V/µs
	-SR	V_{OUT} = +5V to -5V	1	+25°C	350	-	V/µs
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	+25°C	5.5	-	MHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 1kΩ, $C_L \leq$ 10pF	1	-55°C to +125°C	10	-	V/V
Rise & Fall Time	T_R	V_{OUT} = 0V to +200mV	1, 4	+25°C	-	30	ns
	T_F	V_{OUT} = 0V to -200mV	1, 4	+25°C	-	30	ns
Overshoot	+OS	V_{OUT} = 0V to +200mV	1	+25°C	-	30	%
	-OS	V_{OUT} = 0V to -200mV	1	+25°C	-	30	%
Output Resistance	R_{OUT}	Open Loop	1	+25°C	-	60	Ω
Quiescent Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	720	mW

NOTES: 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).

3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)

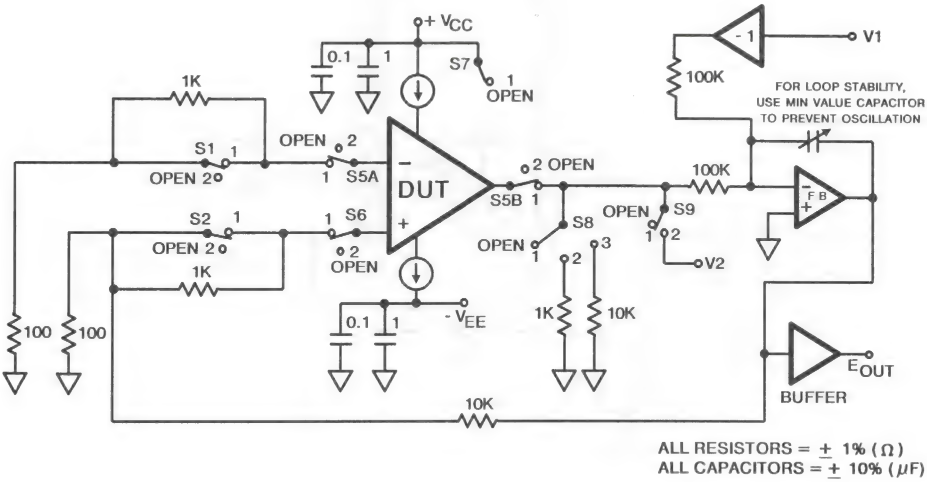
4. Measured between 10% and 90% points.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6
Group A Test Requirements	1, 2, 3, 4, 5, 6
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

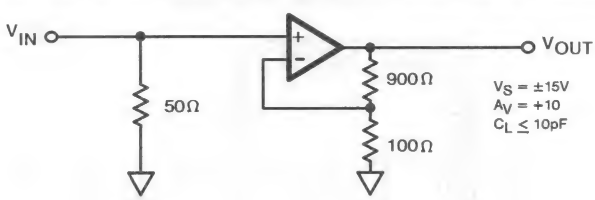
Test Circuit (Applies to Table 1)



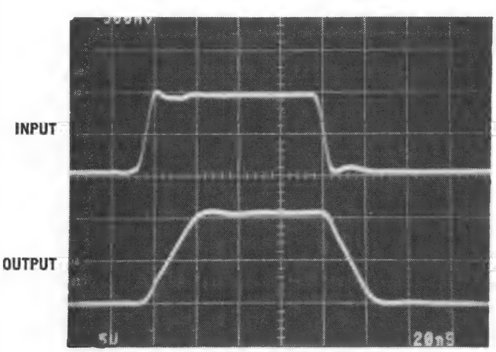
For Detailed Information, Refer to HA-2540/883 Test Tech Brief

Test Waveforms

SIMPLIFIED TEST CIRCUIT FOR LARGE AND SMALL SIGNAL RESPONSE (Applies to Table 3)

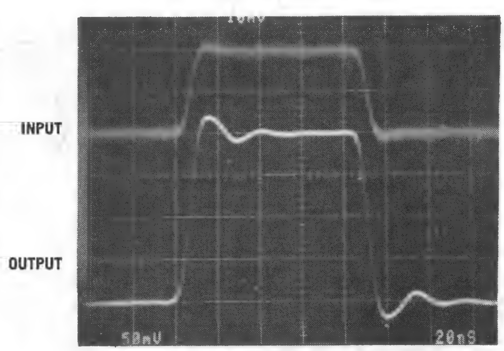


MEASURED LARGE SIGNAL RESPONSE
Vertical Scale: Input = 500mV/Div., Output = 5V/Div.
Horizontal Scale: Time: 20ns/Div.



$A_V = +10V/V$, $R_L = 1k\Omega$

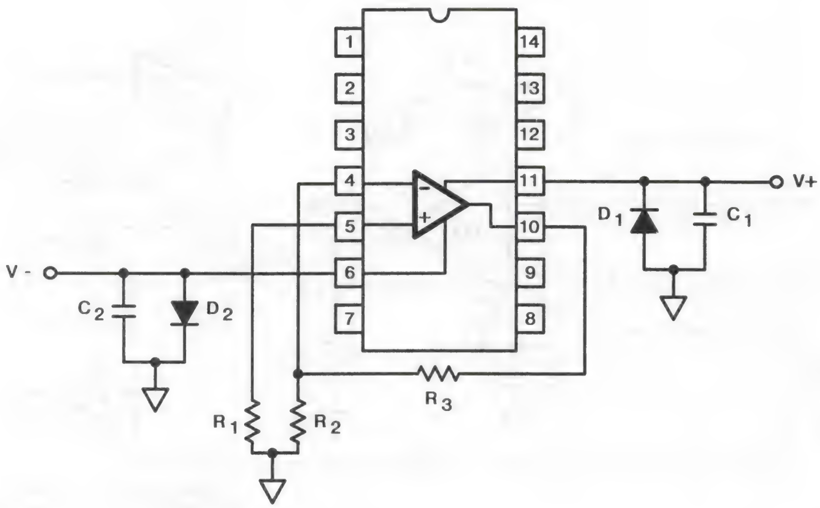
MEASURED SMALL SIGNAL RESPONSE
Vertical Scale: Input = 10mV/Div., Output = 50mV/Div.
Horizontal Scale: 20ns/Div.



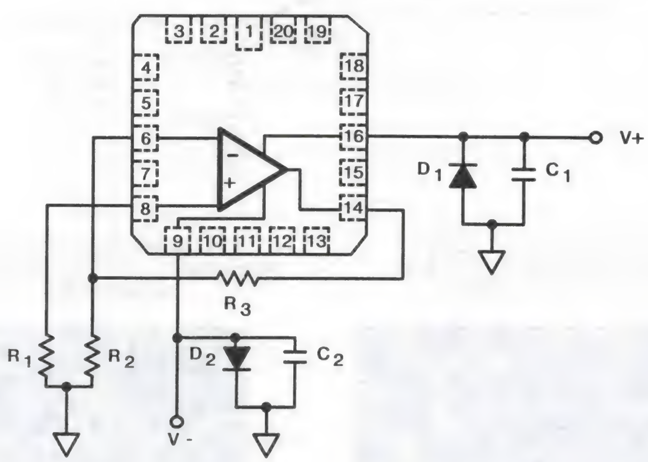
$A_V = +10V/V$, $R_L = 1k\Omega$

Burn-In Circuits

HA1-2540/883 CERAMIC DIP



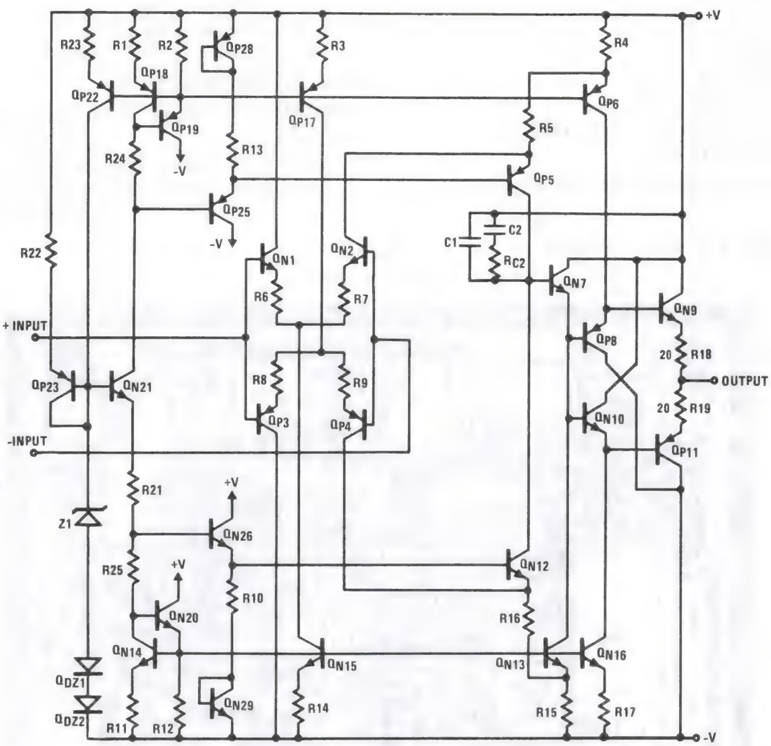
HA4-2540/883 CERAMIC LCC



NOTES:

R_1 = 1kΩ, ±5%, 1/4W (Min)
R_2 = 1kΩ, ±5%, 1/4W (Min)
R_3 = 10kΩ, ±5%, 1/4W (Min)
$C_1 = C_2$ = 0.01μF/Socket (Min) or 0.1μF/Row, (Min)
$D_1 = D_2$ = IN4002 or Equivalent/Board
$|(V+) - (V-)|$ = 30V

Schematic Diagram



Die Characteristics

DIE DIMENSIONS:
75.2 x 61 x 19 mils
(1910 x 1550 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 20kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
2 x 10^5A/cm^2 @ 11mA

SUBSTRATE POTENTIAL (POWERED UP): V-

GLASSIVATION:
Type: Nitride over Silox
Silox Thickness: 12kÅ ± 2kÅ
Nitride Thickness: 3.5kÅ ± 1kÅ

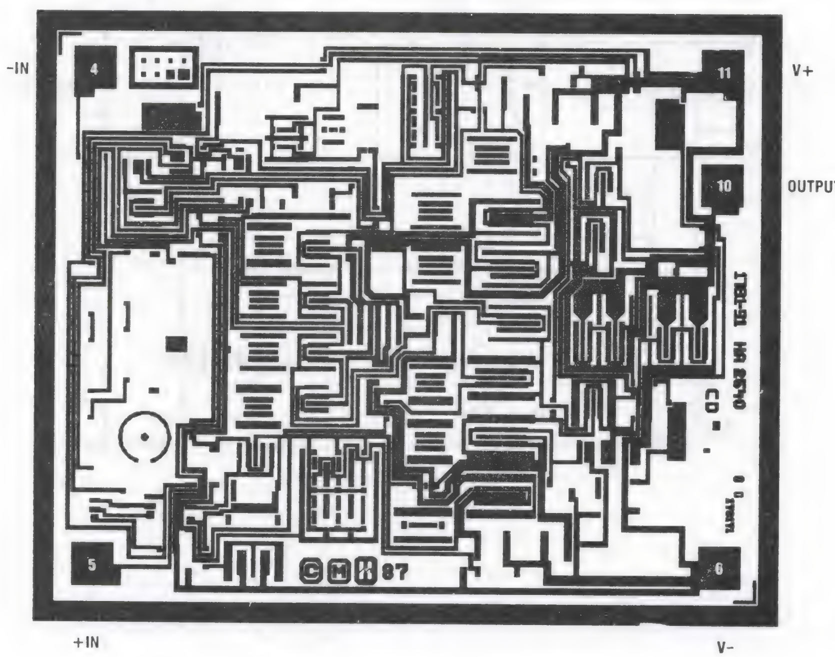
TRANSISTOR COUNT: 30

PROCESS: High Frequency Bipolar Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

Metallization Mask Layout

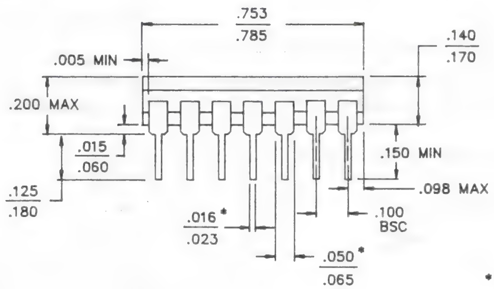
HA-2540/883

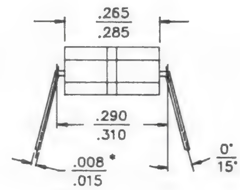


NOTE: Pin Numbers Correspond to 14 Pin DIP Package Only.

Packaging†

14 PIN CERAMIC DIP



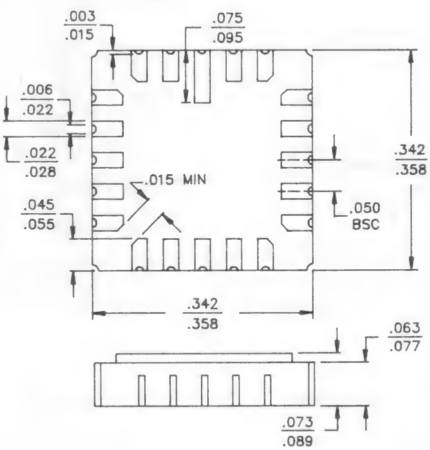


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-1

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

3
OP AMPs & COMPARATORS

HARRIS

HA-2540

DESIGN INFORMATION

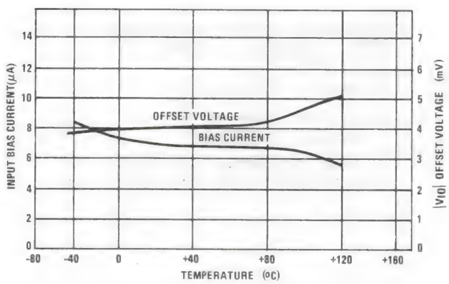
Wideband, Fast Settling Operational Amplifier

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

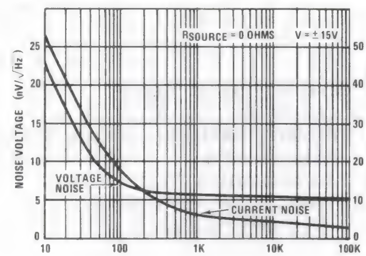
Typical Performance Curves

Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

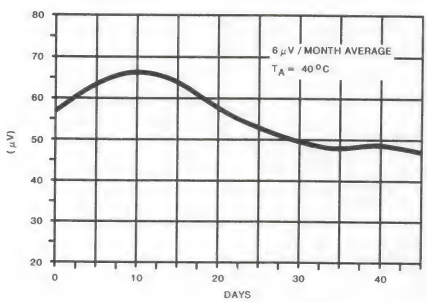
INPUT OFFSET VOLTAGE AND BIAS CURRENT vs. TEMPERATURE



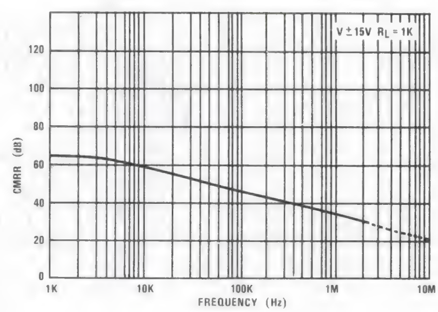
INPUT NOISE VOLTAGE AND NOISE CURRENT vs. FREQUENCY



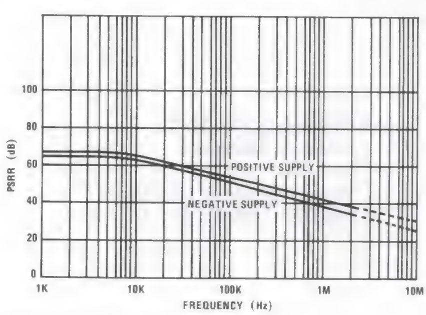
HA-2540 OFFSET VOLTAGE DRIFT vs. TIME



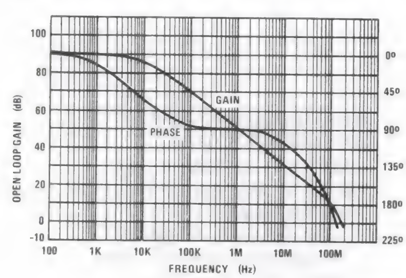
COMMON MODE REJECTION RATIO vs. FREQUENCY



POWER SUPPLY REJECTION RATIO vs. FREQUENCY



OPEN LOOP GAIN/PHASE vs. FREQUENCY HA-2540

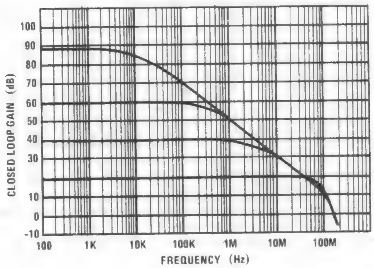


DESIGN INFORMATION (Continued)

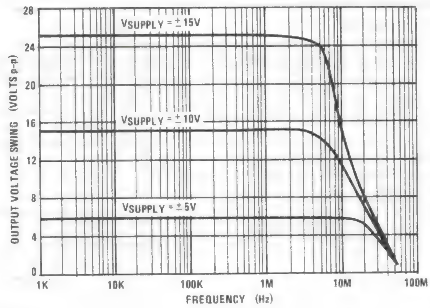
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

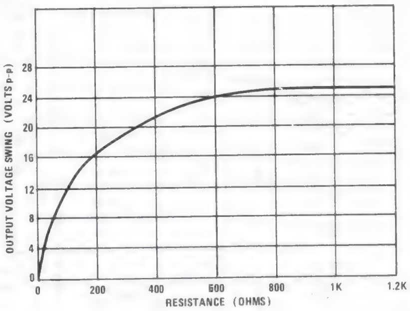
CLOSED LOOP FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS



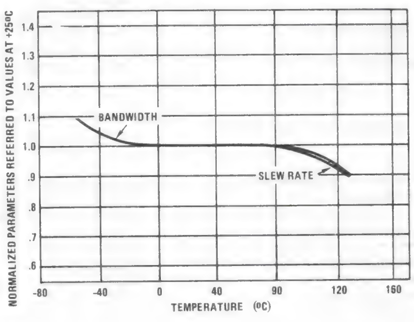
OUTPUT VOLTAGE SWING vs. FREQUENCY



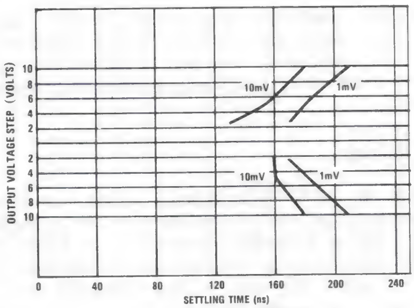
OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



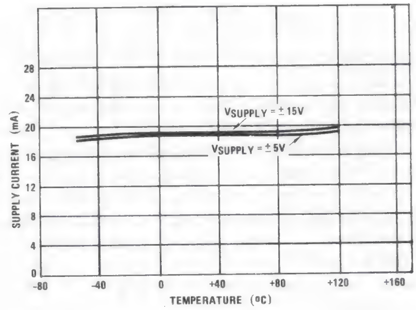
NORMALIZED AC PARAMETERS vs. TEMPERATURE



SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



POWER SUPPLY CURRENT vs. TEMPERATURE AND SUPPLY VOLTAGE



DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_L = 1kΩ, $C_L \leq$ 10pF, A_V = 10V/V, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage	V_{CM} = 0V	+25°C	8	Table 1	mV
Average Offset Voltage Drift	Versus Temperature	-55°C to +125°C	20	30	µV/°C
	Versus Time	+40°C	6	12	µV/Month
Bias Current	V_{CM} = 0V	+25°C	6	Table 1	µA
Differential Input Resistance		+25°C	10	5	kΩ
Input Capacitance		+25°C	1	3	pF
Input Noise Voltage Density	f_O = 10Hz	+25°C	22	40	$nV/\sqrt{Hz}$
	f_O = 100Hz	+25°C	8	20	$nV/\sqrt{Hz}$
	f_O = 1kHz	+25°C	6	15	$nV/\sqrt{Hz}$
Input Noise Current Density	f_O = 10Hz	+25°C	50	80	$pA/\sqrt{Hz}$
	f_O = 100Hz	+25°C	20	30	$pA/\sqrt{Hz}$
	f_O = 1kHz	+25°C	6	10	$pA/\sqrt{Hz}$
Broadband Noise	0.1Hz to 1MHz	+25°C	50	75	μV_{p-p}
Slew Rate	V_{OUT} = ±5V	+25°C	400	Table 2	V/µs
		-55°C to +125°C	280	250	V/µs
Full Power Bandwidth	V_{PEAK} = 10V	+25°C	6.4	Table 2	MHz
		-55°C to +125°C	4.5	4.0	MHz
Settling Time	A_V = -10V/V, 10V to 0.1%	+25°C	140	200	ns
Differential Gain Error	$f_O \leq$ 5MHz	+25°C	3	5	%
Differential Phase Error	$f_O \leq$ 5MHz	+25°C	1	2	Degree
Output Resistance	Open Loop	+25°C	30	Table 3	Ω
Supply Current	I_{OUT} = 0mA	-55°C to +125°C	19	Table 1	mA
Minimum Supply Voltage	Functional Operation Only. Other Parameters Will Vary.	+25°C	±5	±7	V

Application Information

When using the HA-2540 for high frequency performance, care must be given in the system's design to optimize this component's use. High frequency layout techniques, ground planning, supply decoupling, and short lead lengths will help eliminate unwanted parasitic effects. A suggested component's choice for the feedback and input resistor is to keep their valve as small as possible, preferably less than 1kΩ. Capacitive loading, which cause a loss of phase margin can be increased by adding series resistance in the output path. Closed loop gain of less than 10 should not be designed due also to a loss of phase margin. If circuits must be designed in lower gains, inverting methods are recommended. Output saturation to the -V rail which may cause regeneration or oscillation during saturation, should also be avoided.

For other application suggestions, please refer to Application Note 541 which includes methods for DC error reductions, frequency compensation, higher output current and voltage circuits and other high frequency circuits.

Heat Sinking

Although not required for compliancy of /883, heat sinking is suggested in high ambient conditions (> 75°C). Suggested models include thermalloy model 6007 or AAVID model 5602B. Junction temperature should be maintained below +175°C. Further information is provided in Application Note 556, and proper thermal resistance values are provided in the thermal information section.

HARRIS

HA-2541/883

Wideband, Fast Settling, Unity Gain Stable, Operational Amplifier

January 1989

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Unity Gain Bandwidth .... 40MHz (Min)**
- **High Slew Rate .... 200V/µs (Min) 250V/µs (Typ)**
- **Low Offset Voltage .... 2mV (Max)**
- **Fast Settling Time (0.1%) .... 90ns (Typ)**
- **Power Bandwidth .... 3MHz (Min) 4MHz (Typ)**
- **Output Voltage Swing .... ±10V (Min)**
- **Unity Gain Stability**
- **Monolithic Bipolar Dielectric Isolation Construction**

Applications

- **Pulse and Video Amplifiers**
- **Wideband Amplifiers**
- **High Speed Sample and Hold Circuits**
- **Fast, Precise D/A Converters**
- **High Speed A/D Input Buffer**

Description

The HA-2541/883 is the first unity gain stable monolithic operational amplifier to achieve 40MHz unity gain bandwidth. A major addition to the Harris series of high speed, wideband op amps, the HA-2541/883 is designed for video and pulse applications requiring stable amplifier response at low closed loop gains.

The uniqueness of the HA-2541/883 is that its slew rate and bandwidth characteristics are specified at unity gain. Historically, high slew rate, wide bandwidth and unity gain stability have been incompatible features for a monolithic operational amplifier. But features such as 250V/µs slew rate and 40MHz unity gain bandwidth clearly show that this is not the case for the HA-2541/883. These features, along with 90ns settling time to 0.1%, make this product an excellent choice for high speed data acquisition systems.

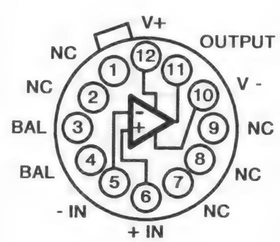
High frequency or video systems which require precise D.C. retention are other applications of the HA-2541/883. Built using dielectric isolation, the HA-2541/883 is specified over the -55°C to +125°C temperature range and is available in a Metal Can (TO-8) package.

3

OP AMPs & COMPARATORS

Pinout

HA2-2541/883 (METAL CAN)
TOP VIEW



Case tied to V-

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage 6V
Voltage at Either Input Terminal .... V+ to V-
Peak Output Current (< 10% Duty Cycle) 50mA
Junction Temperature (T_J) .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... < 2000V
Lead Temperature (Soldering 10 sec) .... +275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Metal Can Package	50°C/W	30°C/W

Package Power Dissipation Limit at +75°C For $T_J \le 175°C$
Metal Can Package 2W
Package Power Dissipation Derating Factor Above +75°C
Metal Can Package .... 20mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±12V to ±15V
$V_{INcm} \le 1/2$ (V+ - V-)
$R_L \ge 1k\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, $R_{SOURCE} = 100\Omega$, $R_{LOAD} = 100k\Omega$, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	V_{CM} = 0V	1	+25°C	-2	2	mV
			2, 3	+125°C, -55°C	-6	6	mV
Input Bias Current	$+I_B$	V_{CM} = 0V $+R_S = 1.1k\Omega$ $-R_S = 100\Omega$	1	+25°C	-25	25	µA
			2, 3	+125°C, -55°C	-35	35	µA
	$-I_B$	V_{CM} = 0V $+R_S = 100\Omega$ $-R_S = 1.1k\Omega$	1	+25°C	-50	50	µA
			2, 3	+125°C, -55°C	-35	35	µA
Input Offset Current	I_{IO}	V_{CM} = 0V $+R_S = 1.1k\Omega$ $-R_S = 1.1k\Omega$	1	+25°C	-50	50	µA
			2, 3	+125°C, -55°C	-9	9	µA
Common Mode Range	+CMR	V+ = 5V V- = -25V	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	-CMR	V+ = 25V V- = -5V	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
Large Signal Voltage Gain	$+A_{VOL}$	V_{OUT} = 0V and +10V $R_L = 1k\Omega$	4	+25°C	10	-	kV/V
			5, 6	+125°C, -55°C	5	-	kV/V
	$-A_{VOL}$	V_{OUT} = 0V and -10V $R_L = 1k\Omega$	4	+25°C	10	-	kV/V
			5, 6	+125°C, -55°C	5	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔV_{CM} = +10V +V = +5V -V = -25V V_{OUT} = -10V	1	+25°C	70	-	dB
			2, 3	+125°C, -55°C	70	-	dB
	-CMRR	ΔV_{CM} = -10V +V = +25V -V = -5V V_{OUT} = +10V	1	+25°C	70	-	dB
			2, 3	+125°C, -55°C	70	-	dB

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 100kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Voltage Swing	$+V_{OUT}$	R_L = 1kΩ	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	$-V_{OUT}$	R_L = 1kΩ	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
Output Current	$+I_{OUT}$	V_{OUT} = -10V	1	+25°C	10	-	mA
			1, 3	+125°C, -55°C	10	-	mA
	$-I_{OUT}$	V_{OUT} = +10V	1	+25°C	-	-10	mA
			2, 3	+125°C, -55°C	-	-10	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-	39	mA
			2, 3	+125°C, -55°C	-	39	mA
	$-I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-39	-	mA
			2, 3	+125°C, -55°C	-39	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = 10V +V = +5V, -V = -15V +V = +15V, -V = -15V	1	+25°C	70	-	dB
			2, 3	+125°C, -55°C	70	-	dB
	-PSRR	ΔV_{SUP} = 10V +V = +15V, -V = -5V +V = +15V, -V = -15V	1	+25°C	70	-	dB
			2, 3	+125°C, -55°C	70	-	dB
Offset Voltage Adjustment	$+V_{IO}Adj$	Note 5	1	+25°C	V_{IO}-1	-	mV
	$-V_{IO}Adj$	Note 5	1	+25°C	V_{IO}+1	-	mV

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Table 2 Intentionally Left Blank. See A.C. Specifications on Table 3.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_{LOAD} = 1kΩ, $C_{LOAD} \leq$ 10pF, A_V = 1V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Differential Input Resistance	R_{IN}	V_{CM} = 0V	1	+25°C	40	-	kΩ
Unity Gain Bandwidth	UGBW	V_O = 90mV	1	+25°C	40	-	MHz
Slew Rate	+SR	V_{OUT} = -3V to +3V	1	+25°C	200	-	V/µs
	-SR	V_{OUT} = +3V to -3V	1	+25°C	200	-	V/µs
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	+25°C	3	-	MHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 1kΩ, $C_L \leq$ 10pF	1	-55°C to +125°C	1	-	V/V
Rise & Fall Time	T_R	V_{OUT} = 0V to +200mV	1, 4	+25°C	-	20	ns
	T_F	V_{OUT} = 0V to -200mV	1, 4	+25°C	-	20	ns
Overshoot	+OS	V_{OUT} = 0V to +200mV	1	+25°C	-	50	%
	-OS	V_{OUT} = 0V to -200mV	1	+25°C	-	50	%
Output Resistance	R_{OUT}	Open Loop	1	+25°C	-	25	Ω
Quiescent Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	1.17	W

NOTES: 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).

3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)

4. Measured between 10% and 90% points.

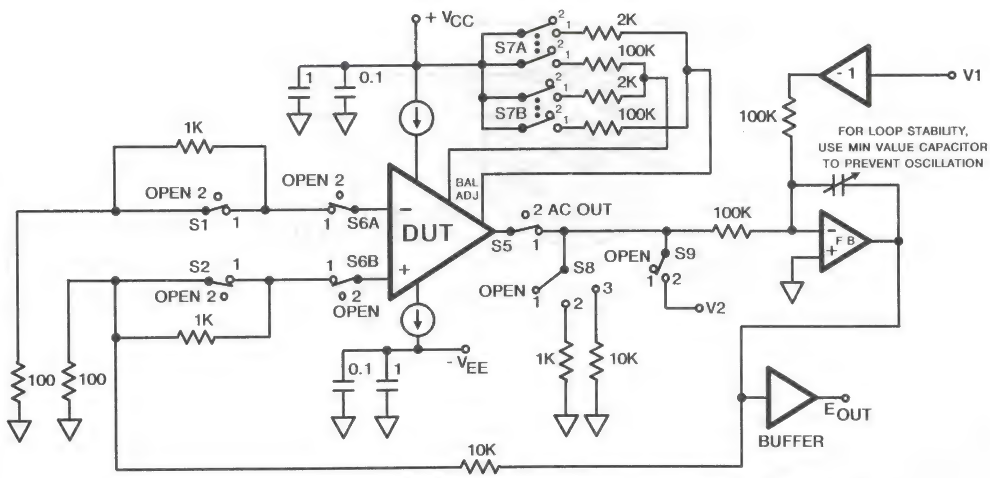
5. Offset adjustment range is [V_{IO} (Measured) ± 1mV] minimum referred to output. This test is for functionality only to assure adjustment through 0V.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6
Group A Test Requirements	1, 2, 3, 4, 5, 6
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

Test Circuit (Applies to Table 1)

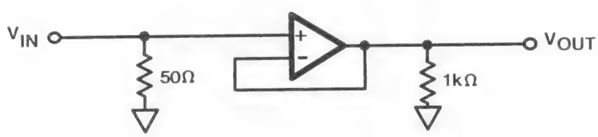


ALL RESISTORS = ± 1% (Ω)
ALL CAPACITORS = ± 10% (μF)

For Detailed Information, Refer to HA-2541/883 Test Tech Brief

Test Waveforms

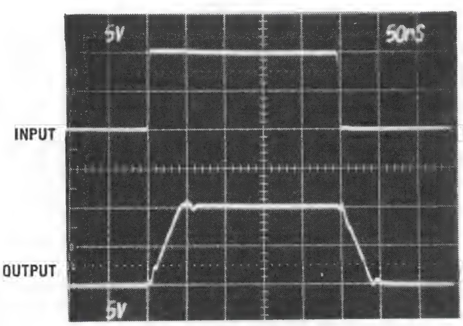
SIMPLIFIED TEST CIRCUIT FOR LARGE AND SMALL SIGNAL RESPONSE (Applies to Table 3)



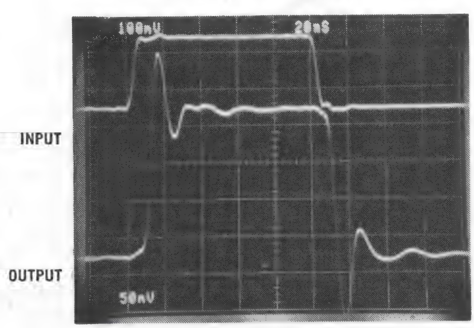
$V_S = \pm 15V$
$A_V = +1$
$C_L \leq 10pF$

Note: No capacitive load, maintain parasitics less than 10pF.

MEASURED LARGE SIGNAL RESPONSE
Vertical Scale: Input = 5V/Div., Output = 5V/Div.
Horizontal Scale: Time: 50ns/Div.

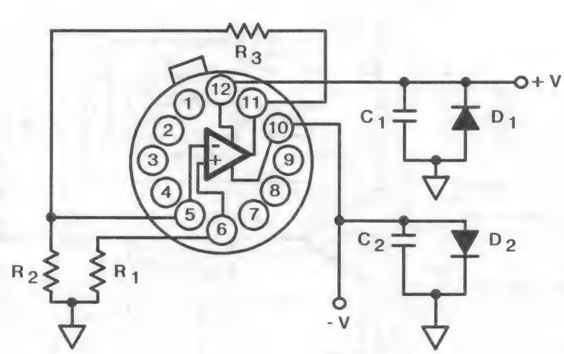


MEASURED SMALL SIGNAL RESPONSE
Vertical Scale: Input = 100mV/Div., Output = 50mV/Div.
Horizontal Scale: 20ns/Div.



Burn-In Circuits

HA2-2541/883 TO-8 METAL CAN



NOTES:

$R_1 = R_2 = 100k\Omega$, ±5%, 1/4W (Min)

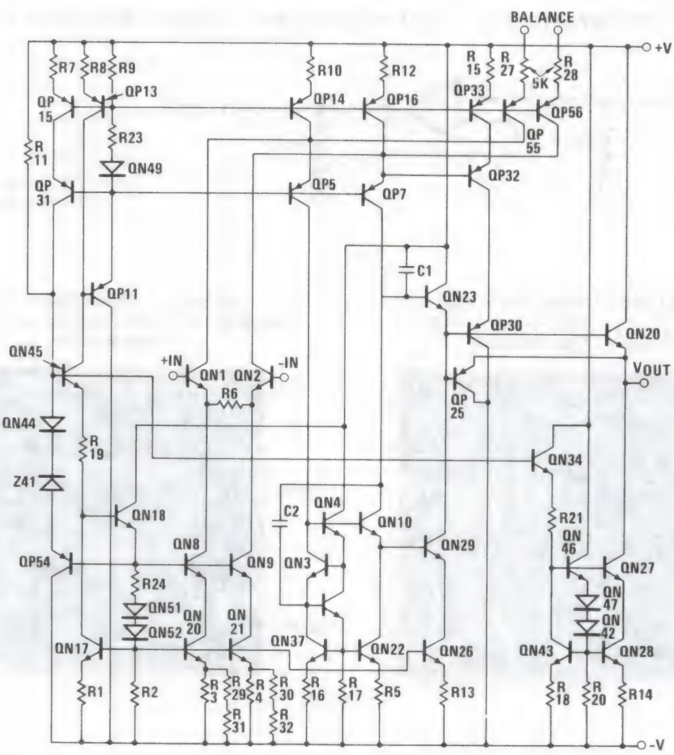
$R_3 = 1M\Omega$, ±5%, 1/4W (Min)

$C_1 = C_2 = 0.01\mu F$/Socket (Min) or $0.1\mu F$/Row, (Min)

$D_1 = D_2 =$ IN4002 or Equivalent/Board

$|(V+) - (V-)| = 30V$

Schematic Diagram



Die Characteristics

DIE DIMENSIONS:
89.8 x 79.5 x 19 mils
(2280 x 2020 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$0.53 \times 10^5 A/cm^2$ @ 2.23mA

SUBSTRATE POTENTIAL (POWERED UP): V-

GLASSIVATION:
Type: Silox
Thickness: 14kÅ ± 1kÅ

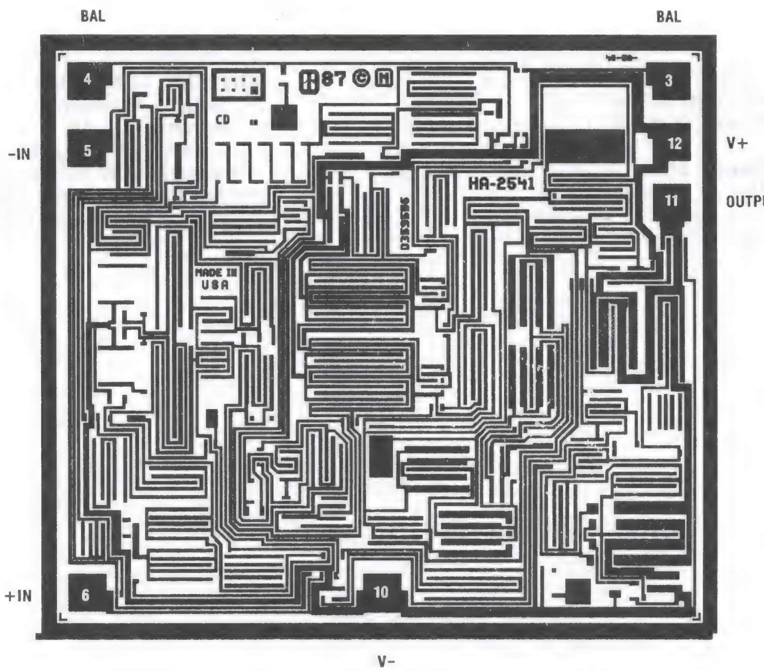
TRANSISTOR COUNT: 41

PROCESS: High Frequency Bipolar Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Metal Can — 420°C (Max)

Metallization Mask Layout

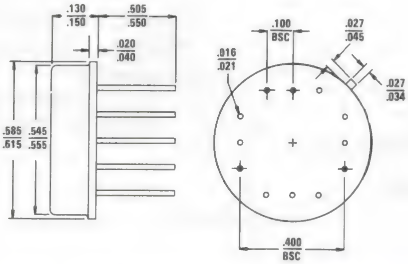
HA-2541/883



NOTE: Pin Numbers Correspond to 12 Pin TO-8 Metal Can Package Only.

Packaging†

12 PIN TO-8 METAL CAN



LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
Material: No Seal Material
Temperature: Room Temperature
Method: Resistance Weld

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
PACKAGE CASE VOLTAGE POTENTIAL: V-
COMPLIANT PACKAGE: None
PACKAGE USED: JEDEC 'AB'

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HA-2541

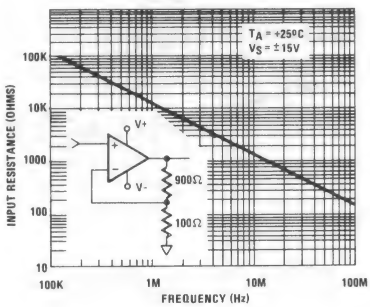
DESIGN INFORMATION

Wideband, Fast Settling, Unity Gain Stable, Operational Amplifier

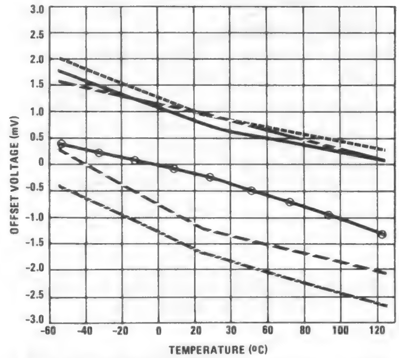
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

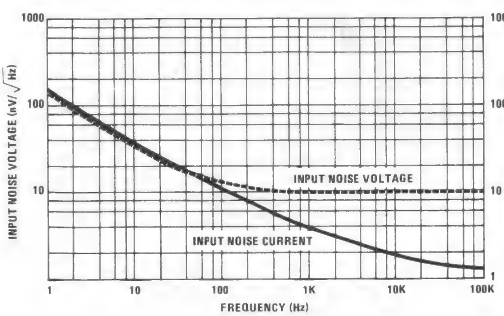
INPUT RESISTANCE vs. FREQUENCY



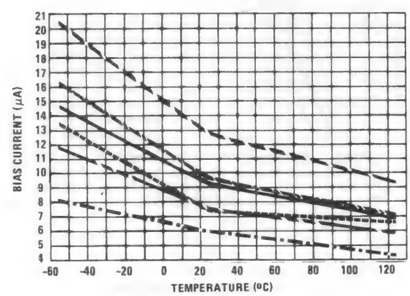
OFFSET VOLTAGE DRIFT WITH TEMPERATURE
Of 6 Representative Units



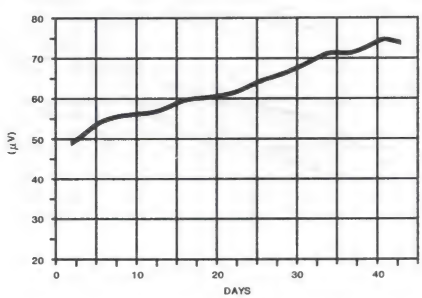
NOISE DENSITY vs. FREQUENCY
$T_A = +25^oC$



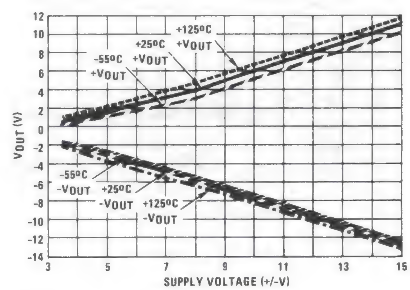
BIAS CURRENT DRIFT WITH TEMPERATURE
Of 6 Representative Units



AVERAGE OFFSET VOLTAGE DRIFT vs. TIME
16.2μV/Month Average



OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE
At Various Temperatures



DESIGN INFORMATION (Continued)

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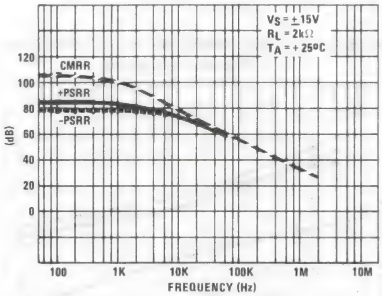
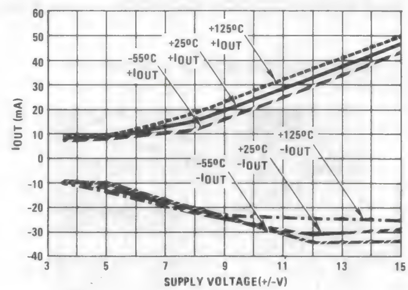
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

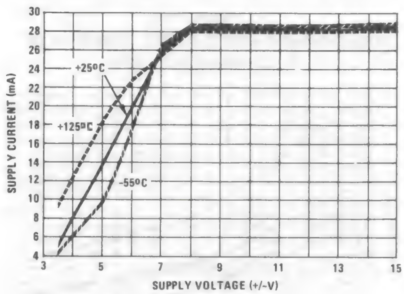
REJECTION RATIOS vs. FREQUENCY



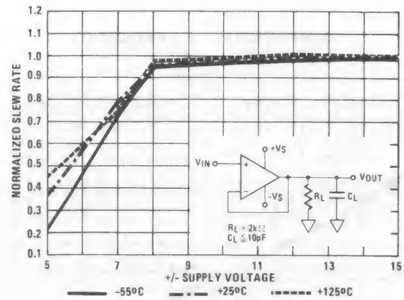
OUTPUT CURRENT vs. SUPPLY VOLTAGE
At Various Temperatures



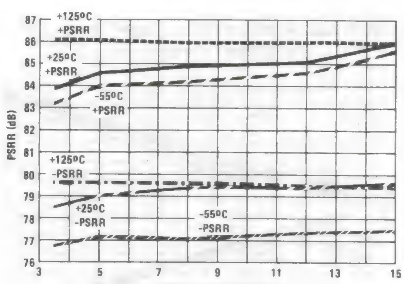
SUPPLY CURRENT vs. SUPPLY VOLTAGE
At Various Temperatures



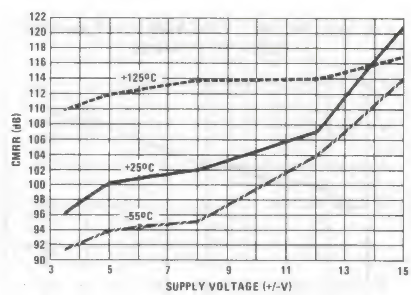
SLEW RATE vs. SUPPLY VOLTAGE
Normalized with $V_S = \pm15V$ at $+25^oC$



PSRR vs. SUPPLY VOLTAGE
Average of 3 Lots at Various Temperatures



CMRR vs. SUPPLY VOLTAGE
Average of 3 Lots at Various Temperatures

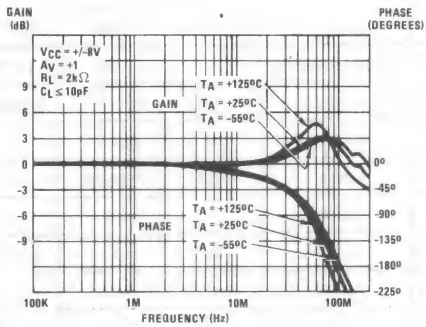


DESIGN INFORMATION (Continued)

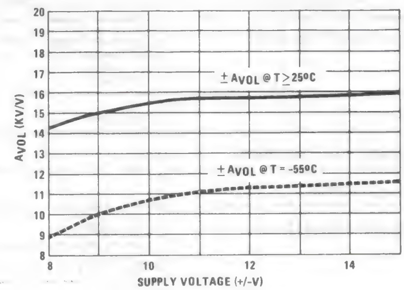
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

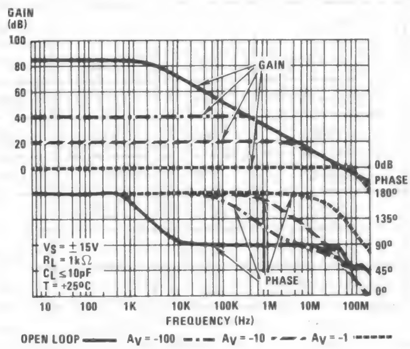
CLOSE LOOP FREQUENCY RESPONSE vs. TEMPERATURE
At $V_S = \pm8V$



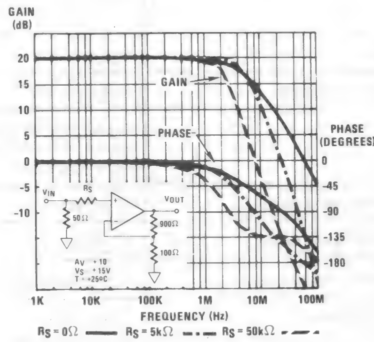
+/- OPEN LOOP GAIN vs. SUPPLY VOLTAGE
Average of 3 Lots Over Temperature



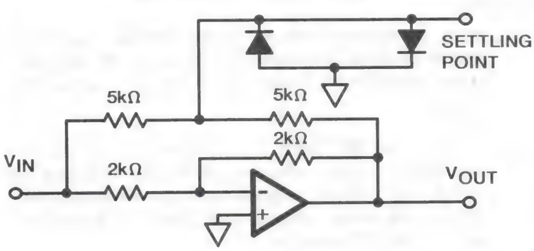
GAIN AND PHASE FREQUENCY RESPONSE
$V_S = \pm15V$, $R_L = 1k$, $C_L \leq 10pF$, $T_A = +25^oC$



SMALL SIGNAL BANDWIDTH vs. SOURCE RESISTANCE
$V_S = \pm15V$, $R_L = 1k\Omega$

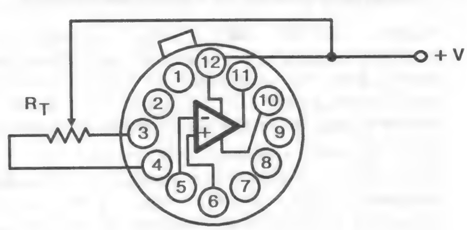


SETTLING TIME TEST CIRCUIT



- $A_V = -1$
- Feedback and Summing Resistors Must Be Matched (0.1%)
- HP5082-2810 Clipping Diodes Recommended
- Tektronix P6201 FET Probe Used At Settling Point.

SUGGESTED OFFSET VOLTAGE ADJUSTMENT



Tested Offset Adjustment Range is $|V_{OS} + 1mV|$ minimum referred to output. Typical range is ±7.5mV with $R_T = 5k\Omega$, or ±15mV with $R_T = 100k\Omega$.

3

OP AMPs & COMPARATORS

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_L = 1kΩ, $C_L \leq$ 100pF, A_V = 1V/V, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMIT	UNITS
Average Offset Voltage Drift	Versus Temperature	-55°C to +125°C	9	15	µV/°C
	Versus Time	+40°C	16	20	µV/Month
Bias Current	V_{CM} = 0V	+25°C	11	Table 1	µA
Differential Input Resistance		+25°C	100	Table 3	kΩ
Input Capacitance		+25°C	1	3	pF
Input Noise Voltage Density	f_O = 10Hz	+25°C	40	60	$nV/\sqrt{Hz}$
	f_O = 100Hz	+25°C	15	30	$nV/\sqrt{Hz}$
	f_O = 1kHz	+25°C	10	20	$nV/\sqrt{Hz}$
Input Noise Current Density	f_O = 10Hz	+25°C	40	80	$pA/\sqrt{Hz}$
	f_O = 100Hz	+25°C	10	30	$pA/\sqrt{Hz}$
	f_O = 1kHz	+25°C	4	10	$pA/\sqrt{Hz}$
Slew Rate	V_{OUT} = ±3V	-55°C to +125°C	250	150	V/µs
Full Power Bandwidth	V_{PEAK} = 10V	-55°C to +125°C	4	2.4	MHz
Settling Time	A_V = -1V/V, 10V Step to 0.1%	+25°C	90	150	ns
	A_V = -1V/V, 10V Step to 0.01%	+25°C	175	300	ns
Differential Gain Error	$f_O \leq$ 5MHz	+25°C	0.1	0.5	%
Differential Phase Error	$f_O \leq$ 5MHz	+25°C	0.2	1	Degree
Propagation Delay	V_{OUT} = ±200mV	-55°C to +125°C	6	10	ns
Output Resistance	Open Loop	+25°C	15	Table 3	Ω
Minimum Supply Voltage	Functional Operation Only. Other Parameters Will Vary.	+25°C	±7	±8	V

Applying the HA-2541 (Also see Applications Note 550)

1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with 0.01µF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.
2. HEAT SINKING: Although not required for /883 qualification, heat sinking is suggested in high ambient conditions. Recommended heat sinks include Thermalloy #2240A or #2268B for TO-8 Metal Can. Also review Application Note 556 for safe operating area information. Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below +175°C.
3. WIRING CONSIDERATIONS: Video pulse circuits should be built on a ground plane. Minimum point to point connections directly to the amplifier terminals should be used. When ground planes cannot be used, good single point grounding techniques should be applied.
4. OUTPUT SHORT CIRCUIT: HA-2541 does not have output short circuit protection. Short circuits to ground can be tolerated for approximately 10 seconds. Short circuits to either supply will result in immediate destruction of the device.
5. HEAVY CAPACITIVE LOADS: When driving heavy capacitive loads ($\geq$ 100pF) a small resistor ($\approx$ 100Ω) should be connected in series with the output and inside the feedback loop.

HARRIS

HA-2542/883

Wideband, High Slew Rate, High Output Current, Operational Amplifier

January 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Stable at Gains of 2 or Greater
- Gain Bandwidth .... 70MHz (Min)
- High Slew Rate .... 300V/µs (Min)
- High Output Current .... 100mA (Min)
- Power Bandwidth .... 5.5MHz (Typ)
- Output Voltage Swing .... ±10V (Min)
- Monolithic Bipolar Dielectric Isolation Construction

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- Coaxial Cable Drivers
- Fast Sample and Hold Circuits
- High Frequency Signal Conditioning Circuits

Description

The HA-2542/883 is a wideband, high slew rate, monolithic operational amplifier featuring an outstanding combination of speed, bandwidth, and output drive capability.

Utilizing the advantages of the Harris D.I. technology this amplifier offers 350V/µs slew rate, 70MHz gain bandwidth, and ±100mA output current. Application of this device is further enhanced though stable operation down to closed loop gains of 2.

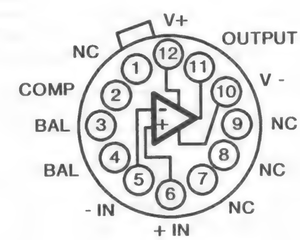
For additional flexibility, offset null and frequency compensation controls are included in the HA-2542/883 pinout.

The capabilities of the HA-2542/883 are ideally suited for high speed coaxial cable driver circuits where low gain and high output drive requirements are necessary. With 5.5MHz full power bandwidth, this amplifier is most suitable for high frequency signal conditioning circuits and pulse video amplifiers. Other applications utilizing the HA-2542/883 advantages include wideband amplifiers and fast sample and hold circuits. The HA-2542/883 is specified over the $-55^{o}C$ to $+125^{o}C$ military temperature range and is available in 12 lead (TO-8) package.

Pinout

HA2-2542/883 (METAL CAN)

TOP VIEW



Case tied to V-

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage 6V
Voltage at Either Input Terminal .... V+ to V-
Peak Output Current (< 10% Duty Cycle) 125mA
Junction Temperature (T_J) .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... < 2000V
Lead Temperature (Soldering 10 sec) .... +275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Metal Can Package	47°C/W	29°C/W

Package Power Dissipation Limit at +75°C For $T_J \leq$ 175°C
Metal Can Package 2.1W
Package Power Dissipation Derating Factor Above +75°C
Metal Can Package .... 21.4mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±12V to ±15V
$V_{INcm} \leq$ 1/2 (V+ - V-)
$R_L \geq 100\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, $R_{SOURCE} = 100\Omega$, $R_{LOAD} = 100k\Omega$, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	V_{CM} = 0V	1	+25°C	-10	10	mV
			2, 3	+125°C, -55°C	-20	20	mV
Input Bias Current	$+I_B$	V_{CM} = 0V $+R_S = 1.1k\Omega$ $-R_S = 100\Omega$	1	+25°C	-35	35	µA
			2, 3	+125°C, -55°C	-50	50	µA
	$-I_B$	V_{CM} = 0V $+R_S = 100\Omega$ $-R_S = 1.1k\Omega$	1	+25°C	-35	35	µA
			2, 3	+125°C, -55°C	-50	50	µA
Input Offset Current	I_{IO}	V_{CM} = 0V $+R_S = 1.1k\Omega$ $-R_S = 1.1k\Omega$	1	+25°C	-7	7	µA
			2, 3	+125°C, -55°C	-9	9	µA
Common Mode Range	+CMR	V+ = 5V V- = -25V	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	-CMR	V+ = 25V V- = -5V	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
Large Signal Voltage Gain	$+A_{VOL}$	V_{OUT} = 0V and +10V $R_L = 1k\Omega$	4	+25°C	10	-	kV/V
			5, 6	+125°C, -55°C	5	-	kV/V
	$-A_{VOL}$	V_{OUT} = 0V and -10V $R_L = 1k\Omega$	4	+25°C	10	-	kV/V
			5, 6	+125°C, -55°C	5	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔV_{CM} = +10V +V = +5V -V = -25V V_{OUT} = -10V	1	+25°C	70	-	dB
			2, 3	+125°C, -55°C	70	-	dB
	-CMRR	ΔV_{CM} = -10V +V = +25V -V = -5V V_{OUT} = +10V	1	+25°C	70	-	dB
			2, 3	+125°C, -55°C	70	-	dB

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 100kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Output Voltage Swing	$+V_{OUT}$	R_L = 1kΩ	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	$-V_{OUT}$	R_L = 1kΩ	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
Output Current	$+I_{OUT}$	V_{OUT} = -5V	1	+25°C	100	-	mA
	$-I_{OUT}$	V_{OUT} = +5V	1	+25°C	100	-	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V, I_{OUT} = 0mA	1	+25°C	-	34.5	mA
			2, 3	+125°C, -55°C	-	34.5	mA
	$-I_{CC}$	V_{OUT} = 0V, I_{OUT} = 0mA	1	+25°C	-34.5	-	mA
			2, 3	+125°C, -55°C	-34.5	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = 10V +V = +5V, -V = -15V +V = +15V, -V = -15V	1	+25°C	70	-	dB
			2, 3	+125°C, -55°C	70	-	dB
	-PSRR	ΔV_{SUP} = 10V +V = +15V, -V = -5V +V = +15V, -V = -15V	1	+25°C	70	-	dB
			2, 3	+125°C, -55°C	70	-	dB
Offset Voltage Adjustment	$+V_{IO}Adj$	Note 5	1	+25°C	V_{IO}-1	-	mV
	$-V_{IO}Adj$	Note 5	1	+25°C	V_{IO}+1	-	mV

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Table 2 Intentionally Left Blank. See A.C. Specifications on Table 3.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_{LOAD} = 1kΩ, C_{LOAD} ≤ 10pF, A_V = 2V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Differential Input Resistance	R_{IN}	V_{CM} = 0V	1	+25°C	40	-	kΩ
Gain Bandwidth Product	GBWP	V_O = 200mV, f_o = 10kHz	1	+25°C	70	-	MHz
		V_O = 200mV, f_o = 1MHz	1	+25°C	70	-	MHz
Slew Rate	+SR	V_{OUT} = -5V to +5V	1	+25°C	300	-	V/µs
	-SR	V_{OUT} = +5V to -5V	1	+25°C	300	-	V/µs
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	+25°C	4.5	-	MHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 1kΩ, C_L ≤ 10pF	1	-55°C to +125°C	2	-	V/V
Rise & Fall Time	T_R	V_{OUT} = 0V to +200mV	1, 4	+25°C	-	10	ns
	T_F	V_{OUT} = 0V to -200mV	1, 4	+25°C	-	10	ns
Overshoot	+OS	V_{OUT} = 0V to +200mV	1	+25°C	-	40	%
	-OS	V_{OUT} = 0V to -200mV	1	+25°C	-	40	%
Output Resistance	R_{OUT}	V_{OUT} = 0V	1	+25°C	-	25	Ω
Quiescent Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	1.035	W

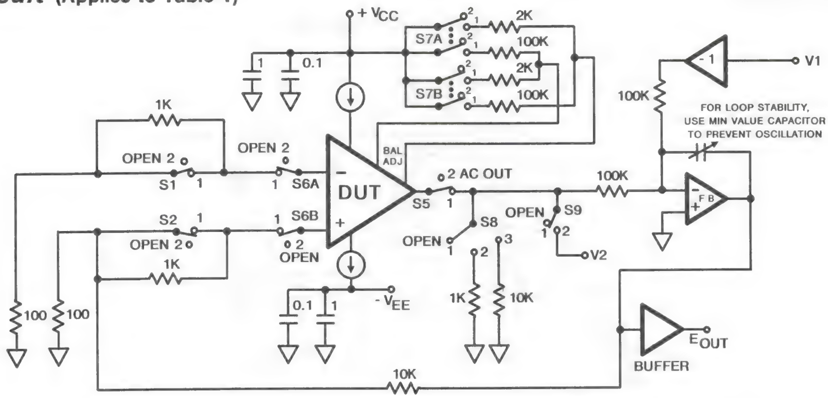
NOTES:
1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).
3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)
4. Measured between 10% and 90% points.
5. Offset adjustment range is [V_{IO} (Measured) ± 1mV] minimum referred to output. This test is for functionality only to assure adjustment through 0V.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6
Group A Test Requirements	1, 2, 3, 4, 5, 6
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

Test Circuit (Applies to Table 1)

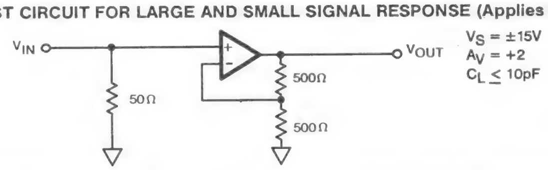


ALL RESISTORS = ± 1% (Ω)
ALL CAPACITORS = ± 10% (μF)

For Detailed Information, Refer to HA-2542/883 Test Tech Brief

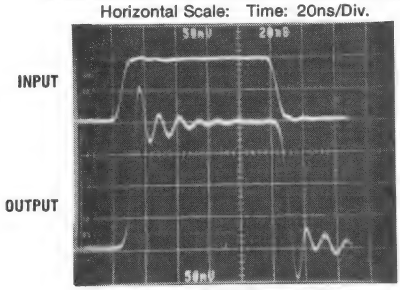
Test Waveforms

SIMPLIFIED TEST CIRCUIT FOR LARGE AND SMALL SIGNAL RESPONSE (Applies to Table 3)



MEASURED LARGE SIGNAL RESPONSE

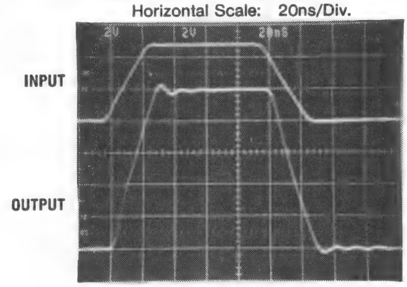
Vertical Scale: Input = 2V/Div., Output = 2V/Div.
Horizontal Scale: Time: 20ns/Div.



$A_V = +2V/V$, $R_L = 1k\Omega$

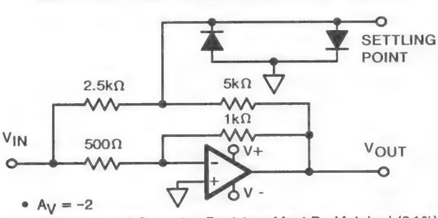
MEASURED SMALL SIGNAL RESPONSE

Vertical Scale: Input = 50mV/Div., Output = 50mV/Div.
Horizontal Scale: 20ns/Div.



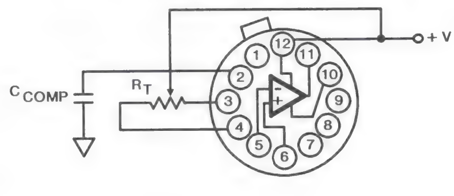
$A_V = +2V/V$, $R_L = 1k\Omega$

SETTLING TIME TEST CIRCUIT FOR TABLE 3



- $A_V = -2$
- Feedback and Summing Resistors Must Be Matched (0.1%).
- HP5082-2810 Clipping Diodes Recommended.
- Tektronix P6201 FET Probe Used At Settling Point.
- For 0.01% settling time, heat sinking is suggested to reduce thermal effects and an analog ground plane with supply decoupling is suggested to minimize ground loop errors.

SUGGESTED OFFSET VOLTAGE ADJUSTMENT AND COMPENSATION CONNECTIONS

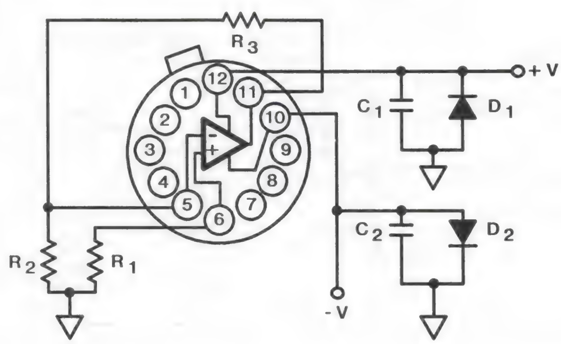


- Suggested compensation scheme 5-20pF
- Tested Offset Adjustment Range is $|V_{OS} + 1mV|$ Minimum Referred To Output. Typical Range For $R_T = 20k\Omega$ is Approximately ±30mV.

3
OP AMPs & COMPARATORS

Burn-In Circuits

HA2-2542/883 TO-8 METAL CAN



NOTES:

$R_1 = R_2 = 100k\Omega$, ±5%, 1/4W (Min)

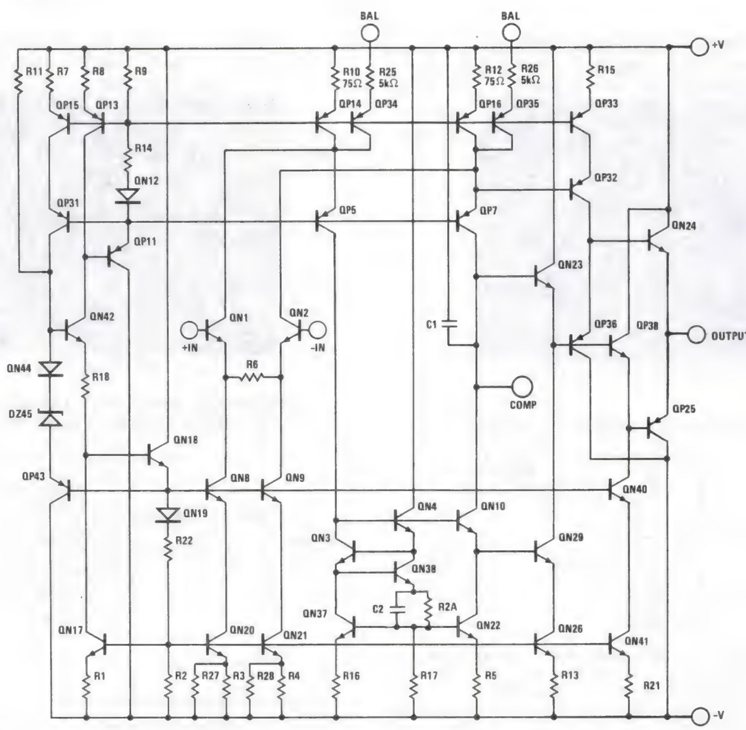
$R_3 = 1M\Omega$, ±5%, 1/4W (Min)

$C_1 = C_2 = 0.01\mu F$/Socket (Min) or $0.1\mu F$/Row, (Min)

$D_1 = D_2$ = IN4002 or Equivalent/Board

$|(V+) - (V-)| = 30V$

Schematic Diagram



Die Characteristics

DIE DIMENSIONS:
106.3 x 72.8 x 19 mils
(2700 x 1850 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$0.4 \times 10^5 A/cm^2$ @ 1.67mA

SUBSTRATE POTENTIAL (POWERED UP): V-

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

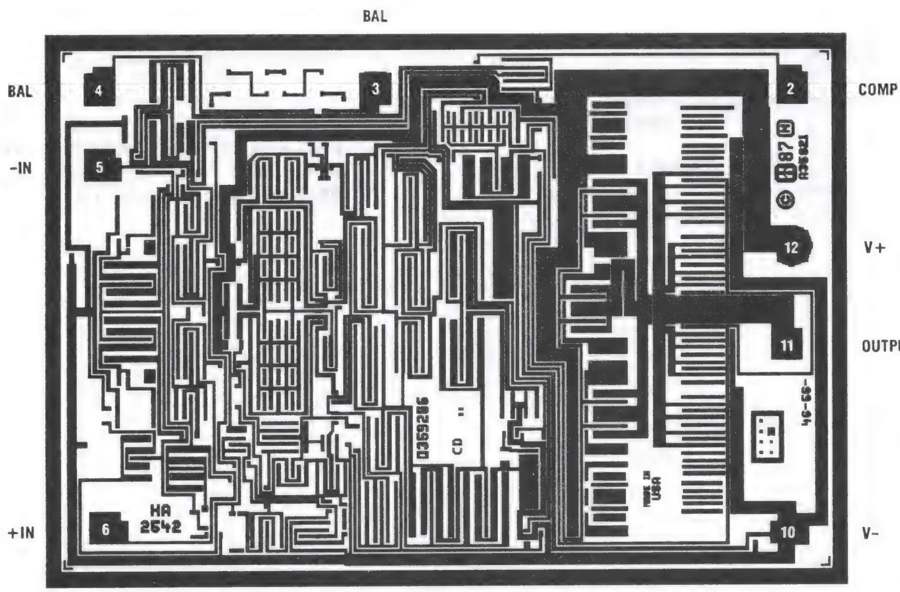
TRANSISTOR COUNT: 43

PROCESS: High Frequency Bipolar Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Metal Can — 420°C (Max)

Metallization Mask Layout

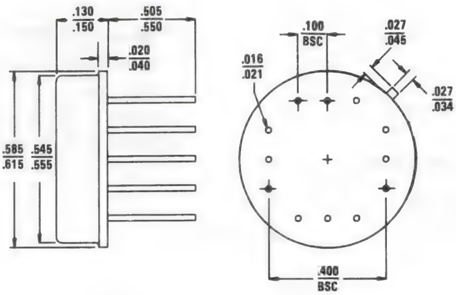
HA-2542/883



NOTE: Pin Numbers Correspond to 12 Pin (TO-8) Metal Can Package Only.

Packaging†

12 PIN TO-8 METAL CAN



LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
Material: No Seal Material
Temperature: Room Temperature
Method: Resistance Weld

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
PACKAGE CASE VOLTAGE POTENTIAL: V-
COMPLIANT PACKAGE: None
PACKAGE USED: JEDEC 'AB'

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

HA-2542

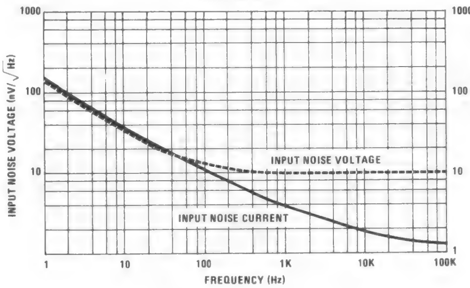
DESIGN INFORMATION

Wideband, High Slew Rate, High Output Current, Operational Amplifier

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

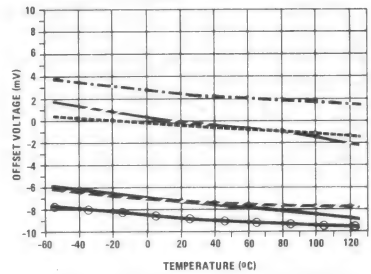
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

INPUT NOISE VOLTAGE AND INPUT NOISE CURRENT vs. FREQUENCY

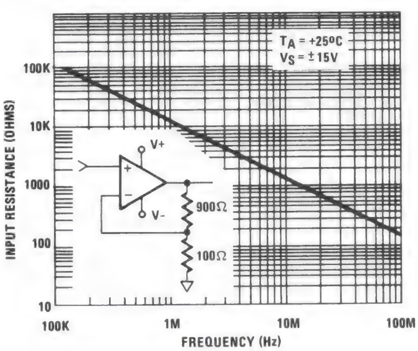


OFFSET VOLTAGE DRIFT WITH TEMPERATURE

Of Six Representative Units, $V_S = +/-12V$

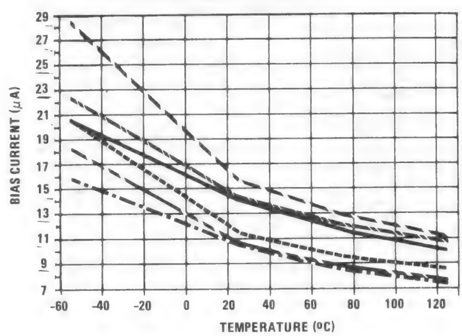


INPUT RESISTANCE vs. FREQUENCY



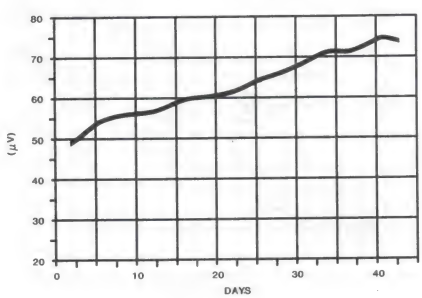
BIAS CURRENT DRIFT WITH TEMPERATURE

Of Six Representative Units, $V_S = +/-12V$



AVERAGE OFFSET VOLTAGE DRIFT vs. TIME

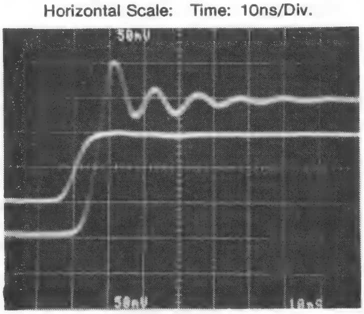
16.2μV/Month Average



TIME DELAY

Vertical Scale: Volts: 100mV/Div.

Horizontal Scale: Time: 10ns/Div.



$V_S = \pm 15V$, $R_L = 1k\Omega$, $T = +25^oC$

Propagation delay variance is negligible over full temperature range.

DESIGN INFORMATION (Continued)

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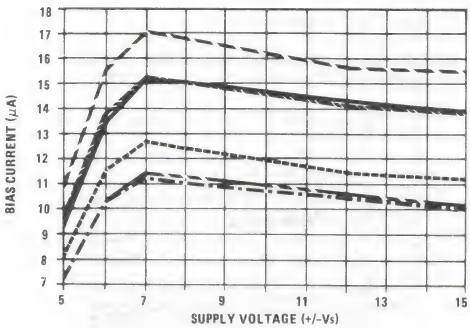
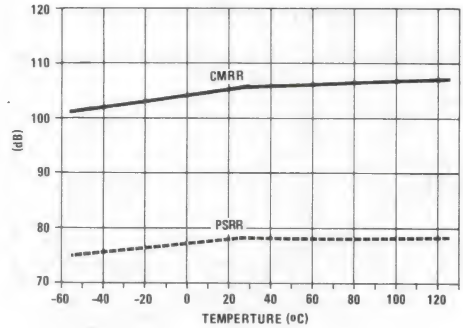
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

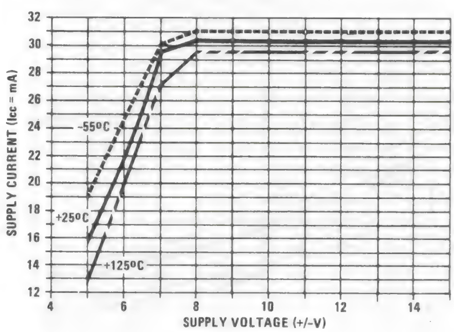
BIAS CURRENT vs. POWER SUPPLY
Six Units At Various Supplies At +25°C



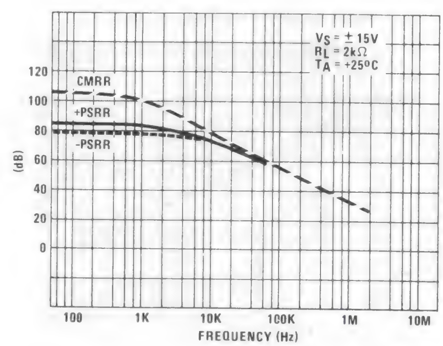
PSRR AND CMRR vs. TEMPERATURE
$V_S = \pm15V$



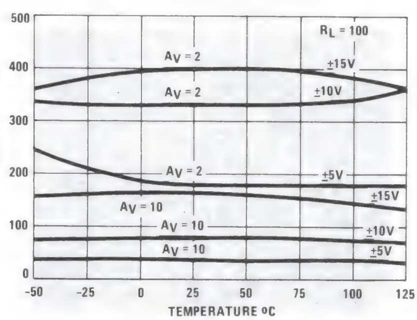
SUPPLY CURRENT vs. SUPPLY VOLTAGE
At Various Temperatures



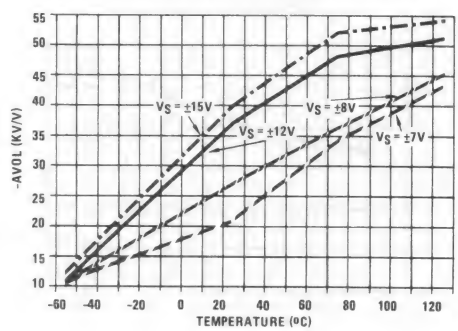
PSRR AND CMRR vs. FREQUENCY



SLEW RATE vs. TEMPERATURE
At Various Supply Voltages With $R_{Load} = 100\Omega$



OPEN LOOP GAIN vs. TEMPERATURE
At Various Supply Voltages



DESIGN INFORMATION (Continued)

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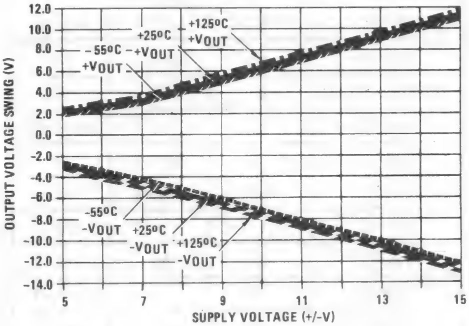
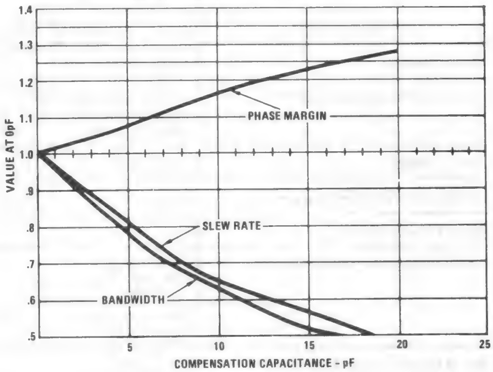
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

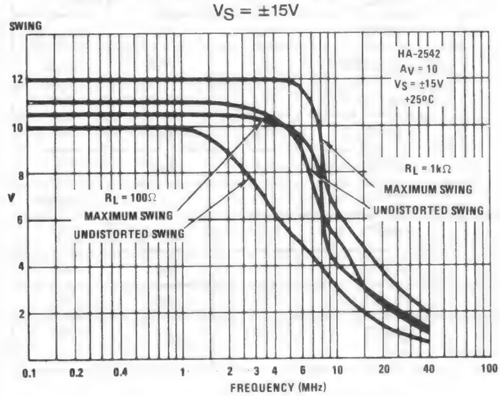
OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE
At Various Temperatures



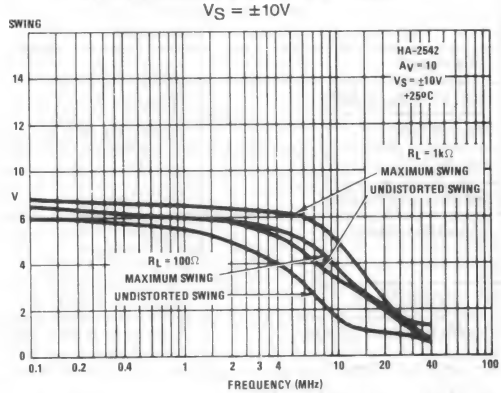
NORMALIZED AC PARAMETERS vs. COMPENSATION CAPACITANCE



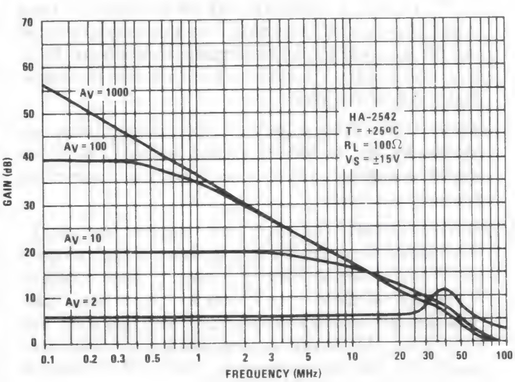
OUTPUT VOLTAGE SWING vs. FREQUENCY
$V_S = \pm15V$



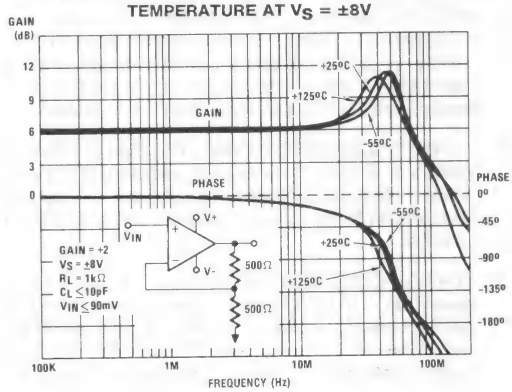
OUTPUT VOLTAGE SWING vs. FREQUENCY
$V_S = \pm10V$



FREQUENCY RESPONSE CURVES



HA-2542 CLOSED LOOP GAIN vs. FREQUENCY AND TEMPERATURE AT $V_S = \pm8V$



DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_L = 1kΩ, C_L ≤ 100pF, A_V = 2V/V, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage	V_{CM} = 0V	+25°C	5	Table 1	mV
Average Offset Voltage Drift	Versus Temperature	-55°C to +125°C	8	15	μV/°C
	Versus Time	+40°C	16	20	μV/Month
Bias Current	V_{CM} = 0V	+25°C	13	Table 1	μA
Differential Input Resistance		+25°C	100	Table 3	kΩ
Input Capacitance		+25°C	1	3	pF
Input Noise Voltage Density	f_O = 10Hz	+25°C	40	60	nV/$\sqrt{Hz}$
	f_O = 100Hz	+25°C	15	30	nV/$\sqrt{Hz}$
	f_O = 1kHz	+25°C	10	20	nV/$\sqrt{Hz}$
Input Noise Current Density	f_O = 10Hz	+25°C	40	80	pA/$\sqrt{Hz}$
	f_O = 100Hz	+25°C	10	30	pA/$\sqrt{Hz}$
	f_O = 1kHz	+25°C	4	10	pA/$\sqrt{Hz}$
Slew Rate	V_{OUT} = ±5V	-55°C to +125°C	400	250	V/μs
Full Power Bandwidth	V_{PEAK} = 10V	-55°C to +125°C	6.4	3.2	MHz
Settling Time	A_V = -2V/V, 10V Step to 0.1%	+25°C	100	150	ns
Differential Gain Error	f_O ≤ 5MHz	+25°C	0.1	0.5	%
Differential Phase Error	f_O ≤ 5MHz	+25°C	0.2	1	Degree
Output Resistance	V_{OUT} = 0V	+25°C	12	Table 3	Ω
	I_{OUT} > 25mA	+25°C	3	10	Ω
Propagation Delay	V_{OUT} = ±200mV	+25°C	12	20	ns
Minimum Supply Voltage	Functional Operation Only. Other Parameters Will Vary.	+25°C	±5	±7	V

Applying the HA-2542

1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with 0.01μF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

2. STABILITY CONSIDERATIONS: HA-2542 is stable at gains ≥ 2. Gains < 2 are covered elsewhere in this data sheet. Feedback resistors should be of carbon composition located as near to the input terminals as possible.

3. WIRING CONSIDERATIONS: Video pulse circuits should be built on a ground plane. Minimum point to point connections directly to the amplifier terminals should be used. When ground planes cannot be used, good single point grounding techniques should be applied.

4. OUTPUT SHORT CIRCUIT: HA-2542 does not have output short circuit protection. Short circuits to ground can be tolerated for approximately 10 seconds. Short circuits to either supply will result in immediate destruction of the device.

5. HEAVY CAPACITIVE LOADS: When driving heavy capacitive loads (≥ 100pF) a small resistor (≈ 100Ω) should be connected in series with the output and inside the feedback loop.

6. HEAT SINKING: Although not required for /883 qualification, heat sinking is suggested in high ambient conditions. Recommended heat sinks include Thermalloy #2240A or #2268B for TO-8 Metal Can. Also review Application Note 556 for safe operating area information. Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below +175°C.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Applications

(Refer to Application Note 552 for further information)

The Harris HA-2542 is a state of the art monolithic device which also approaches the "ALL-IN-ONE" amplifier concept. This device features an outstanding set of AC parameters augmented by excellent output drive capability providing for suitable application in both high speed and high output drive circuits.

Primarily intended to be used in balanced 50Ω and 75Ω coaxial cable systems as a driver, the HA-2542 could also be used as a power booster in audio systems as well as a power amp in power supply circuits. This device would also be suitable as a small DC motor driver.

Prototyping Guidelines

For best overall performance in any application, it is recommended that high frequency layout techniques be used. This should include: 1) mounting the device through a ground plane; 2) connecting unused pins (N.C.) to the ground plane; 3) mounting feedback components on Teflon standoffs and/or locating these components as close to the device as possible; 4) placing power supply decoupling capacitors from device supply pins to ground.

As a result of speed and bandwidth optimization, the HA-2542 can's case potential, when powered-up, is equal to the V- potential. Therefore, contact with other circuitry or ground should be avoided.

Frequency Compensation

The HA-2542 may be externally compensated with a single capacitor to ground. This provides the user the additional flexibility in tailoring the frequency response of the amplifier. A guideline to the response is demonstrated on the typical performance curve showing the normalized A.C. parameters versus compensation capacitance. It is suggested that the user check and tailor the accurate compensation value for each application. As shown additional phase margin is achieved at the loss of slew rate and bandwidth.

For example, for a voltage gain of +2 (or -1) and a load of 500pF/2kΩ, 20pF is needed for compensation to give a small signal bandwidth of 30MHz with 40^{o} of phase margin. If a full power output voltage of ±10V is needed, this same configuration will provide a bandwidth of 5MHz and a slew rate of 200V/μs.

If maximum bandwidth is desired and no compensation is needed, care must be given to minimize parasitic capacitance at the compensation pin. In some cases where minimum gain applications are desired, bending up or totally removing this pin may be the solution. In this case, care, must also be given to minimize load capacitance.

For wideband positive unity gain applications, the HA-2542 can also be over-compensated with capacitance greater than 30pF to achieve bandwidths of around 25MHz. This over-compensation will also improve capacitive load handling or lower the noise bandwidth. This versatility along with the ±100mA output current makes the HA-2542 an excellent high speed driver for many power applications.

HARRIS

HA-2544/883

January 1989

Video Operational Amplifier

Features

- **This Circuit Is Processed In Accordance to Mil-Std-883 and Is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Wide Unity Gain Bandwidth .... 45MHz (Min)**
- **High Slew Rate .... 100V/µs (Min)**
- **Low Supply Current .... 12mA (Max)**
- **Differential Gain Error .... 0.04dB (Max)**
- **Differential Phase Error .... 0.11% (Max)**
- **Gain Tolerance @ 3.58MHz or 4.43MHz .... 0.15dB (Max)**
- **Fast Settling Time (10V to 0.1%) .... 120ns (Typ)**

Applications

- **Video Systems**
- **Video Test Equipment**
- **Radar Displays**
- **Imaging Systems**
- **Pulse Amplifiers**
- **Signal Conditioning Circuits**
- **Data Acquisition Systems**

Description

The HA-2544/883 is a fast, unity gain stable, monolithic op amp designed to meet the needs required for accurate reproduction of video or high speed signals. It offers high voltage gain (3.5kV/V min, 6kV/V typ), wide unity gain bandwidth of 45MHz minimum and phase margin of 65 degrees (open loop). Built from high quality Dielectric Isolation, the HA-2544/883 is another addition to the Harris series of high speed, wideband op amps, and offers true video performance combined with the versatility of an op amp.

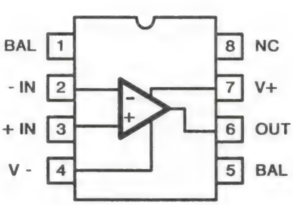
The primary features of the HA-2544/883, include wide bandwidth, 150V/µs (typ) slew rate, < 0.05dB differential gain error, < 0.11 degrees differential phase error and gain tolerance of just 0.15dB at 3.58 MHz and 4.43MHz, therefore proving to be sufficient for video amplification. High performance and low power requirements are met with a supply current of only 10mA typically and 12mA over the full temperature range.

Uses of the HA-2544/883 range from video test equipment guidance systems, radar displays and other precise imaging systems where stringent gain and phase requirements have previously been met with costly hybrids and discrete circuitry. The HA-2544/883 will also be used in non-video systems requiring high speed signal conditioning such as data acquisition systems, medical electronics, specialized instrumentation and communication systems.

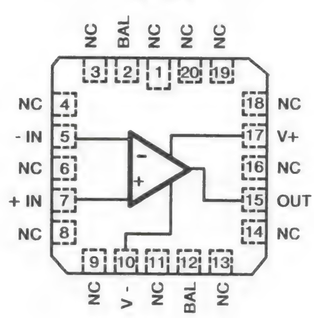
The HA-2544/883 is guaranteed over the military range of -55°C to +125°C and is offered in the 8 pin TO-99 Metal Can and Ceramic Mini-DIP or the 20 pad LCC.

Pinouts

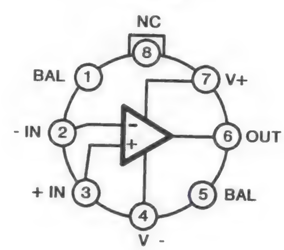
HA1-2544/883 (CERAMIC DIP)
TOP VIEW



HA4-2544/883 (CERAMIC LCC)
TOP VIEW



HA2-2544/883 (METAL CAN)
TOP VIEW



Case tied to V-

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 33V
Differential Input Voltage (Note 8) 6V
Voltage at Either Input Terminal .... V+ to V-
Peak Output Current (< 10% Duty Cycle) 40mA
Junction Temperature (T_J) .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... < 2000V
Lead Temperature (Soldering 10 sec) .... +275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	129°C/W	47°C/W
Ceramic LCC Package	92°C/W	32°C/W
Metal Can Package	116°C/W	35°C/W

Package Power Dissipation Limit at +75°C For $T_J \leq$ 175°C
- Ceramic DIP Package 780mW
- Ceramic LCC Package 1.1W
- Metal Can Package 860mW

Package Power Dissipation Derating Factor Above +75°C
- Ceramic DIP Package .... 7.8mW/°C
- Ceramic LCC Package .... 11mW/°C
- Metal Can Package .... 8.6mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±12V to ±15V
$V_{INcm} \leq 1/2$ (V+ - V-)
$R_L \geq 1k\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, $R_{SOURCE} = 10\Omega$, $R_{LOAD} = 500k\Omega$, $C_{LOAD} \leq 10pF$, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	V_{CM} = 0V	1	+25°C	-15	15	mV
			2, 3	+125°C, -55°C	-20	20	mV
Input Bias Current	$+I_B$	V_{CM} = 0V, $+R_S = 1k\Omega$, $-R_S = 10\Omega$	1	+25°C	-15	15	µA
			2, 3	+125°C, -55°C	-20	20	µA
	$-I_B$	V_{CM} = 0V, $+R_S = 10\Omega$, $-R_S = 1k\Omega$	1	+25°C	-15	15	µA
			2, 3	+125°C, -55°C	-20	20	µA
Input Offset Current	I_{IO}	V_{CM} = 0V, $+R_S = 1k\Omega$, $-R_S = 1k\Omega$	1	+25°C	-2	2	µA
			2, 3	+125°C, -55°C	-3	3	µA
Common Mode Range	+CMR	V+ = 5V, V- = -25V	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	-CMR	V+ = 25V, V- = -5V	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
Large Signal Voltage Gain	$+A_{VOL}$	V_{OUT} = 0V and +10V, $R_L = 1k\Omega$	4	+25°C	3.5	-	kV/V
			5, 6	+125°C, -55°C	2.5	-	kV/V
	$-A_{VOL}$	V_{OUT} = 0V and -10V, $R_L = 1k\Omega$	4	+25°C	3.5	-	kV/V
			5, 6	+125°C, -55°C	2.5	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔV_{CM} = +10V, +V = +5V, -V = -25V, V_{OUT} = -10V	1	+25°C	75	-	dB
			2, 3	+125°C, -55°C	75	-	dB
	-CMRR	ΔV_{CM} = -10V, +V = +25V, -V = -5V, V_{OUT} = +10V	1	+25°C	75	-	dB
			2, 3	+125°C, -55°C	75	-	dB

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 10Ω, R_{LOAD} = 500kΩ, $C_{LOAD} \leq$ 10pF, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Output Voltage Swing	$+V_{OUT}$	R_L = 1kΩ	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	$-V_{OUT}$	R_L = 1kΩ	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
Output Current	$+I_{OUT}$	V_{OUT} = -10V	1	+25°C	25	-	mA
	$-I_{OUT}$	V_{OUT} = +10V	1	+25°C	-	-25	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-	12	mA
			2, 3	+125°C, -55°C	-	12	mA
	$-I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-12	-	mA
			2, 3	+125°C, -55°C	-12	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = 10V +V = +10V, -V = -15V +V = +20V, -V = -15V	1	+25°C	70	-	dB
			2, 3	+125°C, -55°C	70	-	dB
	-PSRR	ΔV_{SUP} = 10V +V = +15V, -V = -10V +V = +15V, -V = -20V	1	+25°C	70	-	dB
			2, 3	+125°C, -55°C	70	-	dB
Offset Voltage Adjustment	$+V_{IO}Adj$	Note 6	1	+25°C	V_{IO}-1	-	mV
	$-V_{IO}Adj$	Note 6	1	+25°C	V_{IO}+1	-	mV

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 1kΩ, $C_{LOAD} \leq$ 10pF, V_{OUT} = 1V/V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Slew Rate	+SR	V_{OUT} = -3V to +3V	7	+25°C	100	-	V/µs
	-SR	V_{OUT} = +3V to -3V	7	+25°C	100	-	V/µs

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_{LOAD} = 1kΩ, $C_{LOAD} \leq$ 10pF, A_V = 1V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Differential Gain	dA_V	R_S = 50Ω, R_L = 1kΩ f_O = 3.58MHz and 4.43MHz	1, 5, 7, 9, 11	+25°C	-	0.04	dB
Differential Phase	dθ	R_S = 50Ω, R_L = 1kΩ f_O = 3.58MHz and 4.43MHz	1, 5, 7, 9	+25°C	-	0.11	Degrees
Unity Gain Bandwidth	UGBW	V_O = 200mV_{RMS}, f @ -3dB	1, 5	+25°C	45	-	MHz
Gain Tolerance	ΔA_V	V_O = 200mV_{RMS}, f_O = 5MHz	1, 5, 7	+25°C	-0.15	0.15	dB
		V_O = 200mV_{RMS}, f_O = 10MHz	1, 5, 7	+25°C	-0.35	0.35	dB
Full Power Bandwidth	FPBW	V_{PEAK} = 1V	1, 2	+25°C	15.9	-	MHz
		V_{PEAK} = 5V	1, 2	+25°C	3.2	-	MHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 1kΩ, $C_L \leq$ 1pF	1, 5	-55°C to +125°C	1	-	V/V
Rise & Fall Time	T_R	V_{OUT} = 0V to +200mV	1, 4	+25°C	-	15	ns
	T_F	V_{OUT} = 0V to -200mV	1, 4	+25°C	-	15	ns
Overshoot	+OS	V_{OUT} = 0V to +200mV	1	+25°C	-	20	%
	-OS	V_{OUT} = 0V to -200mV	1	+25°C	-	20	%
Settling Time	T_S	To 0.1% for a 10V Step	1	+25°C	-	150	ns
Output Resistance	R_{OUT}	Open Loop	1	+25°C	-	40	Ω
Quiescent Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	360	mW

NOTES:
1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).
3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)
4. Measured between 10% and 90% points.
5. Sample tested on every lot.
6. Offset adjustment range is [V_{IO} (Measured) ± 1mV] minimum referred to output. This test is for functionality only to assure adjustment through 0V.
7. The video parameter specifications will degrade as the output load resistance decreases.
8. To achieve optimum AC performance, the input stage was designed without protective diode clamps. Exceeding the maximum differential input voltage results in reverse breakdown to the base-emitter junction of the input transistors and probable degradation of the input parameters especially V_{OS}, I_{OS} and Noise.
9. Test signal used is 200mV_{RMS} at each frequency on a 0 and 1 volt offset. For adaquate test repeatability, a minimum warm-up of 2 minutes is suggested.
10. C-L Gain and C-L Delay was less than the resolution to the test equipment used which is 0.1dB and 7ns, respectively.
11. $A_D(\%) = \left[10^{\frac{A_D\,(dB)}{20}} - 1\right] \times 100$

TABLE 4. ELECTRICAL TEST REQUIREMENTS

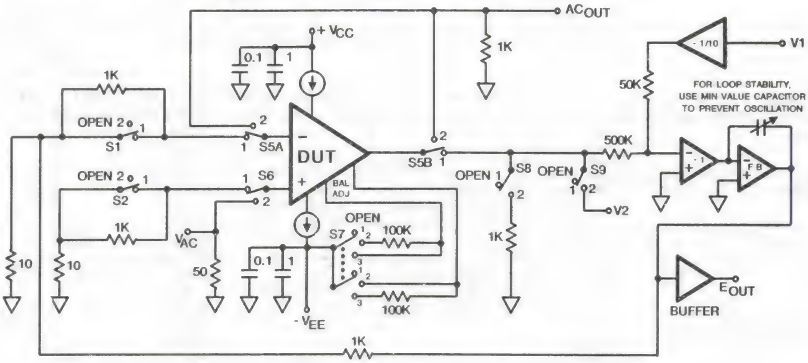
MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6, 7
Group A Test Requirements	1, 2, 3, 4, 5, 6, 7
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

3

OP AMPs & COMPARATORS

Test Circuit (Applies to Table 1)

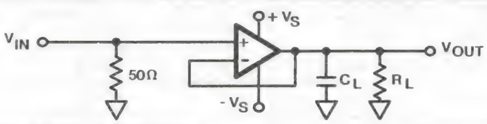


ALL RESISTORS = ± 1% (Ω)
ALL CAPACITORS = ± 10% (μF)

For Detailed Information, Refer to HA-2544/883 Test Tech Brief

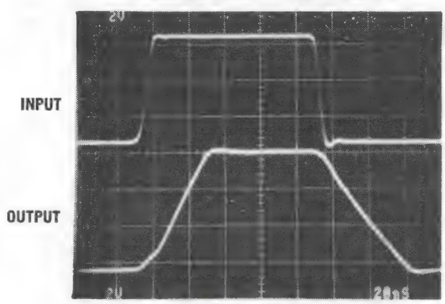
Test Waveforms

SIMPLIFIED TEST CIRCUIT FOR LARGE AND SMALL SIGNAL RESPONSE (Applies to Tables 2 and 3)



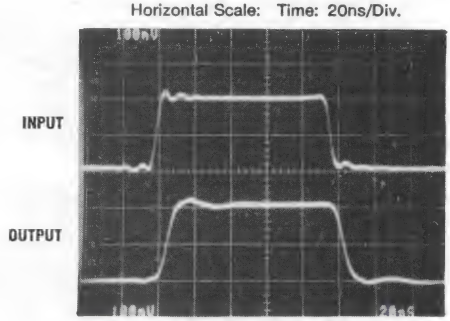
$V_S = \pm15V$, $A_V = +1$
$R_L = 1k\Omega$, $C_L \leq 10pF$
V_{IN} for Large Signal = ±3V,
V_{IN} for Small Signal = 0 to +200mV and 0 to -200mV

MEASURED LARGE SIGNAL RESPONSE
Vertical Scale: (2V/Div.)
Horizontal Scale: Time: 20ns/Div.



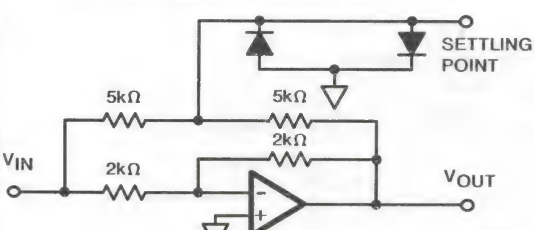
$A_V = +1V/V$, $R_L = 1k\Omega$

MEASURED SMALL SIGNAL RESPONSE
Vertical Scale: (100mV/Div.)
Horizontal Scale: Time: 20ns/Div.



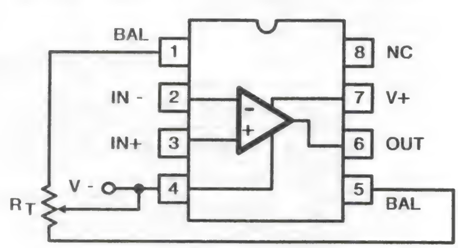
$A_V = +1V/V$, $R_L = 1k\Omega$
Note: Tested on both positive and negative edges.

SETTLING TIME TEST CIRCUIT FOR TABLE 3



- $A_V = -1$
- Feedback and Summing Resistors Must Be Matched (0.1%).
- HP5082-2810 Clipping Diodes Recommended.
- Tektronix P6201 FET Probe Used At Settling Point.

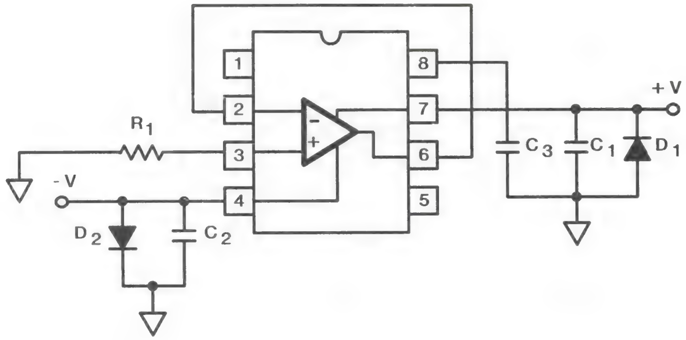
OFFSET VOLTAGE ADJUSTMENT CONNECTIONS



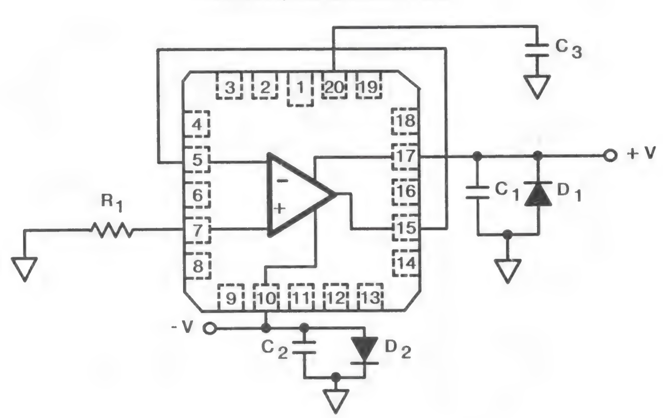
Tested Offset Adjustment Range is $|V_{OS} + 1mV|$ Minimum Referred To Output. Typical Range For $R_T = 20k\Omega$ is Approximately ±30mV.

Burn-In Circuits

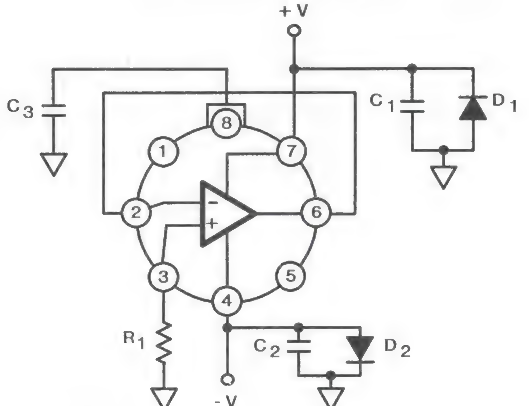
HA7-2544/883 CERAMIC DIP



HA4-2544/883 CERAMIC LCC



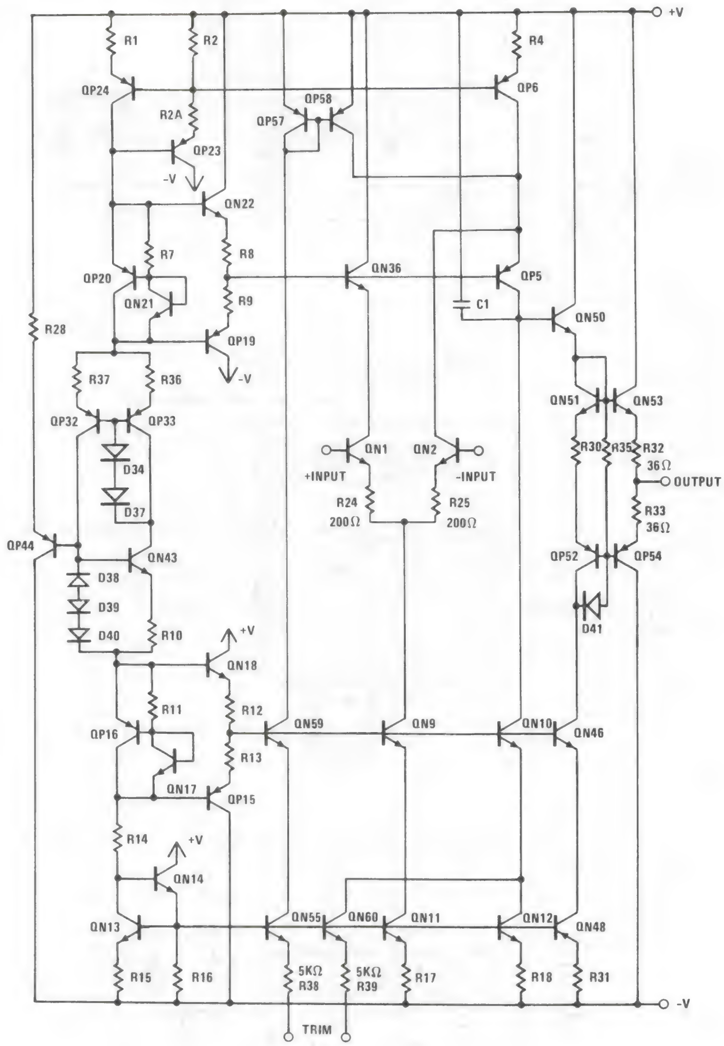
HA2-2544/883 TO-99 METAL CAN



NOTES:

R_1 = 1MΩ, ±5%, 1/4W (Min)
$C_1 = C_2$ = 0.01μF/Socket (Min) or 0.1μF/Row, (Min)
C_3 = 0.01μF/Socket, 10%
$D_1 = D_2$ = IN4002 or Equivalent/Board
$|(V+) - (V-)|$ = 30V
(C_3 is not required for HA-2544/883 compensation. It is shown here as standard pinout fixturing from B.I. boards used.)

Schematic Diagram



Die Characteristics

DIE DIMENSIONS:
79.9 x 64.2 x 19 mils
(2030 x 1630 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$0.3 \times 10^5 A/cm^2$

SUBSTRATE POTENTIAL (POWERED UP): V-

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

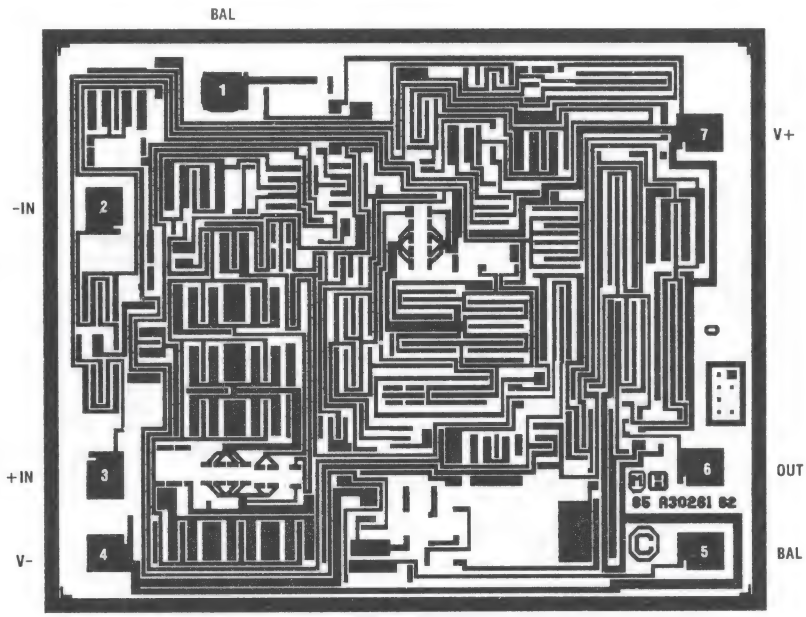
TRANSISTOR COUNT: 44

PROCESS: High Frequency Bipolar Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)
Metal Can — 420°C (Max)

Metallization Mask Layout

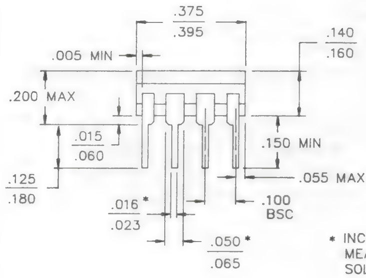
HA-2544/883

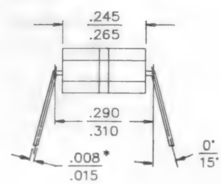


NOTE: Pin Numbers Correspond to Ceramic Mini-DIP and 8 Pin (TO-99) Metal Can Packages Only.

Packaging †

8 PIN CERAMIC DIP

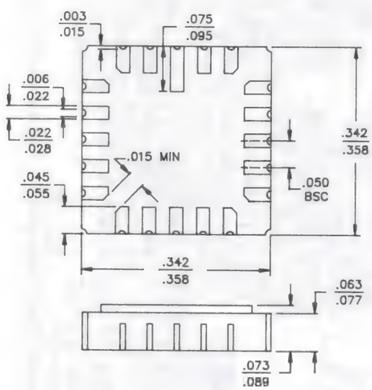




* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

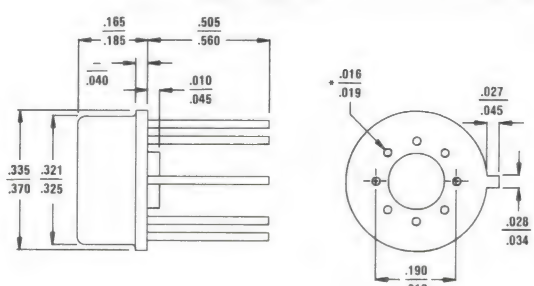
LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-4

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Ceramic, 90% Al_2O_3
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

8 PIN TO-99 METAL CAN



LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
Material: No Seal Material
Temperature: Room Temperature
Method: Resistance Weld
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic Bonded
COMPLIANT OUTLINE: 38510 A-1

*Dimension Maximum Limits Are Increased by 0.003 inches for Solder Dip Finish

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

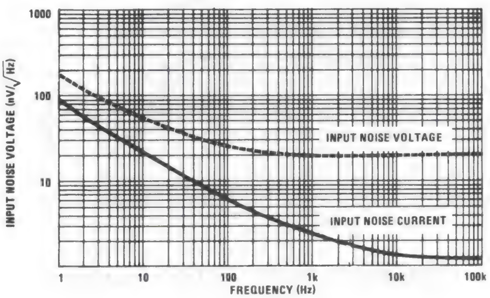
DESIGN INFORMATION

Video Operational Amplifier

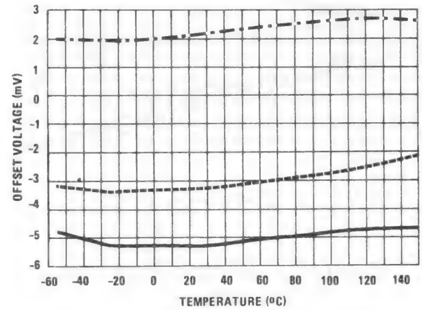
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves
Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

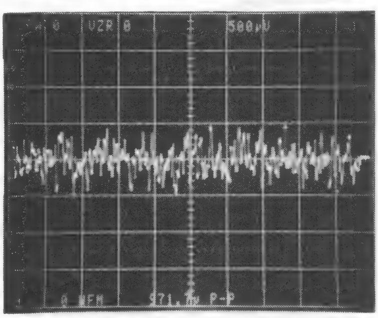
INPUT NOISE VOLTAGE AND NOISE CURRENT vs. FREQUENCY



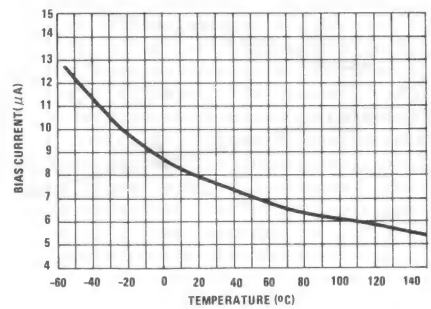
INPUT OFFSET VOLTAGE vs. TEMPERATURE
3 Typical Units



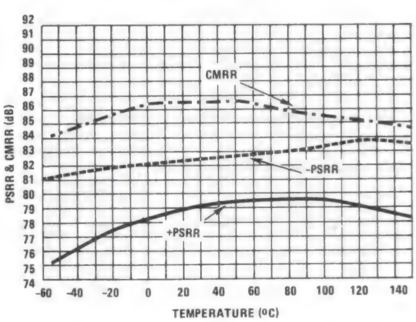
BROADBAND NOISE
$A_V = 1000$, 0.1Hz to 10Hz, Noise Voltage = $0.97\mu V_{p-p}$



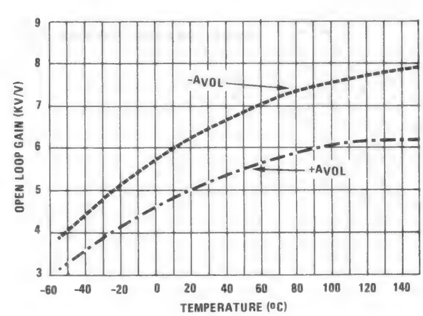
INPUT BIAS CURRENT vs. TEMPERATURE
$V_S = \pm15V$, $R_L = 1k\Omega$



PSRR AND CMRR vs. TEMPERATURE
$V_S = \pm15V$, $R_L = 1k\Omega$



OPEN LOOP GAIN vs. TEMPERATURE
$V_S = \pm15V$, $R_L = 1k\Omega$



DESIGN INFORMATION (Continued)

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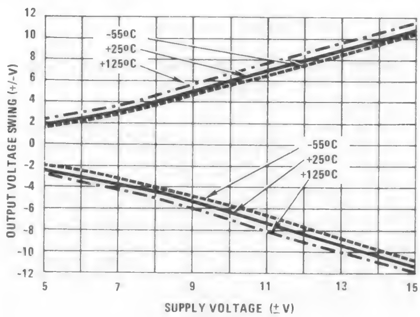
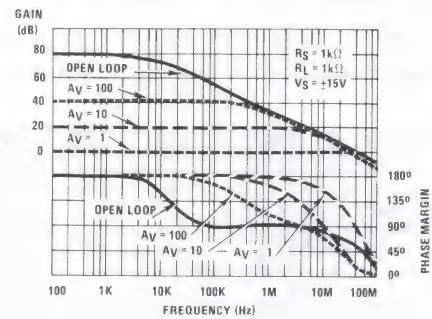
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

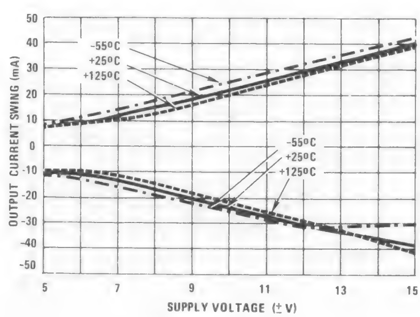
OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE
(Over Full Temperature)



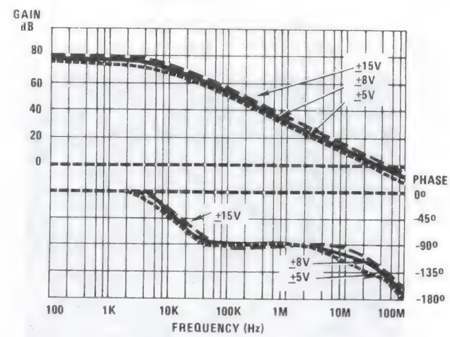
FREQUENCY RESPONSE AT VARIOUS GAINS
$R_S = 1k\Omega$, $R_L = 1k\Omega$, $V_S = \pm15V$



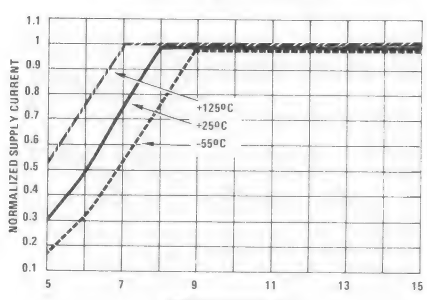
OUTPUT CURRENT vs. SUPPLY VOLTAGE
(Over Full Temperature)



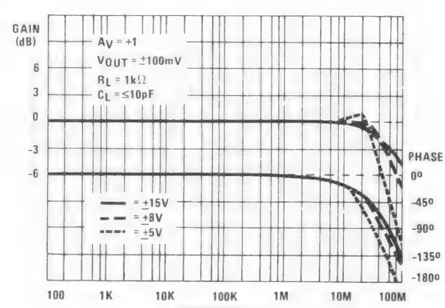
OPEN LOOP RESPONSE vs. SUPPLY VOLTAGE
$V_{OUT} = \pm100mV$



SUPPLY CURRENT vs. SUPPLY VOLTAGE
Normalized at $V_S = \pm15V$ at $+25^oC$



VOLTAGE FOLLOWER RESPONSE vs. SUPPLY VOLTAGE
$A_V = +1$, $R_L = 1K$, $C_L \leq 10pF$

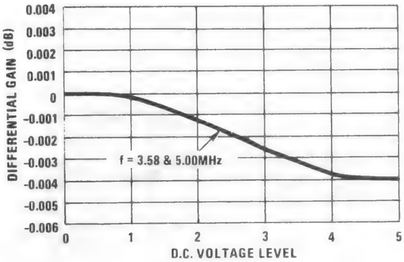


DESIGN INFORMATION (Continued)

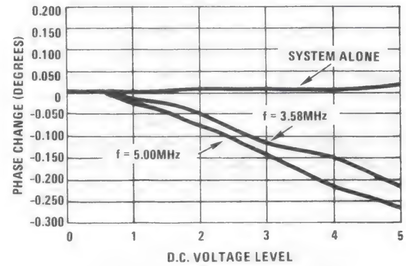
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Video Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

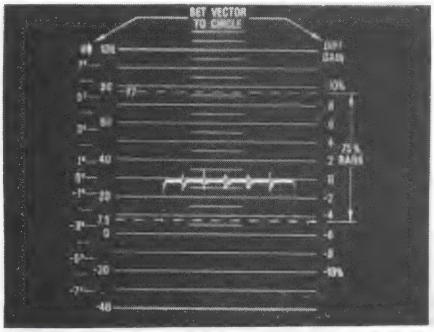
A.C. GAIN VARIATION vs. D.C. OFFSET LEVELS
(Differential Gain)



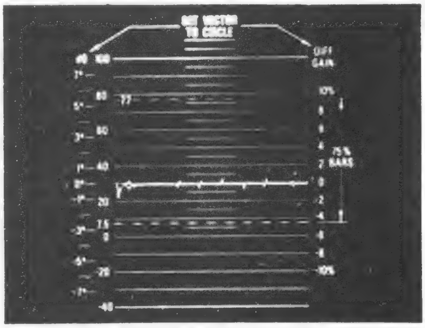
A.C. PHASE VARIATION vs. D.C. OFFSET LEVELS
(Differential Phase)



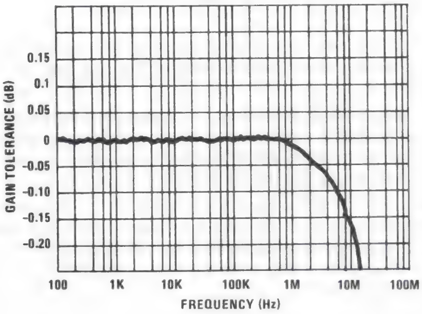
DIFFERENTIAL GAIN
NTSC Method, $R_L = 1k\Omega$
Differential Gain < 0.05% at $T_A = +75^oC$
No Visual Difference at $T_A = -55^oC$ of $+125^oC$



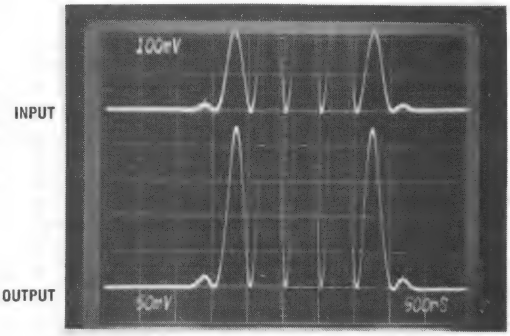
DIFFERENTIAL PHASE
NTSC Method, $R_L = 1k\Omega$
Differential Phase < 0.05 Degree at $T_A = +75^oC$
No Visual Difference at $T_A = -55^oC$ or $+125^oC$



GAIN TOLERANCE
$A_V = +1$, $V_{IN} = \pm100mV$
$R_L = 1K$, $C_L \leq 10pF$



CHROMINANCE TO LUMINANCE DELAY
NTSC Method, $R_L = 1k\Omega$
C-L Delay < 7ns at $T_A = +75^oC$
No Visual Difference at $T_A = -55^oC$ or $+125^oC$



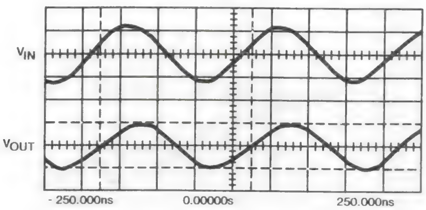
Vertical Scale: Input = 100mV/Div.
Output = 50mV/Div.
Horizontal Scale: 500ns/Div.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

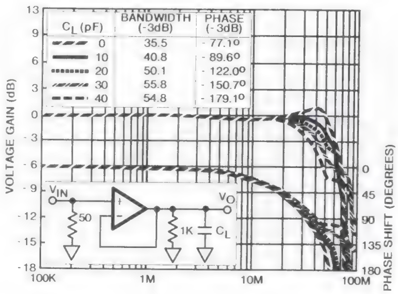
Typical Video Performance Curves (Continued) Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

±2 VOLT OUTPUT SWING
With $R_{LOAD} = 75\Omega$ (frequency = 5.00MHz)



V_{IN} = 2.0V/Div., V_{OUT} = 2.0V/Div.
Timebase = 50ns/Div.

BANDWIDTH vs. LOAD CAPACITANCE
$A_V = +1$, $V_S = \pm 15V$, $R_L = 1k\Omega$



Applications And Product Guidelines

The HA-2544 is a true differential op amp that is as versatile as any op amp but offers the advantages of high unity gain bandwidth, high speed and low supply current. More important than its' general purpose applications is that the HA-2544 was especially designed to meet the requirements found in a video amplifier system. These requirements include fine picture resolution and accurate color rendition, and must meet broadcast quality standards.

In a video signal, the video information is carried in the amplitude and phase as well as in the D.C. level. The amplifier must pass the 30Hz line rate luminance level and the 3.58MHz (NTSC) or 4.43MHz (PAL) color band without altering phase or gain. The HA-2544's key specifications aimed at meeting this include high bandwidth (50MHz), very low gain tolerance (< ±0.15dB at 5MHz), near unmeasurable differential gain and differential phase (< 0.04dB and 0.11 degrees), and low noise ($20nV/\sqrt{Hz}$). The HA-2544 meets these quidelines and are sample tested for standard grade product (/883, -2, -7, -5) at 5 and/or 10MHz. If a customer wishes to 100% test these specifications, arrangement can be made.

The HA-2544 also offers the advantage of a full output voltage swing of ±10V into a 1K ohm load. This equates to a full power bandwidth of 2.4MHz for this ±10V signal. If video signal levels of ±2V maximum is used (with R_L = 1K ohm), the full power bandwidth would be 11.9MHz without clipping distortion. Another usage might be required for a direct 50 ohm or 75 ohm load where the HA-2544 will still swing this ±2V signal as shown in the above display. One important note that must be realized is that as load resistance decreases the video parameters are also degraded. For optimal video performance a 1kΩ load is recommended.

If lower supply voltage are required, such as ±5V, many of the characterization curves indicate where the parameters vary. As shown the bandwidth, slew rate and supply current are still very well maintained.

Prototyping and PC Board Layout

When designing with the HA-2544 video op amp as with any high performance device, care should be taken to use high frequency layout techniques to avoid unwanted parasitic effects. Short lead lengths, low source impedance and lower value feedback resistors help reduce unwanted poles or zeros. This layout would also include ground plane construction and power supply decoupling as close to the supply pins with suggested parallel capacitors of 0.1μF and 0.001μF ceramic to ground.

In the noninverting configuration, the amplifier is sensitive to stray capacitance (< 40pF) to ground at the inverting input. Therefore, the inverting node connections should be kept to a minimum. Phase shift will also be introduced as load parasitic capacitance is increased. A small series resistor (20 ohm to 100 ohm) before the capacitance effectively decouples this effect.

Stability/Phase Margin/Compensation

The HA-2544 has not sacrificed unity gain stability in achieving its superb AC performance. For this device, the phase margin exceeds 60 degrees at the unity crossing point of the open loop frequency response. Large phase margin is critical in order to reduce the differential phase and differential gain errors caused by most other op amps. Because this part is unity gain stable, no compensation pin is brought out. If compensation is desired to reduce the noise bandwidth, most standard methods may be used. One method suggested for an inverting scheme would be a series R-C from the inverting node to ground which will reduce bandwidth, but not effect slew rate. If the user wishes to achieve even higher bandwidth (> 50MHz), and can tolerate some slight gain peaking and lower phase margin, experimenting with various load capacitance can be done.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_L = 1kΩ, $C_L \leq$ 10pF, A_V = 1V/V, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage	V_{CM} = 0V	+25°C	6	Table 1	mV
Average Offset Voltage Drift	Versus Temperature	Full	10	15	μV/°C
Bias Current	V_{CM} = 0V	+25°C	7	Table 1	μA
Average Bias Current Drift	Versus Temperature	Full	0.04	0.1	μA/°C
Offset Current	V_{CM} = 0V	+25°C	0.2	Table 1	μA
		Full	0.8	Table 1	μA
Common Mode Range		Full	±11.5	Table 1	V
Differential Input Resistance		+25°C	90	50	kΩ
Differential Input Capacitance		+25°C	3	4	pF
Input Noise Voltage Density	$f_O \geq$ 1kHz	+25°C	20	24	nV/$\sqrt{Hz}$
Input Noise Current Density	$f_O \geq$ 1kHz	+25°C	2.4	4	pA/$\sqrt{Hz}$
Large Signal Voltage Gain	V_{OUT} = ±5V	+25°C	6	Table 1	kV/V
		Full	3.5	Table 1	kV/V
CMRR	ΔV_{CM} = ±10V	Full	89	Table 1	dB
Gain Bandwidth Product		+25°C	50	45	MHz
Phase Margin	0dB GBWP Crossing	+25°C	65	55	Degrees
Output Voltage Swing		Full	±11	Table 1	V
Full Power Bandwidth	V_{PEAK} = 5V	+25°C	4.2	3.5	MHz
Peak Output Current	Note A	+25°C	±35	Table 1	mA
Output Resistance	Open Loop	+25°C	20	40	Ω
Rise/Fall Time	V_{OUT} = +200mV, -200mV	+25°C	7	Table 3	ns
± Overshoot	V_{OUT} = +200mV, -200mV	+25°C	10	Table 3	%
+ Slew Rate	V_{OUT} = -5V to +5V	+25°C	+165	Table 2	V/μs
- Slew Rate	V_{OUT} = +5V to -5V	+25°C	-125	Table 2	V/μs
Settling Time	A_V = -1V/V, 10V to 0.1%	+25°C	110	140	ns
	A_V = -1V/V, 10V to 0.01%	+25°C	120	150	ns
Differential Phase	R_S = 50Ω to 75Ω, Notes 7 and 9	+25°C	0.05	Table 3	Degrees
	R_S = 1kΩ, Notes 7 and 9	+25°C	0.4	0.6	Degrees
Differential Gain	R_S = 50Ω to 75Ω, Notes 7, 9, 11	+25°C	0.02	Table 3	dB
	R_S = 1kΩ, Notes 7, 9, 11	+25°C	0.15	0.3	dB
Chrominance to Luminance Gain	Note 10	+25°C	0.1	N/A	dB
Chrominance to Luminance Delay	Note 10	+25°C	7	N/A	ns
Gain Tolerance	5MHz	+25°C	-0.10	Table 3	dB
	10MHz	+25°C	-0.12	Table 3	dB
Supply Current	I_{OUT} = 0mA	Full	10	Table 1	mA
PSRR	ΔV_S = ±10V to ±20V	Full	80	Table 1	dB
Minimum Supply Voltage	Functional Operation Only. Other Parameters Will Vary.	+25°C	±5	±6	V
Saturation Recovery Time	Full Saturation	+25°C	0.6	1.1	μs

HARRIS

HA-2600/883
HA-2602/883

Wideband, High Impedance Operational Amplifiers

January 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- High Input Impedance (HA-2600/883) .... 100MΩ Min, 500MΩ Typ
- High Slew Rate .... 4V/μs Min, 7V/μs Typ
- Low Input Bias Current (HA-2600/883) .... 10nA Max, 1nA Typ
- Low Input Offset Voltage (HA-2600/883) .. 4mV Max
- Wide Unity Gain Bandwidth .... 12MHz Typ
- Output Short Circuit Protection

Applications

- Video Amplifer
- Pulse Amplifier
- High-Q Active Filters
- High Speed Compartators
- Low Distortion Oscillators

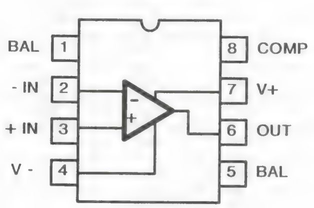
Description

HA-2600/883 and HA-2602/883 are internally compensated bipolar operational amplifiers that feature very high input impedance coupled with wideband AC performance. The high resistance of the input stage is complemented by low offset voltage ($4mV_{max}$ @ +25°C for HA-2600/883) and low bias and offset current (10nA max @+25°C for HA-2600/883) to facilitate accurate signal processing. Offset voltage can be reduced further by means of an external nulling potentiometer. The 4V/μs minimum slew rate @ +25°C and the minimum open loop gain of 100kV/V @ +25°C enables the HA-2600/883 to perform high gain amplification of fast, wideband signals. These dynamic characteristics, coupled with fast settling times, make these amplifiers ideally suited to pulse amplification designs as well as high frequency or video applications. The frequency response of the amplifier can be tailored to exact design requirements by means of an external bandwidth control capacitor. Other high performance designs such as high gain, low distortion audio amplifiers, high-Q and wideband active filters and high speed comparators, are excellent uses of this part.

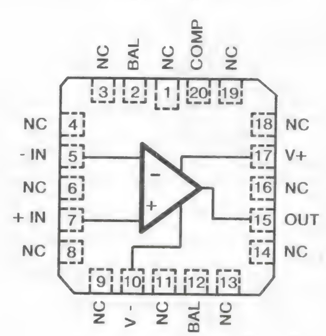
The HA-2600/883 and the HA-2602/883 are available as MIL-STD-883 compliant devices screened to class B level. These devices are sensitive to electrostatic discharge and are in microcircuit group number 49 (see MIL-M-38510, Appendix E). The HA-2600/883 and the HA-2602/883 have guaranteed operation over the military temperature range from -55°C to +125°C and are available in 8 pin Metal Can and Ceramic Mini-DIP packages. The HA-2602/883 is also available in a 20 pin Ceramic LCC package.

Pinouts

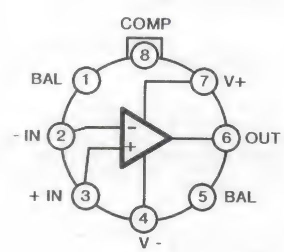
HA7-2600/883 (CERAMIC MINI-DIP)
HA7-2602/883 (CERAMIC MINI-DIP)
TOP VIEW



HA4-2602/883 (CERAMIC LCC)
TOP VIEW



HA2-2600/883 (METAL CAN)
HA2-2602/883 (METAL CAN)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage 12V
Voltage at Either Input Terminal .... V+ to V-
Peak Output Current .... Full Short Circuit Protection
Junction Temperature (T_J) .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... < 2000V
Lead Temperature (Soldering 10 sec) .... 275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	136°C/W	58°C/W
Ceramic LCC Package	98°C/W	41°C/W
Metal Can Package	136°C/W	41°C/W

Package Power Dissipation Limit at +75°C for $T_J \leq +175°C$
Ceramic DIP Package 740mW
Ceramic LCC Package 1.02W
Metal Can Package 740mW

Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 7.4mW/°C
Ceramic LCC Package .... 10.2mW/°C
Metal Can Package .... 7.4mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±15V
$V_{INcm} \leq 1/2\ (V+ - V-)$
$R_L \geq 2k\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, $R_{SOURCE} = 100\Omega$, $R_{LOAD} = 500k\Omega$, $V_{OUT} = 0V$, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	HA-2600/883		HA-2602/883		UNITS
					MIN	MAX	MIN	MAX	
Input Offset Voltage	V_{IO}	$V_{CM} = 0V$	1	+25°C	-4	4	-5	5	mV
			2, 3	+125°C, -55°C	-6	6	-7	7	mV
Input Bias Current	$+I_B$	$V_{CM} = 0V$ $+R_S = 100k\Omega$ $-R_S = 100\Omega$	1	+25°C	-10	10	-25	25	nA
			2, 3	+125°C, -55°C	-30	30	-60	60	nA
	$-I_B$	$V_{CM} = 0V$ $+R_S = 100\Omega$ $-R_S = 100k\Omega$	1	+25°C	-30	10	-25	25	nA
			2, 3	+125°C, -55°C	-30	30	-60	60	nA
Input Offset Current	I_{IO}	$V_{CM} = 0V$ $+R_S = 100k\Omega$ $-R_S = 100k\Omega$	1	+25°C	-10	10	-25	25	nA
			2, 3	+125°C, -55°C	-30	30	-60	60	nA
Common Mode Range	+CMR	V+ = 4V V- = -26V	1	+25°C	11	-	11	-	V
			2, 3	+125°C, -55°C	11	-	11	-	V
	-CMR	V+ = 26V V- = -4V	1	+25°C	-	-11	-	-11	V
			2, 3	+125°C, -55°C	-	-11	-	-11	V
Large Signal Voltage Gain	$+A_{VOL}$	V_{OUT} = 0V and +10V $R_L = 2k\Omega$	4	+25°C	100	-	80	-	kV/V
			5, 6	+125°C, -55°C	70	-	60	-	kV/V
	$-A_{VOL}$	V_{OUT} = 0V and -10V $R_L = 2k\Omega$	4	+25°C	100	-	80	-	kV/V
			5, 6	+125°C, -55°C	70	-	60	-	kV/V
Common Mode Rejection Ratio	+CMRR	$\Delta V_{CM} = +10V$ +V = +5V -V = -25V $V_{OUT} = -10V$	1	+25°C	80	-	74	-	dB
			2, 3	+125°C, -55°C	80	-	74	-	dB
	-CMRR	$\Delta V_{CM} = -10V$ +V = +25V -V = -5V $V_{OUT} = +10V$	1	+25°C	80	-	74	-	dB
			2, 3	+125°C, -55°C	80	-	74	-	dB

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	HA-2600/883		HA-2602/883		UNITS
					MIN	MAX	MIN	MAX	
Output Voltage Swing	$+V_{OUT}$	R_L = 2kΩ	4	+25°C	10	-	10	-	V
			5, 6	+125°C, -55°C	10	-	10	-	V
	$-V_{OUT}$	R_L = 2kΩ	4	+25°C	-	-10	-	-10	V
			5, 6	+125°C, -55°C	-	-10	-	-10	V
Output Current	$+I_{OUT}$	V_{OUT} = -10V	4	+25°C	15	-	10	-	mA
			5, 6	+125°C, -55°C	10	-	7.5	-	mA
	$-I_{OUT}$	V_{OUT} = +10V	4	+25°C	-	-15	-	-10	mA
			5, 6	+125°C, -55°C	-	-10	-	-7.5	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V, I_{OUT} = 0mA	1	+25°C	-	3.7	-	3.7	mA
			2, 3	+125°C, -55°C	-	4.0	-	4.0	mA
	$-I_{CC}$	V_{OUT} = 0V, I_{OUT} = 0mA	1	+25°C	-3.7	-	-3.7	-	mA
			2, 3	+125°C, -55°C	-4.0	-	-4.0	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = ± 5 +V = +10V, -V = -15V +V = +20V, -V = -15V	1	+25°C	80	-	74	-	dB
			2, 3	+125°C, -55°C	80	-	74	-	dB
	-PSRR	ΔV_{SUP} = ± 5V +V = +15V, -V = -10V +V = +15V, -V = -20V	1	+25°C	80	-	74	-	dB
			2, 3	+125°C, -55°C	80	-	74	-	dB
Offset Voltage Adjustment	$+V_{IO}Adj$	Note 4	1	+25°C	$V_{IO}-1$	-	$V_{IO}-1$	-	mV
			2, 3	+125°C, -55°C	$V_{IO}-1$	-	$V_{IO}-1$	-	mV
	$-V_{IO}Adj$	Note 4	1	+25°C	$V_{IO}+1$	-	$V_{IO}+1$	-	mV
			2, 3	+125°C, -55°C	$V_{IO}+1$	-	$V_{IO}+1$	-	mV

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_{VCL} = +1V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	HA-2600/883		HA-2602/883		UNITS
					MIN	MAX	MIN	MAX	
Slew Rate	+SR	V_{OUT} = -5V to +5V	7	+25°C	4	-	4	-	V/µs
			8A, 8B	+125°C, -55°C	3	-	3	-	V/µs
	-SR	V_{OUT} = +5V to -5V	7	+25°C	4	-	4	-	V/µs
			8A, 8B	+125°C, -55°C	3	-	3	-	V/µs
Rise & Fall Time	T_R	V_{OUT} = 0 to +200mV $10\% \le T_R \le 90\%$	7	+25°C	-	60	-	60	ns
			8A, 8B	+125°C, -55°C	-	70	-	70	ns
	T_F	V_{OUT} = 0 to -200mV $10\% \le T_F \le 90\%$	7	+25°C	-	60	-	60	ns
			8A, 8B	+125°C, -55°C	-	70	-	70	ns
Overshoot	+OS	V_{OUT} = 0 to +200mV	7	+25°C	-	40	-	40	%
			8A, 8B	+125°C, -55°C	-	50	-	50	%
	-OS	V_{OUT} = 0 to -200mV	7	+25°C	-	40	-	40	%
			8A, 8B	+125°C, -55°C	-	50	-	50	%

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_V = +1, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	HA-2600/883		HA-2602/883		UNITS
					MIN	MAX	MIN	MAX	
Differential Input Resistance	R_{IN}	V_{CM} = 0V	1	+25°C	100	-	40	-	MΩ
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	+25°C	50	-	50	-	kHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 2kΩ, C_L = 50pF	1	-55°C to +125°C	1	-	1	-	V/V
Output Short Circuit Current	$+I_{SC}$	V_{OUT} = 1V, R_L = 10Ω	1	+25°C	-	50	-	50	mA
			1	+125°C	-	45	-	45	mA
			1	-55°C	-	60	-	60	mA
	$-I_{SC}$	V_{OUT} = -1V, R_L = 10Ω	1	+25°C	-50	-	-50	-	mA
			1	+125°C	-45	-	-45	-	mA
			1	-55°C	-60	-	-60	-	mA
Quiescent Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	120	-	120	mW

NOTES: 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).

3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)

4. Offset adjustment range is [$V_{IO(Measured)}$ ± 1mV] minimum referred to output. This test is for functionality only to assure adjustment through 0V.

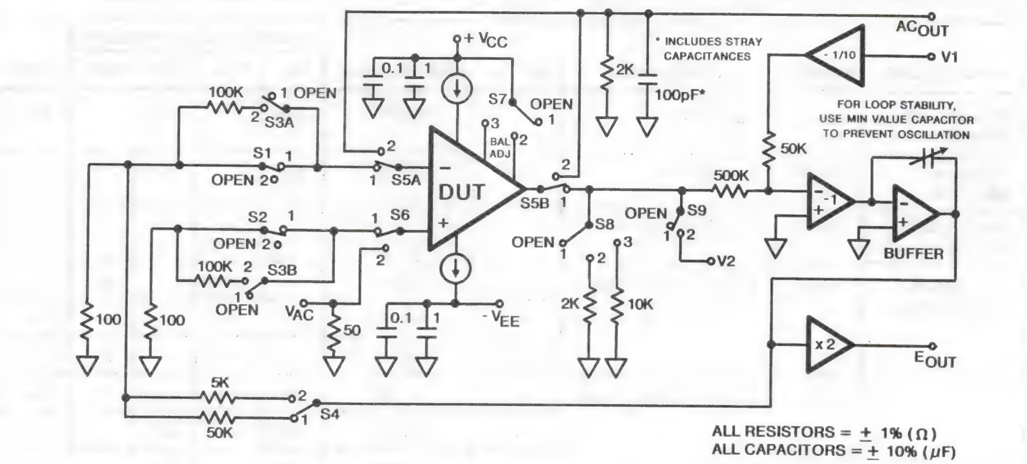
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6, 7, 8A, 8B
Group A Test Requirements	1, 2, 3, 4, 5, 6, 7, 8A, 8B
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

The Subgroup assignments of the parameters in these tables were patterned after Mil-M-38510/122, device type 02.

Test Circuit (Applies to Tables 1 and 2)

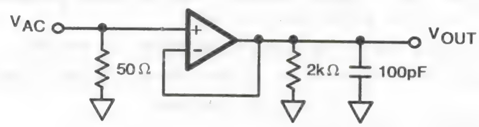


ALL RESISTORS = ± 1% (Ω)
ALL CAPACITORS = ± 10% (μF)

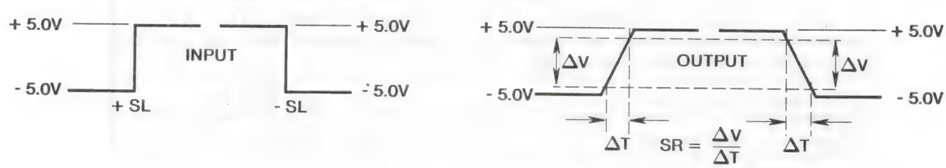
For Detailed Information, Refer to HA-2600/883; HA-2602/883 Test Tech Brief

Test Waveforms

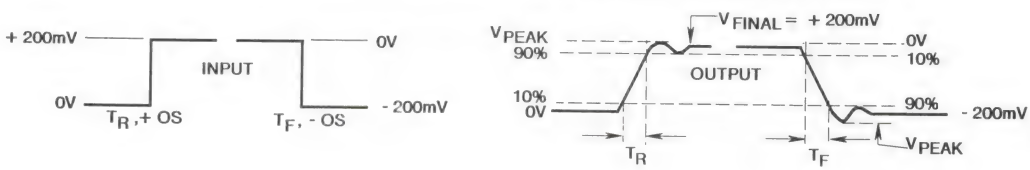
SIMPLIFIED TEST CIRCUIT (Applies to Table 2)



SLEW RATE WAVEFORMS



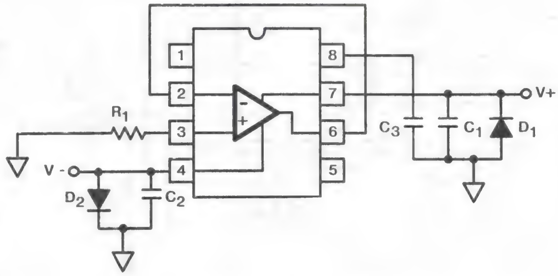
OVERSHOOT, RISE & FALL TIME WAVEFORMS



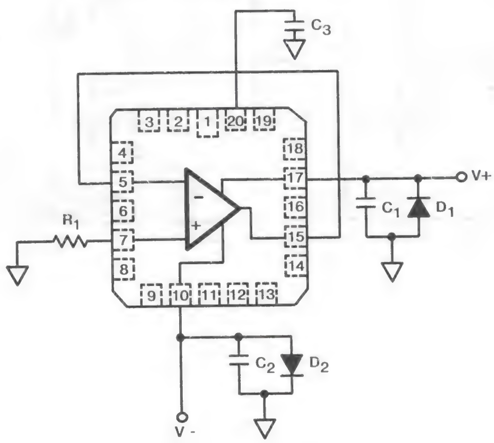
NOTE: Measured on both positive and negative transitions.
Capacitance at Compensation pin should be minimized.

Burn-In Circuits

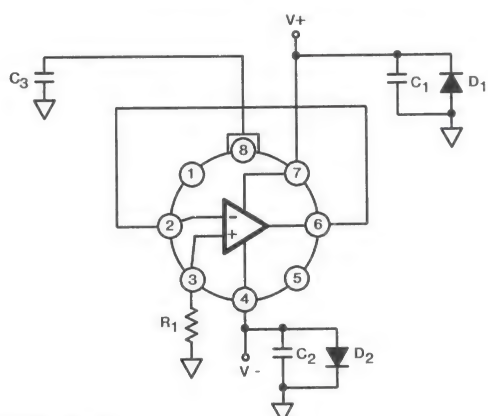
HA7-2600/883 CERAMIC MINI-DIP
HA7-2602/883 CERAMIC MINI-DIP



HA4-2602/883 CERAMIC LCC

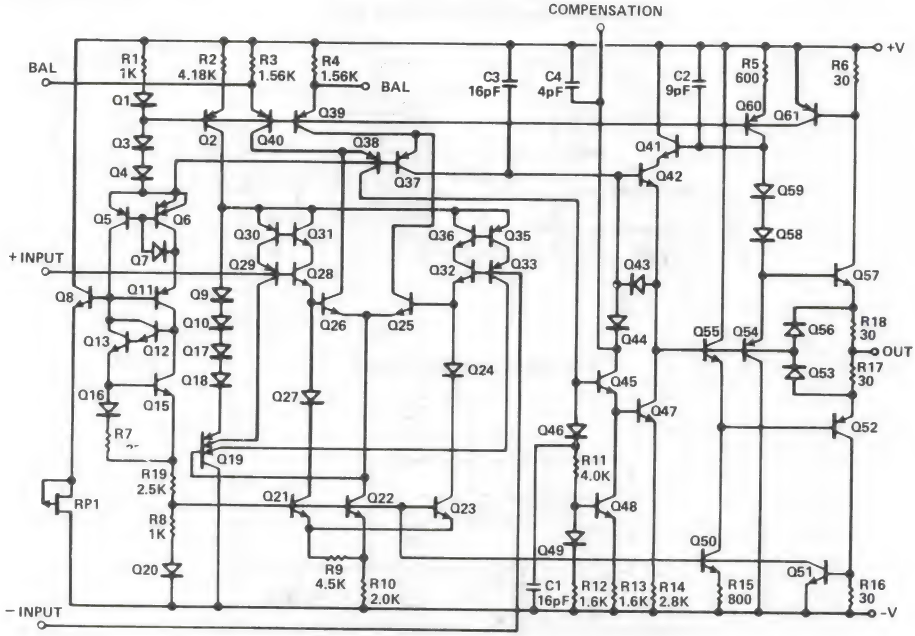


HA2-2600/883 (TO-99) METAL CAN
HA2-2602/883 (TO-99) METAL CAN



NOTES:
R_1 = 1MΩ, ±5%, 1/4W (Min)
$C_1 = C_2$ = 0.01μF/Socket (Min) or 0.1μF/Row (Min)
C_3 = 0.01μF/Socket (10%)
$D_1 = D_2$ = IN4002 or Equivalent/Board
$|(V+) - (V-)|$ = 30V

Schematic Diagram



Die Characteristics

DIE DIMENSIONS:
73 x 52 x 19 mils
(1860 x 1320 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
1.5×10^5 A/cm^2 @ 19mA

SUBSTRATE POTENTIAL (Powered Up):
Unbiased

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

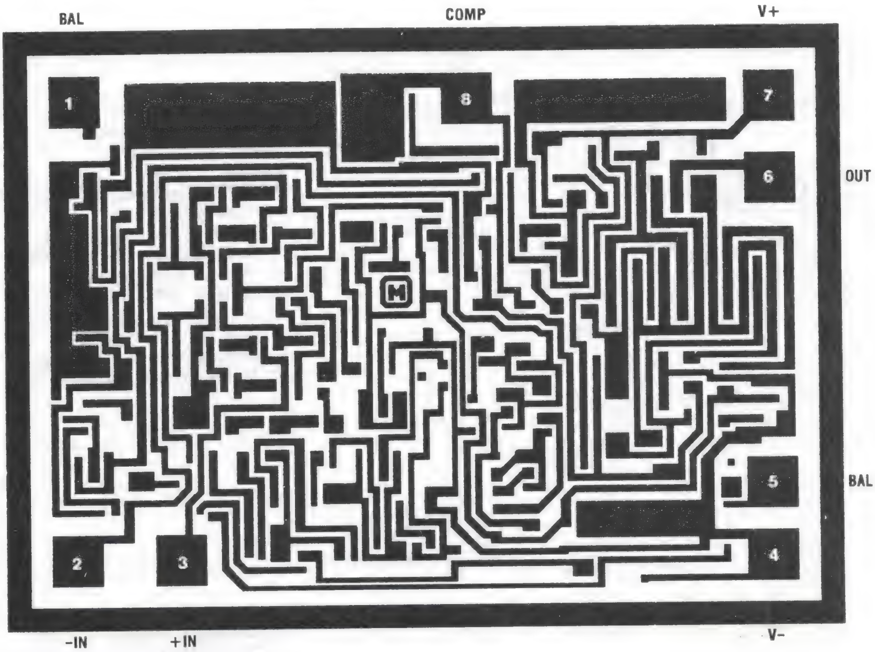
TRANSISTOR COUNT:
HA-2600/883: 140
HA-2602/883: 140

PROCESS: Std. Linear Bipolar Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)
Metal Can — 420°C (Max)

Metallization Mask Layout

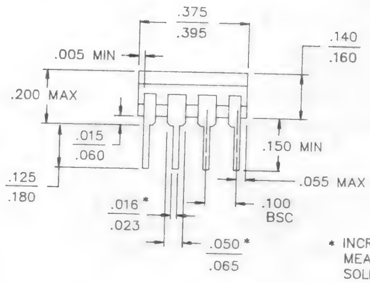
HA-2600/883 HA-2602/883

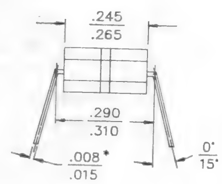


NOTE: Pad Numbers Correspond to Metal Can and Mini-DIP Packages Only.

Packaging †

8 PIN CERAMIC DIP

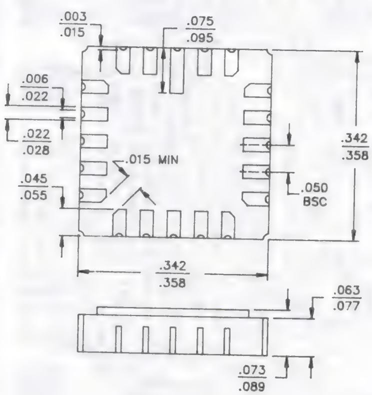




* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

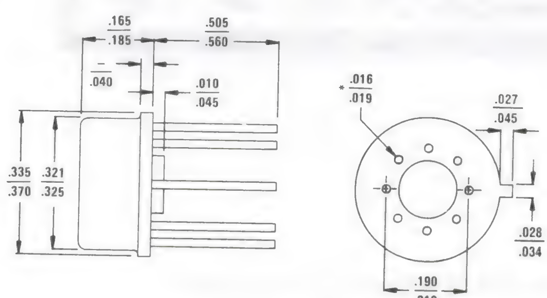
LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-4

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Ceramic, 90% Al_2O_3
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

8 PIN TO-99 METAL CAN



LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
Material: No Seal Material
Temperature: Room Temperature
Method: Resistance Weld
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic Bonded
COMPLIANT OUTLINE: 38510 A-1

*Dimension Maximum Limits Are Increased by 0.003 inches for Solder Dip Finish

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

HA-2600
HA-2602

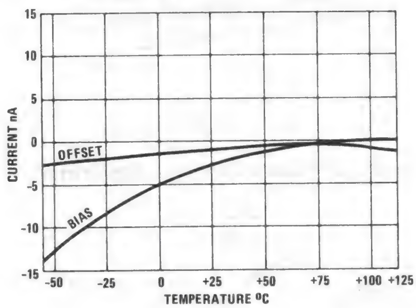
DESIGN INFORMATION

Wideband, High Impedance Operational Amplifiers

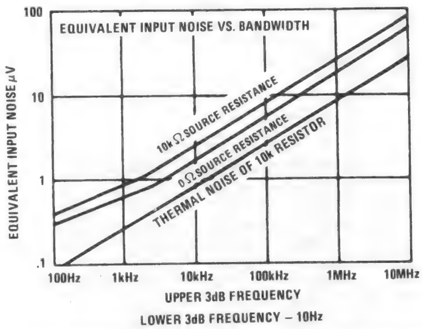
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

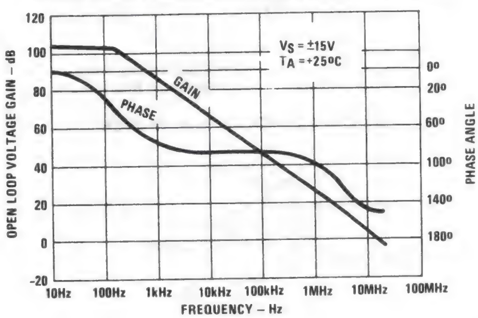
INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



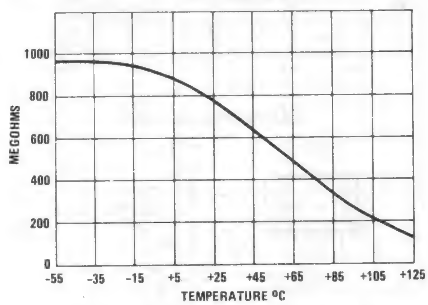
LOWER 3dB FREQUENCY-10Hz BROADBAND NOISE CHARACTERISTICS



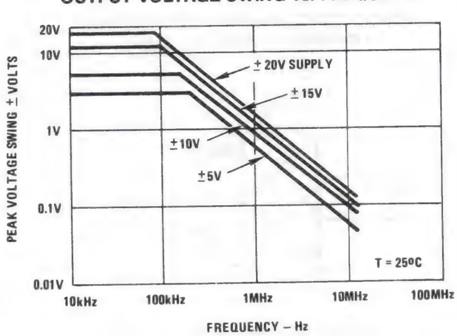
OPEN LOOP FREQUENCY AND PHASE RESPONSE



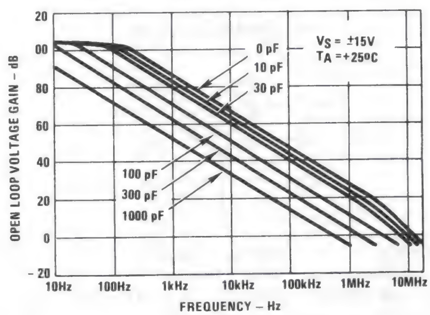
INPUT IMPEDANCE vs. TEMPERATURES, 100Hz



OUTPUT VOLTAGE SWING vs. FREQUENCY



OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND



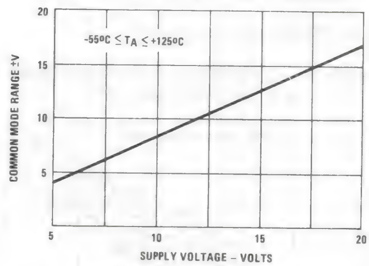
NOTE: External compensation components are not required for stability. But may be added to reduce bandwidth if desired. If external compensation is used, also connect 100µF Capacitor from output to ground.

DESIGN INFORMATION (Continued)

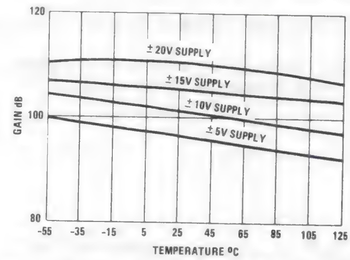
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



OPEN LOOP VOLTAGE GAIN vs. TEMPERATURE



COMMON MODE REJECTION RATIO

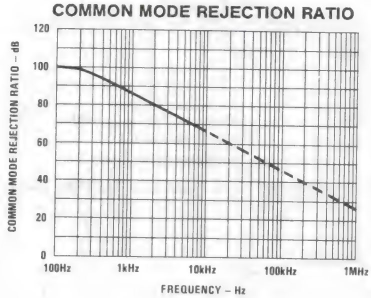
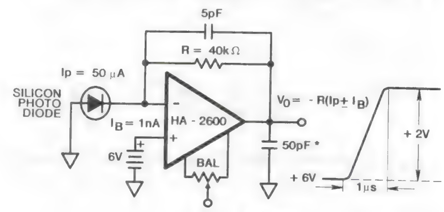
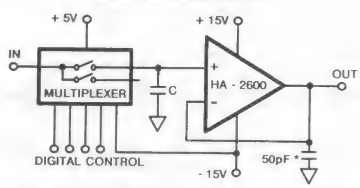


PHOTO CURRENT TO VOLTAGE CONVERTER



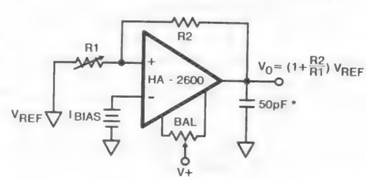
Features
- Constant Cell Voltage
- Minimum Bias Current Error

SAMPLE-AND-HOLD



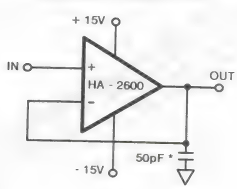
Drift Rate = $\frac{I_{bias}}{C}$ If C = 1000pF Drift = 0.01V/ms Max

REFERENCE VOLTAGE AMPLIFIER



Features
- Minimum Bias Current in Reference Cell
- Short Circuit Protection

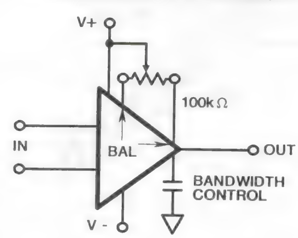
VOLTAGE FOLLOWER



1.000 Gain 0.999	Slew Rate = 4V/μs Min
$Z_{IN} = 10^{12}$ Min	B.W. = 12MHz Typ
$Z_{OUT} = 0.01\Omega$ Max	Output Swing = ± 10V Min to 50kHz

* A small load capacitance is recommended in all applications where practical to prevent possible high frequency oscillations resulting from external wiring parasitics. Capacitance up to 100pF has negligible effect on the bandwidth or slew rate.

SUGGESTED V_{OS} ADJUSTMENT AND COMPENSATION HOOK-UP



Typical Range is ± 10mV with $R_T = 100k\Omega$

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: V_S = ±15V, R_L = 2K, C_L = 50pF, A_V = +1, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	HA-2600 TYPICAL	HA-2602 TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage	V_{CM} = 0V	+25°C	0.5	3	Table 1	mV
		Full	2	4	Table 1	mV
Offset Voltage Average Drift	Versus Temperature	Full	5	5	15	μV/°C
Offset Current Average Drift	Versus Temperature	Full	100	100	200	pA/°C
Differential Input Resistance		+25°C	500	300	Table 3	MΩ
Input Noise Voltage Density	f_O = 10Hz	+25°C	45	45	60	$nV/\sqrt{Hz}$
	f_O = 100Hz	+25°C	25	25	40	$nV/\sqrt{Hz}$
	f_O = 1kHz to 100kHz	+25°C	15	15	Table 3	$nV/\sqrt{Hz}$
Input Noise Current Density	f_O = 10Hz	+25°C	1	1	2	$pA/\sqrt{Hz}$
	f_O = 100Hz	+25°C	0.25	0.25	0.5	$pA/\sqrt{Hz}$
	f_O = 1kHz to 100kHz	+25°C	0.16	0.16	0.3	$pA/\sqrt{Hz}$
Output Voltage Swing	R_L = 2kΩ	Full	±12	±12	Table 1	V
Large Signal Voltage Gain	V_{OUT} = ±10V	+25°C	150	150	Table 1	kV/V
CMRR	V_{CM} = ±10V	Full	100	100	Table 1	dB
PSRR	ΔV_{Supply} = ±10V	Full	90	90	Table 1	dB
Gain Bandwidth Product (Small Signal)	f_O = 10kHz, C_{COMP} = 0pF	+25°C	15	15	10	MHz
	f_O = 1MHz, C_{COMP} = 0pF	+25°C	15	15	10	MHz
Unity Gain Bandwidth	A_V = +1, C_{COMP} = 0pF	+25°C	12	12	8	MHz
Rise/Fall Time	V_{OUT} = ±200mV	+25°C	30	30	Table 2	ns
Overshoot	V_{OUT} = ±200mV	+25°C	25	25	Table 2	%
Slew Rate	V_{OUT} = ±10V	+25°C	7	7	Table 2	V/μs
Full Power Bandwidth	V_{PEAK} = 10V, (Note 2)	+25°C	75	75	Table 3	kHz
Settling Time	10V Step to 0.1%	+25°C	1.5	1.5	4	μs
Output Resistance	Open Loop	+25°C	30	30	65	Ω
Minimum Supply Voltage	Functional Operation Only. Other Parameters Will Vary.	+25°C	±7	±7	±8V	V

HARRIS

HA-2620/883
HA-2622/883

Very Wideband, High Impedance Uncompensated Operational Amplifiers

January 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- High Input Impedance (HA-2620/883) .... 65MΩ Min
- High Gain (HA-2620/883) .... 100kV/V Min; 150kV/V Typ
- High Slew Rate (HA-2620/883) .... 25V/μs Min; 35V/μs Typ
- Low Input Bias Current (HA-2620/883) .... 15nA Max; 5nA Typ
- Low Input Offset Voltage (HA-2620/883) .. 4mV Max
- Wide Gain Bandwidth Product ($A_V \geq 5$) ... 100MHz Typ
- Output Short Circuit Protection

Applications

- Video and R.F. Amplifiers
- Pulse Amplifiers
- Audio Amplifiers and Filters
- High-Q Active Filters
- High Speed Comparators

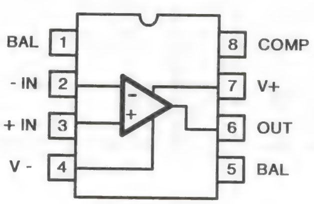
Description

HA-2620/883 and HA-2622/883 are bipolar operational amplifiers that feature very high input impedance coupled with wideband A.C. performance. The high resistance of the input stage is complemented by low offset voltage ($4mV_{max}$ @ $+25^oC$ for HA-2620/883) and low bias and offset current ($15nA_{max}$ @ $+25^oC$ for HA-2620/883) to facilitate accurate signal processing. Offset voltage can be reduced further by means of an external nulling potentiometer. With the HA-2620/883, which is stable for closed loop gains greater than 5, the 25V/μs minimum slew rate at $+25^oC$ and the 100kV/V minimum open loop gain at $+25^oC$, enables the HA-2620/883 to perform high gain amplification of very fast, wideband signals. These dynamic characteristics, coupled with fast settling times, make these amplifiers ideally suited to pulse amplification designs as well as high frequency or video applications. The frequency response of the amplifier can be tailored to exact design requirements by means of an external bandwidth control capacitor. Other high performance designs such as high gain, low distortion audio amplifiers, high-Q and wideband active filters and high speed comparators are excellent uses of this part.

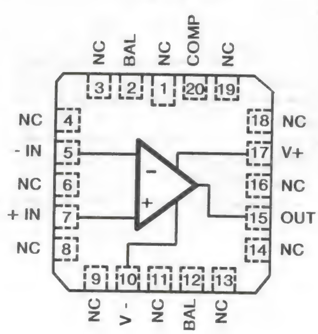
The HA-2620/883 and the HA-2622/883 are available as MIL-STD-883 compliant devices screened to class B level. These devices are sensitive to electrostatic discharge and are in microcircuit group number 49 (see MIL-M-38510, Appendix E). The HA-2620/883 and the HA-2622/883 have guaranteed operation over the military temperature range from -55^oC to $+125^oC$ and are available in 8 pin Metal Can and Ceramic Mini-DIP packages. The HA-2622/883 is also available in a 20 pin Ceramic LCC package.

Pinouts

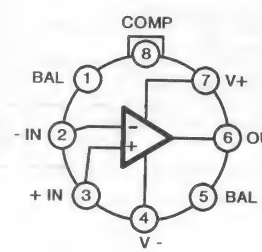
HA7-2620/883 (CERAMIC MINI-DIP)
HA7-2622/883 (CERAMIC MINI-DIP)
TOP VIEW



HA4-2622/883 (CERAMIC LCC)
TOP VIEW



HA2-2620/883 (METAL CAN)
HA2-2622/883 (METAL CAN)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage 12V
Voltage at Either Input Terminal .... V+ to V-
Peak Output Current .... Full Short Circuit Protection
Junction Temperature (T_J) .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... < 2000V
Lead Temperature (Soldering 10 sec) .... 275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	82°C/W	28°C/W
Ceramic LCC Package	74°C/W	20°C/W
Metal Can Package	136°C/W	41°C/W

Package Power Dissipation Limit at +75°C for $T_J \leq$ +175°C
Ceramic DIP Package 730mW
Ceramic LCC Package 1.35W
Metal Can Package 740mW

Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 7.4mW/°C
Ceramic LCC Package .... 13.4mW/°C
Metal Can Package .... 7.4mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±15V
$V_{INcm} \leq$ 1/2 (V+ - V-)
$R_L \geq$ 2kΩ

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	HA-2620/883 MIN	HA-2620/883 MAX	HA-2622/883 MIN	HA-2622/883 MAX	UNITS
Input Offset Voltage	V_{IO}	V_{CM} = 0V	1	+25°C	-4	4	-5	5	mV
			2, 3	+125°C, -55°C	-6	6	-7	7	mV
Input Bias Current	$+I_B$	V_{CM} = 0V $+R_S$ = 100kΩ $-R_S$ = 100Ω	1	+25°C	-15	15	-25	25	nA
			2, 3	+125°C, -55°C	-30	30	-60	60	nA
	$-I_B$	V_{CM} = 0V $+R_S$ = 100Ω $-R_S$ = 100kΩ	1	+25°C	-15	15	-25	25	nA
			2, 3	+125°C, -55°C	-30	30	-60	60	nA
Input Offset Current	I_{IO}	V_{CM} = 0V $+R_S$ = 100kΩ $-R_S$ = 100kΩ	1	+25°C	-15	15	-25	25	nA
			2, 3	+125°C, -55°C	-30	30	-60	60	nA
Common Mode Range	+CMR	V+ = 4V V- = -26V	1	+25°C	11	-	11	-	V
			2, 3	+125°C, -55°C	11	-	11	-	V
	-CMR	V+ = 26V V- = -4V	1	+25°C	-	-11	-	-11	V
			2, 3	+125°C, -55°C	-	-11	-	-11	V
Large Signal Voltage Gain	$+A_{VOL}$	V_{OUT} = 0V and +10V R_L = 2kΩ	4	+25°C	100	-	80	-	kV/V
			5, 6	+125°C, -55°C	70	-	60	-	kV/V
	$-A_{VOL}$	V_{OUT} = 0V and -10V R_L = 2kΩ	4	+25°C	100	-	80	-	kV/V
			5, 6	+125°C, -55°C	70	-	60	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔV_{CM} = +10V +V = +5V -V = -25V V_{OUT} = -10V	1	+25°C	80	-	74	-	dB
			2, 3	+125°C, -55°C	80	-	74	-	dB
	-CMRR	ΔV_{CM} = -10V +V = +25V -V = -5V V_{OUT} = +10V	1	+25°C	80	-	74	-	dB
			2, 3	+125°C, -55°C	80	-	74	-	dB

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	HA-2620/883 MIN	HA-2620/883 MAX	HA-2622/883 MIN	HA-2622/883 MAX	UNITS
Output Voltage Swing	$+V_{OUT}$	R_L = 2kΩ	4	+25°C	10	-	10	-	V
			5, 6	+125°C, -55°C	10	-	10	-	V
	$-V_{OUT}$	R_L = 2kΩ	4	+25°C	-	-10	-	-10	V
			5, 6	+125°C, -55°C	-	-10	-	-10	V
Output Current	$+I_{OUT}$	V_{OUT} = -10V	4	+25°C	15	-	10	-	mA
			5, 6	+125°C, -55°C	10	-	7.5	-	mA
	$-I_{OUT}$	V_{OUT} = +10V	4	+25°C	-	-15	-	-10	mA
			5, 6	+125°C, -55°C	-	-10	-	-7.5	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V	1	+25°C	-	3.7	-	3.7	mA
		I_{OUT} = 0mA	2, 3	+125°C, -55°C	-	4.0	-	4.0	mA
	$-I_{CC}$	V_{OUT} = 0V	1	+25°C	-3.7	-	-3.7	-	mA
		I_{OUT} = 0mA	2, 3	+125°C, -55°C	-4.0	-	-4.0	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = ± 5 +V = +10V, -V = -15V +V = +20V, -V = -15V	1	+25°C	80	-	74	-	dB
			2, 3	+125°C, -55°C	80	-	74	-	dB
	-PSRR	ΔV_{SUP} = ± 5V +V = +15V, -V = -10V +V = +15V, -V = -20V	1	+25°C	80	-	74	-	dB
			2, 3	+125°C, -55°C	80	-	74	-	dB

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_{VCL} = +5V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	HA-2620/883 MIN	HA-2620/883 MAX	HA-2622/883 MIN	HA-2622/883 MAX	UNITS
Slew Rate	+SR	V_{OUT} = -5V to +5V	7	+25°C	25	-	20	-	V/μs
			8A, 8B	+125°C, -55°C	20	-	15	-	V/μs
	-SR	V_{OUT} = +5V to -5V	7	+25°C	25	-	20	-	V/μs
			8A, 8B	+125°C, -55°C	20	-	15	-	V/μs
Rise & Fall Time	T_R	V_{OUT} = 0 to +200mV 10% ≤ T_R ≤ 90%	7	+25°C	-	45	-	45	ns
			8A, 8B	+125°C, -55°C	-	60	-	70	ns
	T_F	V_{OUT} = 0 to -200mV 10% ≤ T_F ≤ 90%	7	+25°C	-	45	-	45	ns
			8A, 8B	+125°C, -55°C	-	60	-	70	ns
Overshoot	+OS	V_{OUT} = 0 to +200mV	7	+25°C	-	70	-	80	%
			8A, 8B	+125°C, -55°C	-	70	-	80	%
	-OS	V_{OUT} = 0 to -200mV	7	+25°C	-	70	-	80	%
			8A, 8B	+125°C, -55°C	-	70	-	80	%

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	HA-2620/883 MIN	HA-2620/883 MAX	HA-2622/883 MIN	HA-2622/883 MAX	UNITS
Differential Input Resistance	R_{IN}	V_{CM} = 0V	1	+25°C	65	-	40	-	MΩ
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	+25°C	400	-	320	-	kHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 2kΩ, C_L = 50pF	1	-55°C to +125°C	5	-	5	-	V/V
Output Short Circuit Current	$+I_{SC}$	V_{OUT} = 1V, R_L = 10Ω	1	+25°C	-	50	-	50	mA
			1	+125°C	-	45	-	45	mA
			1	-55°C	-	60	-	60	mA
	$-I_{SC}$	V_{OUT} = -1V, R_L = 10Ω	1	+25°C	-50	-	-50	-	mA
			1	+125°C	-45	-	-45	-	mA
			1	-55°C	-60	-	-60	-	mA
Output Resistance	R_{OUT}	Open Loop	1	+25°C	-	30	-	30	Ω
Quiescent Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	240	-	240	mW

NOTES: 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).

3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)

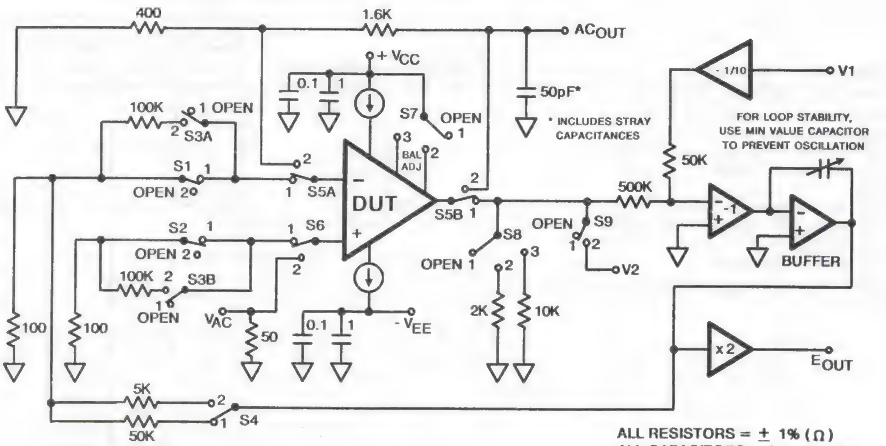
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6, 7, 8A, 8B
Group A Test Requirements	1, 2, 3, 4, 5, 6, 7, 8A, 8B
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

The Subgroup assignment of the parameters in these tables were patterned after Mil-M-38510/112, device type 03.

Test Circuit (Applies to Table 1 and 2)

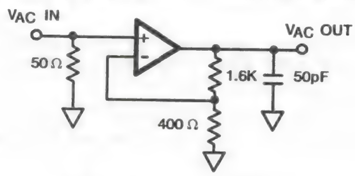


ALL RESISTORS = ± 1% (Ω)
ALL CAPACITORS = ± 10% (μF)

For Detailed Information, Refer to HA-2620/883; HA-2622/883 Test Tech Brief

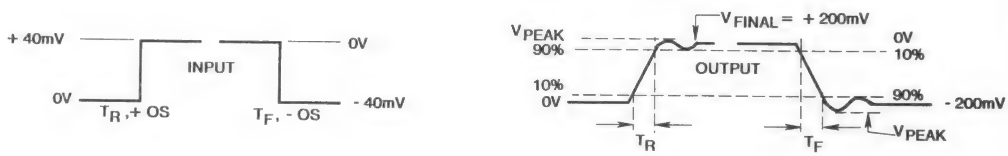
Test Waveforms

SIMPLIFIED TEST CIRCUIT (Applies to Table 2)



SLEW RATE WAVEFORMS

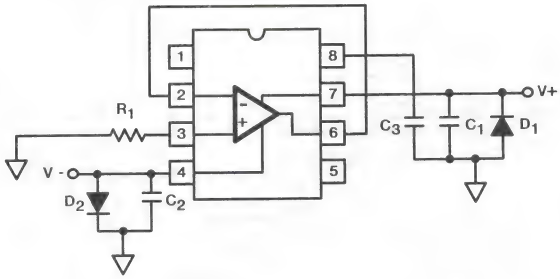
OVERSHOOT, RISE & FALL TIME WAVEFORMS



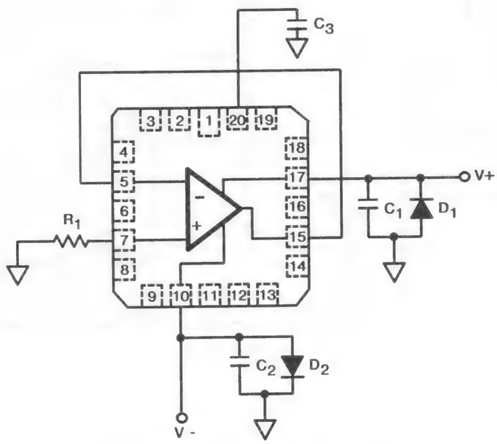
NOTE: Measured on both positive and negative transitions.
Capacitance at Compensation pin should be minimized.

Burn-In Circuits

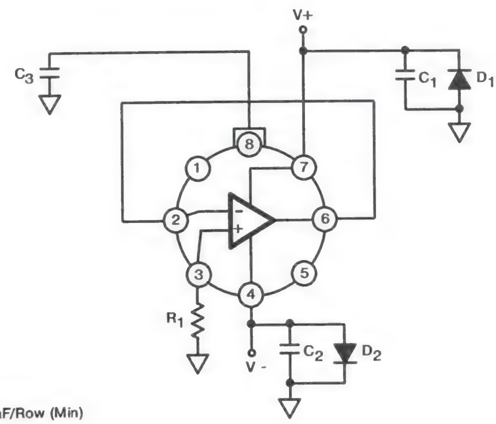
HA7-2620/883 CERAMIC MINI-DIP
HA7-2622/883 CERAMIC MINI-DIP



HA4-2622/883 CERAMIC LCC

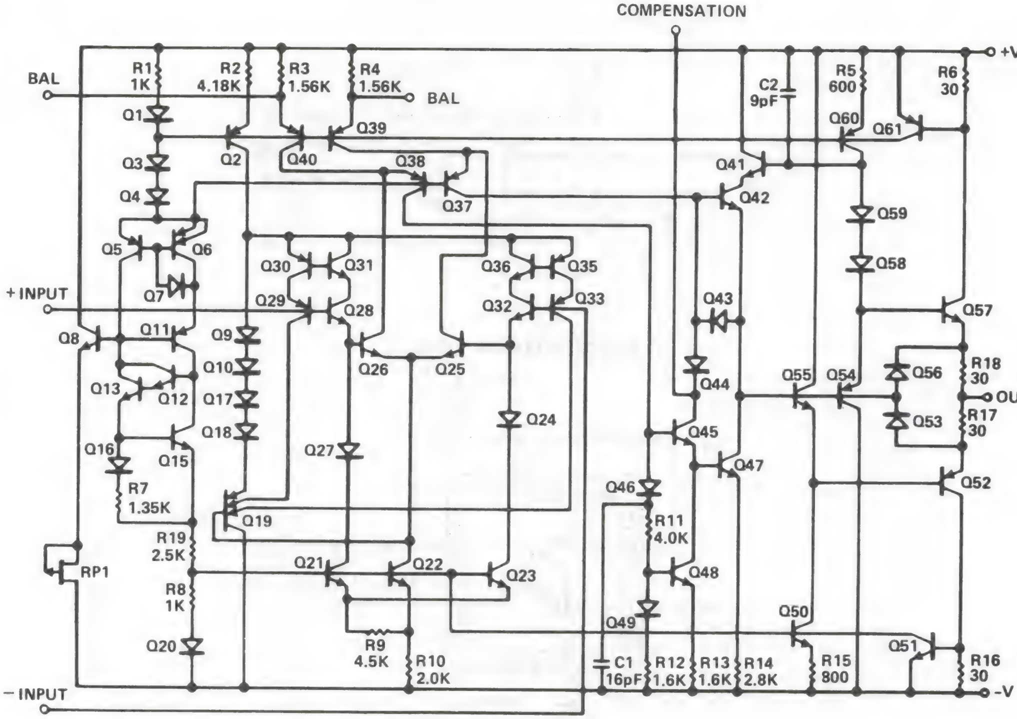


HA2-2620/883 (TO-99) METAL CAN
HA2-2622/883 (TO-99) METAL CAN



NOTES:
R_1 = 1MΩ, ±5%, 1/4W (Min)
$C_1 = C_2$ = 0.01µF/Socket (Min) or 0.1µF/Row (Min)
C_3 = 0.01µF/Socket (10%)
$D_1 = D_2$ = IN4002 or Equivalent/Board
$|(V+) - (V-)| = 30V$

Schematic Diagram



Die Characteristics

DIE DIMENSIONS:
73 x 52 x 19 mils
(1860 x 1320 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$1.5 \times 10^5 A/cm^2$ @ 19mA

SUBSTRATE POTENTIAL (Powered Up):
Unbiased

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

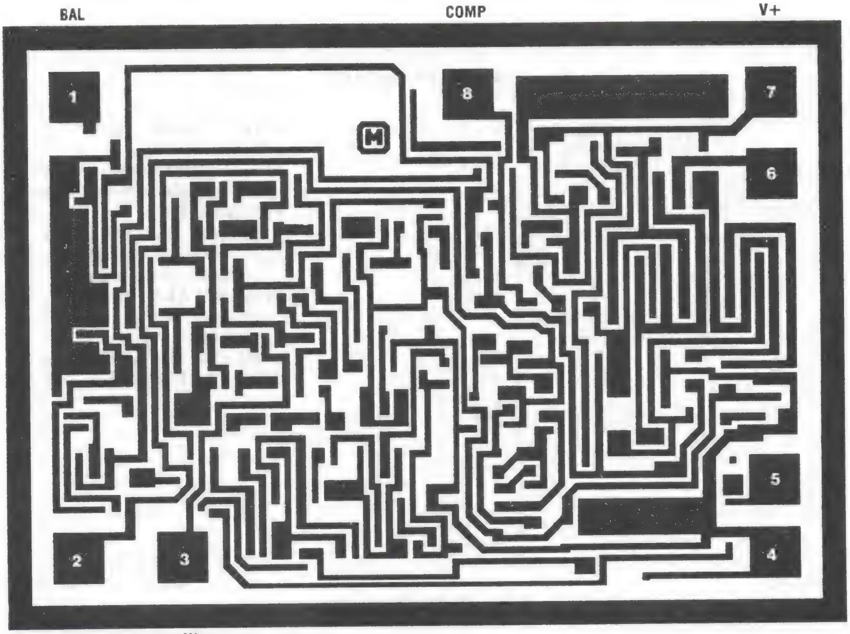
TRANSISTOR COUNT:
HA-2620/883: 140
HA-2622/883: 140

PROCESS: Std. Linear Bipolar Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)
Metal Can — 420°C (Max)

Metallization Mask Layout

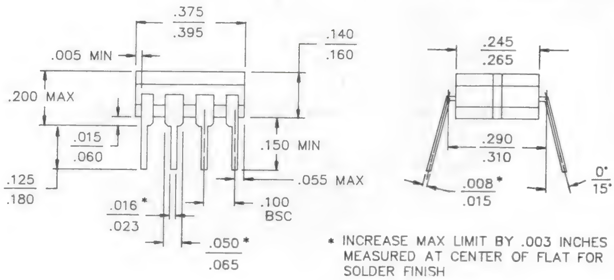
HA-2620/883 HA-2622/883



NOTE: Pin Numbers Correspond to 8 Pin Metal Can and Ceramic Mini-Dip Packages Only.

Packaging †

8 PIN CERAMIC DIP

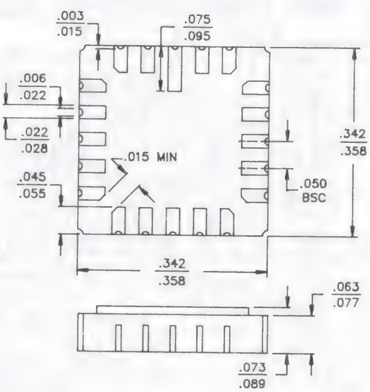


LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
- Material: Glass Frit
- Temperature: 450°C ± 10°C
- Method: Furnace Seal

INTERNAL LEAD WIRE:
- Material: Aluminum
- Diameter: 1.25 Mil
- Bonding Method: Ultrasonic

COMPLIANT OUTLINE: 38510 D-4

20 PAD CERAMIC LCC

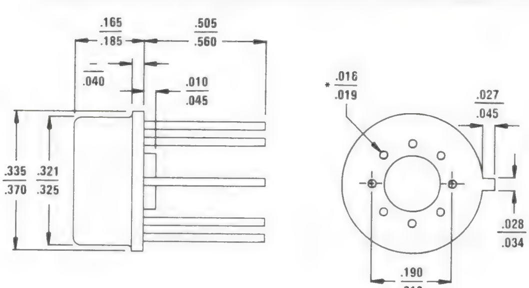


PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Ceramic, 90% Al_2O_3
PACKAGE SEAL:
- Material: Gold/Tin (80/20)
- Temperature: 320°C ± 10°C
- Method: Furnace Braze

INTERNAL LEAD WIRE:
- Material: Aluminum
- Diameter: 1.25 Mil
- Bonding Method: Ultrasonic

COMPLIANT OUTLINE: 38510 C-2

8 PIN TO-99 METAL CAN



LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
- Material: No Seal Material
- Temperature: Room Temperature
- Method: Resistance Weld

INTERNAL LEAD WIRE:
- Material: Aluminum
- Diameter: 1.25 Mil
- Bonding Method: Ultrasonic Bonded

COMPLIANT OUTLINE: 38510 A-1

*Dimension Maximum Limits Are Increased by 0.003 inches for Solder Dip Finish

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

HA-2620
HA-2622

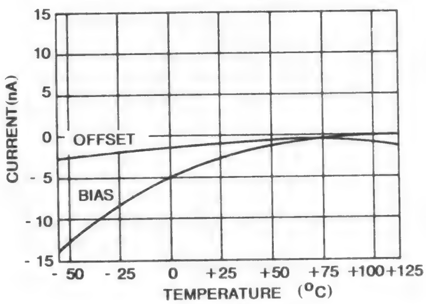
DESIGN INFORMATION

Very Wideband, Uncompensated Operational Amplifiers

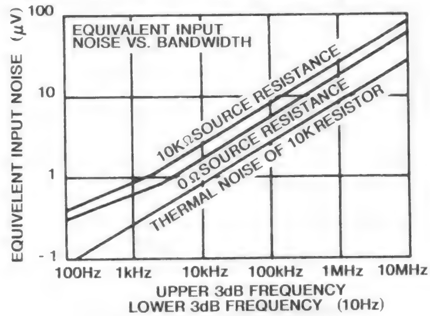
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

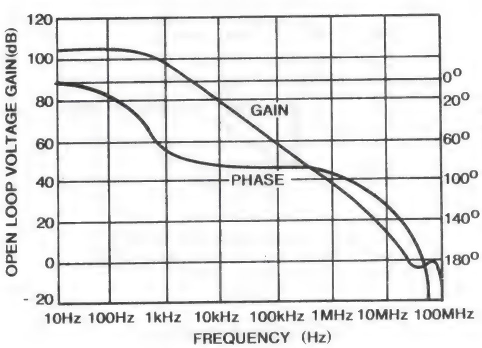
INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



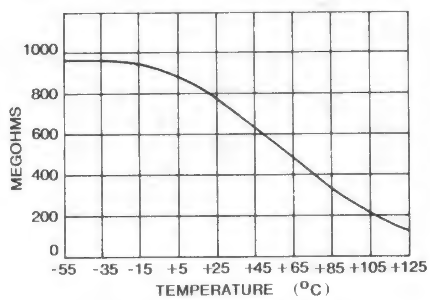
EQUIVALENT INPUT NOISE vs. BANDWIDTH



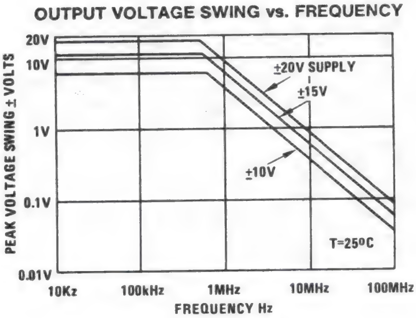
OPEN LOOP FREQUENCY AND PHASE RESPONSE



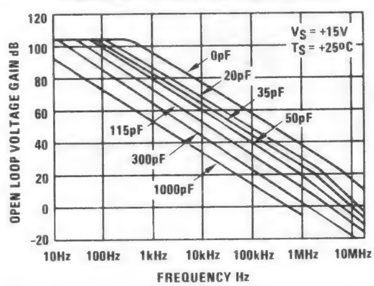
INPUT IMPEDANCE vs. TEMPERATURES, 100Hz



OUTPUT VOLTAGE SWING vs. FREQUENCY



OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND



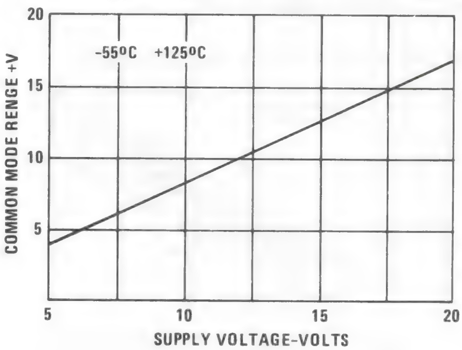
NOTE: External compensation components is required for Closed Loop Gain $\leq$ 5. If external compensation is used, also connect 100pF Capacitor from output to ground for H.F. filtering.

DESIGN INFORMATION (Continued)

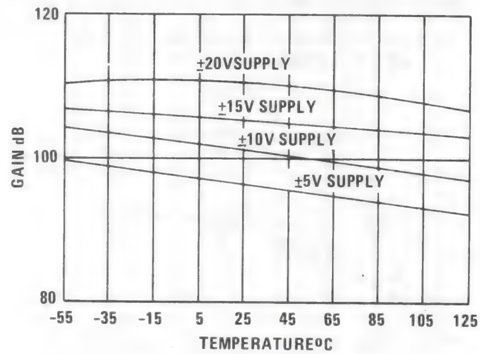
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

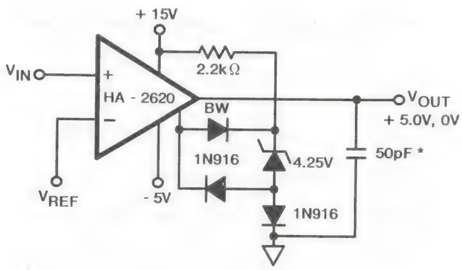
COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



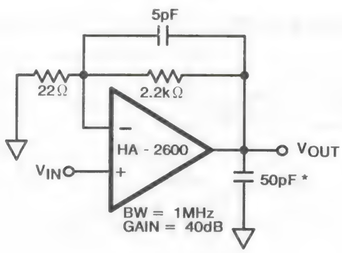
OPEN LOOP VOLTAGE GAIN vs. TEMPERATURE



HIGH IMPEDANCE COMPARATOR

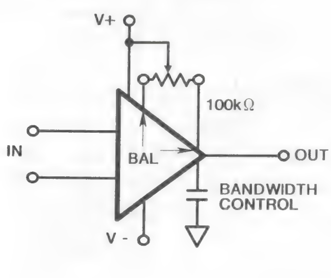


VIDEO AMPLIFIER

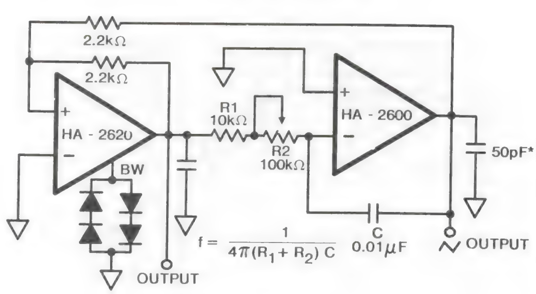


* A small load capacitance of at least 30pF (including stray capacitance) is recommended to prevent high frequency oscillations.

SUGGESTED V_{OS} ADJUSTMENT AND COMPENSATION HOOK-UP



FUNCTION GENERATOR



$$f = \frac{1}{4\pi(R_1 + R_2)\,C}$$

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: $V_S = \pm15V$, $R_L = 2K$, $C_L = 50pF$, $A_V \leq 5$, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	HA-2620 TYPICAL	HA-2622 TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage	$V_{CM} = 0V$	+25°C	0.5	3	Table 1	mV
		Full	2	4	Table 1	mV
Offset Voltage Average Drift	Versus Temperature	Full	5	5	15	μV/°C
Offset Current Average Drift	Versus Temperature	Full	100	100	200	pA/°C
Differential Input Resistance		+25°C	500	300	Table 3	MΩ
Input Noise Voltage Density	$f_o = 10Hz$	+25°C	45	45	60	$nV/\sqrt{Hz}$
	$f_o = 100Hz$	+25°C	25	25	40	$nV/\sqrt{Hz}$
	$f_o = 1kHz$ to $100kHz$	+25°C	15	15	Table 3	$nV/\sqrt{Hz}$
Input Noise Current Density	$f_o = 10Hz$	+25°C	1	1	2	$pA/\sqrt{Hz}$
	$f_o = 100Hz$	+25°C	0.25	0.25	0.5	$pA/\sqrt{Hz}$
	$f_o = 1kHz$ to $100kHz$	+25°C	0.16	0.16	0.3	$pA/\sqrt{Hz}$
Output Voltage Swing	$R_L = 2k\Omega$	Full	±12	±12	Table 1	V
Large Signal Voltage Gain	$V_{OUT} = \pm10V$	+25°C	150	150	Table 1	kV/V
CMRR	$V_{CM} = \pm10V$	Full	100	100	Table 1	dB
PSRR	$\Delta V_{Supply} = \pm10V$	Full	90	90	Table 1	dB
Gain Bandwidth Product (Small Signal)	$f_o = 10kHz$, $C_{COMP} = 0pF$	+25°C	100	100	80	MHz
	$f_o = 1MHz$, $C_{COMP} = 0pF$	+25°C	100	100	60	MHz
Rise/Fall Time	$V_{OUT} = \pm200mV$	+25°C	17	17	Table 2	ns
Overshoot	$V_{OUT} = \pm200mV$	+25°C	35	35	Table 2	%
Slew Rate	$V_{OUT} = \pm10V$	+25°C	±35	±35	Table 2	V/μs
Full Power Bandwidth	$V_{PEAK} = 10V$, (Note 2)	+25°C	600	600	Table 3	kHz
Settling Time	10V Step to 0.1%	+25°C	1	1	2	μs
Output Resistance	Open Loop	+25°C	30	30	65	Ω
Minimum Supply Voltage	Functional Operation Only. Other Parameters Will Vary.	+25°C	±7	±7	±8V	V

HARRIS

HA-2640/883

High Voltage Operational Amplifier

January 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Output Voltage Swing ....±35V (Min)
- Supply Voltage .... ±10V to ±40V (Min)
- Slew Rate .... 3V/μs (Min)
- Common Mode Input Voltage Swing ......±35V (Min)
- Offset Current .... 12nA (Max)
- Unity Gain Bandwidth ....5MHz (Typ)
- Output Overload Protection

Applications

- Industrial Control Systems
- Power Supplies
- High Voltage Regulators
- Resolver Excitation
- Signal Conditioning

Description

HA-2640/883 monolithic operational amplifier is designed to deliver unprecedented dynamic specification for a high voltage internally compensated device. This dielectrically isolated device offer very low values for offset voltage and offset current coupled with large output voltage swing and common mode input voltage.

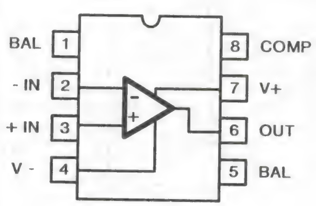
For maximum reliability, the HA-2640/883 offers unconditional output overload protection through output short circuit current limiting. This circuitry will limit the output to typically ±25mA output drive current.

These amplifiers deliver ±35V common mode input voltage swing, ±35V output voltage swing, and up to ±40V supply range for use in such designs as regulators, power supplies, and industrial control systems. The 5MHz typical gain-bandwidth product and 5V/μs slew rate (typ) make these devices excellent components for high performance signal conditioning applications. To insure compliance, all devices are 100% tested for slew rate, rise/fall time and overshoot. Outstanding input and output voltage swings coupled with a low 5nA offset current (typ), make these amplifiers excellent components for resolver excitation designs.

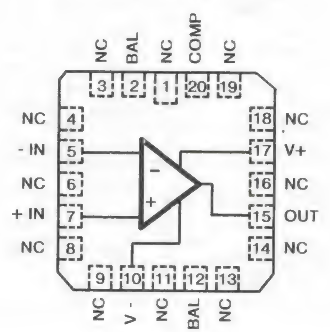
The HA-2640/883 is specified from -55°C to +125°C and is available in the hermetic 8 pin Metal Can, Ceramic Mini-DIP, and also the 20 pin Ceramic LCC.

Pinouts

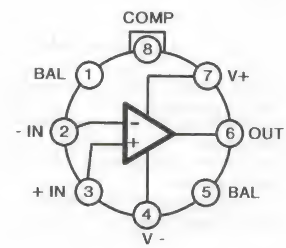
HA7-2640/883 (CERAMIC MINI-DIP)
TOP VIEW



HA4-2640/883 (CERAMIC LCC)
TOP VIEW



HA2-2640/883 (METAL CAN)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 100V
Differential Input Voltage 100V
Input Voltage Range .... ±37V
Output Current .... Full Short Circuit Protection
Output Short Circuit Duration .... 5 Seconds
Junction Temperature (T_J) .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... < 2000V
Lead Temperature (Soldering 10 sec) .... 275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	125°C/W	43°C/W
Ceramic LCC Package	88°C/W	20°C/W
Metal Can Package	107°C/W	33°C/W

Package Power Dissipation Limit at +75°C for $T_J \leq$ +175°C
- Ceramic DIP Package 800mW
- Ceramic LCC Package 1.14mW
- Metal Can Package 930mW

Package Power Dissipation Derating Factor Above +75°C
- Ceramic DIP Package .... 8mW/°C
- Ceramic LCC Package .... 11.4mW/°C
- Metal Can Package .... 9.3mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±10V to ± 40V
$V_{INcm} \leq$ 1/2 (V+ - V-)
$R_L \geq 500\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±40V, $R_{SOURCE} = 100\Omega$, $R_{LOAD} = 500k\Omega$, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	V_{CM} = 0V	1	+25°C	-4	4	mV
			2, 3	+125°C, -55°C	-6	6	mV
Input Bias Current	$+I_B$	V_{CM} = 0V $+R_S = 100k\Omega$ $-R_S = 100\Omega$	1	+25°C	-25	25	nA
			2, 3	+125°C, -55°C	-50	50	nA
	$-I_B$	V_{CM} = 0V $+R_S = 100\Omega$ $-R_S = 100k\Omega$	1	+25°C	-25	25	nA
			2, 3	+125°C, -55°C	-50	50	nA
Input Offset Current	I_{IO}	V_{CM} = 0V $+R_S = 100k\Omega$ $-R_S = 100k\Omega$	1	+25°C	-12	12	nA
			2, 3	+125°C, -55°C	-35	35	nA
Common Mode Range	+CMR	V+ = 15V V- = -65V	1	+25°C	25	-	V
			2, 3	+125°C, -55°C	25	-	V
	-CMR	V+ = 65V V- = -15V	1	+25°C	-	-25	V
			2, 3	+125°C, -55°C	-	-25	V
Large Signal Voltage Gain	$+A_{VOL}$	V_{OUT} = 0V and +30V $R_L = 5k\Omega$	4	+25°C	100	-	kV/V
			5, 6	+125°C, -55°C	75	-	kV/V
	$-A_{VOL}$	V_{OUT} = 0V and -30V $R_L = 5k\Omega$	4	+25°C	100	-	kV/V
			5, 6	+125°C, -55°C	75	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔV_{CM} = +20V +V = +20V -V = -60V V_{OUT} = -20V	4	+25°C	80	-	dB
			5, 6	+125°C, -55°C	80	-	dB
	-CMRR	ΔV_{CM} = -20V +V = +60V -V = -20V V_{OUT} = +20V	4	+25°C	80	-	dB
			5, 6	+125°C, -55°C	80	-	dB

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±40V, R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Voltage Swing	$+V_{OUT}$	R_L = 5kΩ	1	+25°C	35	-	V
			2, 3	+125°C, -55°C	35	-	V
	$-V_{OUT}$	R_L = 5kΩ	1	+25°C	-	-35	V
			2, 3	+125°C, -55°C	-	-35	V
Output Current	$+I_{OUT}$	V_{OUT} = -10V	4	+25°C	12	-	mA
	$-I_{OUT}$	V_{OUT} = +10V	4	+25°C	-	-12	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-	3.8	mA
			2, 3	+125°C, -55°C	-	4.0	mA
	$-I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-3.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = 30V +V = +10V, -V = -40V +V = +40V, -V = -40V	4	+25°C	80	-	dB
			5, 6	+125°C, -55°C	80	-	dB
	-PSRR	ΔV_{SUP} = 30V +V = +40V, -V = -10V +V = +40V, -V = -40V	4	+25°C	80	-	dB
			5, 6	+125°C, -55°C	80	-	dB
Offset Voltage Adjustment	$+V_{IO}Adj$	Note 4	1	+25°C	V_{IO}-1	-	mV
			2, 3	+125°C, -55°C	V_{IO}-1	-	mV
	$-V_{IO}Adj$	Note 4	1	+25°C	V_{IO}+1	-	mV
			2, 3	+125°C, -55°C	V_{IO}+1	-	mV

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 5kΩ, C_{LOAD} = 50pF, A_{VCL} = +1V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Slew Rate	+SR	V_{OUT} = -3V to +3V	4	+25°C	3	-	V/µs
	-SR	V_{OUT} = +3V to -3V	4	+25°C	3	-	V/µs
Rise & Fall Time	T_R	V_{OUT} = 0 to +200mV $10\% \le T_R \le 90\%$	4	+25°C	-	100	ns
	T_F	V_{OUT} = 0 to -200mV $10\% \le T_F \le 90\%$	4	+25°C	-	100	ns
Overshoot	+OS	V_{OUT} = 0 to +200mV	4	+25°C	-	30	%
	-OS	V_{OUT} = 0 to -200mV	4	+25°C	-	30	%

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±40V, R_{LOAD} = 5kΩ, C_{LOAD} = 50pF, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Differential Input Resistance	R_{IN}	V_{CM} = 0V	1	+25°C	50	-	MΩ
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	+25°C	45	-	kHz
		V_{PEAK} = 35V	1, 2	+25°C	13.6	-	kHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 5kΩ, C_L = 50pF	1	-55°C to +125°C	1	-	V/V
Output Short Circuit Current	$+I_{SC}$	V_{OUT} = 0V, R_L = 10Ω	1	+25°C	-	25	mA
	$-I_{SC}$	V_{OUT} = 0V, R_L = 10Ω	1	+25°C	-25	-	mA
Output Resistance	R_{OUT}	Open Loop	1	+25°C	-	600	Ω
Quiescent Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	320	mW

NOTES:
1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).
3. Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)
4. Offset adjustment range is [V_{IO} (Measured) ± 1mV] minimum referred to output. This test is for functionality only to assure adjustment through 0V.

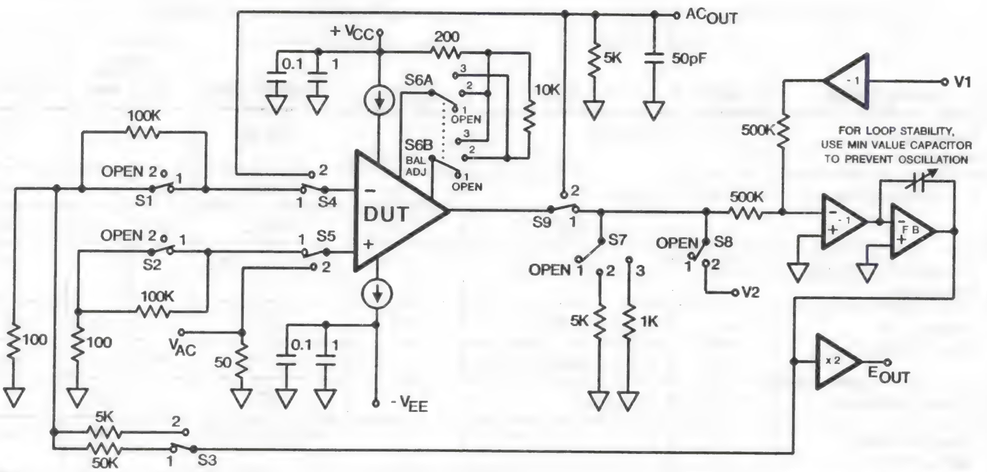
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6
Group A Test Requirements	1, 2, 3, 4, 5, 6
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

The Subgroup assignments of the parameters in these tables were patterned after SMD #78003, device type 02.

Test Circuit (Applies to Tables 1 and 2)

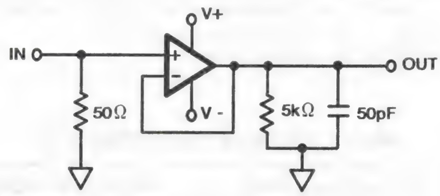


ALL RESISTORS = ± 1% (Ω)
ALL CAPACITORS = ± 10% (μF)

For Detailed Information, Refer to HA-2640/883 Test Tech Brief

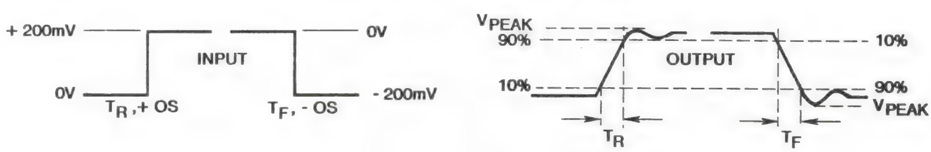
Test Waveforms

SIMPLIFIED TEST CIRCUIT (Applies to Table 2)



SLEW RATE WAVEFORMS

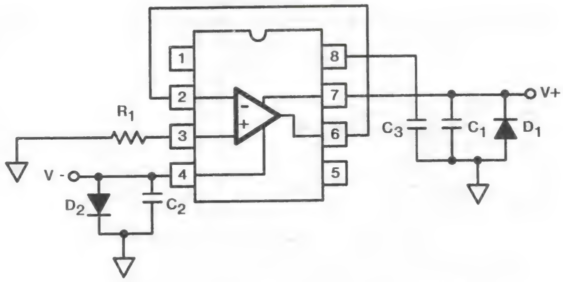
OVERSHOOT, RISE & FALL TIME WAVEFORMS



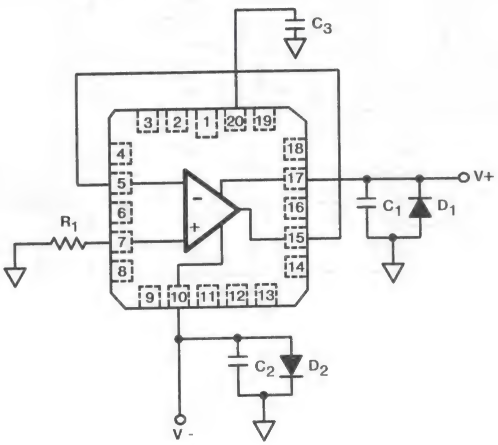
NOTE: Measured on both positive and negative transitions.
Capacitance at Compensation pin should be minimized.

Burn-In Circuits

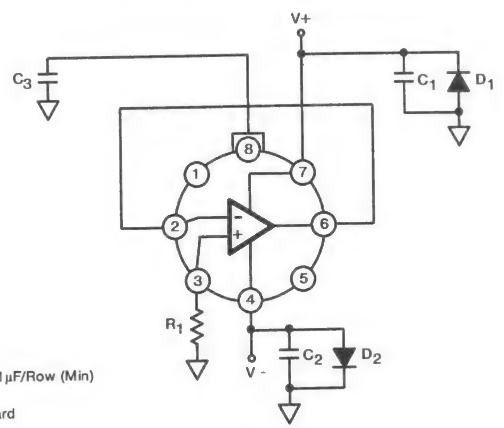
HA7-2640/883 CERAMIC MINI-DIP



HA4-2640/883 CERAMIC LCC



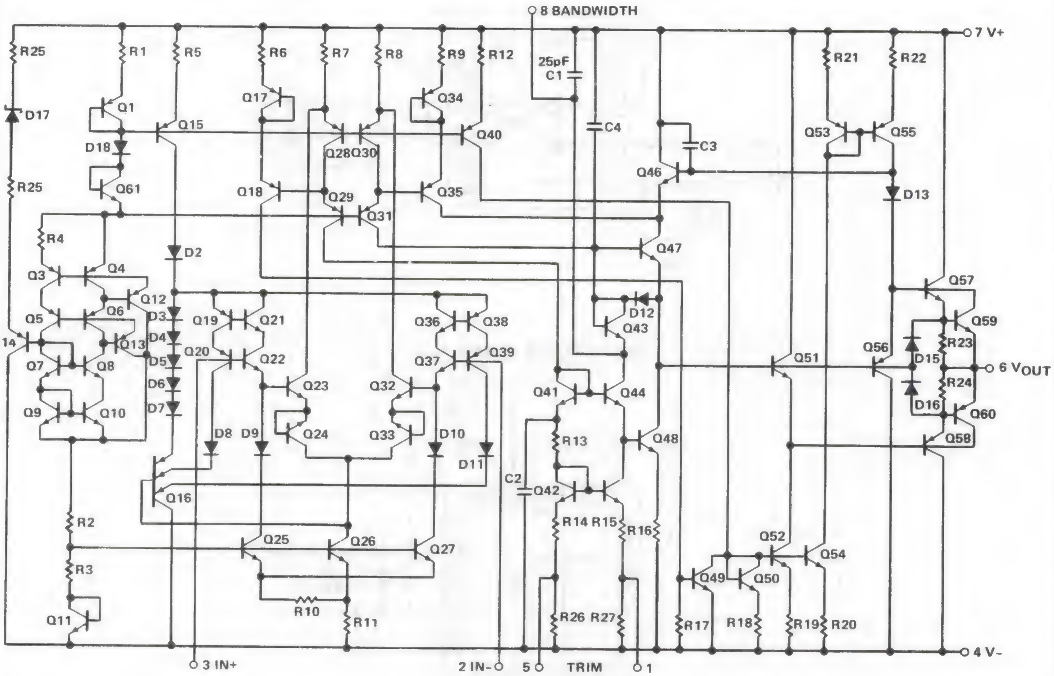
HA2-2640/883 (TO-99) METAL CAN



NOTES:

R_1 = 1MΩ, ±5%, 1/4W (Min)
$C_1 = C_2$ = 0.01μF/Socket (Min) or 0.1μF/Row (Min)
C_3 = 0.01μF/Socket (10%)
$D_1 = D_2$ = IN4002 or Equivalent/Board
$|(V+) - (V-)|$ = 40V

Schematic Diagram



Die Characteristics

DIE DIMENSIONS:
84 x 70 x 19 mils
(2140 x 1780 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$2.14 \times 10^5 A/cm^2$ @ 12mA
This device meets Glassivation Integtrity Test requirement per Mil-Std-883 Method 2021 and Mil-M-38510 paragraph 3.5.5.4.

SUBSTRATE POTENTIAL (Powered Up):
Unbiased

GLASSIVATION:
Type: Silox
Thickness: 7kÅ ± 0.7kÅ

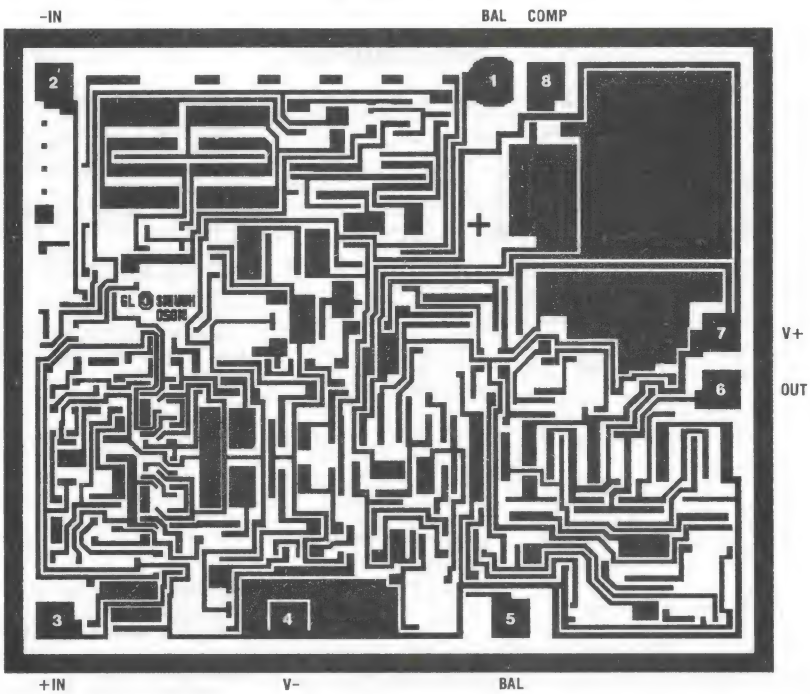
TRANSISTOR COUNT: 76

PROCESS: HV200 Std. Linear Bipolar
Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)
Metal Can — 420°C (Max)

Metallization Mask Layout

HA-2640/883



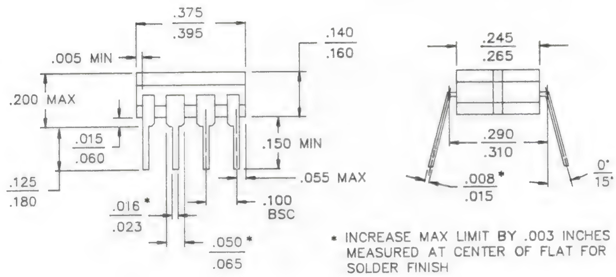
NOTE: Pad Numbers Correspond to Metal Can and Ceramic Mini-DIP Packages Only.

3

OP AMPs & COMPARATORS

Packaging †

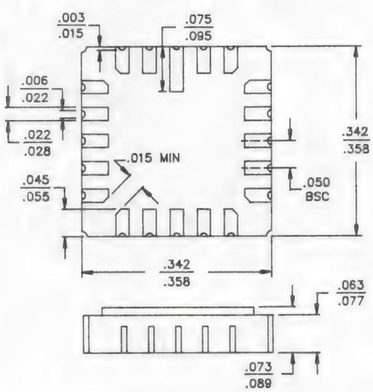
8 PIN CERAMIC DIP



* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

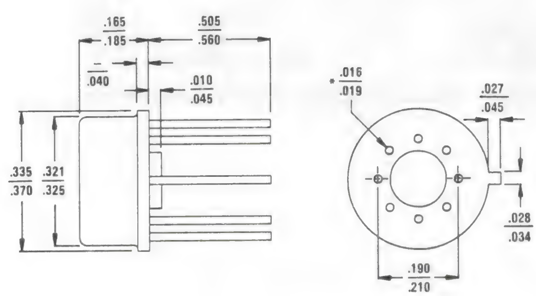
LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-4

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Ceramic, 90% Al_2O_3
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

8 PIN TO-99 METAL CAN



LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
Material: No Seal Material
Temperature: Room Temperature
Method: Resistance Weld
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic Bonded
COMPLIANT OUTLINE: 38510 A-1

*Dimension Maximum Limits Are Increased by 0.003 inches for Solder Dip Finish

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HA-2640

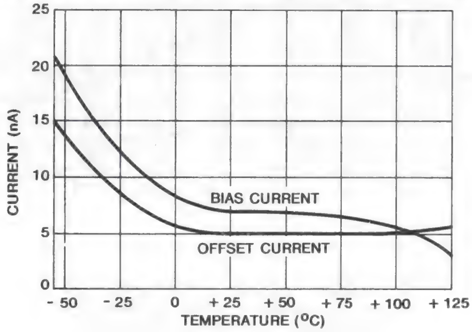
DESIGN INFORMATION

High Voltage Operational Amplifier

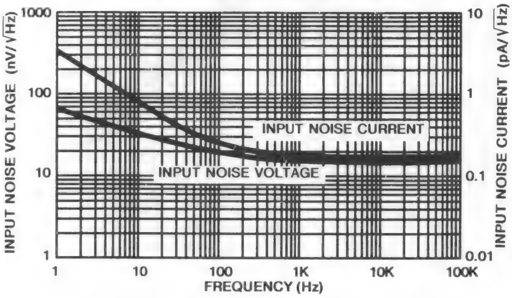
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm40V$

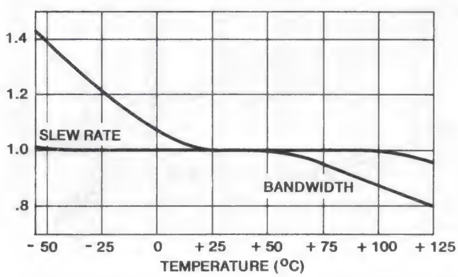
INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



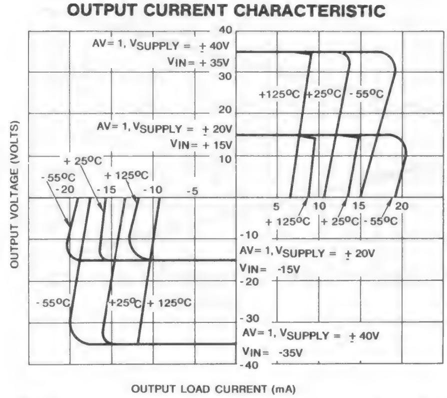
INPUT NOISE CHARACTERISTICS



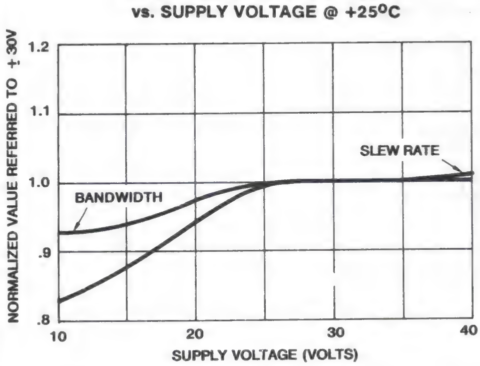
NORMALIZED A.C. PARAMETERS vs. TEMPERATURE



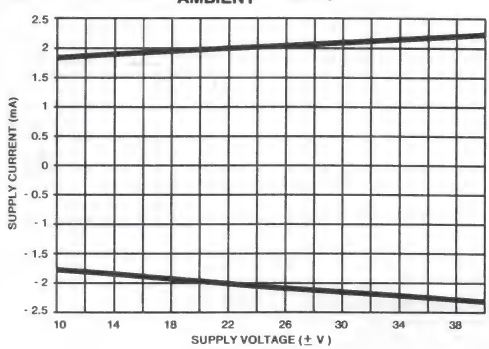
OUTPUT CURRENT CHARACTERISTIC



NORMALIZED A.C. PARAMETERS vs. SUPPLY VOLTAGE @ +25°C



QUIESCENT SUPPLY CURRENT vs. SUPPLY CURRENT
$T_{AMBIENT}$ = +25°C

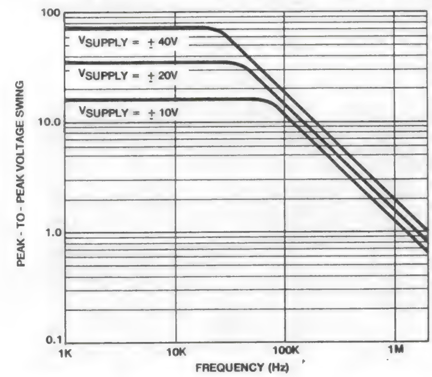


DESIGN INFORMATION (Continued)

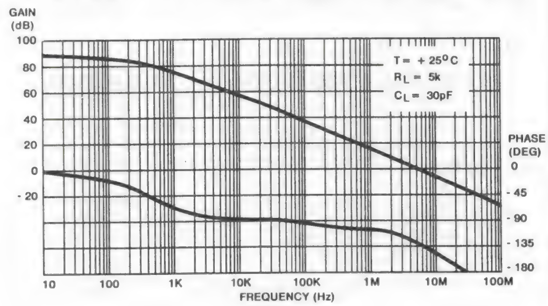
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm40V$

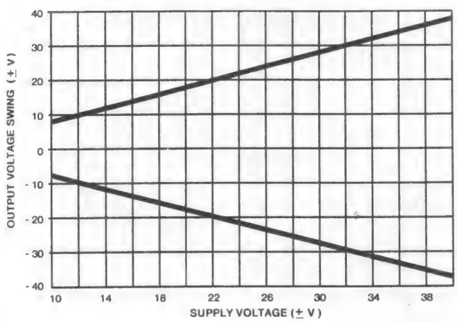
OUTPUT VOLTAGE SWING vs. FREQUENCY @ +25°C



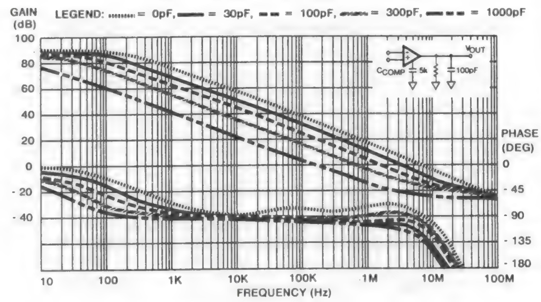
OPEN LOOP GAIN AND PHASE RESPONSE vs. FREQUENCY



OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE
$T_{AMBIENT} = +25^oC$

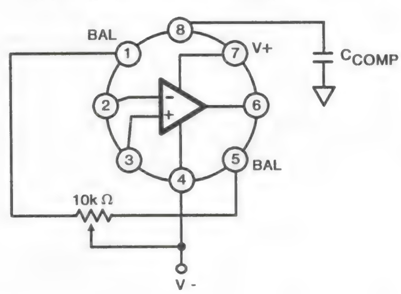


OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS AT COMPENSATION PIN TO GROUND



NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired. If external compensation is used, also connect 30pF to 100pF capacitor from output to ground to act as a high frequency filter. This value may be tailored (or omitted) to help insure stability.

SUGGESTED OFFSET VOLTAGE ADJUSTMENT AND COMPENSATION CONNECTION



Tested Offset Adjustment is $|V_{OS} + 1mV|$ Minimum Referred to Output.
Typical Range is ±20mV for $R_T = 10k\Omega$

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±40V, R_L = 5kΩ, C_L = 50pF, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage	V_{CM} = 0V	+25°C	2	Table 1	mV
Average Offset Voltage Drift	Versus Temperature	Full	15	20	μV/°C
Bias Current	V_{CM} = 0V	+25°C	1	Table 1	nA
Input Noise Voltage Density	f_O = 10Hz	+25°C	30	60	$nV/\sqrt{Hz}$
	f_O = 100Hz	+25°C	20	40	$nV/\sqrt{Hz}$
	f_O = 1kHz	+25°C	16	30	$nV/\sqrt{Hz}$
Input Noise Current Density	f_O = 10Hz	+25°C	0.8	2	$pA/\sqrt{Hz}$
	f_O = 100Hz	+25°C	0.25	0.8	$pA/\sqrt{Hz}$
	f_O = 1kHz	+25°C	0.18	0.4	$pA/\sqrt{Hz}$
Large Signal Voltage Gain	R_L = 5kΩ	+25°C	2	Table 1	MV/V
CMRR	ΔV_{CM} = ±20V	+25°C	110	Table 1	dB
PSRR	ΔV_{SUPPLY} = ±30V	+25°C	110	Table 1	dB
Unity Gain Bandwidth	V_{OUT} = 100mV	+25°C	6	5	MHz
Gain Bandwidth Product	f_O = 10kHz	+25°C	7	5	MHz
	f_O = 1MHz	+25°C	6	5	MHz
Phase Margin	Open Loop, 0dB Crossing	+25°C	60	45	Degrees

HA-4741/883

January 1989

Quad Operational Amplifier

Features

- This Circuit Is Processed in Accordance to Mil-Std-883 and Is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Slew Rate .... 0.9V/μs (Min)
- Bandwidth .... 2.5MHz (Min)
- Input Offset Voltage .... 3mV (Max)
- Input Bias Current .... 200nA (Max)
- Input Voltage Noise .... $9nV/\sqrt{Hz}$ (Typ)
- No Crossover Distortion
- Standard Quad Pinout

Applications

- Universal Active Filters
- D3 Communications Filters
- Audio Ampliers
- Battery-Powered Equipment

Description

The Harris HA-4741/883, which contains four amplifiers on a monolithic chip, provides a new measure of performance for general purpose operational amplifiers. Each amplifier in the HA-4741/883 operating specifications that equal or exceed those of the 741-type amplifier in all categories of performance.

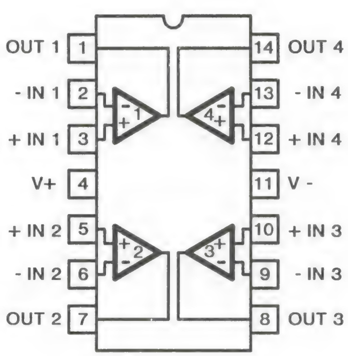
The HA-4741/883 is well suited to applications requiring accurate signal processing by virtue of its low values of input offset voltage (3mV max), input bias current (200nA max) and input voltage noise ($9nV/\sqrt{Hz}$ typ @1kHz). The 2.5MHz bandwidth, coupled with high open loop gain, allow the HA-4741/883 to be used in designs requiring amplifiers of wide band signals, such as audio amplifiers. Audio application is further enhanced by the HA-4741/883's negligible output crossover distortion. These excellent dynamic characteristics also make the HA-4741/883 ideal for a wide range of active filter designs. Performance integrity of multi-channel designs is assured by a high level of amplifier-to-amplifier isolation (90dB @ 10kHz).

A wide range of supply voltages (±2V to ±20V) can be used to power the HA-4741/883, making it compatible with almost any system including battery-powered equipment.

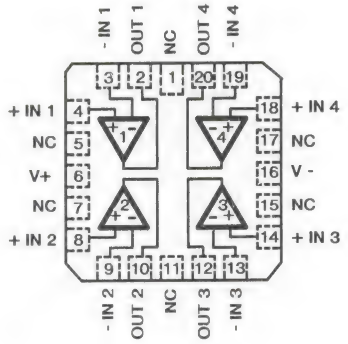
The HA-4741/883 is available in a 20 pin Ceramic LCC package as well as the 14 pin Ceramic DIP. The HA-4741/883 operates from -55°C to +125°C.

Pinouts

HA1-4741/883 (CERAMIC DIP)
TOP VIEW



HA4-4741/883 (CERAMIC LCC)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage 15V
Voltage at Either Input Terminal .... V+ to V-
Output Current .... Indefinite (One Amplifier Shorted to GND)
Junction Temperature (T_J) .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... <2000V
Lead Temperature (Soldering 10 sec) .... +275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	87°C/W	23°C/W
Ceramic LCC Package	85°C/W	26°C/W

Package Power Dissipation Limit at +75°C for $T_J \leq$ +175°C
Ceramic DIP Package 1.15W
Ceramic LCC Package 1.18W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 11.5mW/°C
Ceramic LCC Package .... 11.8mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±5V to ± 15V
$V_{INcm} \leq 1/2$ (V+ - V-)
$R_L \geq 2k\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	V_{CM} = 0V	1	+25°C	-3	3	mV
			2, 3	+125°C, -55°C	-5	5	mV
Input Bias Current	$+I_B$	V_{CM} = 0V $+R_S$ = 10kΩ $-R_S$ = 100Ω	1	+25°C	-200	200	nA
			2, 3	+125°C, -55°C	-325	325	nA
	$-I_B$	V_{CM} = 0V $+R_S$ = 100Ω $-R_S$ = 10kΩ	1	+25°C	-200	200	nA
			2, 3	+125°C, -55°C	-325	325	nA
Input Offset Current	I_{IO}	V_{CM} = 0V $+R_S$ = 10kΩ $-R_S$ = 10kΩ	1	+25°C	-30	30	nA
			2, 3	+125°C, -55°C	-75	75	nA
Common Mode Range	+CMR	V+ = 3V V- = -27V	1	+25°C	12	-	V
			2, 3	+125°C, -55°C	12	-	V
	-CMR	V+ = 27V V- = -3V	1	+25°C	-	-12	V
			2, 3	+125°C, -55°C	-	-12	V
Large Signal Voltage Gain	$+A_{VOL}$	V_{OUT} = 0V and +10V R_L = 2kΩ	4	+25°C	50	-	kV/V
			5, 6	+125°C, -55°C	25	-	kV/V
	$-A_{VOL}$	V_{OUT} = 0V and -10V R_L = 2kΩ	4	+25°C	50	-	kV/V
			5, 6	+125°C, -55°C	25	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔV_{CM} = -10V +V = +5V -V = -25V V_{OUT} = -10V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	74	-	dB
	-CMRR	ΔV_{CM} = +10V +V = +25V -V = -5V V_{OUT} = +10V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	74	-	dB

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

3
OP AMPs & COMPARATORS

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Voltage Swing	$+V_{OUT1}$	R_L = 10kΩ	4	+25°C	12	-	V
			5, 6	+125°C, -55°C	12	-	V
	$-V_{OUT1}$	R_L = 10kΩ	4	+25°C	-	-12	V
			5, 6	+125°C, -55°C	-	-12	V
	$+V_{OUT2}$	R_L = 2kΩ	4	+25°C	10	-	V
			5, 6	+125°C, -55°C	10	-	V
	$-V_{OUT2}$	R_L = 2kΩ	4	+25°C	-	-10	V
			5, 6	+125°C, -55°C	-	-10	V
Output Current	$+I_{OUT}$	V_{OUT} = -10V	4	+25°C	5	-	mA
			5, 6	+125°C, -55°C	5	-	mA
	$-I_{OUT}$	V_{OUT} = +10V	4	+25°C	-	-5	mA
			5, 6	+125°C, -55°C	-	-5	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-	5	mA
			2, 3	+125°C, -55°C	-	7	mA
	$-I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-5	-	mA
			2, 3	+125°C, -55°C	-7	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = +5V +V = +10V, -V = -15V +V = +20V, -V = -15V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	-PSRR	ΔV_{SUP} = -5V +V = +15V, -V = -10V +V = +15V, -V = -20V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_{VCL} = +1V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Slew Rate	+SR	V_{OUT} = -5V to +5V	7	+25°C	0.9	-	V/µs
	-SR	V_{OUT} = +5V to -5V	7	+25°C	0.9	-	V/µs
Rise & Fall Time	T_R	V_{OUT} = 0 to +200mV 10% ≤ T_R ≤ 90%	7	+25°C	-	140	ns
	T_F	V_{OUT} = 0 to -200mV 10% ≤ T_F ≤ 90%	7	+25°C	-	140	ns
Overshoot	+OS	V_{OUT} = 0 to +200mV	7	+25°C	-	40	%
	-OS	V_{OUT} = 0 to -200mV	7	+25°C	-	40	%
Gain Bandwidth Product (Small Signal)	GBWP	V_{OUT} = 50mV	7	+25°C	2.5	-	MHz

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Differential Input Resistance	R_{IN}	V_{CM} = 0V	1	+25°C	260	-	kΩ
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	+25°C	14	-	kHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 2kΩ, C_L = 50pF	1	-55°C to +125°C	1	-	V/V
Output Resistance	R_{OUT}	Open Loop	1	+25°C	-	350	Ω
Quiescent Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	180	mW
Channel Separation	CS	f = 10kHz, R_S = 1kΩ Referred to Input A_V = 100V/V	1	+25°C	-90	-	dB

NOTES: 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).

3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)

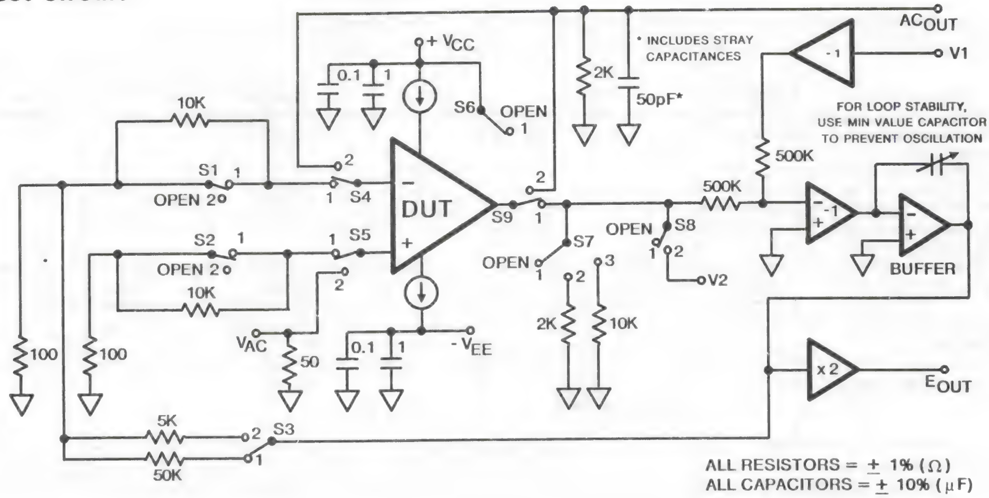
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6, 7
Group A Test Requirements	1, 2, 3, 4, 5, 6, 7
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

The Subgroup assignments of the parameters in these tables were patterned after Mil-M-38510/110.

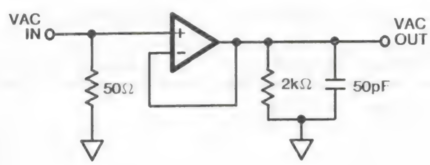
Test Circuit



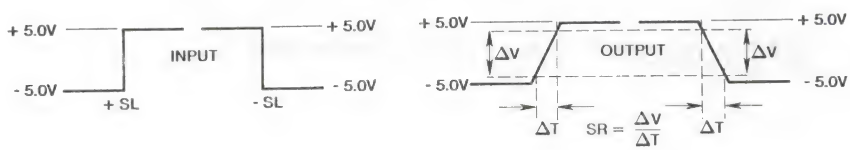
One of the Four Loops. For Detailed Information, Refer to HA-4741/883 Test Tech Brief.

Test Waveforms

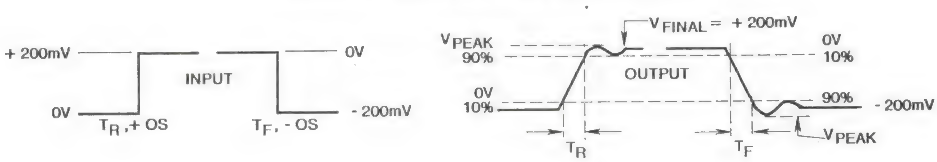
SIMPLIFIED TEST CIRCUIT



SLEW RATE WAVEFORMS

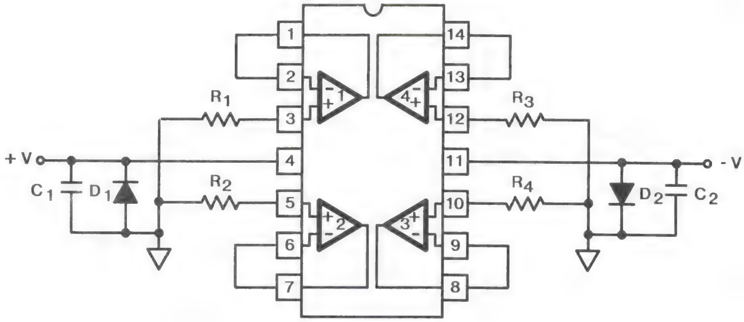


OVERSHOOT, RISE & FALL TIME WAVEFORMS

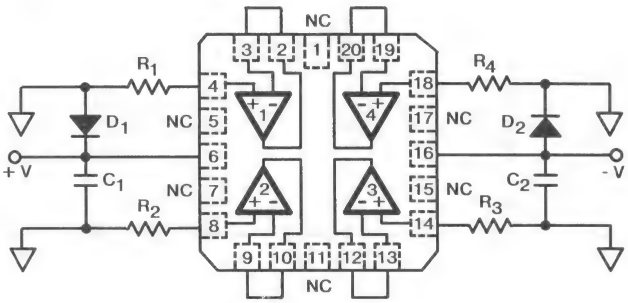


Burn-In Circuits

HA1-4741/883 CERAMIC DIP



HA4-4741/883 CERAMIC LCC

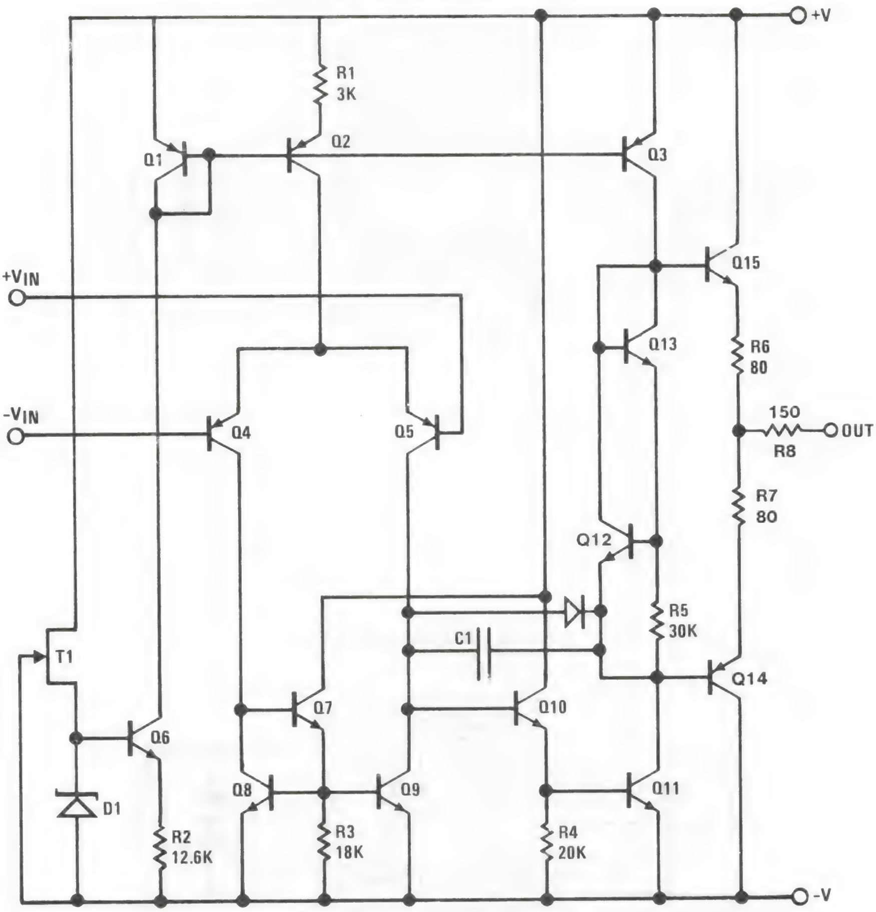


NOTES:

$R_1 = R_2 = R_3 = R_4 = 1M\Omega$, ±5%, 1/4W (Min)
$C_1 = C_2 = 0.01\mu F$/Socket (Min) or $0.1\mu F$/Row (Min)
$D_1 = D_2$ = IN4002 or Equivalent/Board
$|(V+) - (V-)| = 30V$

3 OP AMPs & COMPARATORS

Schematic Diagram (¼ HA-4741/883)



Die Characteristics

DIE DIMENSIONS:
87 x 75 x 19 mils
(2210 x 1910 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
1.68×10^5 A/cm^2

SUBSTRATE POTENTIAL (Powered Up): V-

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

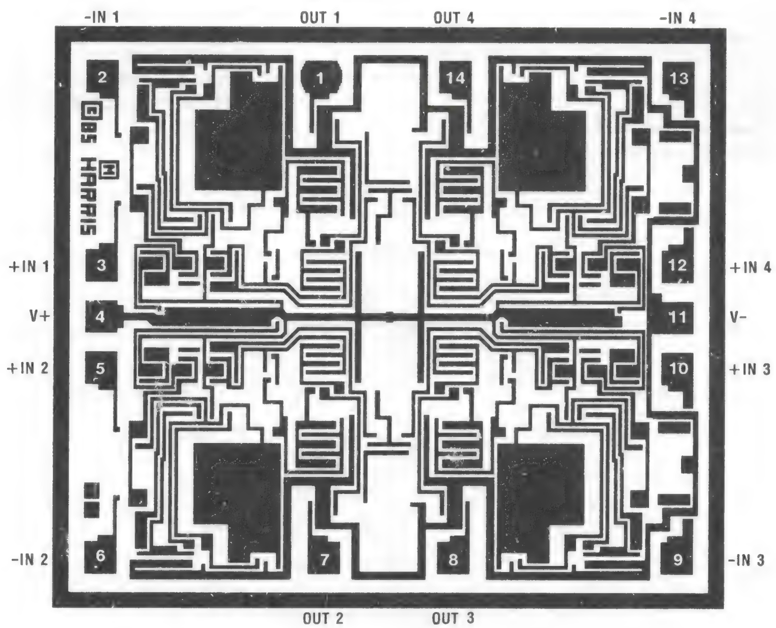
TRANSISTOR COUNT: 72

PROCESS: Junction Isolated Bipolar/JFET

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

Metallization Mask Layout

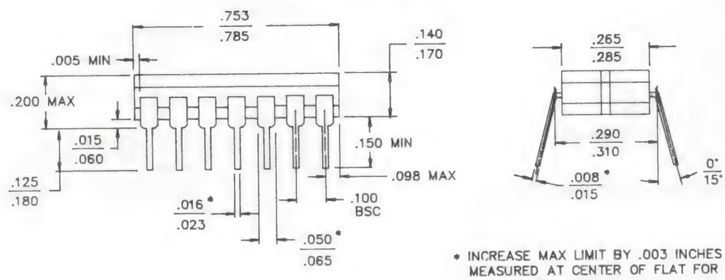
HA-4741/883



NOTE: Pin Numbers Correspond to Ceramic DIP Package Only.

Packaging†

14 PIN CERAMIC DIP

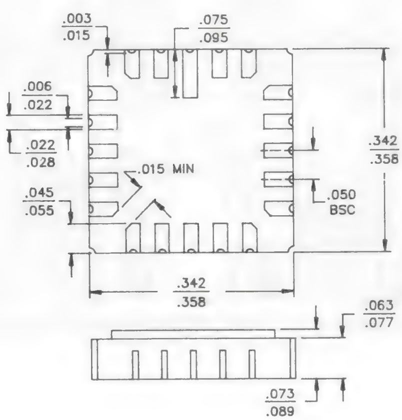


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-1

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

HA-4741

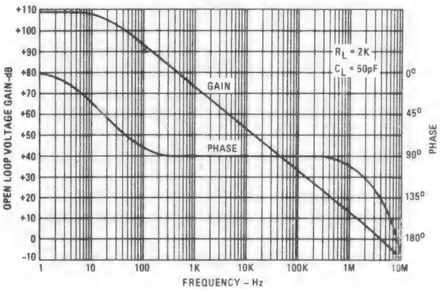
DESIGN INFORMATION

Quad Operational Amplifier

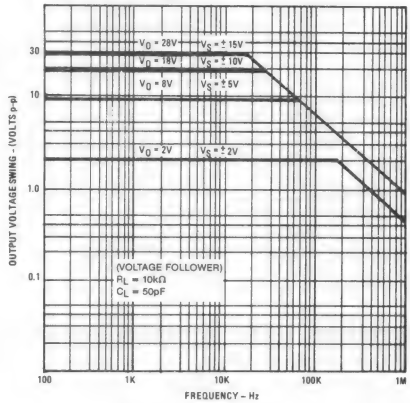
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

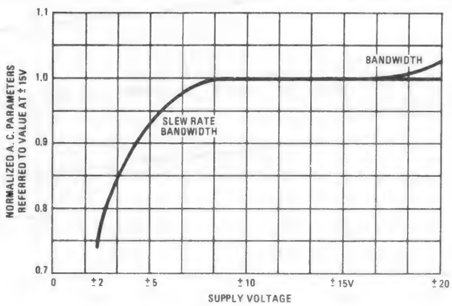
OPEN LOOP FREQUENCY RESPONSE



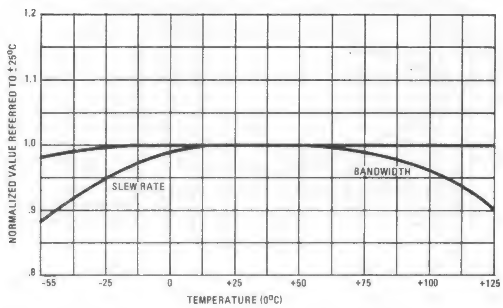
OUTPUT VOLTAGE SWING vs. FREQUENCY



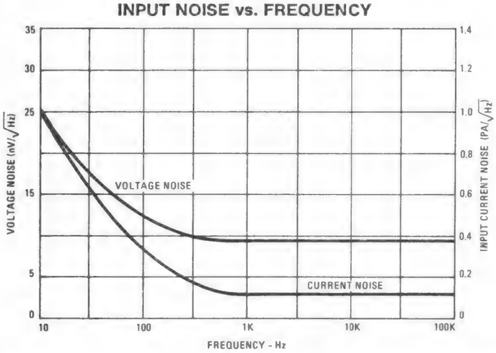
NORMALIZED A.C. PARAMETERS vs. SUPPLY VOLTAGE



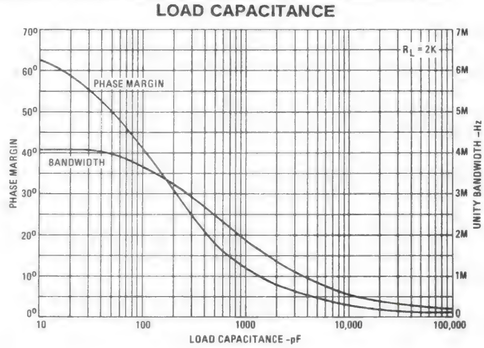
NORMALIZED A.C. PARAMETERS vs. TEMPERATURE



INPUT NOISE vs. FREQUENCY



SMALL SIGNAL BANDWIDTH AND PHASE MARGIN vs. LOAD CAPACITANCE



3

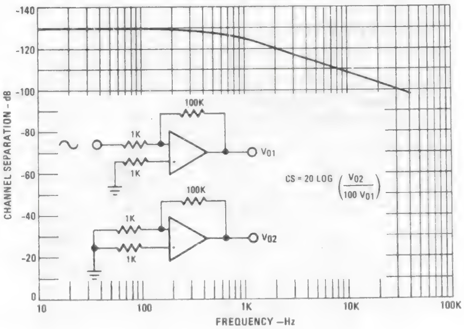
OP AMPs & COMPARATORS

DESIGN INFORMATION (Continued)

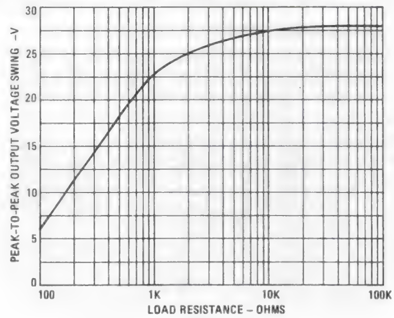
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

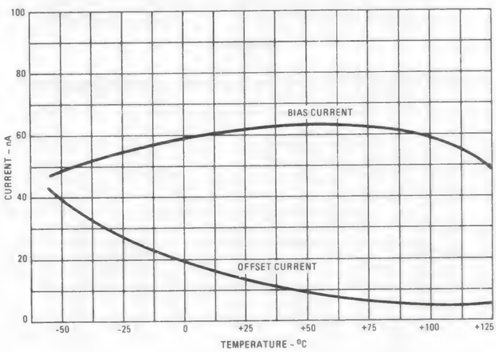
CHANNEL SEPARATION vs. FREQUENCY



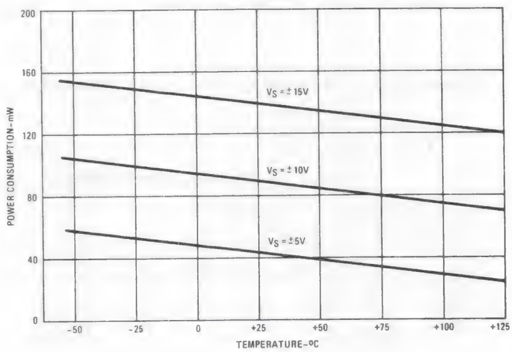
MAXIMUM OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



POWER CONSUMPTION vs. TEMPERATURE



DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_L = 2kΩ, C_L = 50pF, A_V = +1 V/V, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage	V_{CM} = 0V	+25°C	1	Table 1	mV
Average Offset Voltage Drift	Versus Temperature	Full	5	10	µV/°C
Bias Current	V_{CM} = 0V	+25°C	50	Table 1	nA
Offset Current	V_{CM} = 0V	+25°C	2	Table 1	nA
Differential Input Resistance		+25°C	800	Table 3	kΩ
Input Noise Voltage Density	$f_o \geq$ 1kHz	+25°C	9	15	$nV/\sqrt{Hz}$
Input Noise Current Density	$f_o \geq$ 1kHz	+25°C	0.1	0.2	$pA/\sqrt{Hz}$
Large Signal Voltage Gain	V_o = ±10V	+25°C	200	Table 1	kV/V
Common Mode Rejection Ratio	ΔV_{CM} = 10V	+25°C	95	Table 1	dB
Channel Separation	$f_o \geq$ 10kHz, R_S = 1kΩ	+25°C	108	Table 3	dB
Small Signal Bandwidth	$V_{OUT} \leq$ 100mV	+25°C	4	Table 2	MHz
Output Voltage Swing	R_L = 10kΩ	+25°C	±13.7	Table 1	V
	R_L = 2kΩ	+25°C	±12.5	Table 1	V
Full Power Bandwidth	V_{PEAK} = 10V, Note 2	+25°C	25	Table 3	kHz
Output Current	V_{OUT} = ±10V	Full	±15	Table 1	mA
Output Resistance	Open Loop	+25°C	300	Table 3	Ω
Rise/Fall Time	V_{OUT} = +200mV, -200mV	+25°C	120	Table 2	nS
		Full	130	150	nS
Overshoot	V_{OUT} = +200mV, -200mV	+25°C	10	Table 2	%
		Full	15	40	%
Slew Rate	V_{OUT} = ±5V	+25°C	1.6	Table 2	V/µS
		Full	1.3	0.9	V/µS
Quiescent Supply Current	No Load	+25°C	4	Table 1	mA
		Full	5	Table 1	mA
Power Supply Rejection Ratio	ΔV_{SUP} = ±5V	Full	95	Table 1	dB
Minimum Supply Voltage	Functional Operation Only. Other Parameters will vary.	+25°C	±2	±5	V

HARRIS HA-4902/883

January 1989

Precision Quad Comparator

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Fast Response Time (+25°C) .... 215ns (Max) 180ns (Typ)
- Low Offset Voltage (+25°C) .... 5mV (Max) 2mV (Typ)
- Low Input Sensitivity .... 0.5mV (Max) 0.05mV (Typ)
- Low Offset Current (+25°C) .... 35nA (Max) 10nA (Typ)
- Single or Dual-Voltage Supply Operation
- Selectable Output Logic Levels
- Active Pull-Up/Pull-Down Output Circuit — No External Resistors Required

Applications

- Threshold Detector
- Zero-Crossing Detector
- Window Detector
- Analog Interfaces for Microprocessors
- High Stability Oscillators
- Logic System Interface

Description

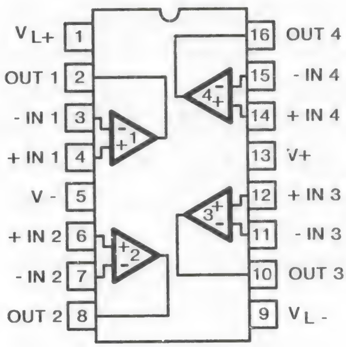
The HA-4902/883 is a monolithic, quad, precision comparator offering fast response time, low offset voltage, low offset current, and virtually no channel-to-channel crosstalk for applications requiring accurate, high speed, signal level detection. This comparator can sense signals at ground level while being operated from either single +5V supply (digital systems) or from dual supplies (analog networks) up to ±15V. The HA-4902/883 contains a unique current driven output stage which can be connected to logic system supplies ($V_{LOGIC}+$ and $V_{LOGIC}-$) to make the output levels directly compatible (no external components needed) with any standard logic or special system logic levels. In combination analog/digital systems, the design employed in the HA-4902/883 input and output stages prevents troublesome ground coupling of signals between analog and digital portions of the system.

This comparator's combination of features makes it an ideal component for signal detection and processing in data acquisition systems, test equipment, and microprocessor/analog signal interface network.

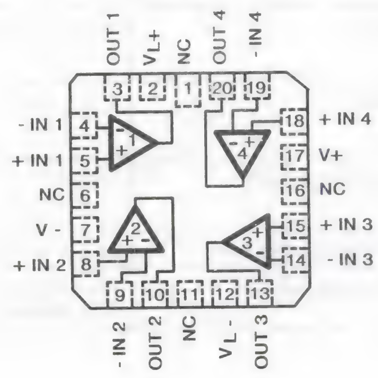
The HA-4902/883 is available in a 16 pin Ceramic DIP package and in a 20 pin Ceramic LCC package and is specified over the military, -55°C to +125°C, temperature range.

Pinouts

HA1-4902/883 (CERAMIC DIP)
TOP VIEW



HA4-4902/883 (CERAMIC LCC)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 33V
Differential Input Voltage ....±15V
Peak Output Current ....±50mA
Output Short Circuit Current Duration .... Indefinite
(One Amplifier Shorted to GND)
Junction Temperature .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating ....< 2000V
Lead Temperature (Soldering 10 sec) .... +275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	76°C/W	17°C/W
Ceramic LCC Package	76°C/W	19°C/W

Package Power Dissipation at +75°C
Ceramic DIP Package 1.31W
Ceramic LCC Package 1.32W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 13.1mW/°C
Ceramic LCC Package .... 13.1mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage ....±15V
Logic Supply Voltage (V_L+) ....+5V
Logic Reference Voltage (V_L−) 0V

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, V_L = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	V_{CM} = 0V, V_{OUT} = 1.4V See Note 3	1	+25°C	-5	5	mV
			2, 3	+125°C, -55°C	-8	8	mV
Input Bias Current	$+I_B$	V_{CM} = 0V	1	+25°C	-150	150	nA
			2, 3	+125°C, -55°C	-200	200	nA
	$-I_B$	V_{CM} = 0V	1	+25°C	-150	150	nA
			2, 3	+125°C, -55°C	-200	200	nA
Input Offset Current	I_{IO}	V_{CM} = 0V	1	+25°C	-35	35	nA
			2, 3	+125°C, -55°C	-45	45	nA
Input Sensitivity	IN_{SEN}	See Note 3	1	+25°C	-0.5	0.5	mV
			2, 3	+125°C, -55°C	-0.6	0.6	mV
Output Voltage Levels	V_{OL}	I_{SINK} = 3mA	1	+25°C	-	0.4	V
			2, 3	+125°C, -55°C	-	0.4	V
	V_{OH}	I_{SOURCE} = 3mA	1	+25°C	3.5	-	V
			2, 3	+125°C, -55°C	3.5	-	V
Output Current	I_{SINK}	$V_{OUT} \leq 0.4V$	1	+25°C	3	-	mA
			2, 3	+125°C, -55°C	3	-	mA
	I_{SOURCE}	$V_{OUT} \geq 3.5V$	1	+25°C	-	-3	mA
			2, 3	+125°C, -55°C	-	-3	mA
Supply Current	$+I_{CC}$	$V_{OUT} = V_{OL}, V_{OH}$	1	+25°C	-	20	mA
			2, 3	+125°C, -55°C	-	20	mA
	$-I_{CC}$	$V_{OUT} = V_{OL}, V_{OH}$	1	+25°C	-	8	mA
			2, 3	+125°C, -55°C	-	10	mA
Logic Current	I_L	$V_{OUT} = V_{OL}, V_{OH}$	1	+25°C	-	6	mA
			2, 3	+125°C, -55°C	-	8	mA

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Table 2 Intentionally Left Blank. See A.C. Specifications on Table 3.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, V_L = GND, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Response Time	t_{pd0}	+100mV Input Step, 10mV Overdrive	1, 2	+25^{o}C	-	200	ns
	t_{pd1}	-100mV Input Step, -10mV Overdrive	1, 2	+25^{o}C	-	215	ns
Common Mode Range	+CMR		1	+25^{o}C	-	12.4	V
	-CMR		1	+25^{o}C	-15	-	V

NOTES: 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

2. F ≈ 100Hz, duty cycle ≈ 50%, inverting input driven, all unused inverting inputs tie to +5V.

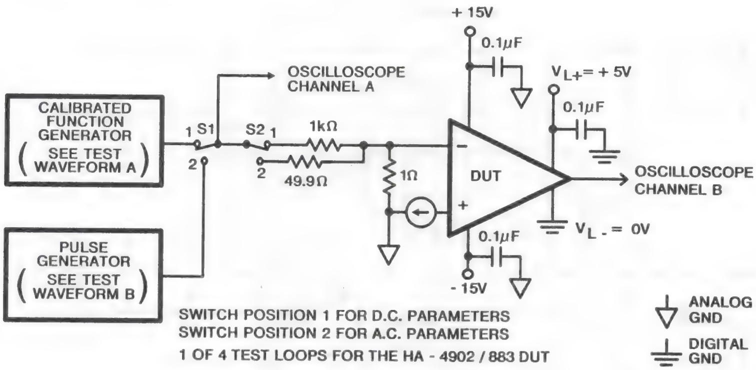
3. Refer to enlarged area of test waveform A. Offset voltage is measured when V_{OUT} = 1.4V. Sensitivity is measured on the transition edge at 0.4V and 3.5V. Sensitivity is the change in differential input voltage required to change the output state. Sensitivity includes the effects of offset voltage, offset current, common mode rejection and voltage gain.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3
Group A Test Requirements	1, 2, 3
Groups C & D Endpoints	1

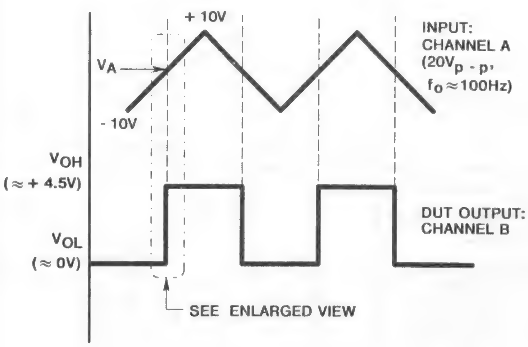
* PDA applies to Subgroup 1 only.

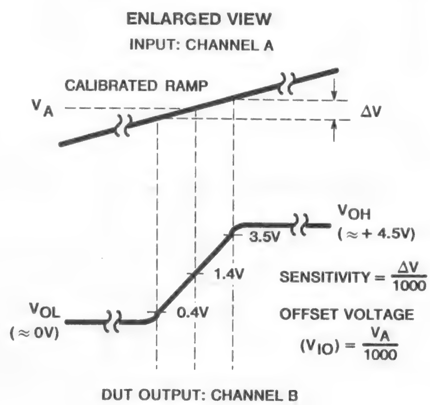
Test Circuit (Applies to Tables 1 and 3)



For Detailed Information, Refer to HA-4902/883 Test Tech Brief

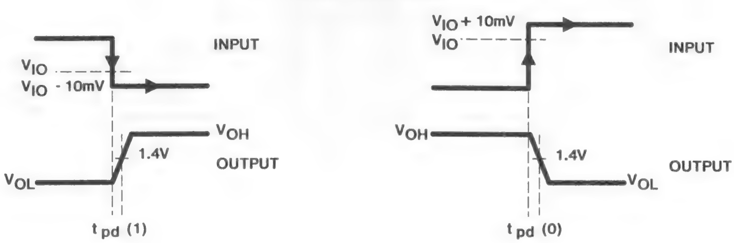
Test Waveform A (Applies to Table 1)





Test Waveform B (Applies to Table 3)

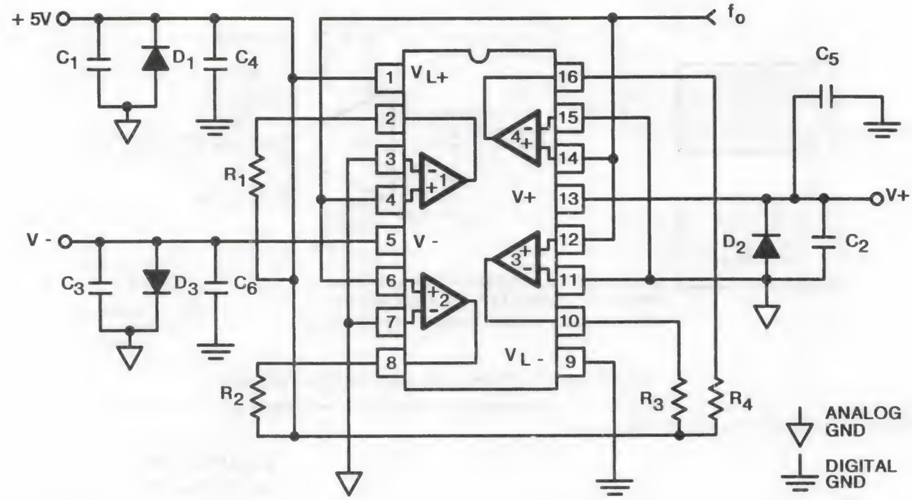
RESPONSE TIME



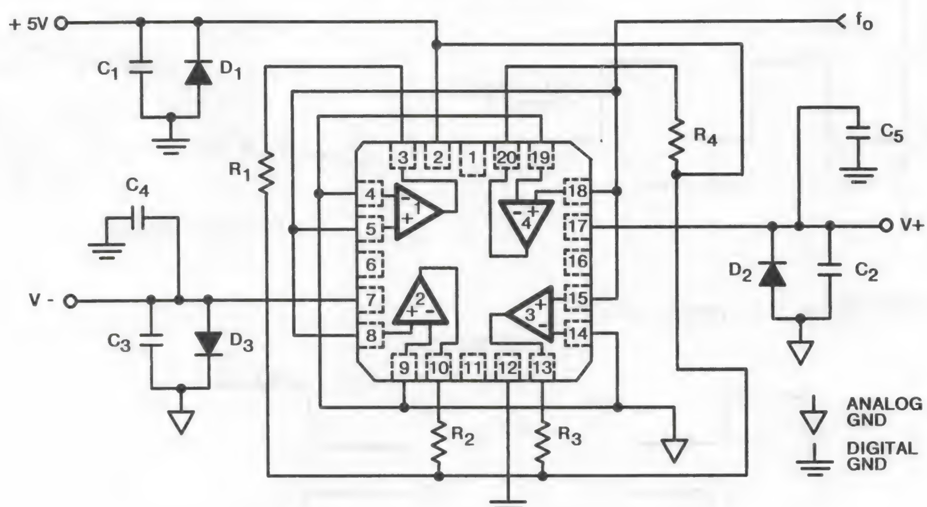
NOTE: Response time testing is done after V_{IO} testing to acquire the actual device offset voltage. 10mV overdrive is then added (or subtracted depending on state) to this measured V_{IO} value.

Burn-In Circuits

HA1-4902/883 CERAMIC DIP



HA4-4902/883 CERAMIC LCC



NOTES:

$R_1 = 5k\Omega, \pm5\%$

$C_1 = C_2 = C_3 = 0.01\mu F$/Socket (Min) or $0.1\mu F$/Row (Min)

$C_4 = C_5 = C_6 = 0.01\mu F$/Socket (Min) or $0.1\mu F$/Row (Min)

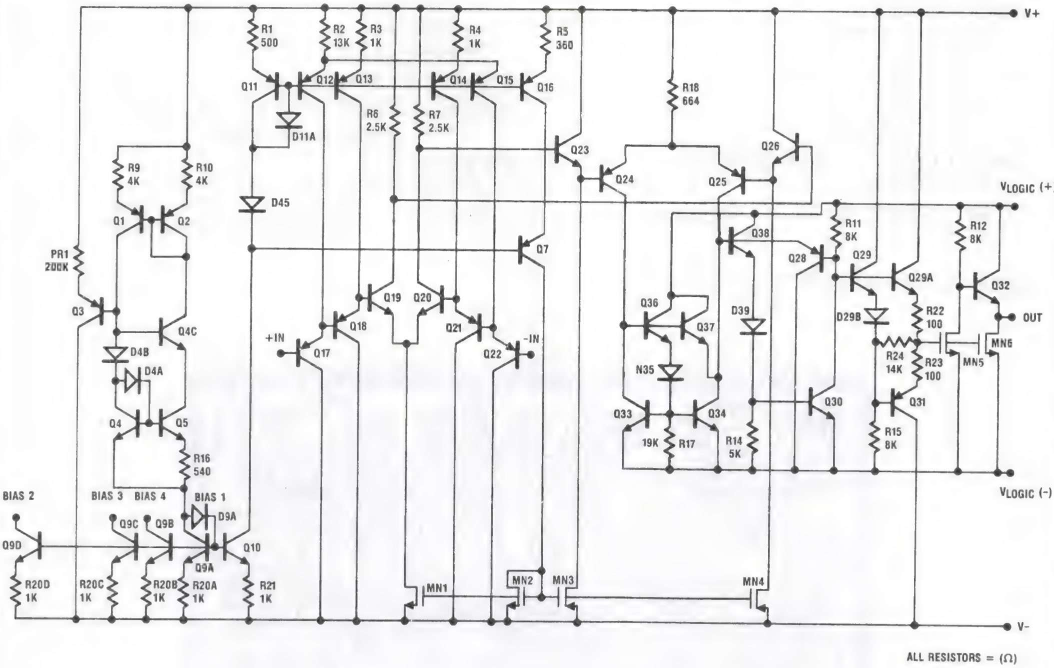
$D_1 = D_2 = D_3$ = IN4002 or Equivalent/Board

$|(V+) - (V-)| = 30V$

$V_L- = 0V$, $V_L+ = 5V$

f_o = 5V (Static Burn-In)

Schematic Diagram (1/4 of HA-4902/883)



Die Characteristics

DIE DIMENSIONS:
95 x 105 x 19 mils
(2420 x 2670 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$0.4 \times 10^5 A/cm^2$

SUBSTRATE POTENTIAL (Powered Up): V-

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

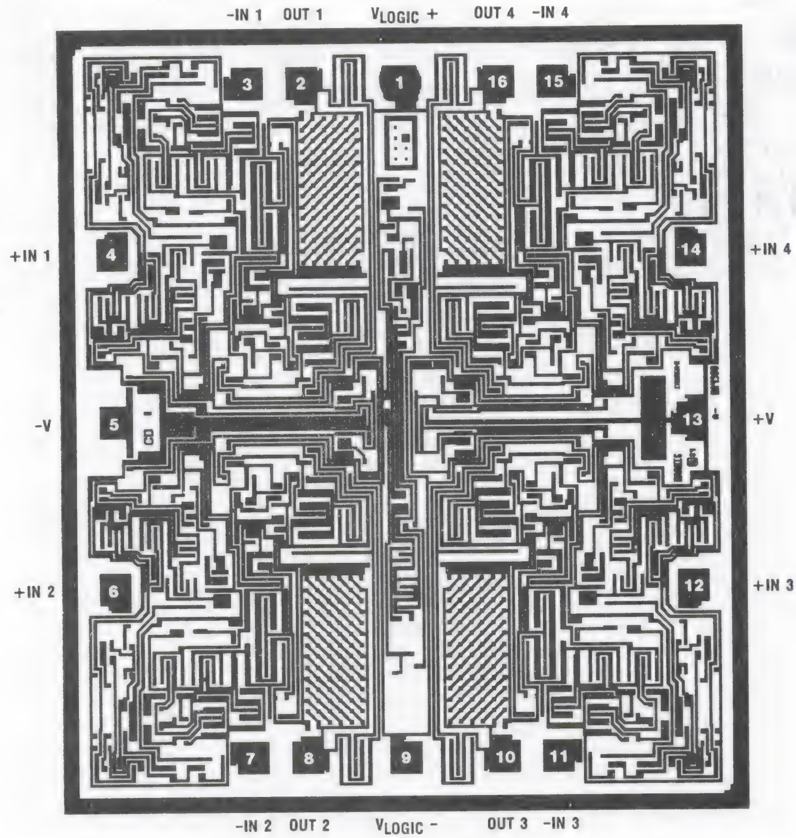
TRANSISTOR COUNT: 137

PROCESS: Combination of Std. Linear and MOS Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

Metallization Mask Layout

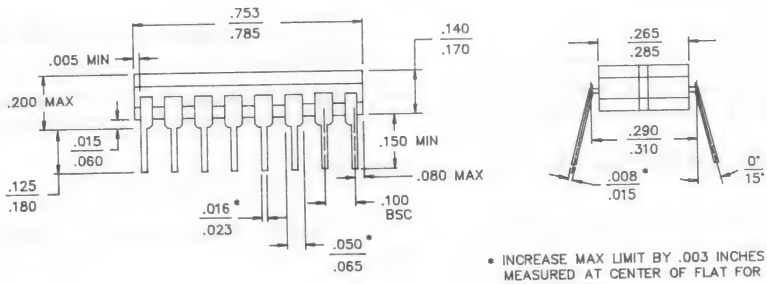
HA-4902/883



NOTE: Bond Pad Numbers Correspond to 16 Pin Ceramic DIP Only.

Packaging†

16 PIN CERAMIC DIP

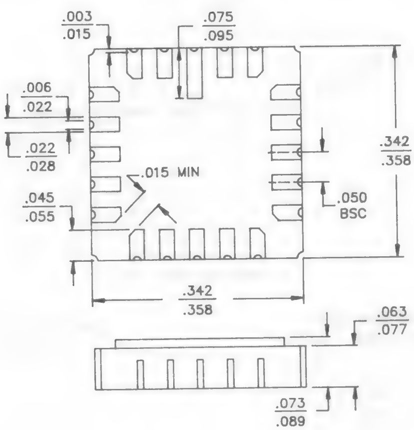


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-2

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

DESIGN INFORMATION

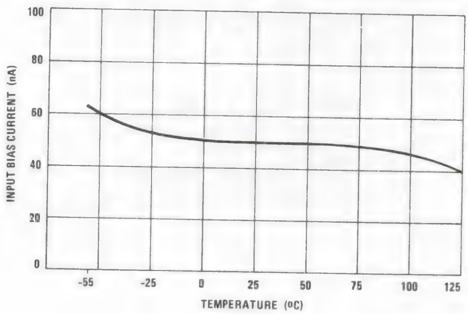
Precision Quad Comparator

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

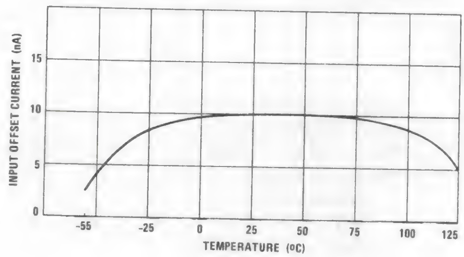
Typical Performance Curves

Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$, $V_{LOGIC}+ = 5V$, $V_{LOGIC}- = 0V$

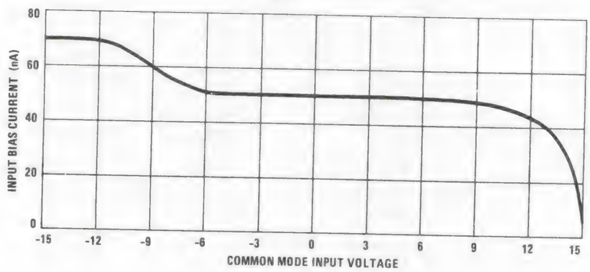
INPUT BIAS CURRENT vs. TEMPERATURE



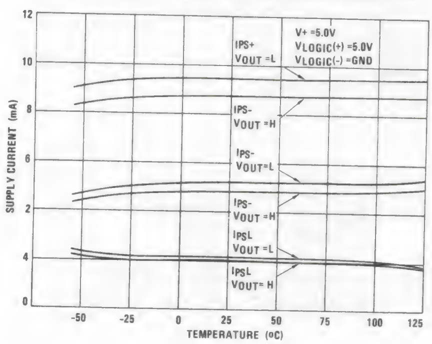
INPUT OFFSET CURRENT vs. TEMPERATURE



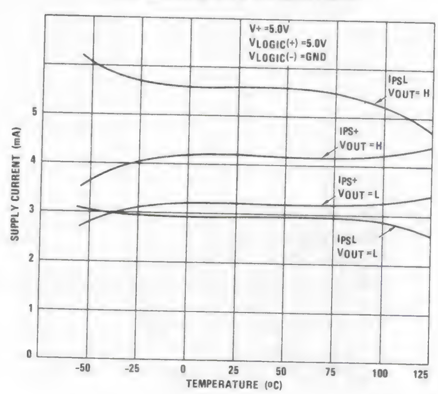
INPUT BIAS CURRENT vs. COMMON MODE INPUT VOLTAGE
($V_{DIFF} = 0V$)



SUPPLY CURRENT vs. TEMPERATURE FOR ±15V SUPPLIES AND +5V LOGIC SUPPLY



SUPPLY CURRENT vs. TEMPERATURE FOR SINGLE +5V OPERATION



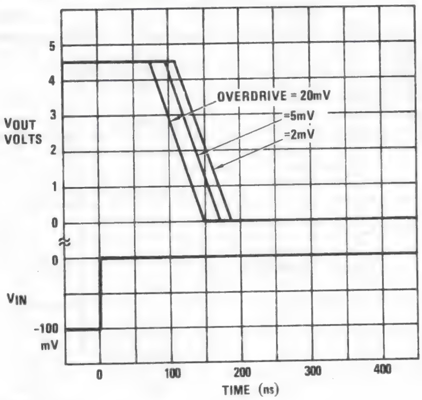
DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

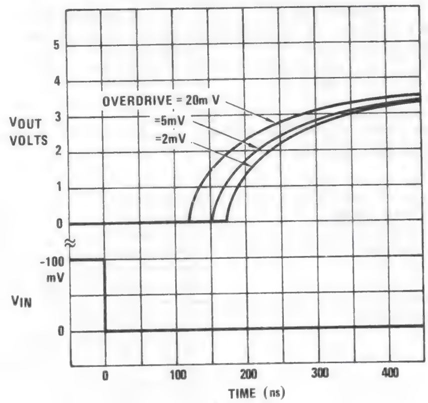
Typical Performance Curves

Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$, $V_{LOGIC}+ = 5V$, $V_{LOGIC}- = 0V$

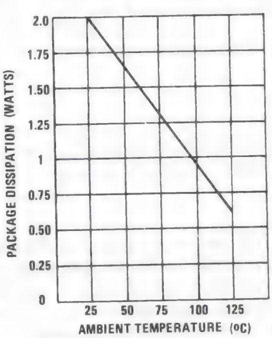
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



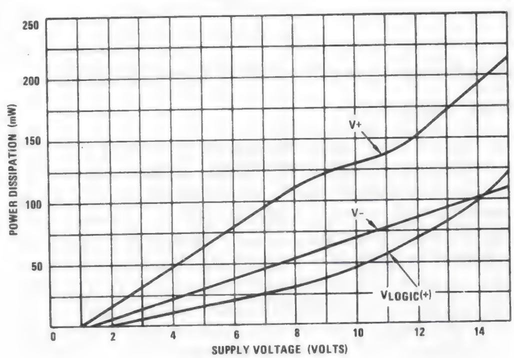
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



MAXIMUM PACKAGE DISSIPATION vs. $T_{AMBIENT}$



MAXIMUM POWER DISSIPATION vs. SUPPLY VOLTAGE
(No Load Condition)



NOTE: Total Power Dissipation (TPD) is the sum of individual dissipation contributions of V+, V- and V_{LOGIC} shown in curves of Power Dissipation vs. Supply Voltages. The calculated TPD is then located on the graph of Maximum Allowable Package Dissipation vs. Ambient Temperature to determine ambient temperature operating limits imposed by the calculated TPD (See Performance Curves). For instance, the combination of ±15V, 5V, 0V (±V, $V_{LOGIC}+$, $V_{LOGIC}-$) gives a TPD of 350mW, the combination ±15V, 0V gives a TPD of 450mW.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, V_L+ = 5V, V_L- = 0V, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage	Note 3	Full	0.5	Table 1	mV
Input Bias Current		+25°C	50	Table 1	nA
		Full	90	Table 1	nA
Input Offset Current		+25°C	10	Table 1	nA
		Full	20	Table 1	nA
Input Sensitivity	Note 3	Full	50	Table 1	µV
Output Level	V_{OL}; I_{SINK} = 3mA	Full	0.15	Table 1	V
	V_{OH}; I_{SOURCE} = 3mA	Full	4.3	Table 1	V
Supply Current	$+I_{CC}$; $V_{OUT} = V_{OH}$	Full	10	Table 1	mA
	$+I_{CC}$; $V_{OUT} = V_{OL}$	Full	15	Table 1	mA
	$-I_{CC}$; $V_{OUT} = V_{OH}$	Full	-6	Table 1	mA
	$-I_{CC}$; $V_{OUT} = V_{OL}$	Full	-8	Table 1	mA
Logic Current	I_L; $V_{OUT} = V_{OH}$	Full	2	Table 1	mA
	I_L; $V_{OUT} = V_{OL}$	Full	4	Table 1	mA
Response Time	t_{pd0}	Full	150	Table 3	ns
	t_{pd1}	Full	150	Table 3	ns

Applying The HA-4902 Comparator

Supply Connections

This device is exceptionally versatile in working with most available power supplies. The voltage applied to the V+ and V- terminals determines the allowable input signal range, while the voltage applied to the V_L+ and V_L- determines the output swing. In systems where dual analog supplies are available, these would be connected to V+ and V-, while the logic supply and return would be connected to V_{LOGIC} + and V_{LOGIC} -. The analog and logic supply commons can be connected together at one point in the system, since the comparator is immune to noise on the logic supply ground. A negative output swing may be obtained by connecting V_L+ to ground and V_L- to a negative supply. Bipolar output swings ($15V_{P-P}$, max.) may be obtained using dual supplies. In systems where only a single logic supply is available (+5V to +15V), V+ and V_{LOGIC} + may be connected together to the positive supply while V- and V_{LOGIC} - are grounded. If an input signal could swing negative with respect to the V- terminal, a resistor should be connected in series with the input to limit input current to < 5mA since the C-B junction of the input transistor would be forward biased.

Unused Inputs

Inputs of unused comparator sections should be tied to a differential voltage source to prevent output "chatter" ($V_{DIFF} \geq V_{IO}$). All unused inverting inputs may be tied to +5V and non-inverting inputs tied to ground.

Crosstalk

Simultaneous high frequency operation of all other channels in the package will not affect the output logic state of a given channel, provided that its differential input voltage is sufficient to define a given logic state ($\Delta V_{IN} \geq \pm V_{IO}$). Low level or high impedance input lines should be shielded from other signal sources to reduce crosstalk and interference.

Power Supply Decoupling

Decouple all power supply lines with 0.01µF ceramic capacitors to a ground line located near the package to reduce coupling between channels or from external sources.

Response Time

Fast rise time (< 200ns) input pulses of several volts amplitude may result in delay times somewhat longer than those illustrated for 100mV steps. Operating speed is optimized by limiting the maximum differential input voltage applied, with resistor-diode clamping networks.

HARRIS HA-5002/883

Monolithic, Wideband, High Slew Rate, High Output Current Buffer

January 1989

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Voltage Gain ($R_L = 1k\Omega$) .... 0.99 (Min)**
  0.995 (Typ)
  ($R_L = 100\Omega$) .... 0.96 (Min)
  0.971 (Typ)
- **High Input Impedance .... 1.5MΩ(Min)**
  3MΩ(Typ)
- **Low Output Impedance .... 10Ω (Max)**
  3Ω(Typ)
- **Very High Slew Rate .... 1V/ns (Min)**
  1.3V/ns (Typ)
- **Wide Small Signal Bandwidth .... 110MHz (Typ)**
- **High Output Current.................... 100mA (Min)**
- **High Pulsed Output Current .... 400mA (Max)**
- **Monolithic Dielectric Isolation Construction**
- **Replaces Hybrid LH0002**

Applications

- **Line Driver**
- **Data Acquistion**
- **110 MHz Buffer**
- **High Power Current Booster**
- **High Power Current Source**
- **Sample and Holds**
- **Radar Cable Driver**
- **Video Products**

Description

The HA-5002/883 is a monolithic, wideband, high slew rate, high output current, buffer amplifier.

Utilizing the advantages of the Harris Dielectric Isolation technologies, the HA-5002/883 current buffer offers 1300V/μsec slew rate typically and 1000V/μS minimum with 110 MHz of bandwidth. The ±100mA minimum output current capability is enhanced by a 3Ω output impedance.

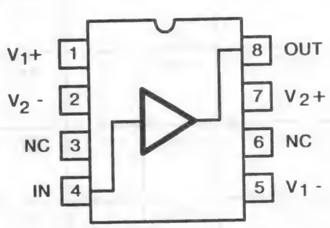
The monolithic HA-5002/883 will replace the hybrid LH0002 with corresponding performance increases. These characteristics range from the 3MΩ (typ) input impedance to the increased output voltage swing. Monolithic design technologies have allowed a more precise buffer to be developed with more than an order of magnitude smaller gain error. The voltage gain is 0.99 guaranteed minimum with a 1kΩ load and 0.96 minimum with a 100Ω load.

The HA-5002/883 will provide many present hybrid users with a higher degree of reliability and at the same time increase overall circuit performance.

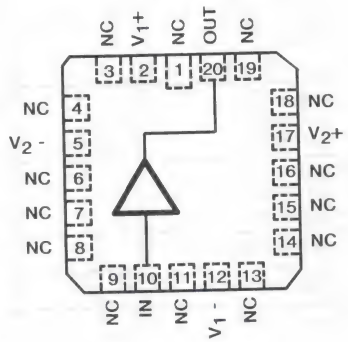
The HA-5002/883 is available in 8-pin Ceramic Mini-DIP, 8-pin Metal Can, and 20-pin Ceramic LCC packages. The HA-5002/883 is specified over the full -55°C to +125°C military temperature range.

Pinouts

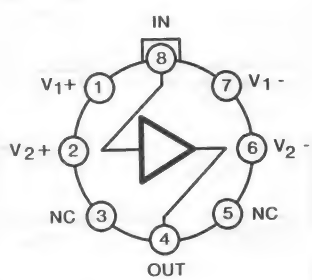
HA7-5002/883 (CERAMIC MINI-DIP)
TOP VIEW



HA4-5002/883 (CERAMIC LCC)
TOP VIEW



HA2-5002/883 (METAL CAN)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 44V
Input Voltage .... Equal to Supplies
Peak Output Current (50ms On, 1s Off) .... ±400mA
Continuous Output Current .... $200mA_{RMS}$
Junction Temperature .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... <2000V
Lead Temperature (Soldering 10 sec) .... 275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	82°C/W	26°C/W
Ceramic LCC Package	74°C/W	20°C/W
Metal Can Package	101°C/W	30°C/W

Package Power Dissipation Limit at +75°C for TJ ≤ 175°C
Ceramic DIP Package 0.82W
Ceramic LCC Package 1.36W
Metal Can Package 1W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 8.2mW/°C
Ceramic LCC Package .... 13.6mW/°C
Metal Can Package .... 10mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±12V to ±15V
$R_L \geq 100\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±12V and ±15V, $R_{SOURCE} = 50\Omega$, $C_{LOAD} \leq 10pF$, $V_{IN} = 0V$, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO1}	$V_{SUP} = \pm12V$	1	+25°C	-20	20	mV
			2, 3	+125°C, -55°C	-30	30	mV
	V_{IO2}	$V_{SUP} = \pm15V$	1	+25°C	-20	20	mV
			2, 3	+125°C, -55°C	-30	30	mV
Input Bias Current	$+I_{B1}$	$V_{SUP} = \pm15V$, $R_S = 1k\Omega$	1	+25°C	-7	7	µA
			2, 3	+125°C, -55°C	-10	10	µA
	$+I_{B2}$	$V_{SUP} = \pm12V$, $R_S = 1k\Omega$	1	+25°C	-7	7	µA
			2, 3	+125°C, -55°C	-10	10	µA
Voltage Gain 1	$+A_{V1}$	$V_{SUP} = \pm12V$, $R_L = 1k\Omega$, $V_{IN} = 10V$	1	+25°C	0.99	-	V/V
			2, 3	+125°C, -55°C	0.99	-	V/V
	$-A_{V1}$	$V_{SUP} = \pm12V$, $R_L = 1k\Omega$, $V_{IN} = -10V$	1	+25°C	0.99	-	V/V
			2, 3	+125°C, -55°C	0.99	-	V/V
Voltage Gain 2	$+A_{V2}$	$V_{SUP} = \pm12V$, $R_L = 100\Omega$, $V_{IN} = 10V$	1	+25°C	0.96	-	V/V
	$-A_{V2}$	$V_{SUP} = \pm12V$, $R_L = 100\Omega$, $V_{IN} = -10V$	1	+25°C	0.96	-	V/V
Voltage Gain 3	$+A_{V3}$	$V_{SUP} = \pm15V$, $R_L = 100\Omega$, $V_{IN} = 10V$	1	+25°C	0.96	-	V/V
	$-A_{V3}$	$V_{SUP} = \pm15V$, $R_L = 100\Omega$, $V_{IN} = -10V$	1	+25°C	0.96	-	V/V
Voltage Gain 4	$+A_{V4}$	$V_{SUP} = \pm15V$, $R_L = 1k\Omega$, $V_{IN} = 10V$	1	+25°C	0.99	-	V/V
			2, 3	+125°C, -55°C	0.99	-	V/V
	$-A_{V4}$	$V_{SUP} = \pm15V$, $R_L = 1k\Omega$, $V_{IN} = -10V$	1	+25°C	0.99	-	V/V
			2, 3	+125°C, -55°C	0.99	-	V/V

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±12V and ±15V, $R_{SOURCE} = 50\Omega$, $C_{LOAD} \leq 10pF$, $V_{OUT} = 0V$, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Voltage Swing	$+V_{OUT1}$	$V_{SUP} = \pm15V$, $R_L = 100\Omega$, $V_{IN} = 15V$	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	$-V_{OUT1}$	$V_{SUP} = \pm15V$, $R_L = 100\Omega$, $V_{IN} = -15V$	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
	$+V_{OUT2}$	$V_{SUP} = \pm15V$, $R_L = 1k\Omega$, $V_{IN} = 15V$	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	$-V_{OUT2}$	$V_{SUP} = \pm15V$, $R_L = 1k\Omega$, $V_{IN} = -15V$	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
	$+V_{OUT3}$	$V_{SUP} = \pm12V$, $R_L = 1k\Omega$, $V_{IN} = 12V$	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	$-V_{OUT3}$	$V_{SUP} = \pm12V$, $R_L = 1k\Omega$, $V_{IN} = -12V$	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
Output Current	$+I_{OUT1}$	$V_{SUP} = \pm15V$, $V_{OUT} = 10V$	1	+25°C	100	-	mA
	$-I_{OUT1}$	$V_{SUP} = \pm15V$, $V_{OUT} = -10V$	1	+25°C	-	-100	mA
	$+I_{OUT2}$	$V_{SUP} = \pm12V$, $V_{OUT} = 10V$	1	+25°C	100	-	mA
	$-I_{OUT2}$	$V_{SUP} = \pm12V$, $V_{OUT} = -10V$	1	+25°C	-	-100	mA
Power Supply Rejection Ratio	$+PSRR_1$	$\Delta V_{SUP} = \pm5V$, +V = 20V, -V = -15V, +V = 10V, -V = -15V	1	+25°C	54	-	dB
			2, 3	+125°C, -55°C	54	-	dB
	$-PSRR_1$	$\Delta V_{SUP} = \pm5V$, +V = 15V, -V = -20V, +V = 15V, -V = -10V	1	+25°C	54	-	dB
			2, 3	+125°C, -55°C	54	-	dB
	$+PSRR_2$	$\Delta V_{SUP} = \pm5V$, +V = 17V, -V = -12V, +V = 7V, -V = -12V	1	+25°C	54	-	dB
			2, 3	+125°C, -55°C	54	-	dB
	$-PSRR_2$	$\Delta V_{SUP} = \pm5V$, +V = 12V, -V = -17V, +V = 12V, -V = -7V	1	+25°C	54	-	dB
			2, 3	+125°C, -55°C	54	-	dB
Power Supply Current	$+I_{CC1}$	$V_{SUP} = \pm12V$, $V_{OUT} = 0V$	1	+25°C	-	10	mA
			2, 3	+125°C, -55°C	-	10	mA
	$-I_{CC1}$	$V_{SUP} = \pm12V$, $V_{OUT} = 0V$	1	+25°C	-10	-	mA
			2, 3	+125°C, -55°C	-10	-	mA
	$+I_{CC2}$	$V_{SUP} = \pm15V$, $V_{OUT} = 0V$	1	+25°C	-	10	mA
			2, 3	+125°C, -55°C	-	10	mA
	$-I_{CC2}$	$V_{SUP} = \pm15V$, $V_{OUT} = 0V$	1	+25°C	-10	-	mA
			2, 3	+125°C, -55°C	-10	-	mA

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Table 2 Intentionally Left Blank. See Table 3 for A.C. Specifications.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V or ±12V, R_{LOAD} = 1kΩ, C_{LOAD} = 10pF, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Resistance	R_{IN1}	V_{SUP} = ±15V	1	+25°C	1.5	-	MΩ
	R_{IN2}	V_{SUP} = ±12V	1	+25°C	1.5	-	MΩ
Slew Rate	$+SR_1$	V_{SUP} = ±15V V_{OUT} = -10V to +10V	1	+25°C	1	-	V/ns
	$-SR_1$	V_{SUP} = ±15V V_{OUT} = +10V to -10V	1	+25°C	1	-	V/ns
	$+SR_2$	V_{SUP} = ±12V V_{OUT} = -10V to +10V	1	+25°C	1	-	V/ns
	$-SR_2$	V_{SUP} = ±12V V_{OUT} = +10V to -10V	1	+25°C	1	-	V/ns
Rise Time	T_R	V_{SUP} = ±15V V_{IN} = 0 to +500mV	1, 2	+25°C	-	10	ns
			1, 2	+125°C, -55°C	-	12	ns
Fall Time	T_F	V_{SUP} = ±15V V_{IN} = 0 to -500mV	1, 2	+25°C	-	10	ns
			1, 2	+125°C, -55°C	-	12	ns
Quiescent Power Consumption	PC_1	V_{SUP} = ±15V V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	300	mW
	PC_2	V_{SUP} = ±15V V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	240	mW
Output Resistance	R_{OUT1}	V_{SUP} = ±15V	1	+25°C	-	10	Ω
				-55°C to +125°C	-	12	Ω
	R_{OUT2}	V_{SUP} = ±12V	1	+25°C	-	10	Ω
				-55°C to +125°C	-	12	Ω

NOTES: 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

2. Measured between 10% and 90%.

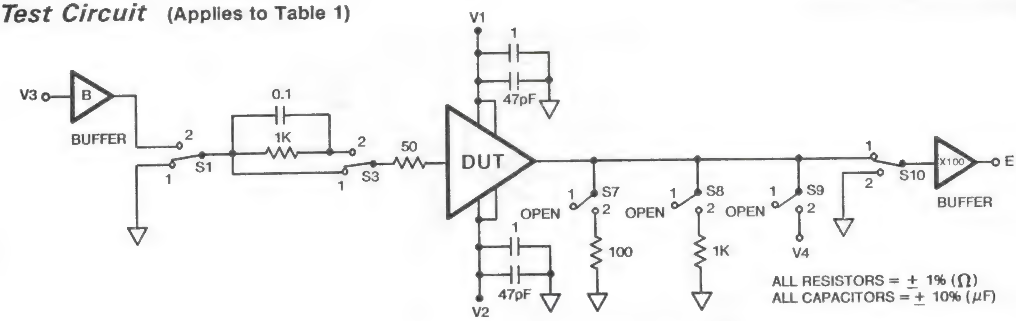
3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3
Group A Test Requirements	1, 2, 3
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

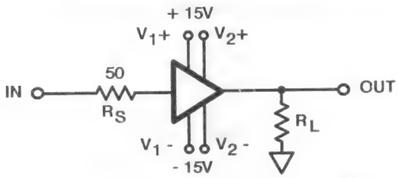
Test Circuit (Applies to Table 1)



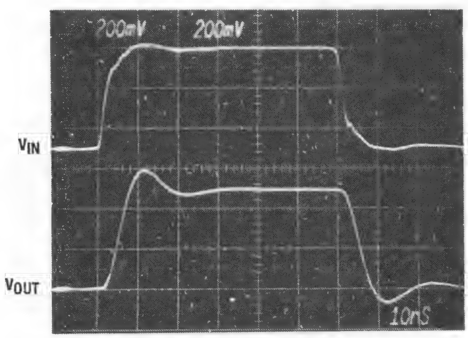
For Detailed Information, Refer to HA-5002/883 Test Tech Brief

Test Waveforms

SIMPLIFIED TEST CIRCUIT (Applies to Table 3)

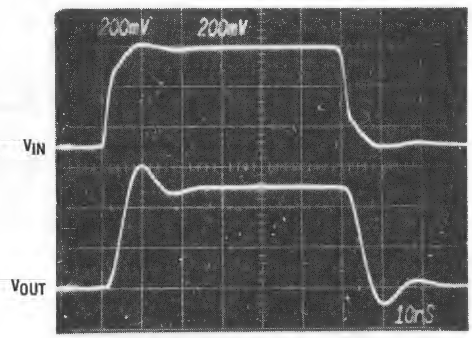


SMALL SIGNAL WAVEFORMS



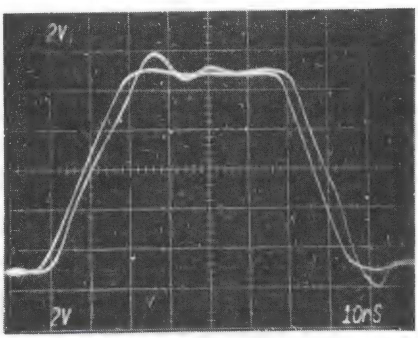
$R_S = 50\Omega$, $R_L = 100\Omega$

SMALL SIGNAL WAVEFORMS



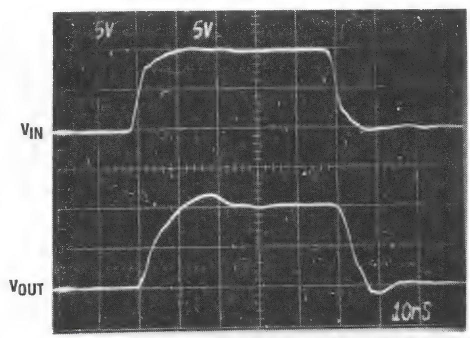
$R_S = 50\Omega$, $R_L = 1k\Omega$

LARGE SIGNAL WAVEFORMS



$R_S = 50\Omega$, $R_L = 100\Omega$

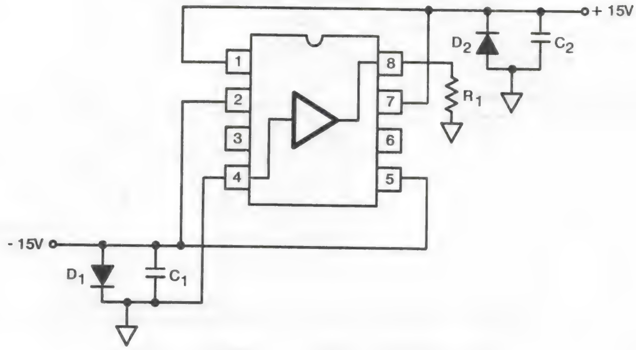
LARGE SIGNAL WAVEFORMS



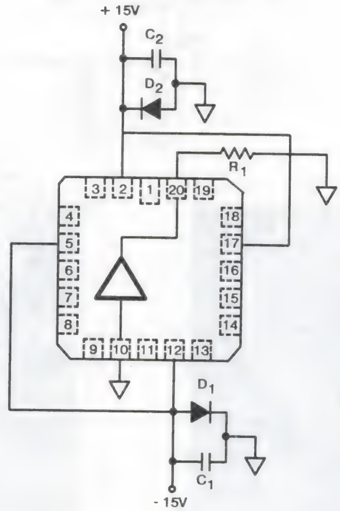
$R_S = 50\Omega$, $R_L = 1k\Omega$

Burn-In Circuits

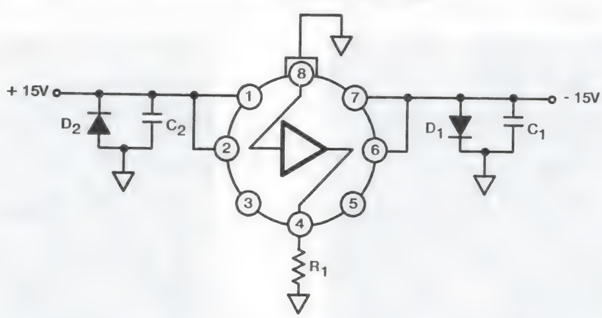
HA7-5002/883 CERAMIC MINI-DIP



HA4-5002/883 CERAMIC LCC



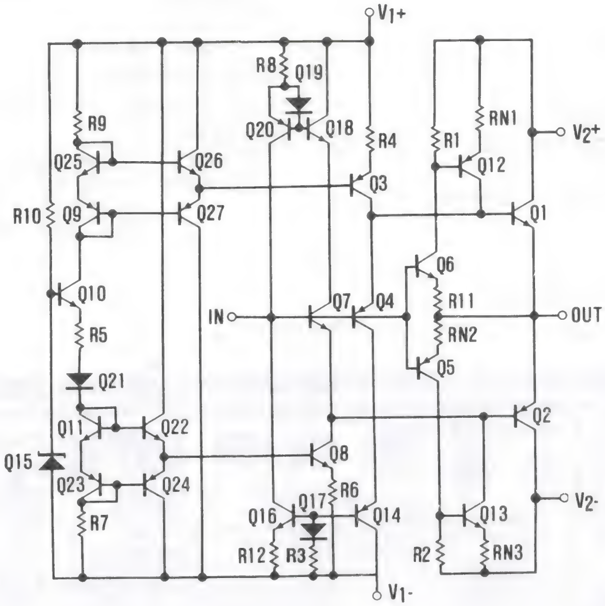
HA2-5002/883 (TO-99) METAL CAN



NOTES:

R_1 = 1kΩ, ±5%, 1/4W (Min)
$C_1 = C_2$ = 0.01μF/Socket (Min) or 0.1μF/Row (Min)
$D_1 = D_2$ = IN4002 or Equivalent/Board
$|(V+) - (V-)| = 30V$

Schematic Diagram



Die Characteristics

DIE DIMENSIONS:
81 x 80 x 19 mils
(2050 x 2030 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 20kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
0.7 X 10^5A/cm^2 @ 3.6mA

SUBSTRATE POTENTIAL (Powered Up): V-

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

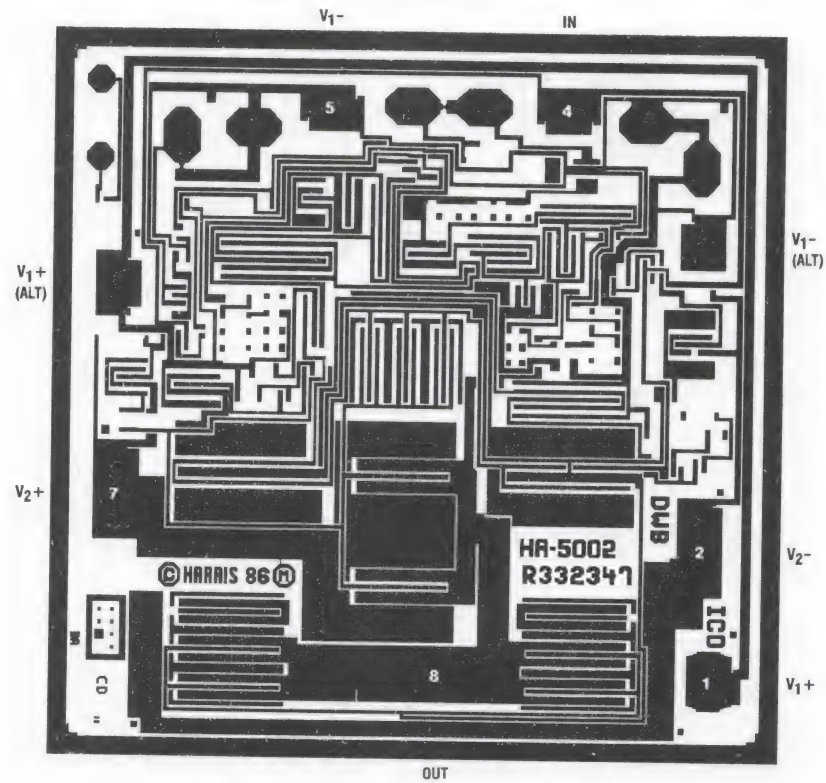
TRANSISTOR COUNT: 27

PROCESS: HFSB Bipolar Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)
Metal Can — 420°C (Max)

Metallization Mask Layout

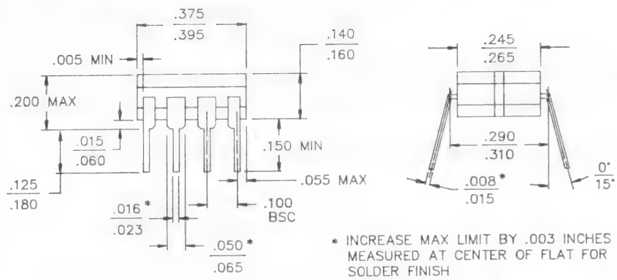
HA-5002/883



NOTE: Labeled Pad Numbers Correspond to Ceramic Mini-DIP Package Only. V_1+ and V_1- Have Two Possible Connections. Use V_1+ (Alt) and V_1- (Alt) for the Metal Can Package.

Packaging †

8 PIN CERAMIC DIP

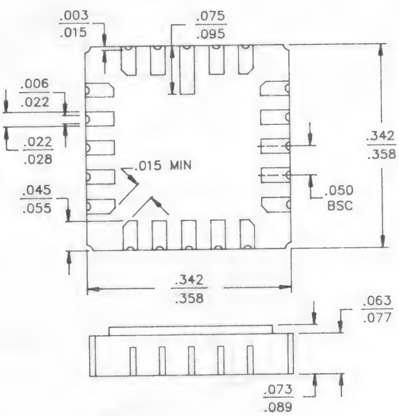


LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
- Material: Glass Frit
- Temperature: 450°C ± 10°C
- Method: Furnace Seal

INTERNAL LEAD WIRE:
- Material: Aluminum
- Diameter: 1.25 Mil
- Bonding Method: Ultrasonic

COMPLIANT OUTLINE: 38510 D-4

20 PAD CERAMIC LCC

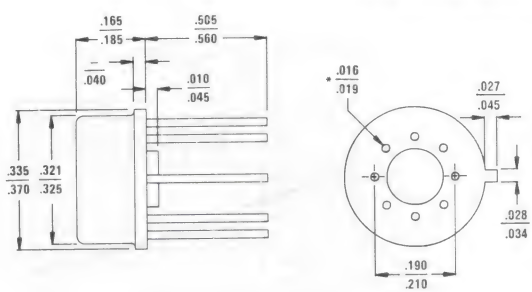


PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Ceramic, 90% Al_2O_3
PACKAGE SEAL:
- Material: Gold/Tin (80/20)
- Temperature: 320°C ± 10°C
- Method: Furnace Braze

INTERNAL LEAD WIRE:
- Material: Aluminum
- Diameter: 1.25 Mil
- Bonding Method: Ultrasonic

COMPLIANT OUTLINE: 38510 C-2

8 PIN TO-99 METAL CAN



LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
- Material: No Seal Material
- Temperature: Room Temperature
- Method: Resistance Weld

INTERNAL LEAD WIRE:
- Material: Aluminum
- Diameter: 1.25 Mil
- Bonding Method: Ultrasonic Bonded

COMPLIANT OUTLINE: 38510 A-1

*Dimension Maximum Limits Are Increased by 0.003 inches for Solder Dip Finish

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

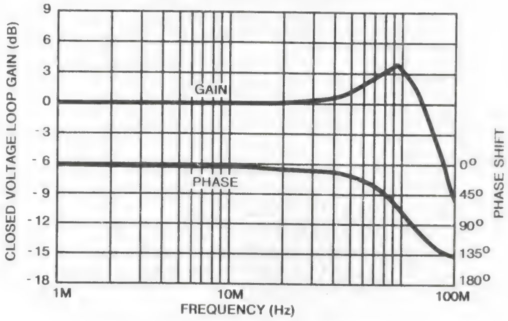
DESIGN INFORMATION

Monolithic, Wideband, High Slew Rate, High Output Current Buffer

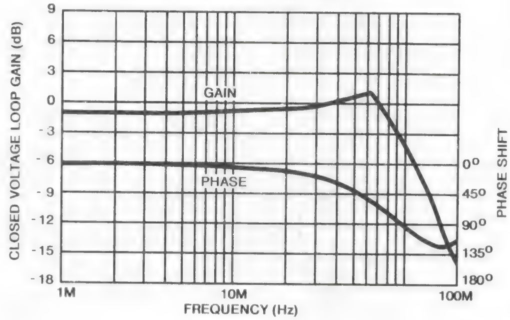
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

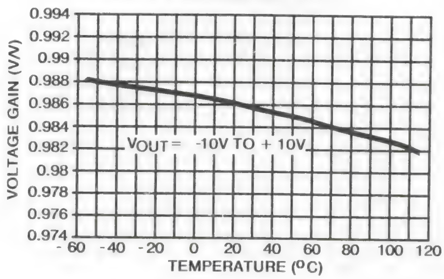
GAIN/PHASE vs. FREQUENCY
$V_{CC} = \pm15V$, $R_L = 1K$, $R_S = 50\Omega$



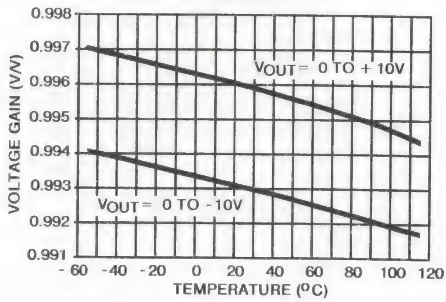
GAIN/PHASE vs. FREQUENCY
$V_{CC} = \pm15V$, $R_L = 50\Omega$, $R_S = 50\Omega$



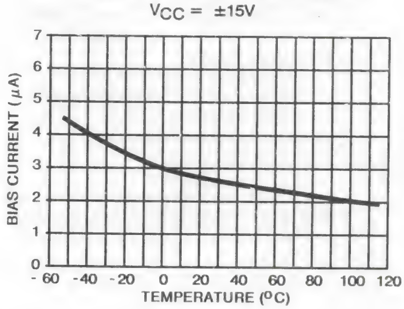
VOLTAGE GAIN vs. TEMPERATURE
$V_{CC} = \pm15V$, $R_{LOAD} = 100\Omega$



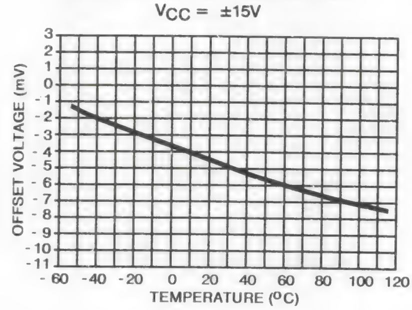
VOLTAGE GAIN vs. TEMPERATURE
$V_{CC} = \pm15V$, $R_{LOAD} = 1K\Omega$



OFFSET VOLTAGE vs. TEMPERATURE
$V_{CC} = \pm15V$



BIAS CURRENT vs. TEMPERATURE
$V_{CC} = \pm15V$



DESIGN INFORMATION (Continued)

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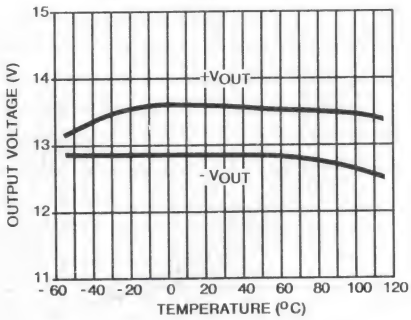
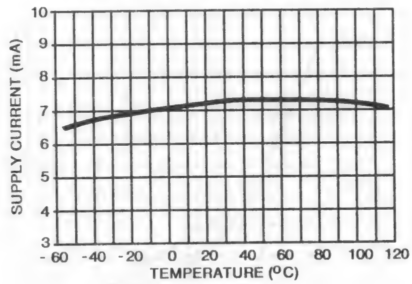
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

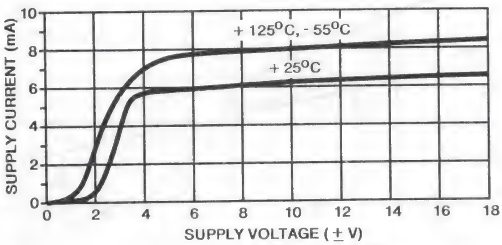
MAXIMUM OUTPUT VOLTAGE vs. TEMPERATURE
$V_{CC} = \pm 15V$, $R_{LOAD} = 100\Omega$



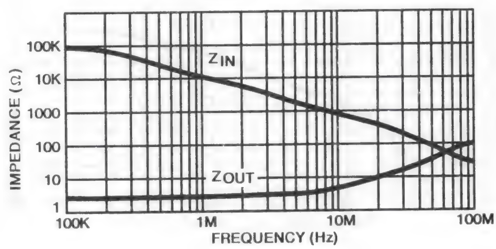
SUPPLY CURRENT vs. TEMPERATURE
$V_{CC} = \pm 15V$, $I_{OUT} = 0mA$



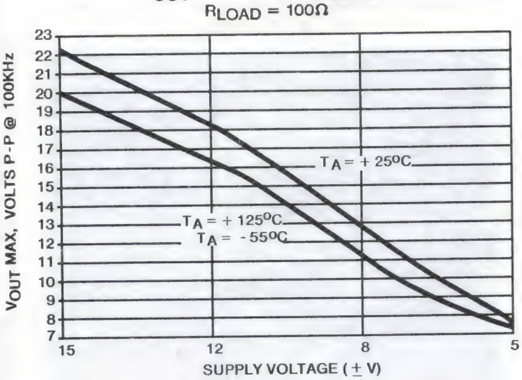
SUPPLY CURRENT vs. SUPPLY VOLTAGE
$I_{OUT} = 0mA$



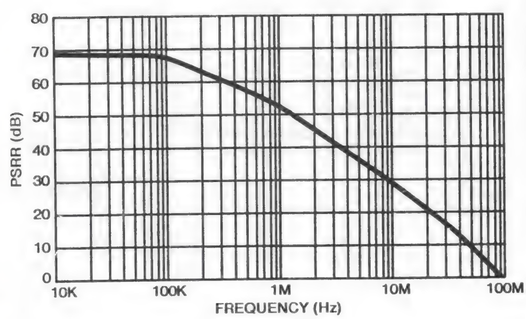
INPUT/OUTPUT IMPEDANCE vs. FREQUENCY
$V_{CC} = \pm 15V$



V_{OUT} MAXIMUM vs. V_{SUPPLY}
$R_{LOAD} = 100\Omega$



PSSR vs. FREQUENCY



DESIGN INFORMATION (Continued)

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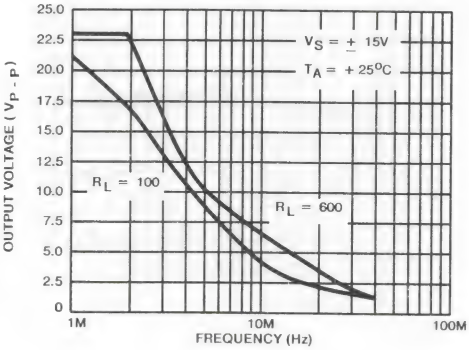
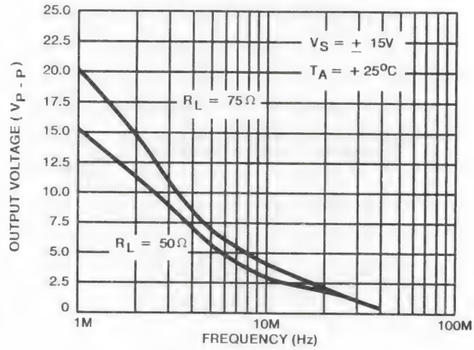
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

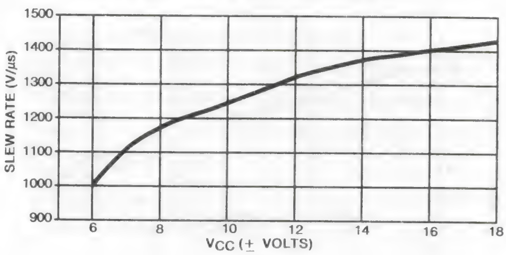
OUTPUT VOLTAGE vs. FREQUENCY
$V_S = \pm15V$, $T_A = +25^oC$



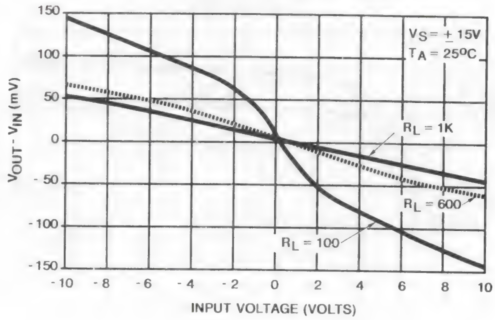
OUTPUT VOLTAGE vs. FREQUENCY
$V_S = \pm15V$, $T_A = +25^oC$



SLEW RATE vs. SUPPLY VOLTAGE

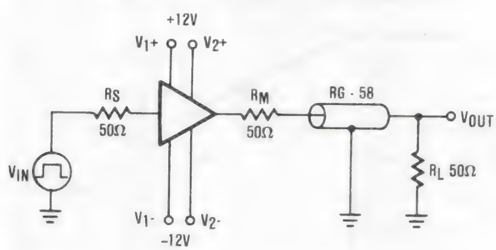


GAIN ERROR vs. INPUT VOLTAGE

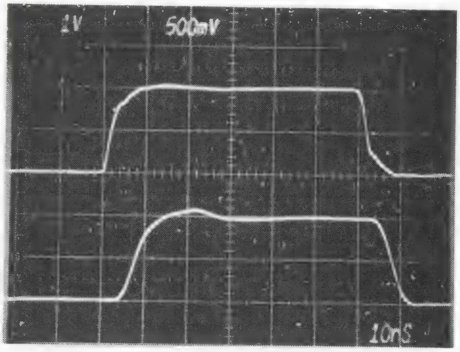


Typical Applications

COAXIAL CABLE DRIVER - 50Ω SYSTEM



MEASURED WAVEFORM FOR COAXIAL DRIVER WITH V_{OUT} = 1V PULSE



DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±12 to ±15V, R_S = 50Ω, R_L = 1kΩ, $C_L \leq$ 10pF, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage		+25°C	5	Table 1	mV
		Full	10	Table 1	mV
Average Offset Voltage Drift	Versus Temperature	Full	15	30	μV/°C
Bias Current		+25°C	2	Table 1	μA
		Full	3.4	Table 1	μA
Average Bias Current Drift	Versus Temperature	Full	0.03	.04	μV/°C
Input Resistance	V_{IN} @ D.C.	Full	3	Table 3	MΩ
Input Noise Voltage	10Hz to 1MHz	+25°C	4	-	μV_{p-p}
Voltage Gain	R_L = 100Ω	+25°C	0.971	Table 1	V/V
	R_L = 1kΩ	+25°C	0.995	Table 1	V/V
-3dB Bandwidth	$V_{IN} = \leq 200mV_{p-p}$	+25°C	110	-	MHz
A.C. Current Gain		+25°C	40	-	A/mA
Output Voltage Swing	R_L = 100Ω	+25°C	±10.7	Table 1	V
	R_L = 1kΩ, V_S = ±15V	Full	±13.5	Table 1	V
	R_L = 1kΩ, V_S = ±12V	Full	±10.5	Table 1	V
Output Resistance		Full	3	Table 3	Ω
Harmonic Distortion	$V_{IN} = 1V_{RMS}$, f_o = 10kHz	+25°C	< 0.005	0.01	%
	$V_{IN} = 5V_{RMS}$, f_o = 1kHz	+25°C	< 0.1	-	%
Full Power Bandwidth	V_{OUT} = 10V	+25°C	11	7	MHz
Rise/Fall Time	V_{OUT} = +500mV, -500mV	+25°C	3.6	Table 3	ns
Propagation Delay	V_{OUT} = +500mV, -500mV	+25°C	2	3	ns
Overshoot	V_{OUT} = +500mV, -500mV	+25°C	30	40	%
Slew Rate	V_{OUT} = ±10V	+25°C	1.3	Table 3	V/ns
Settling Time	V_{OUT} = +10V to 0.1%	+25°C	50	80	ns
Supply Current	No Load	+25°C	8.3	Table 1	mA
Power Supply Rejection Ratio	ΔV_{SUPPLY} = 10V	Full	64	Table 1	dB
Minimum Supply Voltage	Functional Operation Only. Other Parameters Will Vary.	+25°C	±4V	±5V	V

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Operating Instructions

Layout Considerations

The wide bandwidth of the HA-5002 necessitates that high frequency circuit layout procedures be followed. Failure to follow these guidelines can result in marginal performance.

Probably the most crucial of the RF/video layout rules is the use of a ground plane. A ground plane provides isolation and minimizes distributed circuit capacitance and inductance which will degrade high frequency performance.

Other considerations are proper power supply bypassing and keeping the input and output connections as short as possible which minimizes distributed capacitance and reduces board space.

Power Supply Decoupling

For optimal device performance it is recommended that the positive and negative power supplies be bypassed with capacitors to ground. Ceramic capacitors ranging in value from 0.01 to 0.1μF will minimize high frequency variations in supply voltage, while low frequency bypassing requires larger valued capacitors since the impedance of the capacitor is dependent on frequency.

It is also recommended that the bypass capacitors be connected close to the HA-5002 (preferably directly to the supply pins).

Heat Sinking

Certain applications of the HA-5002/883 may require the use of a heat sink. High ambient temperatures, low impedance loads or high supply voltages may cause the internal power disssipation to force the junction temperature above the maximum rating of +175°C. Also, an indefinite short of the output to ground will cause excessive power dissipation. Manufacturers such as Thermalloy, AAVID, or IERC produce suitable heat sinks.

Thermal resistance values are shown on the second page of this data sheet and because Gold-Eutectic Die Attach is required for HA-5002/883, lower theta value are shown over other temperature grades.

Operation At Reduced Supply Levels

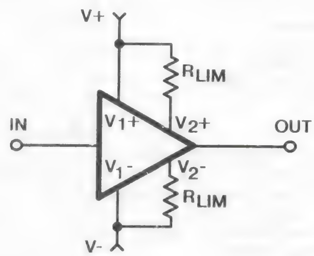
The HA-5002 can operate at supply voltage levels as low as ±5V and lower. Output swing is directly affected as well as slight reductions in slew rate and bandwidth.

Short Circuit Protection

The output current can be limited by using the following circuit:

$$R_{LIM} = \frac{V+}{I_{OUTMAX}} = \frac{V-}{I_{OUTMAX}}$$

I_{OUTMAX} = 200mA (Continuous)



Capacitive Loading

The HA-5002 will drive large capacitive loads without oscillation but peak current limits should not be exceeded. Following the formula $I = C^{dv}/_{dt}$ implies that the slew rate or the capacitive load must be controlled to keep peak current below the maximum or use the current limiting approach as shown. The HA-5002 can become unstable with small capacitive loads (50pF) if certain precautions are not taken. Stability is enhanced by any one of the following: a source resistance in series with the input of 50Ω to 1K; increasing capacitive load to 150pF or greater; decreasing C_{LOAD} to 20pF or less; adding an output resistor of 10Ω to 50Ω; or adding feedback capacitance of 50pF or greater. Adding source resistance generally yields the best results.

HARRIS HA-5033/883

January 1989

Video Buffer

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Differential Phase Error .... 0.1 Degree (Typ)
- Differential Gain Error .... 0.1% (Typ)
- Voltage Gain ($R_L = 1k\Omega$) .... 0.94 (Min)
  0.99 (Typ)
  ($R_L = 100\Omega$) .... 0.93 (Min)
  0.95 (Typ)
- High Slew Rate .... 1V/ns (Min)
  1.3V/ns (Typ)
- Wide Small Signal Bandwidth .... 250MHz (Typ)
- Fast Rise Time .... 6ns (Max)
  3ns (Typ)
- High Output Drive .... ±8V into 100Ω (Min)
- Wide Power Bandwidth .... D.C. to 65MHz (Typ)
- Wide Power Supply Range .... ±5V to ±16V
- Replace Costly Hybrids

Applications

- Video Buffer
- High Frequency Buffer
- Isolation Buffer
- High Speed Line Driver
- Impedance Matching
- Current Boosters
- High Speed A/D Input Buffers
- For Further Application Ideas, See App. Note 548

Description

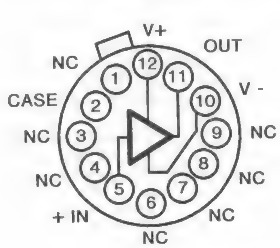
The HA-5033/883 is a unity gain monolithic I.C. designed for any application requiring a fast, wideband buffer. Featuring a bandwidth of 250MHz and outstanding differential phase/gain characteristics, this high performance voltage follower is an excellent choice for video circuit design. Other features, which include a minimum slew rate of 1000V/µs and high output drive capability, make the HA-5033/883 applicable for line driver and high speed data conversion circuits.

The high performance of this product is a result of the Harris Dielectric Isolation process. A major feature of this process is that it produces both PNP and NPN high frequency transistors which makes wide bandwidth designs, such as the HA-5033/883, practical.

The HA-5033/883 is available in a 12 pin (TO-8) Metal Can and is specified over the full -55°C to +125°C military temperature range.

Pinout

HA2-5033/883 (METAL CAN)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Input Voltage .... Equal to Supplies
Peak Output Current (50ms On, 1s Off) .... ±200mA
Junction Temperature (T_J) .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... < 2000V
Lead Temperature (Soldering 10 sec) .... 275°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Metal Can Package	82°C/W	32°C/W

Package Power Dissipation Limit at +75°C for $T_J \leq$ 175°C
Metal Can Package 1.2W
Package Power Dissipation Derating Factor Above +75°C
Metal Can Package .... 12.1mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±12V to ±15V
$R_L \geq 100\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±12V and ±15V, $R_{SOURCE} = 50\Omega$, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	V_{SUP} = ±12V, V_{IN} = 0V	1	+25°C	-15	15	mV
			2, 3	+125°C, -55°C	-25	25	mV
Input Bias Current	I_B	V_{SUP} = ±12V, $R_S = 1k\Omega$	1	+25°C	-35	35	µA
			2, 3	+125°C, -55°C	-50	50	µA
Voltage Gain 1	$+A_{V1}$	V_{SUP} = ±12V, $R_L = 100\Omega$, V_{IN} = +2V	1	+25°C	0.93	-	V/V
			2, 3	+125°C, -55°C	0.92	-	V/V
	$-A_{V1}$	V_{SUP} = ±12V, $R_L = 100\Omega$, V_{IN} = -2V	1	+25°C	0.93	-	V/V
			2, 3	+125°C, -55°C	0.92	-	V/V
Voltage Gain 2	$+A_{V2}$	V_{SUP} = ±12V, $R_L = 1k\Omega$, V_{IN} = 10V	1	+25°C	0.94	-	V/V
	$-A_{V2}$	V_{SUP} = ±12V, $R_L = 1k\Omega$, V_{IN} = -10V	1	+25°C	0.94	-	V/V
Output Voltage Swing	$+V_{OUT1}$	V_{SUP} = ±12V, $R_L = 100\Omega$, V_{IN} = +12V	1	+25°C	8.5	-	V
			2, 3	+125°C, -55°C	8	-	V
	$-V_{OUT1}$	V_{SUP} = ±12V, $R_L = 100\Omega$, V_{IN} = -12V	1	+25°C	-	-8.5	V
			2, 3	+125°C, -55°C	-	-8	V
	$+V_{OUT2}$	V_{SUP} = ±15V, $R_L = 1k\Omega$, V_{IN} = +15V	1	+25°C	12	-	V
			2, 3	+125°C, -55°C	12	-	V
	$-V_{OUT2}$	V_{SUP} = ±15V, $R_L = 1k\Omega$, V_{IN} = -15V	1	+25°C	-	-12	V
			2, 3	+125°C, -55°C	-	-12	V
Output Current	$+I_{OUT}$	V_{SUP} = ±12V, V_{IN} = +12V	1	+25°C	80	-	mA
	$-I_{OUT}$	V_{SUP} = ±12V, V_{IN} = -12V	1	+25°C	-	-80	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = ±5V, +V = 17V, -V = -12V, +V = 7V, -V = -12V	1	+25°C	54	-	dB
			2, 3	+125°C, -55°C	54	-	dB
	-PSRR	ΔV_{SUP} = ±5V, +V = 12V, -V = -17V, +V = 12V, -V = -7V	1	+25°C	54	-	dB
			2, 3	+125°C, -55°C	54	-	dB
Power Supply Current	$+I_{CC}$	V_{SUP} = ±12V, V_{OUT} = 0V	1	+25°C	-	25	mA
			2, 3	+125°C, -55°C	-	25	mA
	$-I_{CC}$	V_{SUP} = ±12V, V_{OUT} = 0V	1	+25°C	-25	-	mA
			2, 3	+125°C, -55°C	-25	-	mA

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Table 2 Intentionally Left Blank, see Table 3 for A.C. Specifications.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±12V or ±15V, R_{LOAD} = 1kΩ, $C_{LOAD} \leq$ 10pF, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Resistance	R_{IN1}	V_{SUP} = ±15V V_{IN} = 12V, R_L = 100Ω	1	+25°C	1	-	MΩ
Slew Rate	+SR	V_{SUP} = ±15V V_{OUT} = -10V to +10V	1	+25°C	1	-	V/ns
	-SR	V_{SUP} = ±15V V_{OUT} = +10V to -10V	1	+25°C	1	-	V/ns
Rise Time	T_R	V_{SUP} = ±12V V_{IN} = 0V to +500mV	1, 2	+25°C	-	6	ns
Fall Time	T_F	V_{SUP} = ±12V V_{IN} = 0V to -500mV	1, 2	+25°C	-	6	ns
Full Power Bandwidth	FPBW	V_{SUP} = ±15V V_{OUT} = ±10V R_L = 1kΩ	1	+25°C	15.9	-	MHz
Quiescent Power Consumption	PC_1	V_{SUP} = ±15V V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	750	mW
	PC_2	V_{SUP} = ±12V V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	600	mW
Output Resistance	R_{OUT1}	V_{SUP} = ±15V	1	+25°C	-	10	Ω
				-55°C to +125°C	-	12	Ω
	R_{OUT2}	V_{SUP} = ±12V	1	+25°C	-	10	Ω
				-55°C to +125°C	-	12	Ω

NOTES: 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

2. Measured between 10% and 90%.

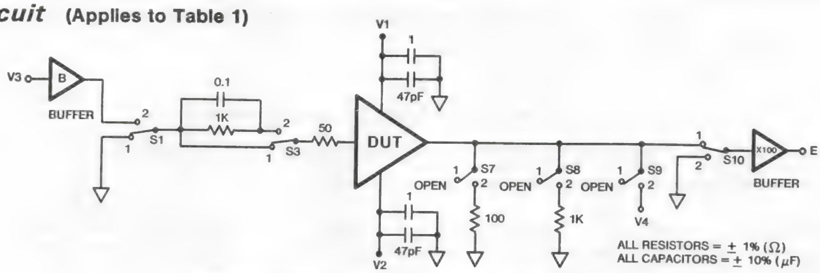
3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3
Group A Test Requirements	1, 2, 3
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

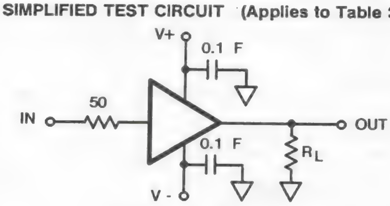
Test Circuit (Applies to Table 1)



For Detailed Information, Refer to HA-5033/883 Test Tech Brief

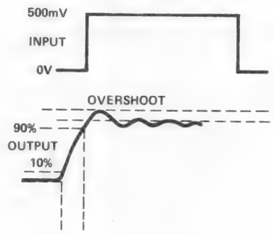
Test Waveforms

SIMPLIFIED TEST CIRCUIT (Applies to Table 3)



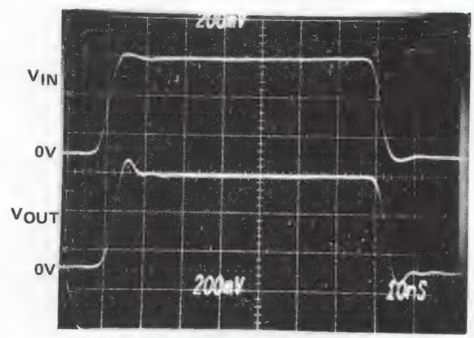
TRANSIENT RESPONSE

RISE TIME



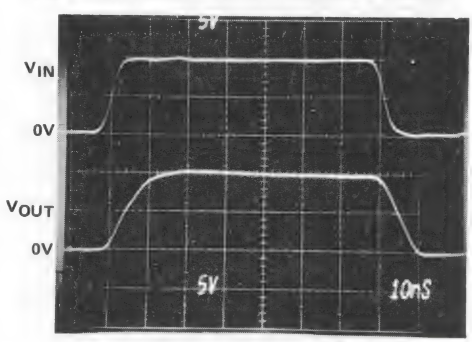
NOTE: Measured on both positive and negative transitions.

MEASURED +0.5V PULSE RESPONSE
$T_A = +25^oC$, $R_S = 50\Omega$, $R_L = 100\Omega$
$V_{IN} = V_{OUT}$ (Scale) = 200mV/Div.; Time Scale = 10ns/Div.

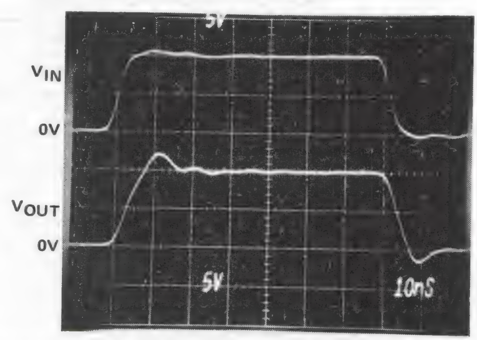


LARGE SIGNAL RESPONSE

MEASURED +10V PULSE RESPONSE
$T_A = +25^oC$, $R_S = 50\Omega$, $R_L = 100\Omega$
$V_{IN} = V_{OUT}$ (Scale) = 5V/Div.; Time Scale = 10ns/Div.

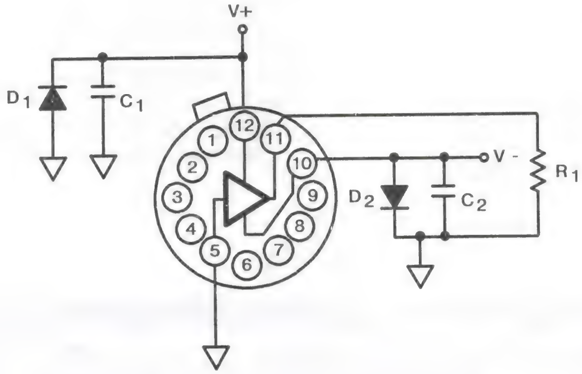


MEASURED +10V RESPONSE
$T_A = +25^oC$, $R_S = 50\Omega$, $R_L = 1k\Omega$
$V_{IN} = V_{OUT}$ (Scale) = 5V/Div.; Time Scale = 10ns/Div.



Burn-In Circuit

HA2-5033/883 (TO-8) METAL CAN



NOTES:

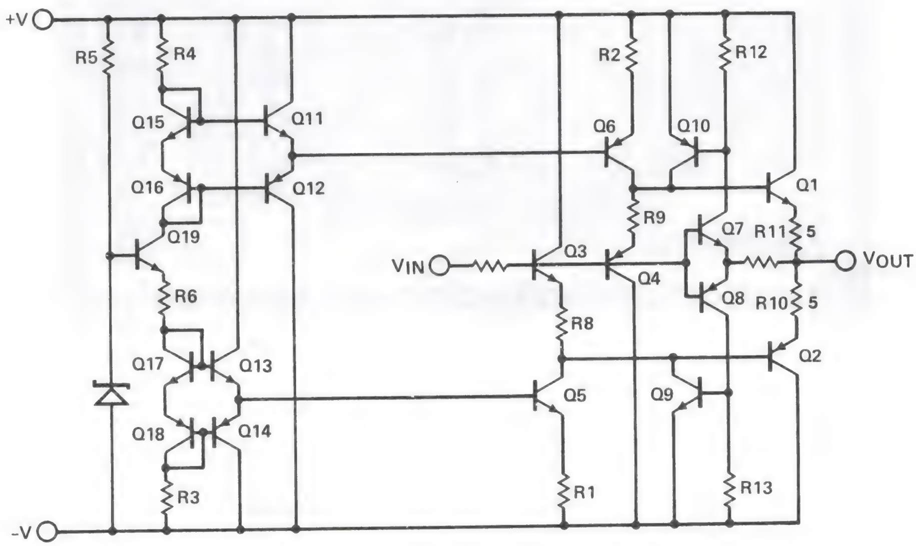
R_1 = 1kΩ, ±5%, 1/4W (Min)

C_1 = 0.01μF/Socket (Min) or 0.1μF/Row (Min)

D_1 = D_2 = IN4002 or Equivalent/Board

$|(V+) - (V-)| = 30V$

Schematic Diagram



Die Characteristics

DIE DIMENSIONS:
66.9 x 51.2 x 19 mils
(1700 x 1300 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 20kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
0.79 X 10^5A/cm^2 @ 25mA

SUBSTRATE POTENTIAL (Powered Up): V-

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

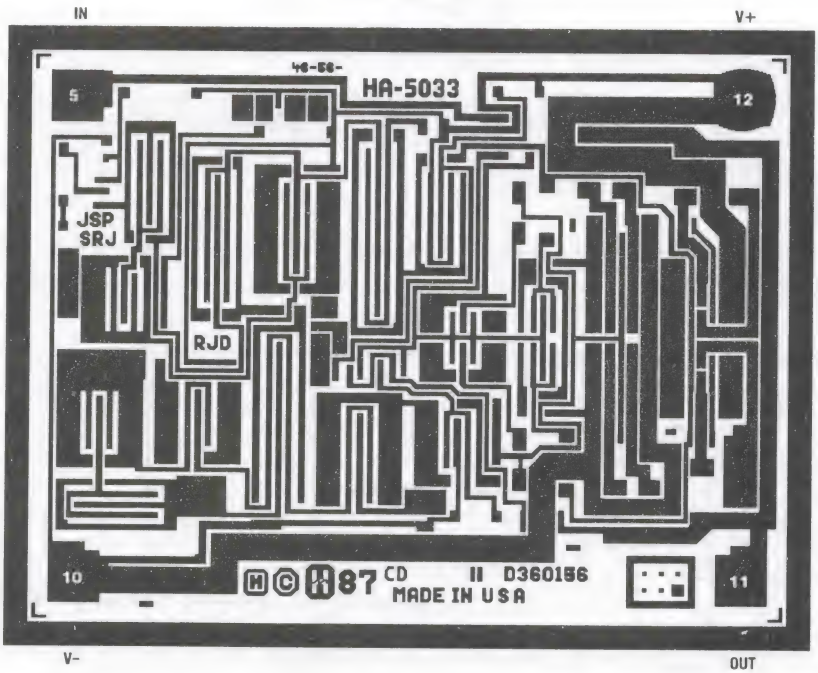
TRANSISTOR COUNT: 20

PROCESS: HFSB Bipolar Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Metal Can — 420°C (Max)

Metallization Mask Layout

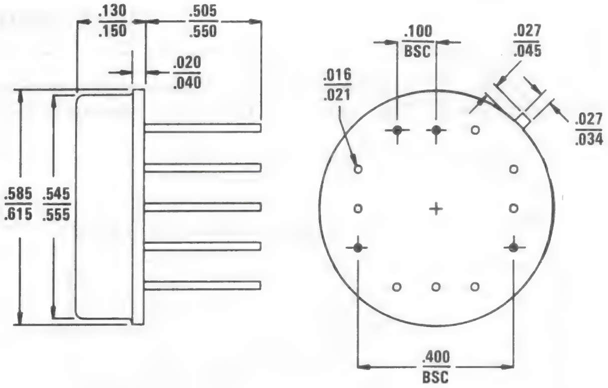
HA-5033/883



NOTE Pin Numbers Correspond to (TO-8) Metal Can Package Only.

Packaging †

12 PIN (TO-8) METAL CAN



LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
- Material: No Seal Material
- Temperature: Room Temperature
- Method: Resistance Weld

INTERNAL LEAD WIRE:
- Material: Aluminum
- Diameter: 1.25 Mil
- Bonding Method: Ultrasonic Bonded

COMPLIANT OUTLINE: None
JEDEC OUTLINE: AB

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

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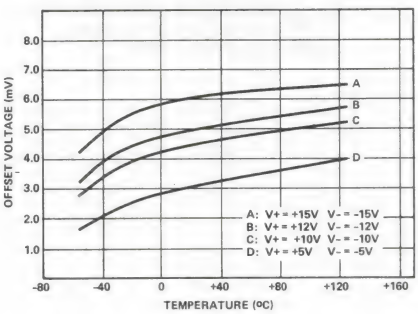
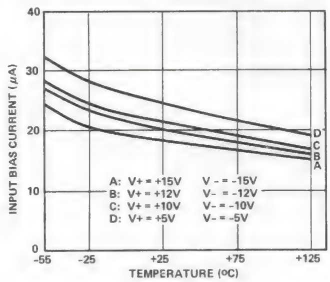
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

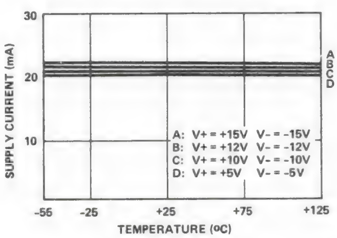
INPUT OFFSET VOLTAGE vs. TEMPERATURE vs. SUPPLY VOLTAGE



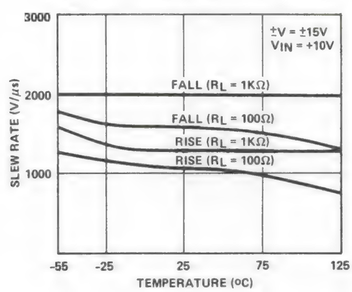
INPUT BIAS CURRENT vs. TEMPERATURE vs. SUPPLY VOLTAGE



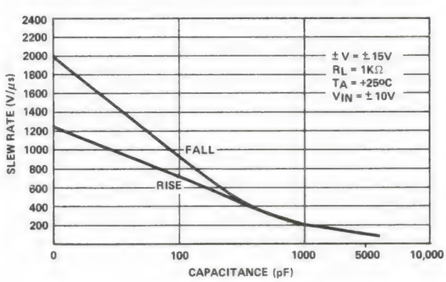
SUPPLY CURRENT vs. TEMPERATURE vs. SUPPLY VOLTAGE



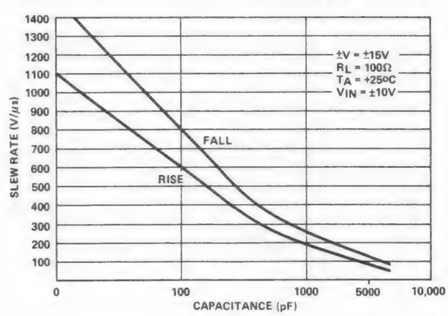
SLEW RATE vs. TEMPERATURE



SLEW RATE vs. LOAD CAPACITANCE ($R_L = 1k\Omega$)



SLEW RATE vs. LOAD CAPACITANCE ($R_L = 100\Omega$)



DESIGN INFORMATION (Continued)

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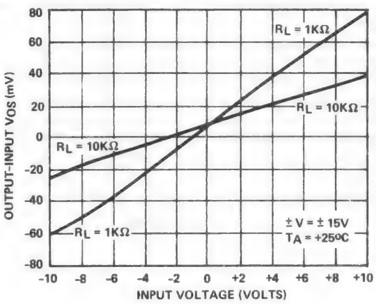
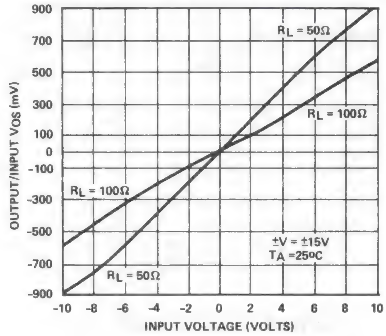
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

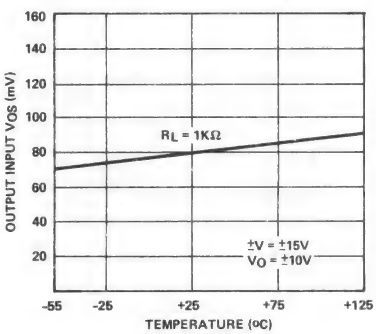
GAIN ERROR vs. INPUT VOLTAGE



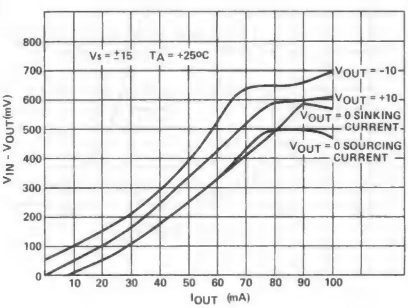
GAIN ERROR vs. INPUT VOTAGE



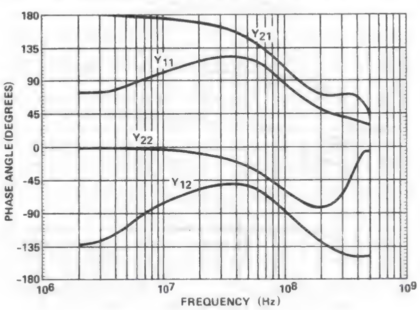
GAIN ERROR vs. TEMPERATURE



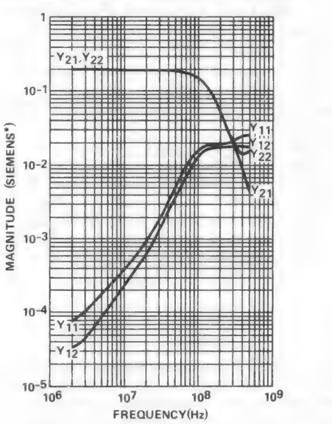
V_{IN} - V_{OUT} vs. I_{OUT}



Y - PARAMETERS PHASE vs. FREQUENCY



Y - PARAMETER MAGNITUDE FREQUENCY



* Siemens = Ω-1

DESIGN INFORMATION (Continued)

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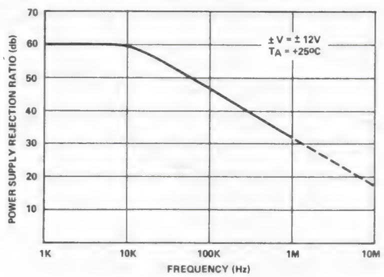
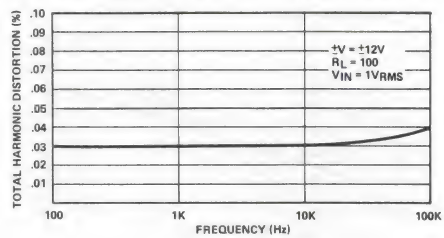
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

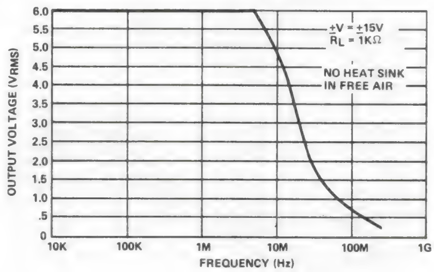
POWER SUPPLY REJECTION RATIO vs. FREQUENCY



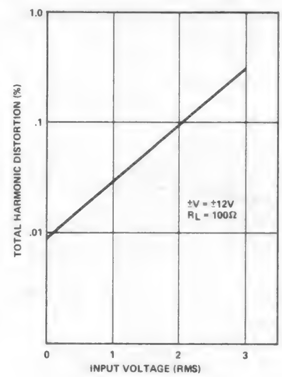
TOTAL HARMONIC DISTORTION vs. FREQUENCY



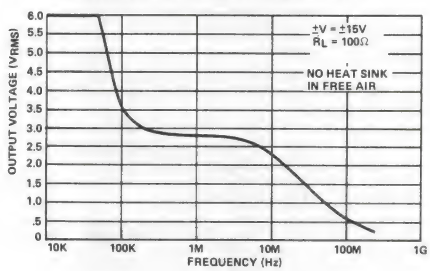
OUTPUT SWING vs. FREQUENCY



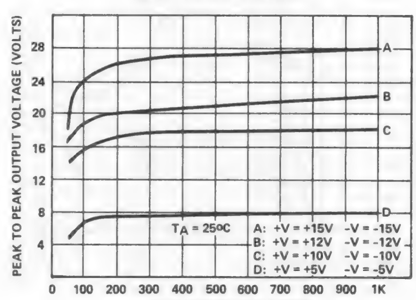
TOTAL HARMONIC DISTORTION vs. RMS INPUT VOLTAGE



OUTPUT SWING vs. FREQUENCY *



OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE vs. SUPPLY VOLTAGE



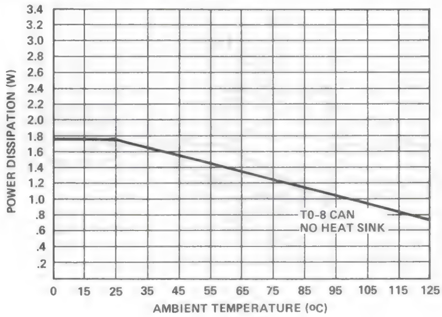
* This curve was obtained by noting the output voltage necessary to produce an observable distortion for a given frequency. If higher distortion is acceptable, then a higher output voltage for a given frequency can be obtained.
However, operating the HA-5033 with increased distortion (to the right of curve shown), will also be accompanied by an increase in supply current. The resulting increase in chip temperature must be considered and heat sinking will be necessary to prevent thermal runaway. This characteristic is the result of the output transistor operation. If the signal amplitude or signal frequency or both are increased beyond the curve shown, the NPN, PNP output transistors will approach a condition of being simultaneously on. Under this condition, thermal runaway can occur.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

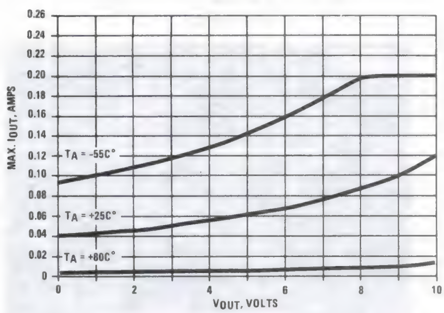
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

MAXIMUM POWER DISSIPATION vs. AMBIENT TEMPERATURE



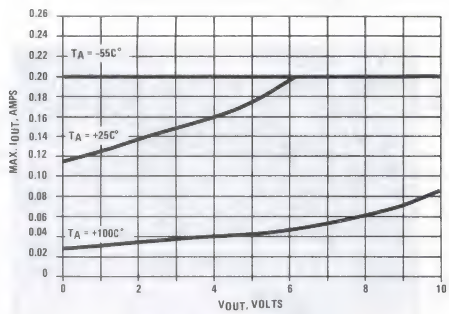
HA-5033 SOA, TO-8, NO SINK

$T_J = +175^oC$, $I_{CC} = 25mA$, $V_{CC} = \pm15$, $\theta_{ja} = 84^oC/W$



HA-5033, TO-8, AAVID 5792 $\theta_{sa} = 25^oC/W$

$T_J = +175^oC$, $I_{CC} = 25mA$, $V_{CC} = \pm15$, $\theta_{jc} = 33^oC/W$



Operating Instructions

Layout Considerations

The wide bandwidth of the HA-5033 necessitates that high frequency circuit layout procedures be followed. Failure to follow these guidelines can result in marginal performance.

Probably the most crucial of the RF/video layout rules is the use of a ground plane. A ground plane provides isolation and minimizes distributed circuit capacitance and inductance which will degrade high frequency performance. This ground plane shielding can also incorporate the metal case of the HA-5033 since pin #2 is internally tied to the package. This feature allows the user to make metal to metal contact between the ground plane and the package, which extends shielding, provides additional heat sinking and eliminates the use of a socket. IC sockets contribute inter-lead capacitance which limits device bandwidth and should be avoided.

Other considerations are proper power supply bypassing and keeping the input and output connections as short as possible which minimizes distributed capacitance and reduces board space.

Power Supply Decoupling

For optimum device performance, it is recommended that the positive and negative power supplies be bypassed with capacitors to ground. Ceramic capacitors ranging in value from 0.01 to 0.1µF will minimize high frequency variations in supply voltage. Solid tantalum capacitors 1µF or larger will optimize low frequency performance.

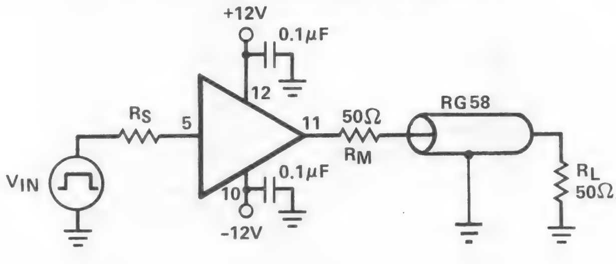
It is also recommended that the bypass capacitors be connected close to the HA-5033 (preferably directly to the supply pins).

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Applications (See Application Note 548)

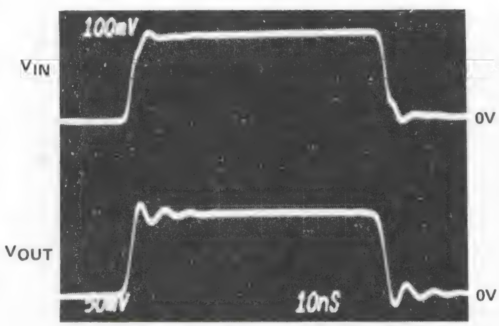
VIDEO COAXIAL LINE DRIVER - 50V SYSTEM



POSITIVE PULSE RESPONSE

$T_A = +25^oC$, $R_S = 50\Omega$, $R_M = R_L = 50\Omega$

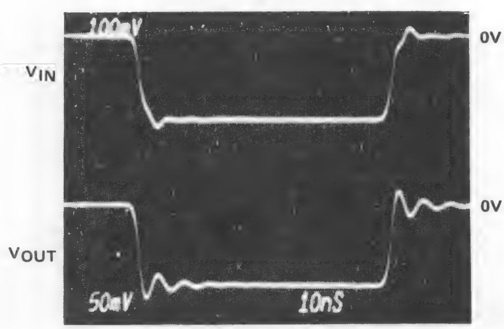
$$V_O = V_{IN}\left(\frac{R_L}{R_L + R_M}\right) = ½\ V_{IN}$$



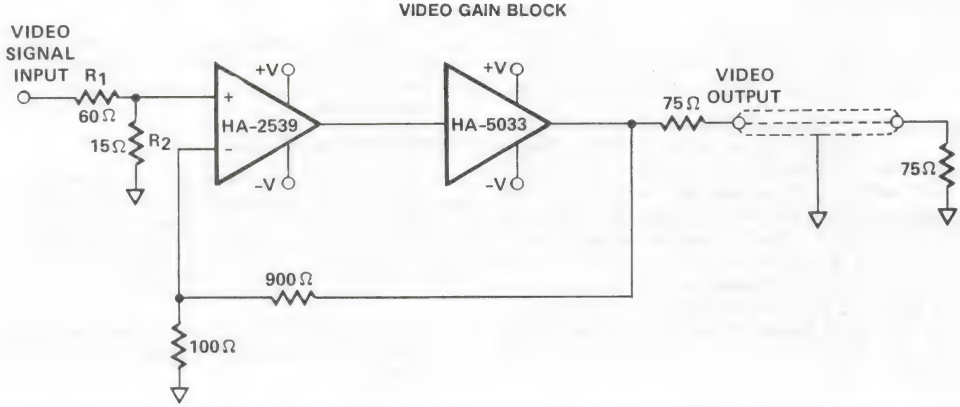
NEGATIVE PULSE RESPONSE

$T_A = +25^oC$, $R_S = 50\Omega$, $R_M = R_L = 50\Omega$

$$V_O = V_{IN}\left(\frac{R_L}{R_L + R_M}\right) = ½\ V_{IN}$$



VIDEO GAIN BLOCK



DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_L = 1kΩ, $C_L \leq$ 10pF, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMPERATURE	TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage		Full	6	Table 1	mV
Average Offset Voltage Drift	Versus Temperature	+25°C to 125°C	20	35	µV/°C
		-55°C to +25°C	50	60	µV/°C
Bias Current		+25°C	18	Table 1	mA
		Full	25	Table 1	µA
Input Resistance	V_{IN} = ±3V	+25°C	1.5	0.9	MΩ
Input Capacitance		+25°C	1.6	3	pF
Input Noise Voltage	10Hz to 10MHz	+25°C	11	20	μV_{p-p}
Voltage Gain	V_{IN} = ±2V, R_L = 100Ω	+25°C	0.97	Table 1	V/V
	V_{IN} = ±2V, R_L = 100Ω	Full	0.95	Table 1	V/V
	V_{IN} = ±3V, R_L = 1kΩ	+25°C	0.993	0.98	V/V
	V_{IN} = ±10V, R_L = 1kΩ	+25°C	0.98	Table 1	V/V
Output Voltage Swing	R_L = 100Ω	Full	±10	Table 1	V
	R_L = 1kΩ	Full	±14	Table 1	V
Full Power Bandwidth	V_{OUT} = 1 V_{RMS}, R_L = 1kΩ	+25°C	65	-	MHz
	V_{OUT} = ±10V, R_L = 1kΩ	+25°C	20	Table 3	MHz
Rise/Fall Time	V_{OUT} = ≤ 500mV	+25°C	3	Table 3	ns
Propagation Delay		+25°C	1	3	ns
Overshoot	V_{OUT} = ≤ 500mV	+25°C	10	20	%
Slew Rate	V_{OUT} = ±10V	+25°C	1.3	Table 3	V/ns
Settling Time	+10V to 0.1%	+25°C	50	75	ns
Differential Phase Error	NTSC Method	+25°C	0.1	0.4	Degree
Differential Gain Error	NTSC Method	+25°C	0.1	0.5	%
Harmonic Distortion	V_{IN} = 1V_{RMS}	+25°C	< 0.1	-	%
Power Supply Rejection Ratio	ΔV_{SUPPLY} = ±5V	Full	65	Table 1	dB
Supply Current	No Load	Full	21	Table 1	mA
Minimum Supply Voltage	Functional Operation Only. Other Parameters Will Vary.	+25°C	±5	±5	V

HARRIS

HA-5101/883

Low Noise, High Performance Operational Amplifier

January 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low Noise Voltage @ 1kHz .... $4.5nV/\sqrt{Hz}$ Max
- Low Noise Current @ 1kHz .... $3pA/\sqrt{Hz}$ Max
- Wide Unity Gain Bandwidth .... 10MHz Min
- High Gain (Full Temp) .... 100kV/V Min
  (Room Temp) .... 1MV/V Typ
- Slew Rate .... 6V/µs Min
- High CMRR/PSRR (Full Temp) .... 80dB Min
- High Output Drive Capability (Full Temp) 25mA

Applications

- High Quality Audio Preamplifiers
- High Q Active Filters
- Low Noise Function Generators
- Low Distortion Oscillators
- Low Noise Comparators

Description

The HA-5101/883 is a dielectrically isolated operational amplifier featuring low noise and high performance. This amplifier has a excellent noise voltage density of $4.5nV/\sqrt{Hz}$ (max) at 1kHz. The unity gain stable HA-5101/883 yields a 10MHz unity gain bandwidth and a 6V/µs slew rate.

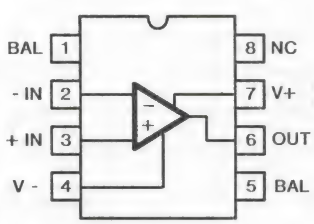
D.C. characteristics of the HA-5101/883 assure accurate performance. The 3mV (max) offset voltage is externally adjustable and offset voltage drift is just 3µV/°C. Low offset currents (200nA max) reduces input errors and with high open loop voltage gain of 100kV/V over temperature, increases the loop gain for low distortion amplification.

The HA-5101/883 is ideal for audio applications, expecially low-level signal amplifiers such as microphone, tape head, and preamplifiers. Additionally, it is well suited for low distortion oscillators, low noise function generators, and high Q filters.

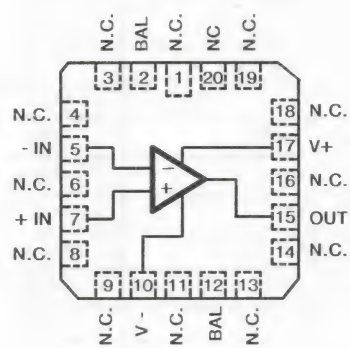
The HA-5101/883 has guaranteed operation from -55°C to +125°C, is available in Ceramic Mini-DIP, TO-99 Metal Can and 20 pin Ceramic LCC packages.

Pinouts

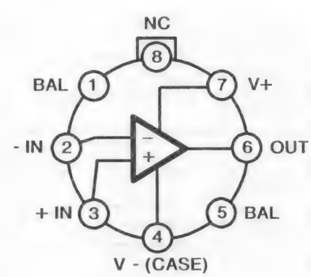
HA7-5101/883 (CERAMIC MINI-DIP)
TOP VIEW



HA4-5101/883 (CERAMIC LCC)
TOP VIEW



HA2-5101/883 (METAL CAN)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage 7V
Voltage at Either Input Terminal .... V+ to V-
Input Current 25mA
Output Short Circuit Duration .... Indefinite
Junction Temperature (T_J) .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... <2000V
Lead Temperature (Soldering 10 sec) .... +275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	82°C/W	23°C/W
Ceramic LCC Package	74°C/W	20°C/W
Metal Can Package	121°C/W	36°C/W

Package Power Dissipation Limit at +75°C for $T_J \leq$ +175°C
Ceramic DIP Package 1.22W
Ceramic LCC Package 1.35W
Metal Can Package 830mW
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 12.2mW/°C
Ceramic LCC Package .... 13.5mW/°C
Metal Can Package .... 8.3mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±5V to ±15V
$V_{INcm} \leq$ 1/2 (V+ - V-)
$R_L \geq$ 500Ω

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	V_{CM} = 0V	1	+25°C	-3	3	mV
			2, 3	+125°C, -55°C	-4	4	mV
Input Bias Current	$+I_B$	V_{CM} = 0V $+R_S$ = 100kΩ $-R_S$ = 100Ω	1	+25°C	-200	200	nA
			2, 3	+125°C, -55°C	-325	325	nA
	$-I_B$	V_{CM} = 0V $+R_S$ = 100Ω $-R_S$ = 100kΩ	1	+25°C	-200	200	nA
			2, 3	+125°C, -55°C	-325	325	nA
Input Offset Current	I_{IO}	V_{CM} = 0V $+R_S$ = 100kΩ $-R_S$ = 100kΩ	1	+25°C	-75	75	nA
			2, 3	+125°C, -55°C	-125	125	nA
Common Mode Range	+CMR	V+ = 3V V- = -27V	1	+25°C	12	-	V
			2, 3	+125°C, -55°C	12	-	V
	-CMR	V+ = 27V V- = -3V	1	+25°C	-	-12	V
			2, 3	+125°C, -55°C	-	-12	V
Large Signal Voltage Gain	$+A_{VOL}$	V_{OUT} = 0V and +10V R_L = 2kΩ	4	+25°C	100	-	kV/V
			5, 6	+125°C, -55°C	100	-	kV/V
	$-A_{VOL}$	V_{OUT} = 0V and -10V R_L = 2kΩ	4	+25°C	100	-	kV/V
			5, 6	+125°C, -55°C	100	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔV_{CM} = +10V +V = +5V -V = -25V V_{OUT} = -10V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	-CMRR	ΔV_{CM} = -10V +V = +25V -V = -5V V_{OUT} = +10V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Voltage Swing	$+V_{OUT1}$	R_L = 2kΩ	1	+25°C	12	-	V
			2, 3	+125°C, -55°C	12	-	V
	$-V_{OUT1}$	R_L = 2kΩ	1	+25°C	-	-12	V
			2, 3	+125°C, -55°C	-	-12	V
	$+V_{OUT2}$	V_{SUPPLY} = ±18V R_L = 600Ω	1	+25°C	15	-	V
			2, 3	+125°C, -55°C	15	-	V
	$-V_{OUT2}$	V_{SUPPLY} = ±18V R_L = 600Ω	1	+25°C	-	-15	V
			2, 3	+125°C, -55°C	-	-15	V
Output Current	$+I_{OUT}$	V_{OUT} = -15V V_{SUPPLY} = ±18V	1	+25°C	25	-	mA
			2, 3	+125°C, -55°C	25	-	mA
	$-I_{OUT}$	V_{OUT} = +15V V_{SUPPLY} = ±18V	1	+25°C	-	-25	mA
			2, 3	+125°C, -55°C	-	-25	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-	6	mA
			2, 3	+125°C, -55°C	-	6	mA
	$-I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-6	-	mA
			2, 3	+125°C, -55°C	-6	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = 10V +V = +10V, -V = -15V +V = +20V, -V = -15V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	-PSRR	ΔV_{SUP} = 10V +V = +15V, -V = -10V +V = +15V, -V = -20V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
Offset Voltage Adjustment	$+V_{IO}Adj$	Note 5 R_L = 2kΩ, C_L = 50pF A_V = +1V/V	1	+25°C	V_{IO}-1	-	mV
			2, 3	+125°C, -55°C	V_{IO}-1	-	mV
	$-V_{IO}Adj$		1	+25°C	V_{IO}+1	-	mV
			2, 3	+125°C, -55°C	V_{IO}+1	-	mV

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_{VCL} = +1V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Slew Rate	+SR	V_{OUT} = -3V to +3V	4	+25°C	6	-	V/µs
	-SR	V_{OUT} = +3V to -3V	4	+25°C	6	-	V/µs
Rise & Fall Time	T_R	V_{OUT} = 0 to +200mV 10% ≤ T_R ≤ 90%	4	+25°C	-	200	ns
			5, 6	+125°C, -55°C	-	400	ns
	T_F	V_{OUT} = 0 to -200mV 10% ≤ T_R ≤ 90%	4	+25°C	-	200	ns
			5, 6	+125°C, -55°C	-	400	ns
Overshoot	+OS	V_{OUT} = 0 to +200mV	4	+25°C	-	35	%
			5, 6	+125°C, -55°C	-	35	%
	-OS	V_{OUT} = 0 to -200mV	4	+25°C	-	35	%
			5, 6	+125°C, -55°C	-	35	%

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_V = +1, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Differential Input Resistance	R_{IN}	V_{CM} = 0V	1	+25°C	250	-	kΩ
Low Frequency Peak-to-Peak Noise	E_{np-p}	0.1Hz to 10Hz	1	+25°C	-	0.2	μV_{p-p}
Input Noise Voltage Density	E_n	R_S = 20Ω, f_o = 1000Hz	1, 4	+25°C	-	4.5	$nV/\sqrt{Hz}$
Input Noise Current Density	I_n	R_S = 2MΩ, f_o = 1000Hz	1, 4	+25°C	-	3	$pA/\sqrt{Hz}$
Unity Gain Bandwidth	UGBW	V_O = 100mV	1	+25°C	10	-	MHz
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	+25°C	95	-	kHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 2kΩ, C_L = 50pF	1	-55°C to +125°C	+1	-	V/V
Output Resistance	R_{OUT}	Open Loop	1	+25°C	-	150	Ω
Quiescent Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	180	mW

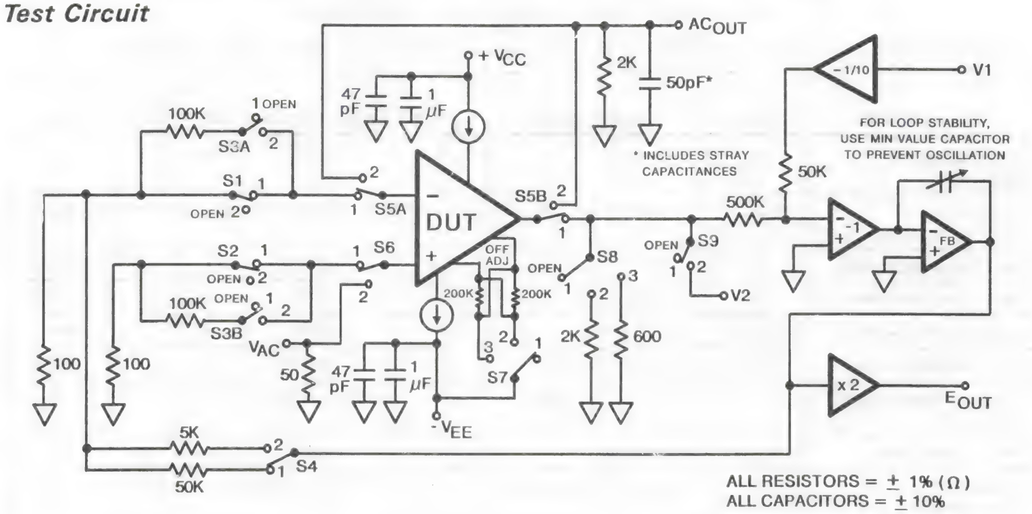
NOTES:
1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).
3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)
4. Input Noise Voltage Density and Input Noise Current Density is sample tested on every lot.
5. Offset adjustment range is [V_{IO} (Measured) ± 1mV] minimum referred to output. This test is for functionality only to assure adjustment through 0V.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6
Group A Test Requirements	1, 2, 3, 4, 5, 6
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

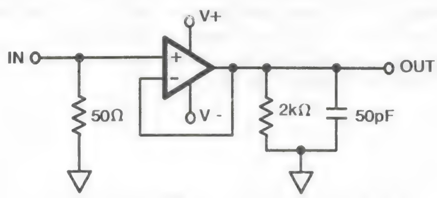
Test Circuit



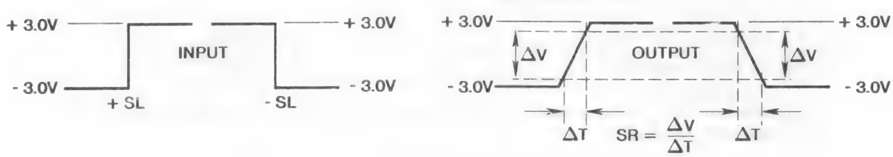
For Detailed Information, Refer to HA-5101/883 Test Tech Brief

Test Waveforms

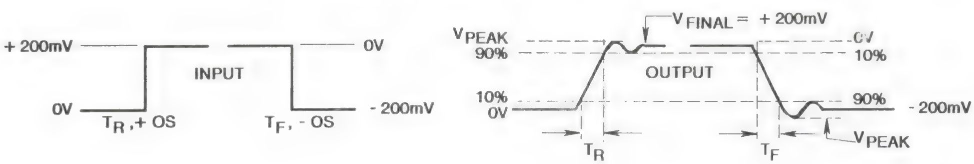
SIMPLIFIED TEST CIRCUIT (Applies To Tables 2 And 3)



SLEW RATE WAVEFORMS

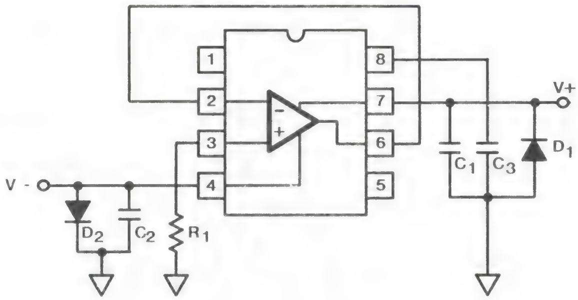


OVERSHOOT, RISE/FALL TIME WAVEFORMS

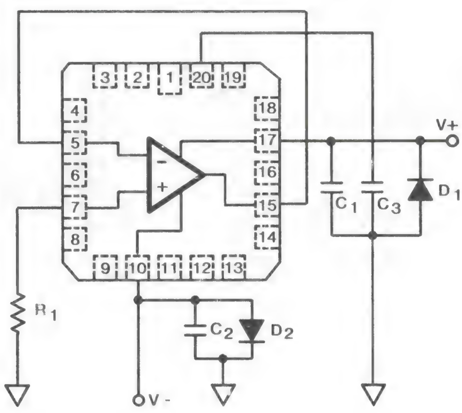


Burn-In Circuits

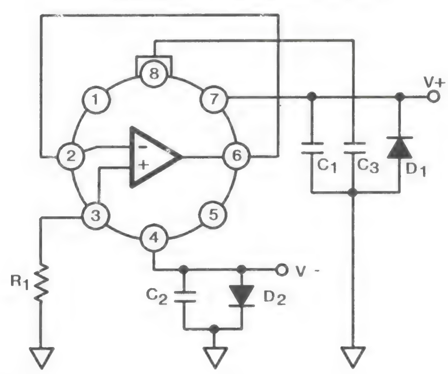
HA7-5101/883 CERAMIC MINI-DIP



HA4-5101/883 CERAMIC LCC



HA2-5101/883 (TO-99) METAL CAN



NOTES:

R_1 = 1MΩ, ±5%, 1/4W (Min)

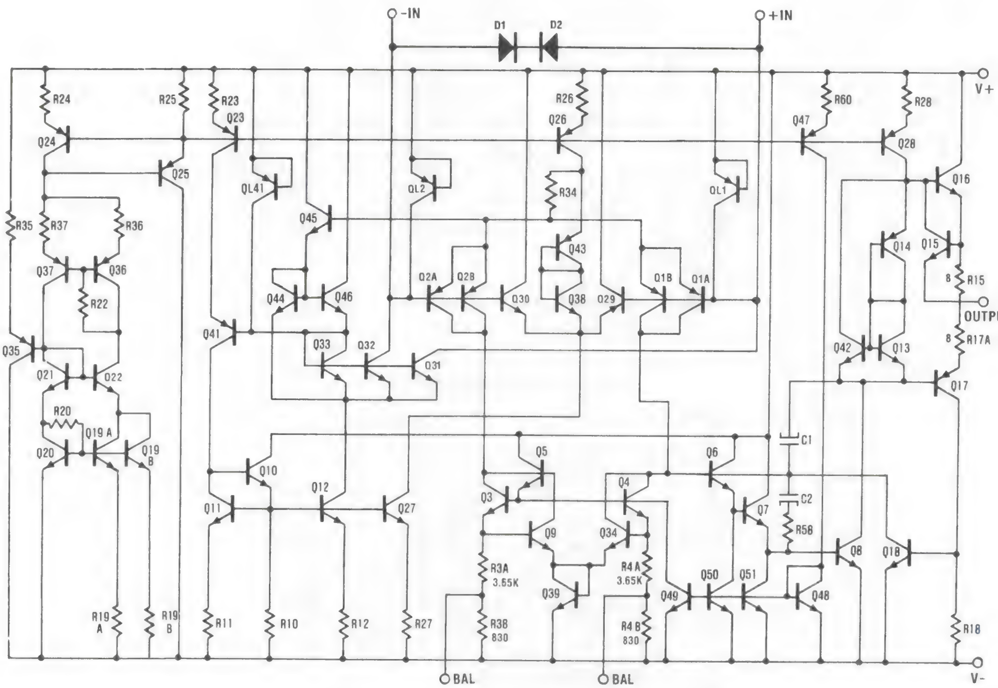
$C_1 = C_2$ = 0.01μF/Socket (Min) or 0.1μF/Row, (Min)

C_3 = 0.01μF/Socket, 10%

$D_1 = D_2$ = IN4002 or Equivalent/Board

$|(V+) - (V-)| = 30V$

Schematic Diagram



Die Characteristics

DIE DIMENSIONS:
68.9 x 69.3 x 19 mils
(1750 x 1760 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
1.38 x 10^5A/cm^2 at 30mA

SUBSTRATE POTENTIAL (POWERED UP): V-

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

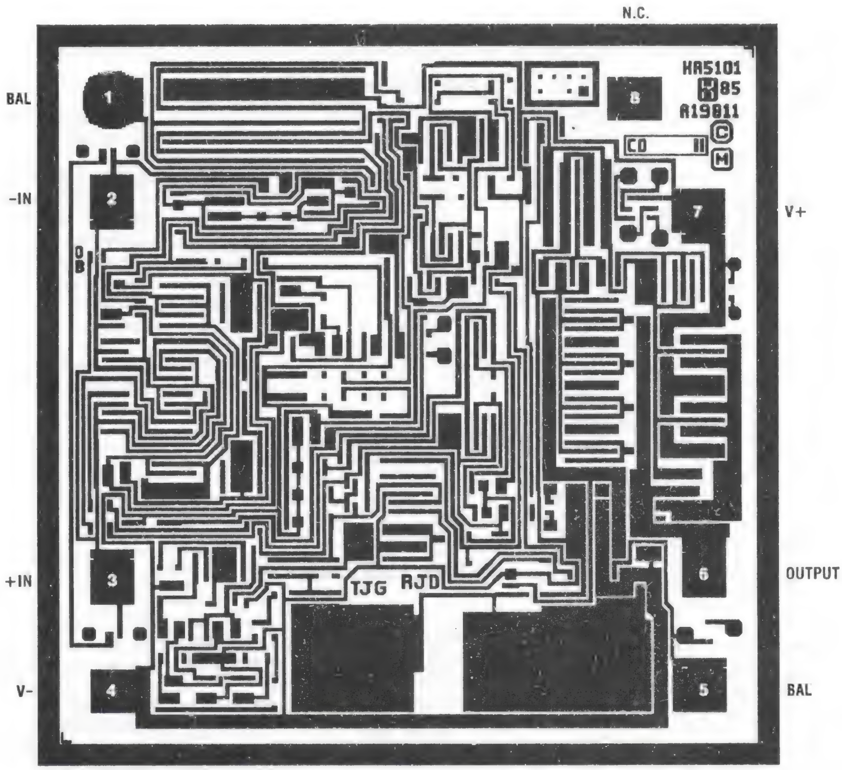
TRANSISTOR COUNT: 54

PROCESS: HFSB Bipolar Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)
Metal Can — 420°C (Max)

Metallization Mask Layout

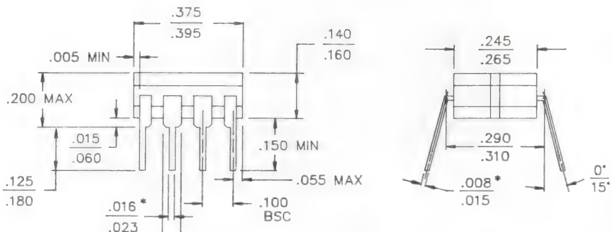
HA-5101/883



NOTE: Pin Numbers Correspond to Ceramic Mini-DIP and Metal Can Packages Only.

Packaging †

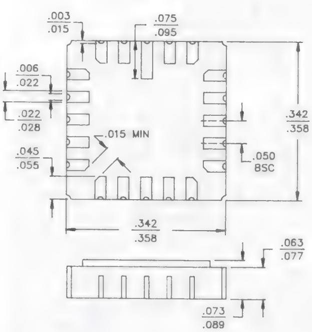
8 PIN CERAMIC DIP



* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

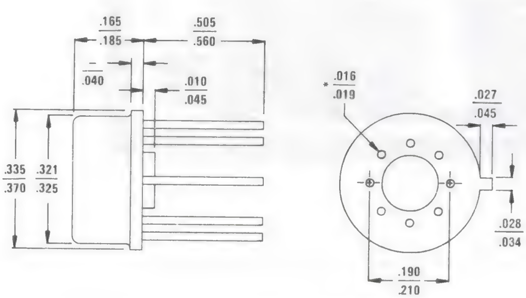
LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-4

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Ceramic, 90% Al_2O_3
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

8 PIN TO-99 METAL CAN



LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
Material: No Seal Material
Temperature: Room Temperature
Method: Resistance Weld
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic Bonded
COMPLIANT OUTLINE: 38510 A-1

*Dimension Maximum Limits Are Increased by 0.003 inches for Solder Dip Finish

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

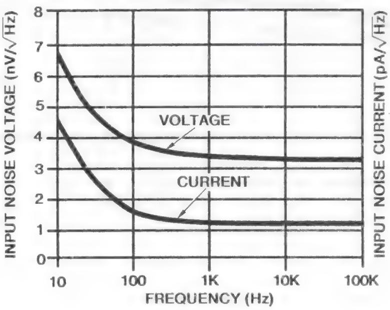
DESIGN INFORMATION

Low Noise, High Performance Operational Amplifier

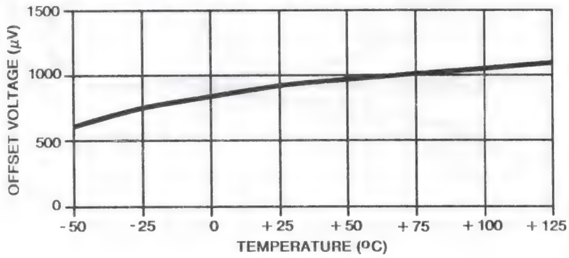
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $V\pm = \pm 15V$, $T_A = +25^oC$

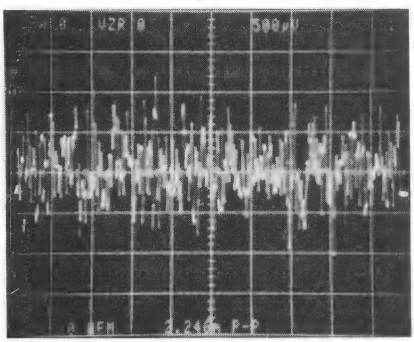
HA-5101 NOISE SPECTRUM



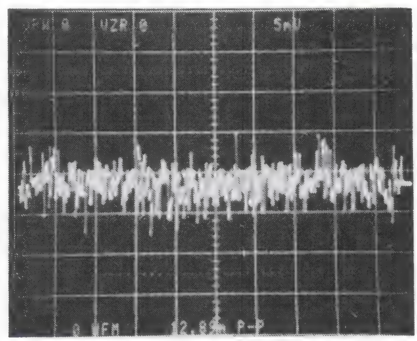
OFFSET VOLTAGE vs. TEMPERATURE



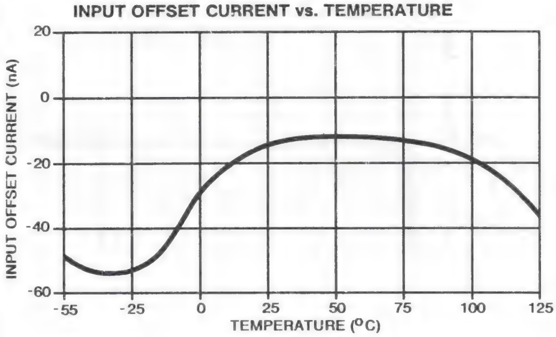
PEAK-TO-PEAK NOISE 0.1Hz TO 10Hz
$A_V = 25{,}000$, $V_{CC} = \pm 15V$
($0.09\mu V_{p-p}$ RTI)



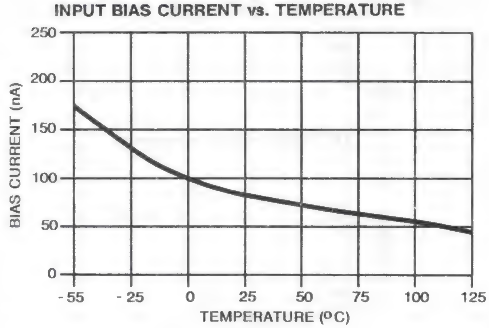
PEAK-TO-PEAK TOTAL NOISE 0.1Hz TO 1MHz
$A_V = 25{,}000$, $V_{CC} = \pm 15V$
($12.89mV_{p-p}$ RTO or $0.52\mu V_{p-p}$ RTI)



INPUT OFFSET CURRENT vs. TEMPERATURE



INPUT BIAS CURRENT vs. TEMPERATURE

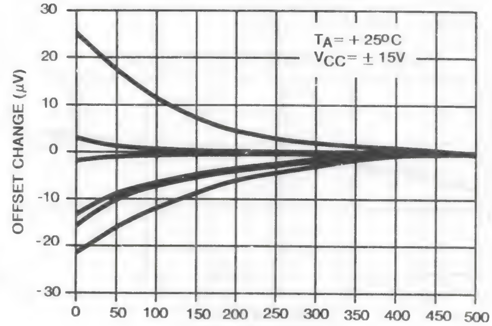


DESIGN INFORMATION (Continued)

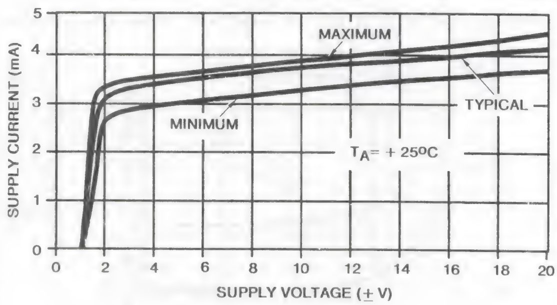
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: V± = ±15V, T_A = +25°C

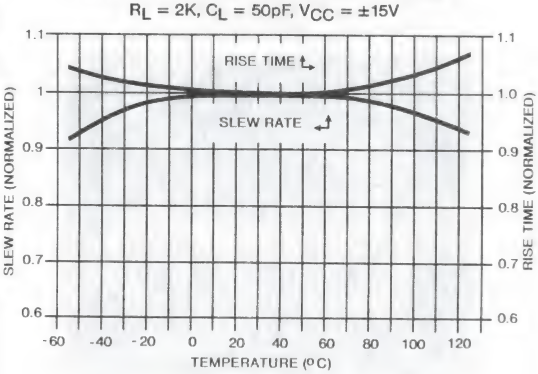
INPUT OFFSET WARMUP DRIFT vs. TIME
(Normalized to Zero Final Value)
(Six Representative Units)



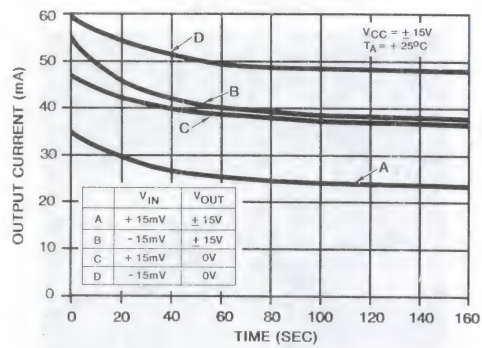
SUPPLY CURRENT vs. SUPPLY VOLTAGE



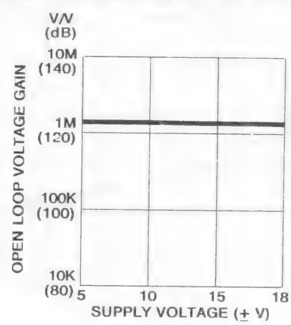
SLEW RATE/RISE TIME vs. TEMPERATURE
R_L = 2K, C_L = 50pF, V_{CC} = ±15V



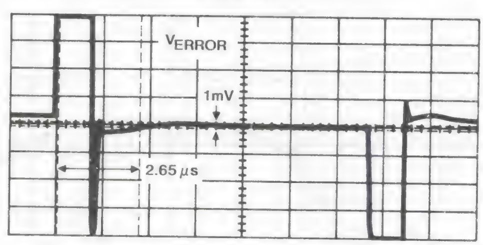
SHORT CIRCUIT CURRENT vs. TIME



D.C. OPEN LOOP VOLTAGE GAIN vs. SUPPLY VOLTAGE



HA-5101 SETTLING WAVEFORM
1.5ms/DIV.



DESIGN INFORMATION (Continued)

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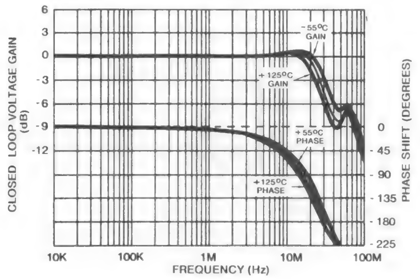
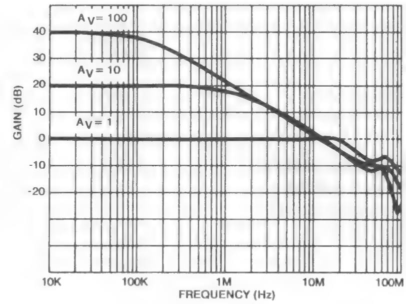
Typical Performance Curves Unless Otherwise Specified: $V\pm = \pm 15V$, $T_A = +25^oC$

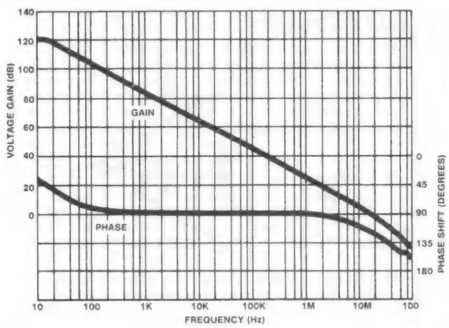
HA-5101 CLOSED LOOP GAIN AND PHASE AT HIGH AND LOW TEMPERATURE
(Typical Response of One Amplifier)
$V_{CC} = \pm 15V$, $A_V = 1V/V$, $R_L = 2K$, $C_L = 50pF$



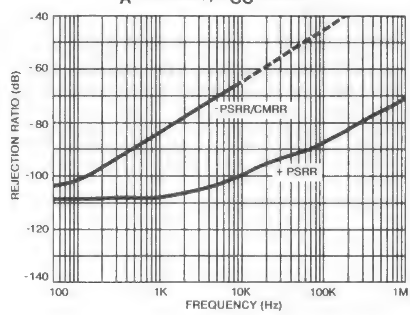
HA-5101 CLOSED LOOP VOLTAGE GAIN vs. FREQUENCY AT DIFFERENT CLOSED LOOP GAINS
$T_A = +25^oC$, $V_{CC} = \pm 15V$, $R_L = 2K$, $C_L = 50pF$



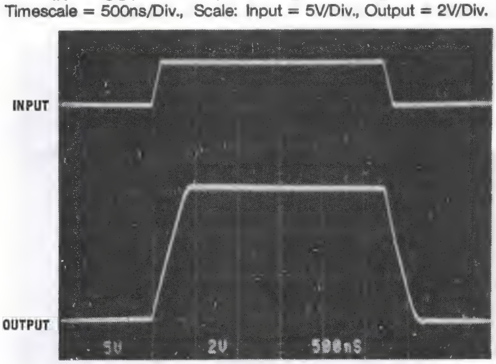
OPEN LOOP GAIN/PHASE vs. FREQUENCY



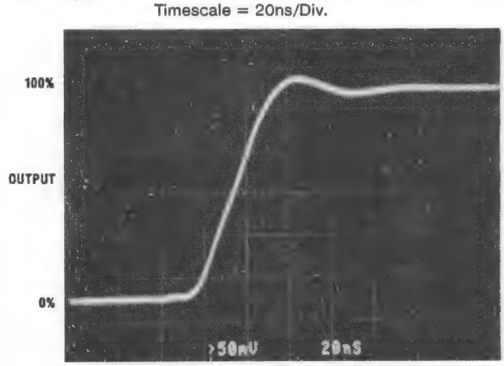
HA-5101 REJECTION RATIOS vs. FREQUENCY
$T_A = +25^oC$, $V_{CC} = \pm 15V$



SLEW RATE WAVEFORM
$V_{IN} = V_{OUT} = \pm 3V$, $A_V = +1$, $R_L = 2k\Omega$, $C_L = 50pF$
Timescale = 500ns/Div., Scale: Input = 5V/Div., Output = 2V/Div.



SMALL SIGNAL WAVEFORM
Rise Time and Overshoot
$V_{IN} = V_{OUT} = 0V$ to $+200mV$, $A_V = +1$, $R_L = 2K$, $C_L = 50pF$
Timescale = 20ns/Div.



DESIGN INFORMATION (Continued)

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Applications Information

OPERATION AT ±5V SUPPLY

The HA-5101 performs well at V_{CC} = ±5V exhibiting typical characteristics as listed below:

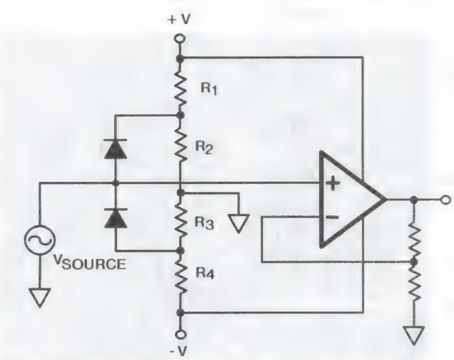
I_{CC}	3.7	mA
V_{IO}	0.5	mV
I_{BIAS}	56	nA
A_{VOL} (V_O = ±3V)	106	KV/V
V_{OUT}	3.7	V
I_{OUT}	13	mA
CMRR (ΔV_{CM} = ±2.5V)	90	dB
PSRR (ΔV_{CC} = 0.5V)	90	dB
Unity Bandwidth (5101)	10	MHz
Slew Rate (5101)	7	V/µs

INPUT PROTECTION

The HA-5101 has built-in back-to-back protection diodes which will limit the differential input voltage to approximately 7V. If the HA-5101 will be used in conditions where that voltage may be exceeded, then current limiting resistors must be used. No more than 25mA should be allowed to flow in the HA-5101 input.

OUTPUT SATURATION

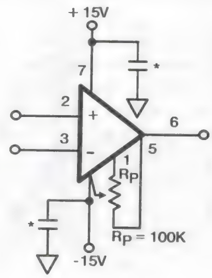
When an operational amplifier is overdriven, output devices can saturate and and sometimes take a long time to recover. Saturation can be avoided (sometimes) by using circuits such as:



If saturation cannot be avoided the HA-5101 recovers from a 25% overdrive in about 6.5µs (see photo).

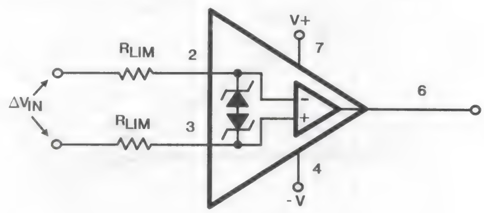
OFFSET ADJUSTMENT

The following is the recommended V_{IO} adjust configuration:



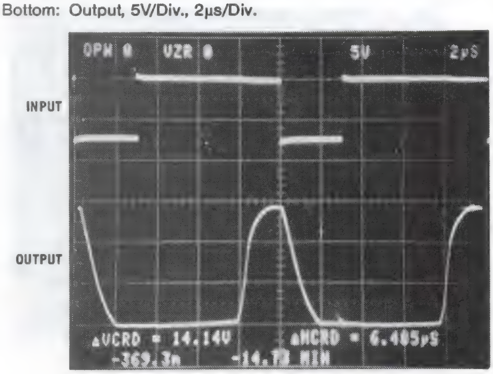
* Proper decoupling is always recommended, 0.1µF high quality capacitors should be at or vary near the device's supply pins.

COMPARATOR CIRCUIT



Choose R_{LIM} Such That $\frac{(\Delta V_{IN}MAX - 7V)}{25mA} \leq 2R_{LIM}$

Top: Input
Bottom: Output, 5V/Div., 2µs/Div.



Output is overdriven negative, recovers after 6µs.

DESIGN INFORMATION (Continued)

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TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_L = 2kΩ, C_L = 50pF, A_{VCL} = +1V/V Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMITS	UNITS
Offset Voltage	V_{CM} = 0V	+25°C	0.8	Table 1	mV
Offset Voltage Average Drift	Versus Temperature	-55°C to +125°C	3	7	μV/°C
Offset Current Average Drift	Versus Temperature	-55°C to +125°C	100	250	pA/°C
Input Bias Current	V_{CM} = 0V	+25°C	65	Table 1	nA
Input Offset Current	V_{CM} = 0V	+25°C	35	Table 1	nA
Differential Input Resistance	V_{CM} = 0V	+25°C	500	Table 3	kΩ
Input Noise Voltage Density	f_O = 10Hz	+25°C	5.4	9	$nV/\sqrt{Hz}$
	f_O = 100Hz	+25°C	3.4	5.5	$nV/\sqrt{Hz}$
	f_O = 1kHz	+25°C	3.2	Table 3	$nV/\sqrt{Hz}$
Input Noise Current Density	f_O = 10Hz	+25°C	6	20	$pA/\sqrt{Hz}$
	f_O = 100Hz	+25°C	1.5	5	$pA/\sqrt{Hz}$
	f_O = 1kHz	+25°C	0.52	Table 3	$pA/\sqrt{Hz}$
Large Signal Voltage Gain	V_{OUT} = ±10V	-55°C	400K	Table 1	V/V
		+25°C	1M	Table 1	V/V
		+125°C	1M	Table 1	V/V
Slew Rate	V_{OUT} = ±3V	-55°C to +125°C	10	5.4	V/μs
Full Power Bandwidth	Note 2, V_{peak} = 10V	-55°C to +125°C	159	85	kHz
Rise and Fall Times	V_{OUT} = ±200mV	-55°C to +125°C	50	Table 2	ns
Overshoot	V_{OUT} = ±200mV	-55°C to +125°C	20	35	%
Settling Time	To 0.1% for 10V Step	+25°C	4.5	6	μs
	To 0.01% for 10V Step	+25°C	6	10	μs
Output Short Circuit Current	t <10 Seconds, V_{OUT} = ±15V	+25°C	±35	±50	mA
Output Resistance	Open Loop	+25°C	110	Table 3	Ω
Supply Current	No Load	+25°C	4.3	Table 1	mA
Minimum Supply Voltage	Functional Operation Only, Other Parameters Will Vary	+25°C	±4	±5	V

HARRIS

HA-5102/883

Dual, Low Noise, High Performance Operational Amplifier

January 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low Input Noise Voltage Density @ 1kHz ... 6nV/$\sqrt{Hz}$ Max, 4.3nV/$\sqrt{Hz}$ Typ
- High Slew Rate ... 1V/μs Min, 3V/μs Typ
- Unity Gain Bandwidth ... 8MHz Typ
- High Open Loop Gain (Full Temp) ... 100kV/V Min, 250kV/V Typ
- High CMRR, PSRR (Full Temp) ... 86dB Min, 100dB Typ
- Low Offset Voltage Drift ... 3μV/°C Typ
- No Crossover Distortion
- Standard Dual Pinout

Applications

- High Quality Audio Preamplifiers
- High Q Active Filters
- Low Noise Function Generators
- Low Distortion Oscillators
- Low Noise Comparators

Description

Low noise and high performance are key words describing the unity gain stable HA-5102/883. This general purpose dual amplifier offers an array of dynamic specifications including 1V/μs slew rate (min), $A_{VCL} \geq 1$, and 8MHz bandwidth (typ). Complementing these outstanding parameters is a very low noise specification of 4.3nV/$\sqrt{Hz}$ at 1kHz (typ), 6nV/$\sqrt{Hz}$ (max).

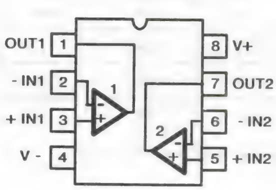
Fabricated using the Harris standard high frequency D.I. process, these operational amplifiers also offer excellent input specifications such as 2.5mV (max) offset voltage and 75nA (max) offset current. Complementing these specifications are 100dB (min) open loop gain and 100dB channel separation (typ). Economically, the HA-5102/883 also consumes a very moderate amount of supply power 180mW/package.

This impressive combination of features make this amplifier ideally suited for designs ranging from audio amplifiers and active filters to the most demanding signal conditioning and instrumentation circuits.

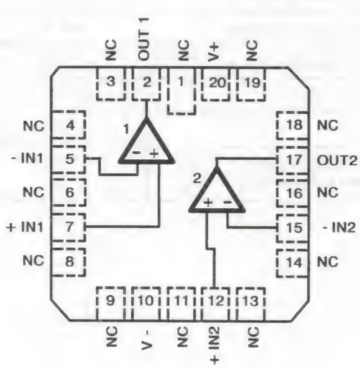
This dual operational amplifier is available with industry standard pinouts allowing for immediate interchangeability with most other dual operational amplifiers. HA-5102/883 is available in an 8 pin Ceramic Mini-DIP, 20 pin LCC and an 8 pin Metal Can (TO-99).

Pinouts

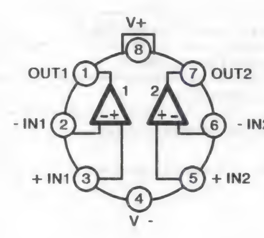
HA7-5102/883 (CERAMIC MINI-DIP)
TOP VIEW



HA4-5102/883 (CERAMIC LCC)
TOP VIEW



HA2-5102/883 (METAL CAN)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage 7V
Voltage at Either Input Terminal .... V+ to V-
Peak Output Current .... Indefinite
(One Amplifier Shorted to Ground)
Junction Temperature (T_J) .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... <2000V
Lead Temperature (Soldering 10 sec) .... +275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	82°C/W	26°C/W
Ceramic LCC Package	74°C/W	20°C/W
Metal Can Package	101°C/W	30°C/W

Package Power Dissipation at +75°C for $T_J \le$ +175°C
Ceramic DIP Package 1.22W
Ceramic LCC Package 1.36W
Metal Can Package 1W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 12.2mW/°C
Ceramic LCC Package .... 13.6mW/°C
Metal Can Package .... 10mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±5V to ±15V
$V_{INcm} \le 1/2 (V+ - V-)$
$R_L \ge 2k\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, $R_{SOURCE} = 100\Omega$, $R_{LOAD} = 500k\Omega$, $V_{OUT} = 0V$, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	$V_{CM} = 0V$	1	+25°C	-2.0	2.0	mV
			2, 3	+125°C, -55°C	-2.5	2.5	mV
Input Bias Current	$+I_B$	$V_{CM} = 0V$ $+R_S = 10k\Omega$ $-R_S = 100\Omega$	1	+25°C	-200	200	nA
			2, 3	+125°C, -55°C	-325	325	nA
	$-I_B$	$V_{CM} = 0V$ $+R_S = 100\Omega$ $-R_S = 10k\Omega$	1	+25°C	-200	200	nA
			2, 3	+125°C, -55°C	-325	325	nA
Input Offset Current	I_{IO}	$V_{CM} = 0V$ $+R_S = 10k\Omega$ $-R_S = 10k\Omega$	1	+25°C	-75	75	nA
			2, 3	+125°C, -55°C	-125	125	nA
Common Mode Range	+CMR	V+ = 3V V- = -27V	1	+25°C	+12	-	V
			2, 3	+125°C, -55°C	+12	-	V
	-CMR	V+ = 27V V- = -3V	1	+25°C	-	-12	V
			2, 3	+125°C, -55°C	-	-12	V
Large Signal Voltage Gain	$+A_{VOL}$	V_{OUT} = 0V and +10V $R_L = 2k\Omega$	4	+25°C	100	-	kV/V
			5, 6	+125°C, -55°C	100	-	kV/V
	$-A_{VOL}$	V_{OUT} = 0V and -10V $R_L = 2k\Omega$	4	+25°C	100	-	kV/V
			5, 6	+125°C, -55°C	100	-	kV/V
Common Mode Rejection Ratio	+CMRR	$\Delta V_{CM} = +5V$ +V = +10V -V = -20V $V_{OUT} = -5V$	1	+25°C	86	-	dB
			2, 3	+125°C, -55°C	86	-	dB
	-CMRR	$\Delta V_{CM} = -5V$ +V = +20V -V = -10V $V_{OUT} = +5V$	1	+25°C	86	-	dB
			2, 3	+125°C, -55°C	86	-	dB

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

3
OP AMPs & COMPARATORS

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Voltage Swing	$+V_{OUT1}$	$R_L = 2k\Omega$	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	$-V_{OUT1}$	$R_L = 2k\Omega$	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
	$+V_{OUT2}$	$R_L = 10k\Omega$	1	+25°C	12	-	V
			2, 3	+125°C, -55°C	12	-	V
	$-V_{OUT2}$	$R_L = 10k\Omega$	1	+25°C	-	-12	V
			2, 3	+125°C, -55°C	-	-12	V
Output Current	$+I_{OUT}$	$V_{OUT} = -5V$	1	+25°C	10	-	mA
			2, 3	+125°C, -55°C	10	-	mA
	$-I_{OUT}$	$V_{OUT} = +5V$	1	+25°C	-	-10	mA
			2, 3	+125°C, -55°C	-	-10	mA
Quiescent Power Supply Current	$+I_{CC}$	$V_{OUT} = 0V$	1	+25°C	-	5.0	mA
		$I_{OUT} = 0mA$	2, 3	+125°C, -55°C	-	6.0	mA
	$-I_{CC}$	$V_{OUT} = 0V$ $I_{OUT} = 0mA$	1	+25°C	-5.0	-	mA
			2, 3	+125°C, -55°C	-6.0	-	mA
Power Supply Rejection Ratio	+PSRR	$\Delta V_{SUP} = 10V$ +V = +10V, -V = -15V +V = +20V, -V = -15V	1	+25°C	86	-	dB
			2, 3	+125°C, -55°C	86	-	dB
	-PSRR	$\Delta V_{SUP} = 10V$ +V = +15V, -V = -10V +V = +15V, -V = -20V	1	+25°C	86	-	dB
			2, 3	+125°C, -55°C	86	-	dB

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_{VCL} = +1V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Slew Rate	+SR	V_{OUT} = -3V to +3V	4	+25°C	1	-	V/µs
	-SR	V_{OUT} = +3V to -3V	4	+25°C	1	-	V/µs
Rise & Fall Time	T_R	V_{OUT} = 0 to +200mV $10\% \leq T_R \leq 90\%$	4	+25°C	-	200	ns
	T_F	V_{OUT} = 0 to -200mV $10\% \leq T_F \leq 90\%$	4	+25°C	-	200	ns
Overshoot	+OS	V_{OUT} = 0 to +200mV	4	+25°C	-	35	%
	-OS	V_{OUT} = 0 to -200mV	4	+25°C	-	35	%

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_{VCL} = 10V/V Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Differential Input Resistance	R_{IN}	$V_{CM} = 0V$	1	+25°C	250	-	kΩ
Input Noise Voltage Density	E_n	$R_S = 20\Omega$, $f_o = 1000Hz$	1	+25°C	-	6	$nV/\sqrt{Hz}$
Input Noise Current Density	I_n	$R_S = 2M\Omega$, $f_o = 1000Hz$	1	+25°C	-	3	$pA/\sqrt{Hz}$
Full Power Bandwidth	FPBW	$V_{PEAK} = 10V$	1, 2	+25°C	32	-	kHz
Minimum Closed Loop Stable Gain	CLSG	$R_L = 2k\Omega$, $C_L = 50pF$	1	-55°C to +125°C	+1	-	V/V
Output Resistance	R_{OUT}	Open Loop	1	+25°C	-	150	Ω
Quiescent Power Consumption	PC	$V_{OUT} = 0V$, $I_{OUT} = 0mA$	1, 3	-55°C to +125°C	-	180	mW
Channel Separation	CS	$R_S = 1k\Omega$, $A_{VCL} = 100V/V$, $V_{IN} = 100mV_{RMS}$ @ 10kHz Referred to Input	1	+25°C	90	-	dB

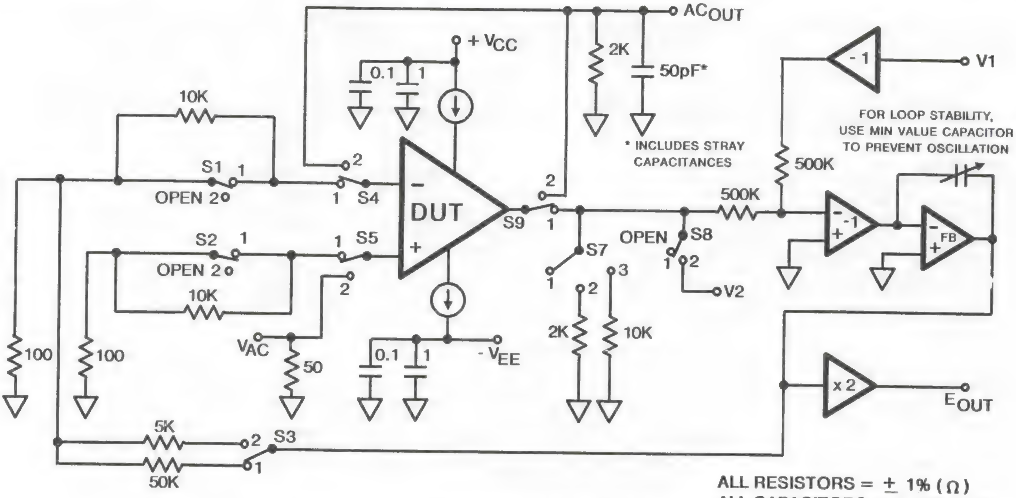
NOTES:
1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).
3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6
Group A Test Requirements	1, 2, 3, 4, 5, 6
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

Test Circuit

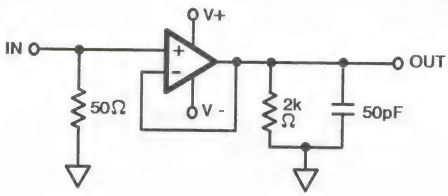


ALL RESISTORS = ± 1% (Ω)
ALL CAPACITORS = ± 10% (μF)
DUT = 1/2 OF HA - 5102/883

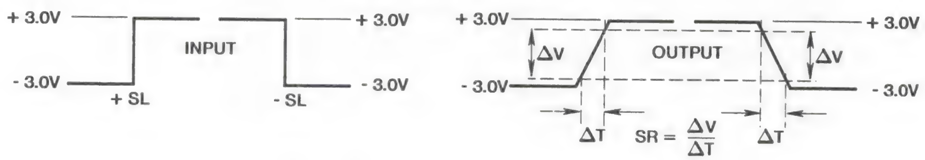
ONE OF TWO TEST LOOPS FOR THE HA - 5102/883

Test Waveforms

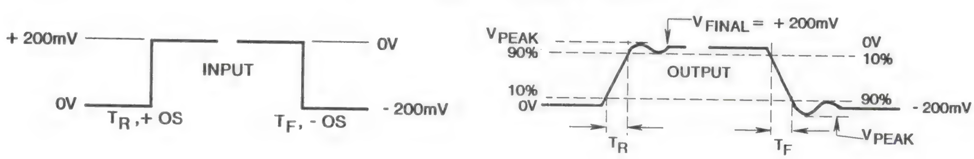
SIMPLIFIED TEST CIRCUIT (Applies To Tables 2 and 3)



SLEW RATE WAVEFORMS

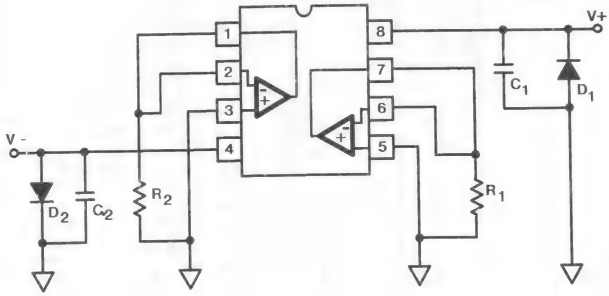


OVERSHOOT, RISE/FALL TIME WAVEFORMS

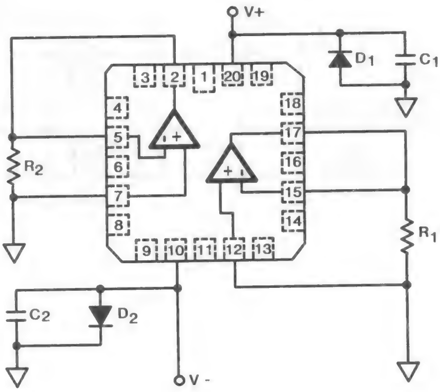


Burn-In Circuits

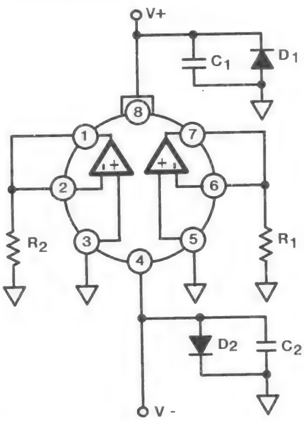
HA7-5102/883 CERAMIC MINI-DIP



HA4-5102/883 CERAMIC LCC



HA2-5102/883 TO-99 METAL CAN



NOTES:

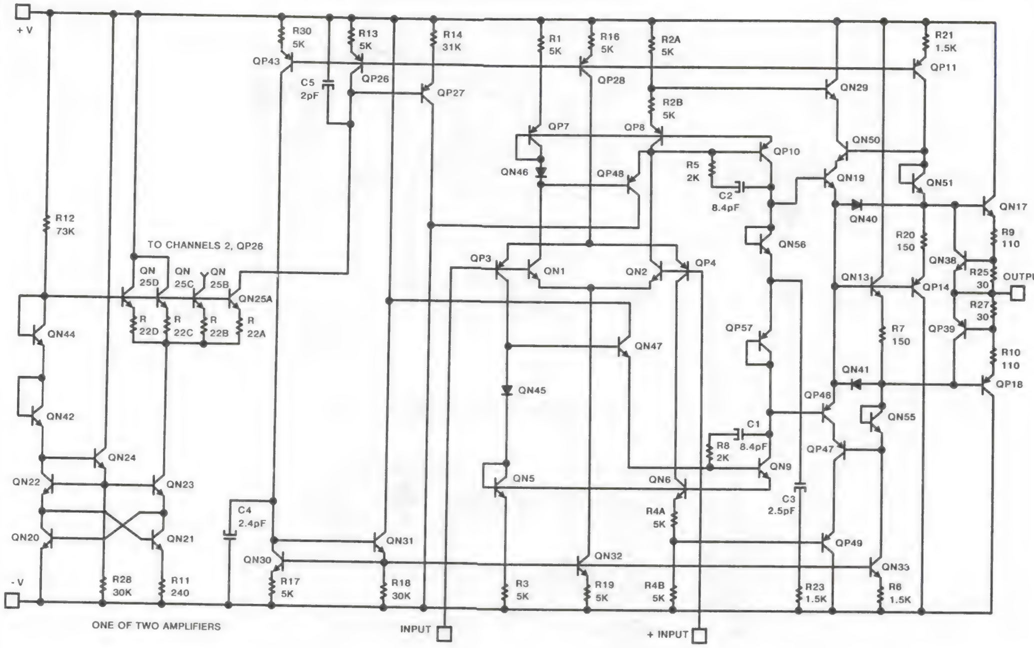
$R_1 = R_2 = 2k\Omega$, ±5%, 1/4W/Socket (Min)

$C_1 = C_2 = 0.01\mu F$/Socket (Min) or $0.1\mu F$/Row (Min)

$D_1 = D_2$ = IN4002 or Equivalent/Board

$|(V+) - (V-)| = 30V$

Schematic Diagram (½ HA-5102/883)



Die Characteristics

DIE DIMENSIONS:
98.4 x 67.3 x 19 mils
(2500 x 1710 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$1.43 \times 10^5 A/cm^2$ at 10mA

SUBSTRATE POTENTIAL (POWERED UP):
Unbiased

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

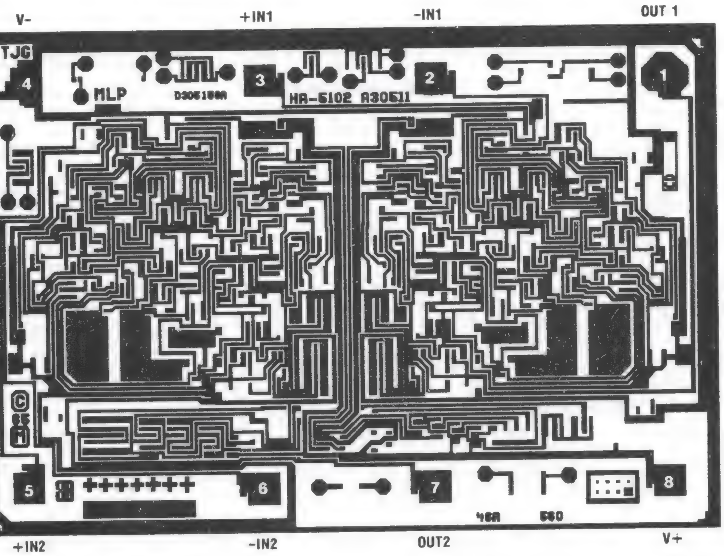
TRANSISTOR COUNT: 93

PROCESS: HFSB Linear Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)
Metal Can — 420°C (Max)

Metallization Mask Layout

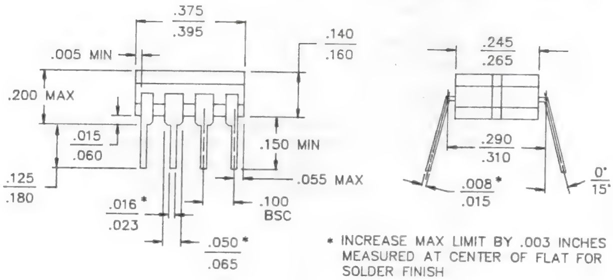
HA-5102/883



NOTE: Pin Numbers Correspond to Mini-DIP and Metal Can Packages Only.

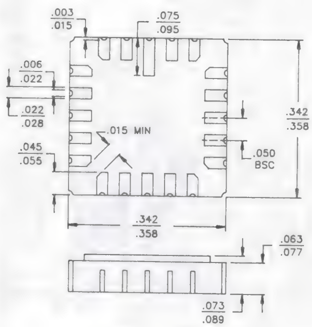
Packaging †

8 PIN CERAMIC DIP



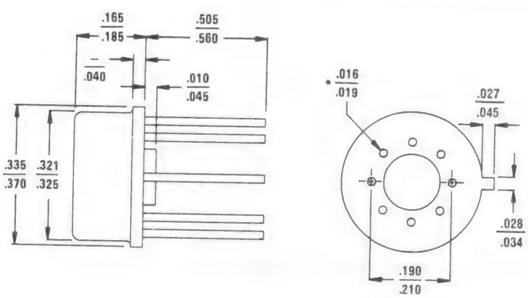
LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-4

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Ceramic, 90% Al_2O_3
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

8 PIN TO-99 METAL CAN



LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
Material: No Seal Material
Temperature: Room Temperature
Method: Resistance Weld
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic Bonded
COMPLIANT OUTLINE: 38510 A-1

*Dimension Maximum Limits Are Increased by 0.003 inches for Solder Dip Finish

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

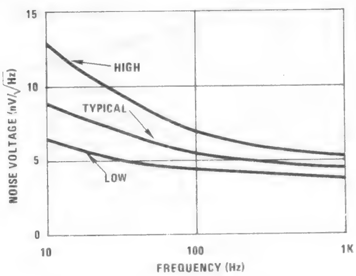
DESIGN INFORMATION

Dual, Low Noise, High Performance Operational Amplifier

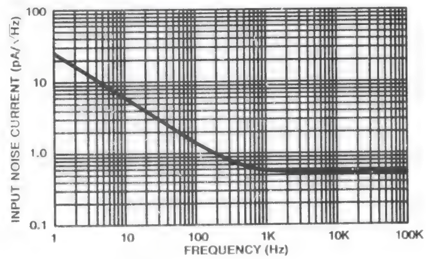
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

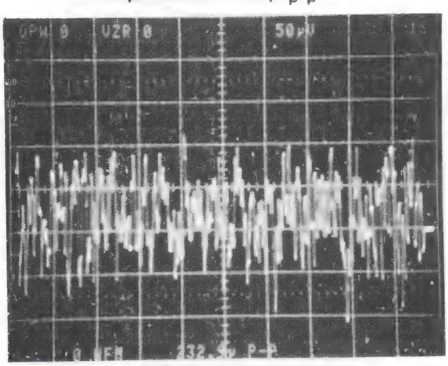
INPUT NOISE VOLTAGE DENSITY
$V_{CC} = \pm15V$, $T_A = +25^oC$



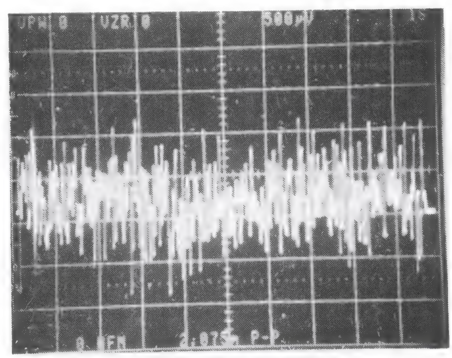
INPUT NOISE CURRENT DENSITY
$V_{CC} = \pm15V$, $T_A = +25^oC$



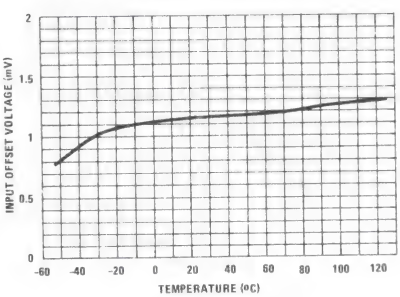
0.1Hz TO 10Hz NOISE
$V_{CC} = \pm15V$, $T_A = +25^oC$
50μV/Div., 1s/Div., A_V = 1000V/V
Input Noise = 0.232μV_{p-p}



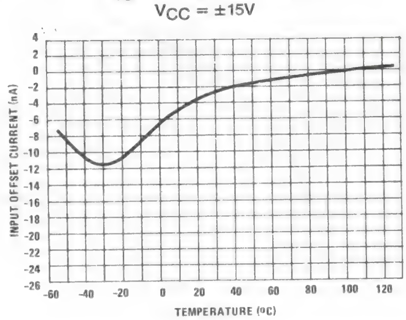
0.1Hz TO 1MHz NOISE
$V_{CC} = \pm15V$, $T_A = +25^oC$
500μV/Div., 1s/Div., A_V = 1000V/V
Total Output Noise = 2.075μV_{p-p}



V_{IO} vs. TEMPERATURE
$V_{CC} = \pm15V$



I_{IO} vs. TEMPERATURE
$V_{CC} = \pm15V$



DESIGN INFORMATION (Continued)

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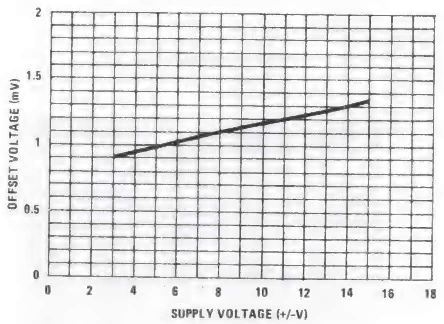
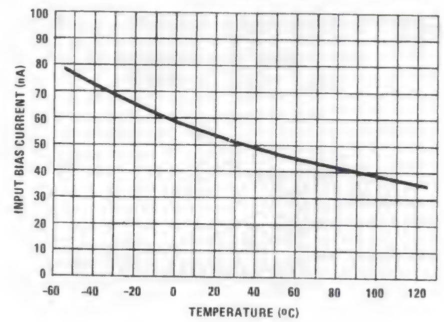
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

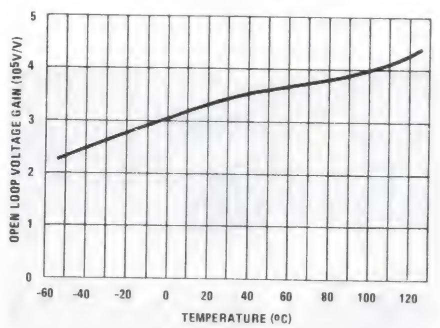
V_{IO} vs. V_{CC}
$T_A = +25^oC$



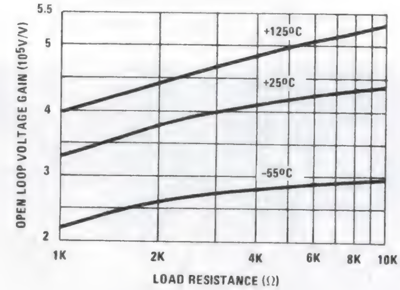
I_{BIAS} vs. TEMPERATURE
$V_{CC} = \pm15V$



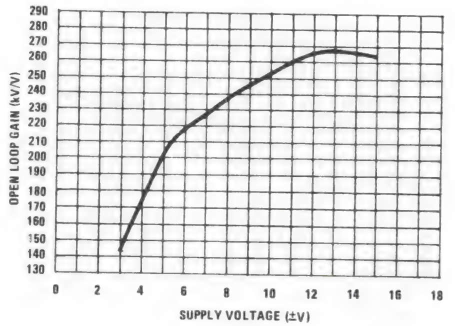
A_{VOL} vs. TEMPERATURE
VCC = $\pm15V$, $\Delta V_O = \pm10V$, R_L = 2K



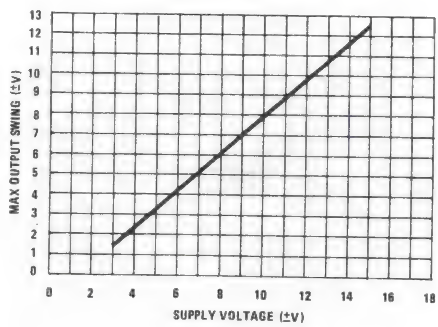
A_{VOL} vs. LOAD RESISTANCE
$V_O = \pm10V$, $V_{CC} = \pm15V$, $T_A = +25^oC$



A_{VOL} vs. V_{CC}
$T_A = +25^oC$, R_L = 2K



V_{OUT} vs. V_{CC}
$T_A = +25^oC$, R_L = 2K



DESIGN INFORMATION (Continued)

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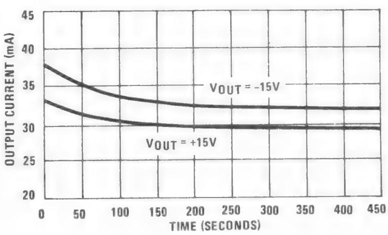
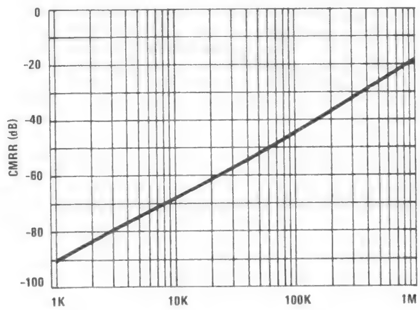
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

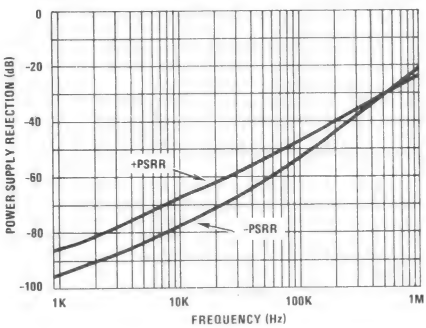
OUTPUT SHORT-CIRCUIT CURRENT vs. TIME
$V_{CC} = \pm 15V$, $T_A = +25^oC$



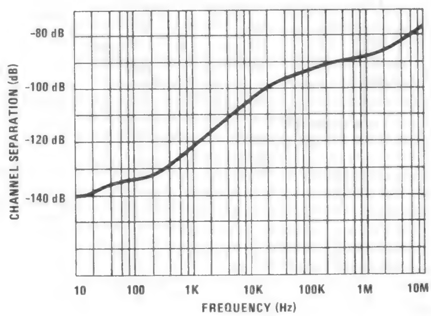
CMRR vs. FREQUENCY



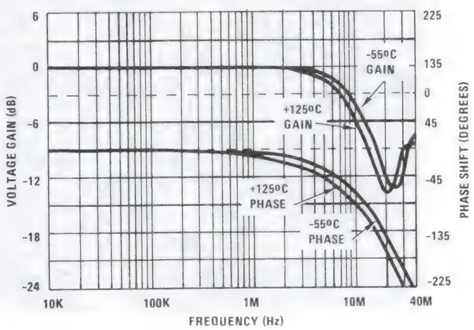
PSRR vs. FREQUENCY



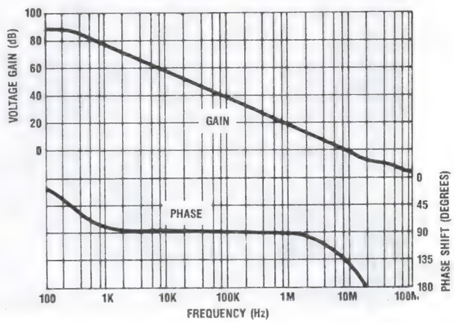
CHANNEL SEPARATION vs. FREQUENCY
$10Hz \leq f \leq 10MHz$



HA-5102 UNITY GAIN FREQUENCY RESPONSE
$V_{CC} = \pm 15V$, $R_L = 2K$, $C_L = 50pF$



OPEN-LOOP GAIN vs. FREQUENCY
$V_{CC} = \pm 15V$, $R_L = 2K$, $C_L = 50pF$, $T_A = +25^oC$



DESIGN INFORMATION (Continued)

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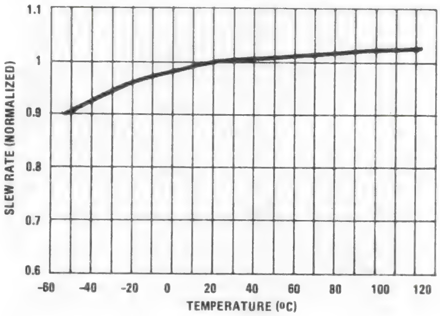
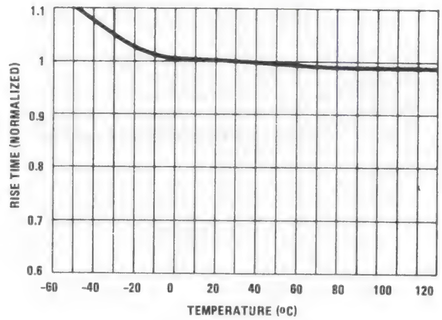
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

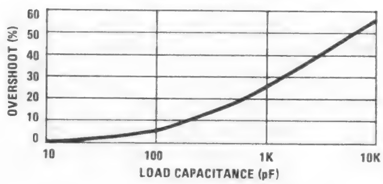
SLEW RATE vs.TEMPERATURE
$R_L = 2K$, $C_L = 50pF$, $V_{CC} = \pm15V$



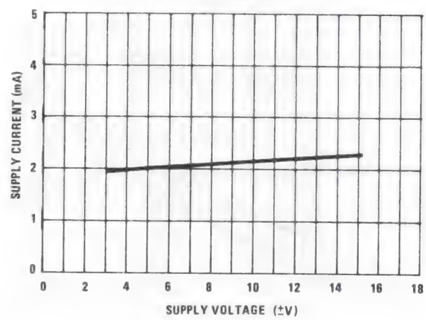
RISE TIME vs. TEMPERATURE
$R_L = 2K$, $C_L = 50pF$, $V_{CC} = \pm15V$



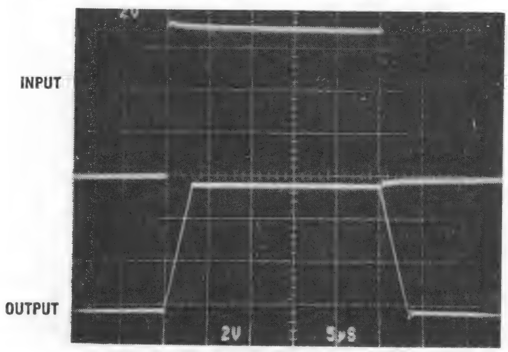
SMALL SIGNAL OVERSHOOT vs. C_{LOAD}
$R_L = 2K$, $T_A = +25^oC$, $V_{CC} = \pm15V$



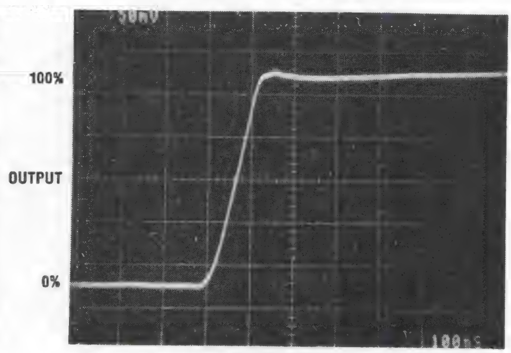
I_{CC} vs. V_{CC}
$T_A = +25^oC$, $I_{OUT} = 0mA$



LARGE SIGNAL RESPONSE
$V_{OUT} = \pm3V$, $A_V = 1$, $R_L = 2k\Omega$, $C_L = 50pF$
Input = 2V/Div., Output = 2V/Div., Timescale = 5µs/Div.



SMALL SIGNAL RESPONSE
V_{OUT} = 0V to +200mV for Rise Time & +Overshoot
$A_V = 1$, $R_L = 2k\Omega$, $C_L = 50pF$, Timescale = 100ns/Div.



DESIGN INFORMATION (Continued)

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TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_L = 2kΩ, C_L = 50pF, A_{VCL} = +1V/V Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMITS	UNITS
Offset Voltage	V_{CM} = 0V	+25°C	0.8	Table 1	mV
Offset Voltage Average Drift	Versus Temperature	-55°C to +125°C	3	7	μV/°C
Offset Current Average Drift	Versus Temperature	-55°C to +125°C	100	250	pA/°C
Input Bias Current	V_{CM} = 0V	+25°C	50	Table 1	nA
Input Offset Current	V_{CM} = 0V	+25°C	25	Table 1	nA
Differential Input Resistance	V_{CM} = 0V	+25°C	500	Table 3	kΩ
Input Noise Voltage Density	f_O = 10Hz	+25°C	10.3	14	$nV/\sqrt{Hz}$
	f_O = 100Hz	+25°C	5.6	8	$nV/\sqrt{Hz}$
	f_O = 1kHz	+25°C	4.3	Table 3	$nV/\sqrt{Hz}$
Input Noise Current Density	f_O = 10Hz	+25°C	6	15	$pA/\sqrt{Hz}$
	f_O = 100Hz	+25°C	1.5	5	$pA/\sqrt{Hz}$
	f_O = 1kHz	+25°C	0.52	Table 3	$pA/\sqrt{Hz}$
Large Signal Voltage Gain	V_{OUT} = ±10V	-55°C	200	Table 1	kV/V
		+25°C	300	Table 1	kV/V
		+125°C	400	Table 1	kV/V
Slew Rate	V_{OUT} = ±3V	-55°C to +125°C	±2	±0.7	V/μs
Full Power Bandwidth	Note 2, V_{peak} = 10V	-55°C to +125°C	30	11	kHz
Unity Gain Bandwidth	V_{OUT} < 200mV	+25°C	8	5	MHz
Rise and Fall Times	V_{OUT} = ±200mV	-55°C to +125°C	80	200	ns
Overshoot	V_{OUT} = ±200mV	-55°C to +125°C	10	35	%
Settling Time	To 0.1% for 10V Step	+25°C	4.5	6	μs
	To 0.01% for 10V Step	+25°C	6.0	10	μs
Output Short Circuit Current	To <10 Seconds, V_{OUT} = ±15V	+25°C	±35	±50	mA
Output Resistance	Open Loop	+25°C	110	Table 3	Ω
Channel Separation	f = 10kHz	+25°C	108	Table 3	dB
Supply Current	No Load	+25°C	2.4	Table 1	mA
Minimum Supply Voltage	Functional Operation Only, Other Parameters Will Vary	+25°C	±4	±5	V

HARRIS

HA-5104/883

Low Noise, High Performance, Quad Operational Amplifier

January 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low Input Noise Voltage Density @ 1kHz . . . 6nV/$\sqrt{Hz}$ Max; 4.3nV/$\sqrt{Hz}$ Typ
- Slew Rate . . . 1V/μs Min; 3V/μs Typ
- Unity Gain Bandwidth . . . 8MHz Typ
- High Open Loop Gain (Full Temp) . . . 100kV/V Min; 250kV/V Typ
- High CMRR, PSRR (Full Temp) . . . 86dB Min; 100dB Typ
- Low Offset Voltage Drift . . . 3μV/°C Typ
- No Crossover Distortion
- Standard Quad Pinout

Applications

- High Q Active Filters
- Audio Amplifiers
- Integrators
- Signal Generators
- Instrumentation Amplifiers

Description

Low noise and high performance are key words describing the unity gain stable HA-5104/883. This general purpose quad amplifier offers an array of dynamic specifications including 1V/μs slew rate (min), and 8MHz bandwidth (typ). Complementing these outstanding parameters is a very low noise specifications of 4.3nV/$\sqrt{Hz}$ at 1kHz (typ) or 6nV/$\sqrt{Hz}$ (max).

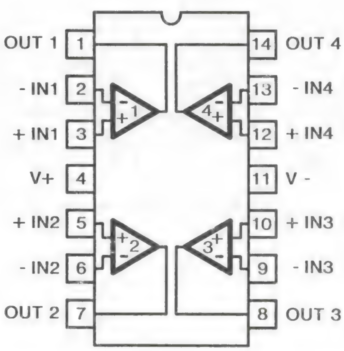
Fabricated using the Harris standard high frequency D.I. process, this operational amplifier also offer excellent input specifications such as 2.5mV (max) offset voltage and 75nA (max) offset current. Complementing these specifications are 100dB (min) open loop gain and 100dB channel separation (typ). Economically, the HA-5104/883 also consumes a very moderate amount of power (225mW per package) while also saving board space and cost.

This impressive combination of features make this amplifier ideally suited for designs ranging from audio amplifiers and active filters to the most demanding signal conditioning and instrumentation circuits.

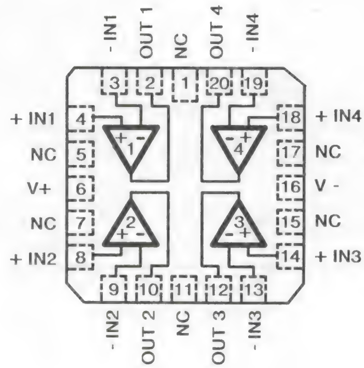
This quad operational amplifier is available with industry standard pinouts allowing for immediate interchangeability with most other quad operational amplifiers. The HA-5104/883 is available in a 14 pin Ceramic DIP and 20 pin Ceramic LCC package.

Pinouts

HA1-5104/883 (CERAMIC DIP)
TOP VIEW



HA4-5104/883 (CERAMIC LCC)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage 7V
Voltage at Either Input Terminal .... V+ to V-
Peak Output Current .... Indefinite (One Amplifier Shorted to Ground)
Junction Temperature (T_J) .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... <2000V
Lead Temperature (Soldering 10 sec) .... 275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	78°C/W	18°C/W
Ceramic LCC Package	76°C/W	19°C/W

Package Power Dissipation Limit at +75°C for $T_J \leq$ +175°C
Ceramic DIP Package 1.29W
Ceramic LCC Package 1.32W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 12.9mW/°C
Ceramic LCC Package .... 13.1mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±5V to ±15V
$V_{INcm} \leq 1/2$ (V+ - V-)
$R_L \geq 2k\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	V_{CM} = 0V	1	+25°C	-2.5	2.5	mV
			2, 3	+125°C, -55°C	-3.0	3.0	mV
Input Bias Current	$+I_B$	V_{CM} = 0V $+R_S$ = 10kΩ $-R_S$ = 100Ω	1	+25°C	-200	200	nA
			2, 3	+125°C, -55°C	-325	325	nA
	$-I_B$	V_{CM} = 0V $+R_S$ = 100Ω $-R_S$ = 10kΩ	1	+25°C	-200	200	nA
			2, 3	+125°C, -55°C	-325	325	nA
Input Offset Current	I_{IO}	V_{CM} = 0V $+R_S$ = 10kΩ $-R_S$ = 10kΩ	1	+25°C	-75	75	nA
			2, 3	+125°C, -55°C	-125	125	nA
Common Mode Range	+CMR	V+ = 3V V- = -27V	1	+25°C	+12	-	V
			2, 3	+125°C, -55°C	+12	-	V
	-CMR	V+ = 27V V- = -3V	1	+25°C	-	-12	V
			2, 3	+125°C, -55°C	-	-12	V
Large Signal Voltage Gain	$+A_{VOL}$	V_{OUT} = 0V and +10V R_L = 2kΩ	4	+25°C	100	-	kV/V
			5, 6	+125°C, -55°C	100	-	kV/V
	$-A_{VOL}$	V_{OUT} = 0V and -10V R_L = 2kΩ	4	+25°C	100	-	kV/V
			5, 6	+125°C, -55°C	100	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔV_{CM} = +5V +V = +10V -V = -20V V_{OUT} = -5V	1	+25°C	86	-	dB
			2, 3	+125°C, -55°C	86	-	dB
	-CMRR	ΔV_{CM} = -5V +V = +20V -V = -10V V_{OUT} = +5V	1	+25°C	86	-	dB
			2, 3	+125°C, -55°C	86	-	dB

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Voltage Swing	$+V_{OUT1}$	R_L = 2kΩ	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	$-V_{OUT1}$	R_L = 2kΩ	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
	$+V_{OUT2}$	R_L = 10kΩ	1	+25°C	12	-	V
			2, 3	+125°C, -55°C	12	-	V
	$-V_{OUT2}$	R_L = 10kΩ	1	+25°C	-	-12	V
			2, 3	+125°C, -55°C	-	-12	V
Output Current	$+I_{OUT}$	V_{OUT} = -5V	1	+25°C	10	-	mA
			2, 3	+125°C, -55°C	10	-	mA
	$-I_{OUT}$	V_{OUT} = +5V	1	+25°C	-	-10	mA
			2, 3	+125°C, -55°C	-	-10	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V	1	+25°C	-	6.5	mA
		I_{OUT} = 0mA	2, 3	+125°C, -55°C	-	7.5	mA
	$-I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-6.5	-	mA
			2, 3	+125°C, -55°C	-7.5	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = 10V +V = +10V, -V = -15V +V = +20V, -V = -15V	1	+25°C	86	-	dB
			2, 3	+125°C, -55°C	86	-	dB
	-PSRR	ΔV_{SUP} = 10V +V = +15V, -V = -10V +V = +15V, -V = -20V	1	+25°C	86	-	dB
			2, 3	+125°C, -55°C	86	-	dB

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_{VCL} = +1V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Slew Rate	+SR	V_{OUT} = -3V to +3V	4	+25°C	1	-	V/μs
	-SR	V_{OUT} = +3V to -3V	4	+25°C	1	-	V/μs
Rise & Fall Time	T_R	V_{OUT} = 0 to +200mV $10\% \le T_R \le 90\%$	4	+25°C	-	200	ns
	T_F	V_{OUT} = 0 to -200mV $10\% \le T_F \le 90\%$	4	+25°C	-	200	ns
Overshoot	+OS	V_{OUT} = 0 to +200mV	4	+25°C	-	35	%
	-OS	V_{OUT} = 0 to -200mV	4	+25°C	-	35	%

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_{VCL} = 10V/V Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Differential Input Resistance	R_{IN}	V_{CM} = 0V	1	+25°C	250	-	kΩ
Input Noise Voltage Density	E_n	R_S = 20Ω, f_o = 1000Hz	1	+25°C	-	6	$nV/\sqrt{Hz}$
Input Noise Current Density	I_n	R_S = 2MΩ, f_o = 1000Hz	1	+25°C	-	3	$pA/\sqrt{Hz}$
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	+25°C	32	-	kHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 2kΩ, C_L = 50pF	1	-55°C to +125°C	+1	-	V/V
Output Resistance	R_{OUT}	Open Loop	1	+25°C	-	150	Ω
Quiescent Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	225	mW
Channel Separation	CS	R_S = 1kΩ, A_{VCL} = 100V/V, V_{IN} = 100mV_{RMS} @ 10kHz Referred to Input	1	+25°C	90	-	dB

NOTES: 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).

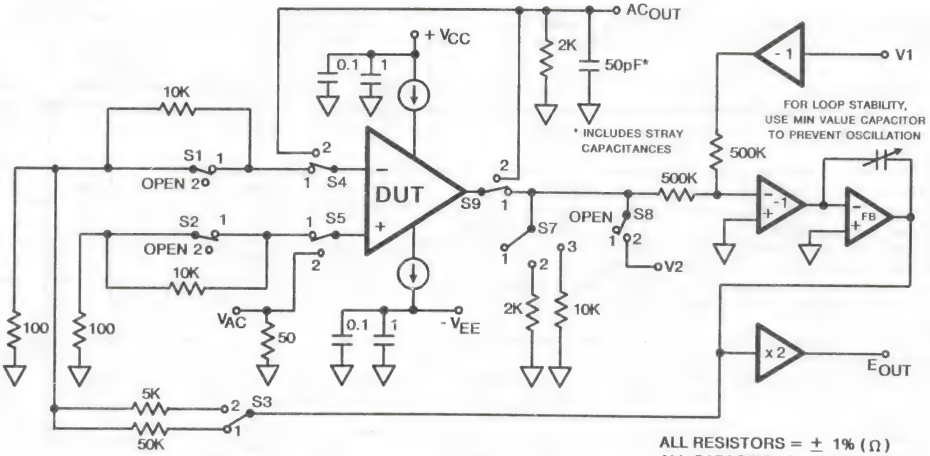
3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6
Group A Test Requirements	1, 2, 3, 4, 5, 6
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

Test Circuit



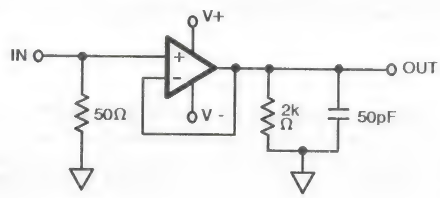
ALL RESISTORS = ± 1% (Ω)
ALL CAPACITORS = ± 10% (μF)
DUT = 1/4 OF HA - 5104/883

ONE OF FOUR TEST LOOPS FOR THE HA - 5104/883

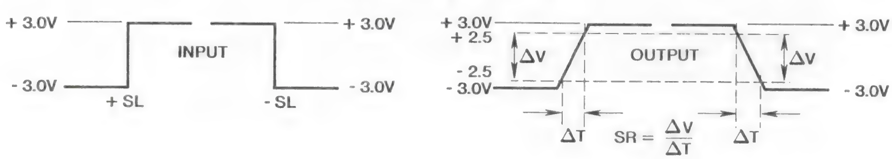
For Detailed Information, Refer to HA-5104/883 Test Tech Brief

Test Waveforms

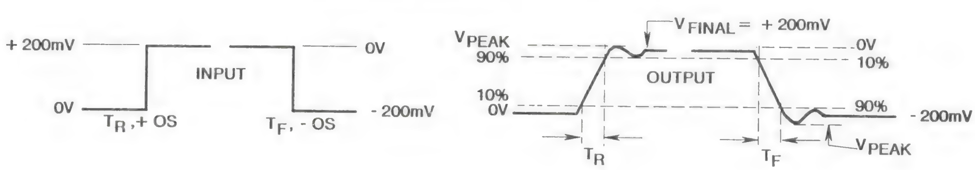
SIMPLIFIED TEST CIRCUIT (Applies To Tables 2 And 3)



SLEW RATE WAVEFORMS

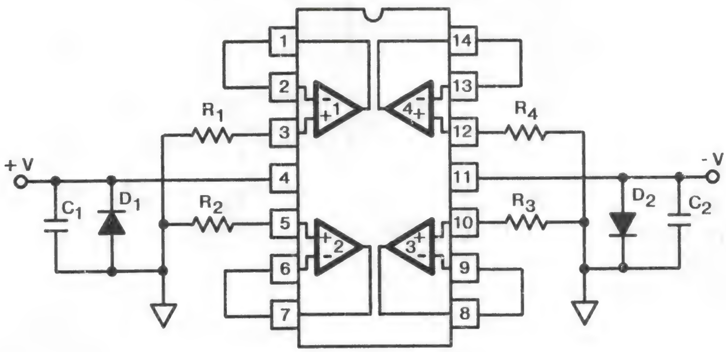


OVERSHOOT, RISE/FALL TIME WAVEFORMS

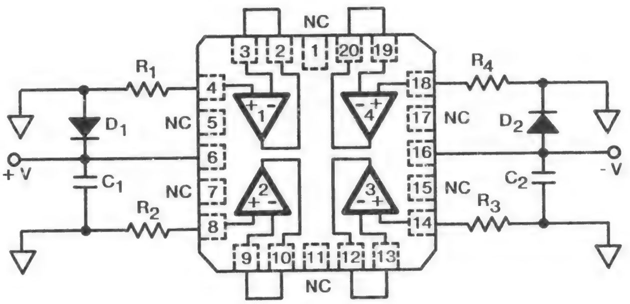


Burn-In Circuits

HA7-5104/883 CERAMIC DIP



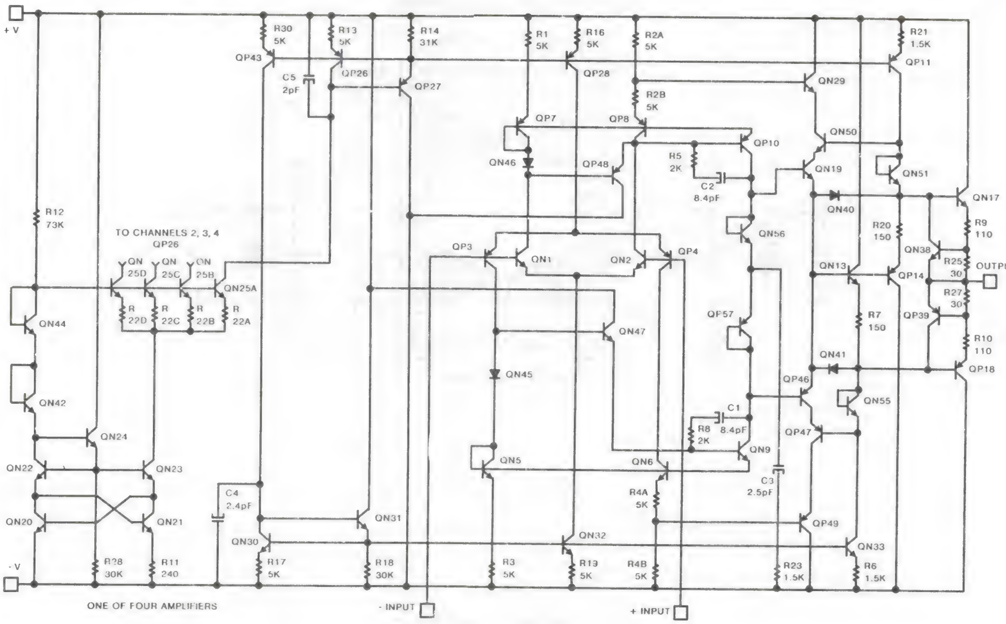
HA4-5104/883 CERAMIC LCC



NOTES:

$R_1 = R_2 = R_3 = R_4 = 1M\Omega$, 5%, 1/4W (Min)
$C_1 = C_2 = 0.1\mu F$/Socket (Min) or $0.01\mu F$/Row (Min)
$D_1 = D_2$ = IN4002 or Equivalent/Board
$|(V+) - (V-)| = 30V$

Schematic Diagram (1/4 HA-5104/883)



Die Characteristics

DIE DIMENSIONS:
99.6 x 95.3 x 19 mils
(2530 x 2420 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$1.43 \times 10^5 A/cm^2$ at 10mA

SUBSTRATE POTENTIAL (POWERED UP):
Unbiased

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

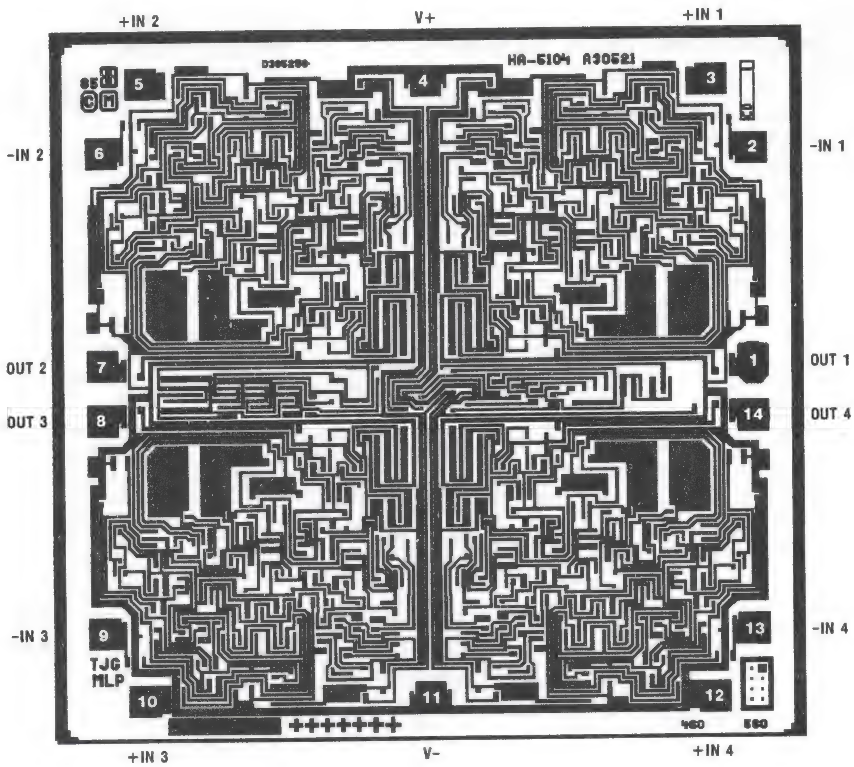
TRANSISTOR COUNT: 175

PROCESS: HFSB Linear Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

Metallization Mask Layout

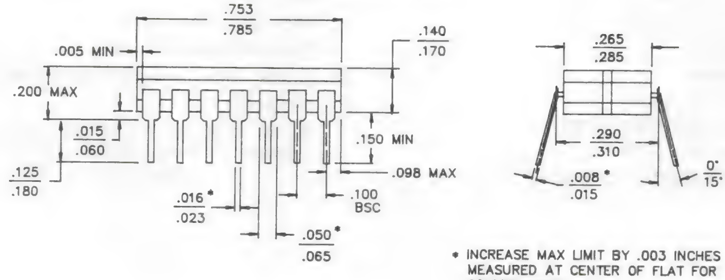
HA-5104/883



NOTE: Pin Numbers Correspond to 14 Pin Ceramic DIP Package Only.

Packaging†

14 PIN CERAMIC DIP

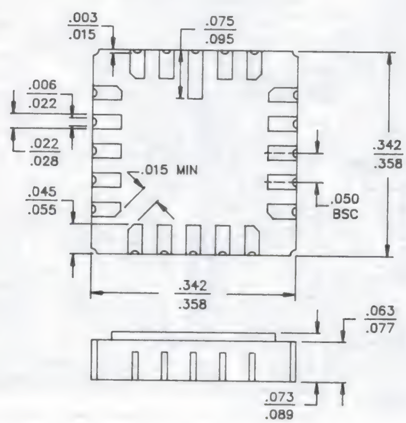


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-1

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

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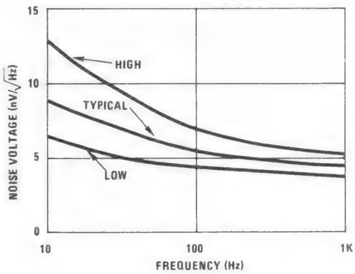
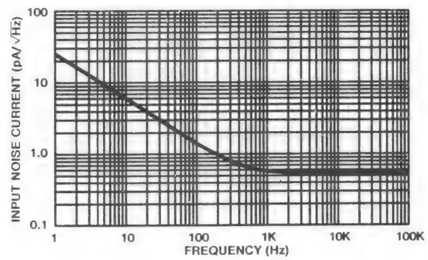
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

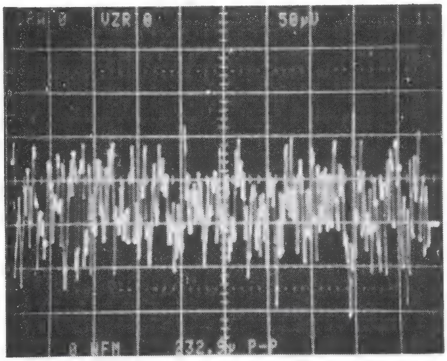
INPUT NOISE VOLTAGE DENSITY
$V_{CC} = \pm15V$, $T_A = +25^oC$



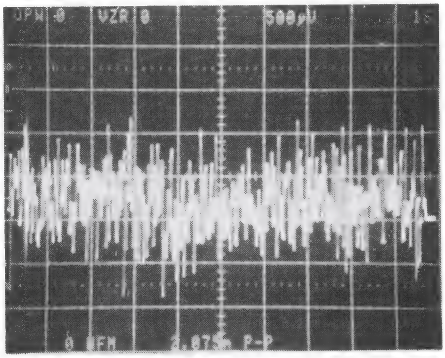
INPUT NOISE CURRENT DENSITY
$V_{CC} = \pm15V$, $T_A = +25^oC$



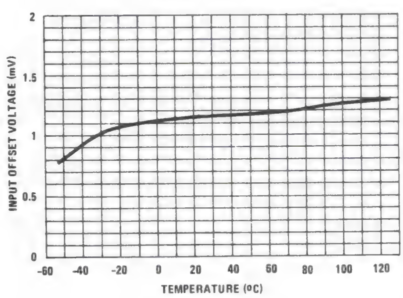
0.1Hz TO 10Hz NOISE
$V_{CC} = \pm15V$, $T_A = +25^oC$
50μV/Div., 1s/Div., A_V = 1000V/V
Input Noise = 0.232μV_{p-p}



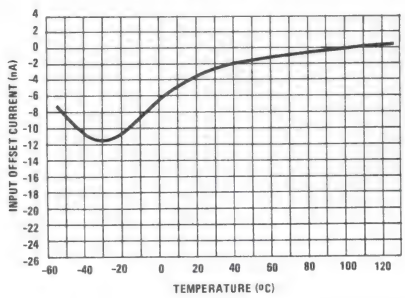
0.1Hz TO 1MHz NOISE
$V_{CC} = \pm15V$, $T_A = +25^oC$
500μV/Div., 1s/Div., A_V = 1000V/V
Total Output Noise = 2.075μV_{p-p}



V_{IO} vs. TEMPERATURE
$V_{CC} = \pm15V$



I_{IO} vs. TEMPERATURE
$V_{CC} = \pm15V$



DESIGN INFORMATION (Continued)

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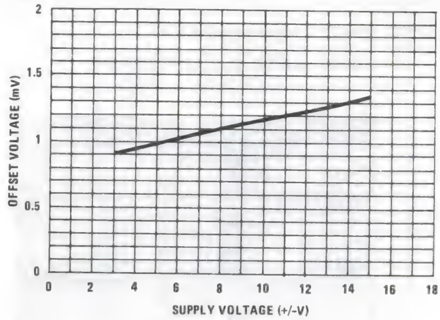
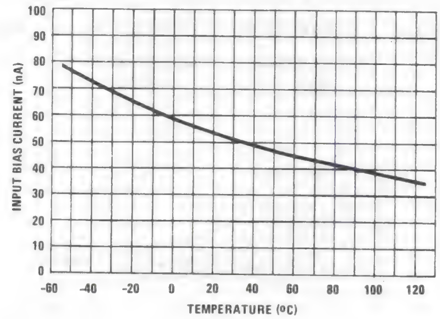
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

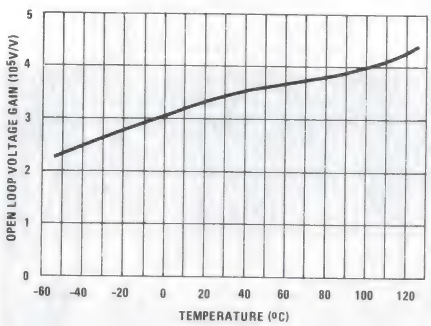
V_{IO} vs. V_{CC}
$T_A = +25^oC$



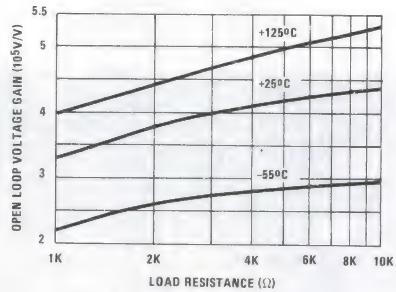
I_{BIAS} vs. TEMPERATURE
$V_{CC} = \pm15V$



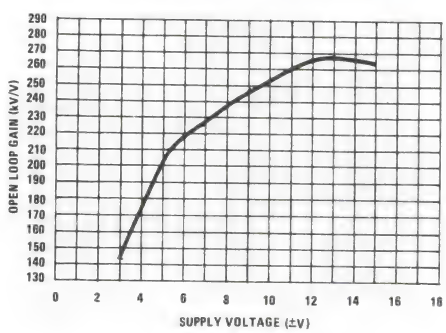
A_{VOL} vs. TEMPERATURE
$VCC = \pm15V$, $\Delta V_O = \pm10V$, $R_L = 2K$



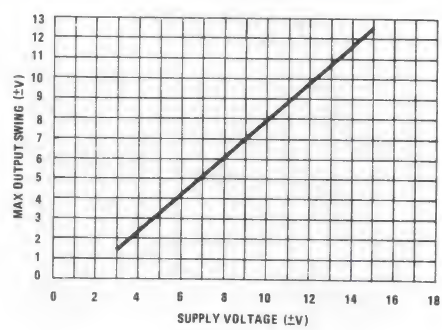
A_{VOL} vs. LOAD RESISTANCE
$V_O = \pm10V$, $V_{CC} = \pm15V$, $T_A = +25^oC$



A_{VOL} vs. V_{CC}
$T_A = +25^oC$, $R_L = 2K$



V_{OUT} vs. V_{CC}
$T_A = +25^oC$, $R_L = 2K$

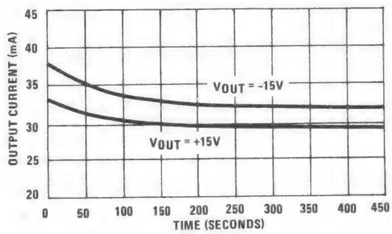


DESIGN INFORMATION (Continued)

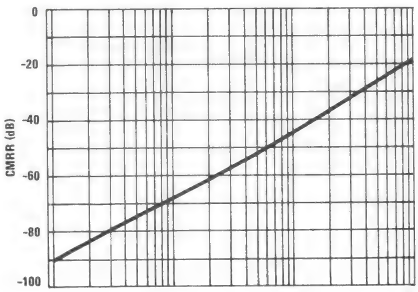
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

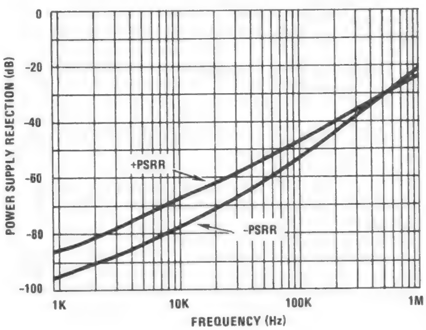
OUTPUT SHORT-CIRCUIT CURRENT vs. TIME
$V_{CC} = \pm15V$, $T_A = +25^oC$



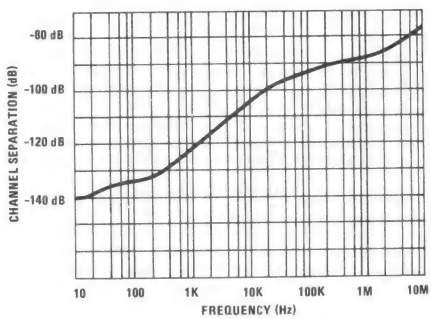
CMRR vs. FREQUENCY



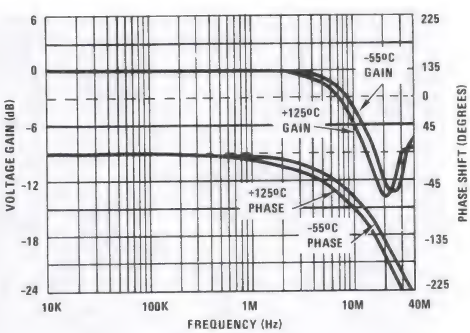
PSRR vs. FREQUENCY



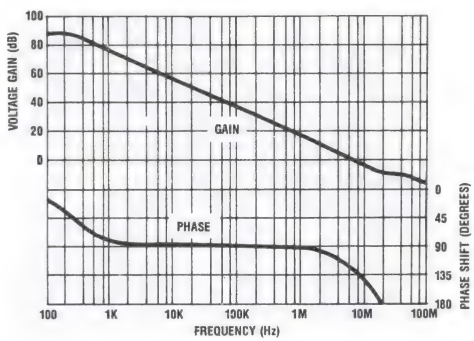
CHANNEL SEPARATION vs. FREQUENCY
$10Hz \leq f \leq 10MHz$



HA-5104 UNITY GAIN FREQUENCY RESPONSE
$V_{CC} = \pm15$, $R_L = 2K$, $C_L = 50pF$



OPEN-LOOP GAIN vs. FREQUENCY
$V_{CC} = \pm15V$, $R_L = 2K$, $C_L = 50pF$, $T_A = +25^oC$



3

OP AMPs & COMPARATORS

DESIGN INFORMATION (Continued)

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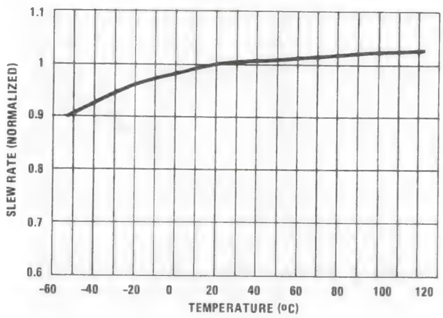
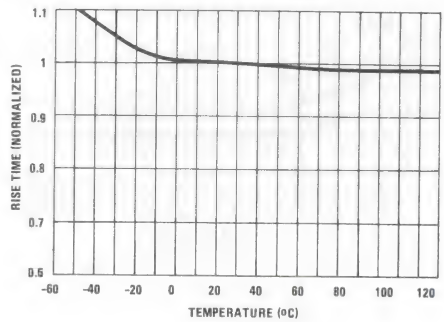
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

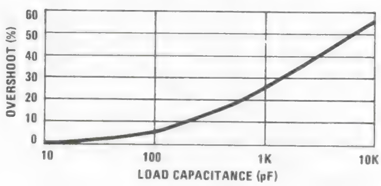
SLEW RATE vs.TEMPERATURE
$R_L = 2K$, $C_L = 50pF$, $V_{CC} = \pm15V$



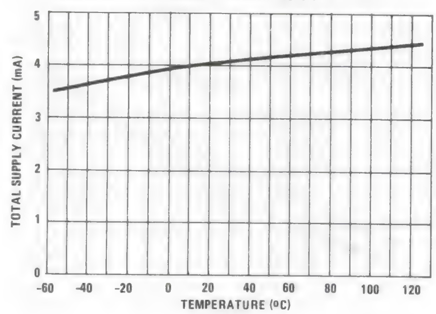
RISE TIME vs. TEMPERATURE
$R_L = 2K$, $C_L = 50pF$, $V_{CC} = \pm15V$



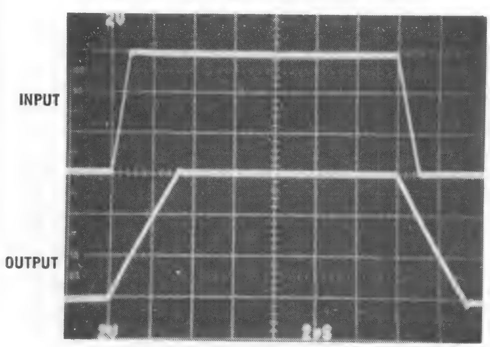
SMALL SIGNAL OVERSHOOT vs. C_{LOAD}
$R_L = 2K$, $T_A = +25^oC$, $V_{CC} = \pm15V$



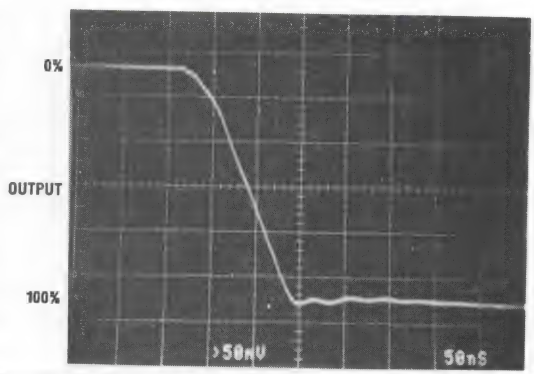
I_{CC} vs. TEMPERATURE
$T_A = +25^oC$, $V_{CC} = \pm15V$, $I_{OUT} = 0mA$



LARGE SIGNAL RESPONSE
$V_{IN} = V_{OUT} = \pm3V$, $A_V = +1$, $R_L = 2k\Omega$, $C_L = 50pF$
Voltage Scale = 2V/Div., Timescale = 2μs/Div.



SMALL SIGNAL RESPONSE
V_{OUT} = 0V to −200mV for Fall Time & −Overshoot
$A_V = +1$, $R_L = 2k\Omega$, $C_L = 50pF$, Timescale = 50ns/Div.



DESIGN INFORMATION (Continued)

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TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_L = 2kΩ, C_L = 50pF, A_{VCL} = +1V/V Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMITS	UNITS
Offset Voltage	V_{CM} = 0V	+25°C	0.8	Table 1	mV
Offset Voltage Average Drift	Versus Temperature	-55°C to +125°C	3	7	µV/°C
Offset Current Average Drift	Versus Temperature	-55°C to +125°C	100	250	pA/°C
Input Bias Current	V_{CM} = 0V	+25°C	50	Table 1	nA
Input Offset Current	V_{CM} = 0V	+25°C	25	Table 1	nA
Differential Input Resistance	V_{CM} = 0V	+25°C	500	Table 3	kΩ
Input Noise Voltage Density	f_O = 10Hz	+25°C	10.3	14	$nV/\sqrt{Hz}$
	f_O = 100Hz	+25°C	5.6	8	$nV/\sqrt{Hz}$
	f_O = 1kHz	+25°C	4.3	Table 3	$nV/\sqrt{Hz}$
Input Noise Current Density	f_O = 10Hz	+25°C	6	15	$pA/\sqrt{Hz}$
	f_O = 100Hz	+25°C	1.5	5	$pA/\sqrt{Hz}$
	f_O = 1kHz	+25°C	0.52	Table 3	$pA/\sqrt{Hz}$
Large Signal Voltage Gain	V_{OUT} = ±10V	-55°C	200	Table 1	kV/V
		+25°C	300	Table 1	kV/V
		+125°C	400	Table 1	kV/V
Slew Rate	V_{OUT} = ±3V	-55°C to +125°C	±2	±0.7	V/µs
Full Power Bandwidth	Note 2, V_{peak} = 10V	-55°C to +125°C	30	11	kHz
Unity Gain Bandwidth	$V_{OUT} \leq$ 200mV	+25°C	8	5	MHz
Rise and Fall Times	V_{OUT} = ±200mV	-55°C to +125°C	80	200	ns
Overshoot	V_{OUT} = ±200mV	-55°C to +125°C	10	35	%
Settling Time	To 0.1% for 10V Step	+25°C	4.5	6	µs
	To 0.01% for 10V Step	+25°C	6.0	10	µs
Output Short Circuit Current	To <10 Seconds, V_{OUT} = ±15V	+25°C	±35	±50	mA
Output Resistance	Open Loop	+25°C	110	Table 3	Ω
Channel Separation	f = 10kHz	+25°C	108	Table 3	dB
Supply Current	No Load	+25°C	4.2	Table 1	mA
Minimum Supply Voltage	Functional Operation Only, Other Parameters Will Vary	+25°C	±4	±5	V

HARRIS

HA-5111/883

Low Noise, High Performance Uncompensated Operational Amplifier

January 1989

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Low Noise Voltage Density @ 1kHz .. 4.5nV/$\sqrt{Hz}$ Max**
- **Low Noise Current Density @ 1kHz .... 3pA/$\sqrt{Hz}$ Max**
- **Wide Gain Bandwidth Product .... 70MHz Min**
  100MHz Typ
- **High Slew Rate .... 40V/µs Min**
  60V/µs Typ
- **High Gain (Full Temp) .... 100kV/V Min**
  (Room Temp) .... 1MV/V Typ
- **High CMRR/PSRR (Full Temp) .... 80dB Min**
- **High Output Drive Capability (Full Temp) 25mA**

Applications

- **High Quality Audio Preamplifiers**
- **High Q Active Filters**
- **Low Noise Function Generators**
- **Low Distortion Oscillators**
- **Low Noise Comparators**

Description

The HA-5111/883 is a dielectrically isolated operational amplifier featuring superb high speed and low noise performance. This amplifier has guaranteed noise voltage density of 4.5nV/$\sqrt{Hz}$ (max) at 1kHz and guaranteed noise current density of 3pA/$\sqrt{Hz}$ at 1kHz. The HA-5111/883 has a minimum gain bandwidth product of 70MHz while maintaining slew rates of 40V/µs minimum and 60V/µs typical.

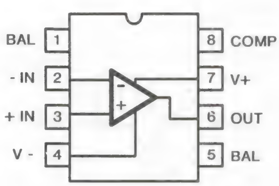
The D.C. characteristics of the HA-5111/883 assure accurate performance by having a high open loop gain of typically 1MV/V at room temperature, or 100kV/V over the full temperature range. The 3mV (max) offset voltage is externally adjustable and has typical offset drift less than 3µV/°C.

The HA-5111/883 is ideal for audio applications, especially low-level signal amplifiers such as microphone, tape head, and preamplifiers. Additionally, it is well suited for low distortion oscillators, low noise function generators, and high Q filters.

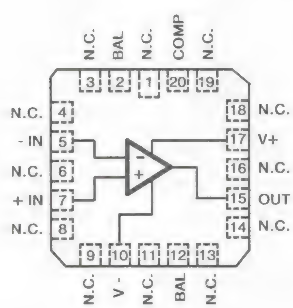
The HA-5111/883 has guaranteed operation from -55°C to +125°C, is available in Ceramic Mini-DIP, TO-99 Metal Can and 20 pin Ceramic LCC packages.

Pinouts

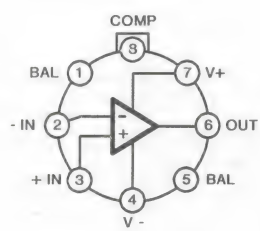
HA7-5111/883 (CERAMIC MINI-DIP)
TOP VIEW



HA4-5111/883 (CERAMIC LCC)
TOP VIEW



HA2-5111/883 (METAL CAN)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage 7V
Voltage at Either Input Terminal . . . . V+ to V-
Input Current 25mA
Output Short Circuit Duration . . . . Indefinite
Junction Temperature (T_J) . . . . +175°C
Storage Temperature Range . . . . -65°C to +150°C
ESD Rating . . . . <2000V
Lead Temperature (Soldering 10 sec) . . . . +275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	82°C/W	27°C/W
Ceramic LCC Package	74°C/W	20°C/W
Metal Can Package	121°C/W	36°C/W

Package Power Dissipation Limit at +75°C for $T_J \leq$ +175°C
Ceramic DIP Package 1.22W
Ceramic LCC Package 1.35W
Metal Can Package 830mW

Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package . . . . 12.2mW/°C
Ceramic LCC Package . . . . 13.5mW/°C
Metal Can Package . . . . 8.3mW/°C

Recommended Operating Conditions

Operating Temperature Range . . . . -55°C to +125°C
Operating Supply Voltage . . . . ±5V to ±15V
$V_{INcm} \leq$ 1/2 (V+ - V-)
$R_L \geq$ 500Ω

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	V_{CM} = 0V	1	+25°C	-3	3	mV
			2, 3	+125°C, -55°C	-4	4	mV
Input Bias Current	$+I_B$	V_{CM} = 0V $+R_S$ = 100kΩ $-R_S$ = 100Ω	1	+25°C	-200	200	nA
			2, 3	+125°C, -55°C	-325	325	nA
	$-I_B$	V_{CM} = 0V $+R_S$ = 100Ω $-R_S$ = 100kΩ	1	+25°C	-200	200	nA
			2, 3	+125°C, -55°C	-325	325	nA
Input Offset Current	I_{IO}	V_{CM} = 0V $+R_S$ = 100kΩ $-R_S$ = 100kΩ	1	+25°C	-75	75	nA
			2, 3	+125°C, -55°C	-125	125	nA
Common Mode Range	+CMR	V+ = 3V V- = -27V	1	+25°C	12	-	V
			2, 3	+125°C, -55°C	12	-	V
	-CMR	V+ = 27V V- = -3V	1	+25°C	-	-12	V
			2, 3	+125°C, -55°C	-	-12	V
Large Signal Voltage Gain	$+A_{VOL}$	V_{OUT} = 0V and +10V R_L = 2kΩ	4	+25°C	100	-	kV/V
			5, 6	+125°C, -55°C	100	-	kV/V
	$-A_{VOL}$	V_{OUT} = 0V and -10V R_L = 2kΩ	4	+25°C	100	-	kV/V
			5, 6	+125°C, -55°C	100	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔV_{CM} = +10V +V = +5V -V = -25V V_{OUT} = -10V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	-CMRR	ΔV_{CM} = -10V +V = +25V -V = -5V V_{OUT} = +10V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Voltage Swing	$+V_{OUT1}$	R_L = 2kΩ	1	+25°C	12	-	V
			2, 3	+125°C, -55°C	12	-	V
	$-V_{OUT1}$	R_L = 2kΩ	1	+25°C	-	-12	V
			2, 3	+125°C, -55°C	-	-12	V
	$+V_{OUT2}$	V_{SUPPLY} = ±18V R_L = 600Ω	1	+25°C	15	-	V
			2, 3	+125°C, -55°C	15	-	V
	$-V_{OUT2}$	V_{SUPPLY} = ±18V R_L = 600Ω	1	+25°C	-	-15	V
			2, 3	+125°C, -55°C	-	-15	V
Output Current	$+I_{OUT}$	V_{OUT} = -15V V_{SUPPLY} = ±18V	1	+25°C	25	-	mA
			2, 3	+125°C, -55°C	25	-	mA
	$-I_{OUT}$	V_{OUT} = +15V V_{SUPPLY} = ±18V	1	+25°C	-	-25	mA
			2, 3	+125°C, -55°C	-	-25	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-	6	mA
			2, 3	+125°C, -55°C	-	6	mA
	$-I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-6	-	mA
			2, 3	+125°C, -55°C	-6	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = 10V +V = +10V, -V = -15V +V = +20V, -V = -15V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	-PSRR	ΔV_{SUP} = 10V +V = +15V, -V = -10V +V = +15V, -V = -20V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
Offset Voltage Adjustment	$+V_{IO}Adj$	Note 6	1	+25°C	V_{IO}-1	-	mV
			2, 3	+125°C, -55°C	V_{IO}-1	-	mV
	$-V_{IO}Adj$	Note 6	1	+25°C	V_{IO}+1	-	mV
			2, 3	+125°C, -55°C	V_{IO}+1	-	mV

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_{VCL} = +10V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Slew Rate	+SR	V_{OUT} = -5V to +5V	4	+25°C	40	-	V/µs
	-SR	V_{OUT} = +5V to -5V	4	+25°C	40	-	V/µs

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_V = +10V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Differential Input Resistance	R_{IN}	V_{CM} = 0V	1	+25°C	250	-	kΩ
Low Frequency Peak-to-Peak Noise	E_{np-p}	0.1Hz to 10Hz	1	+25°C	-	0.2	μV_{p-p}
Input Noise Voltage Density	E_n	R_S = 20Ω, f_o = 1000Hz	1, 5	+25°C	-	4.5	$nV/\sqrt{Hz}$
Input Noise Current Density	I_n	R_S = 2MΩ, f_o = 1000Hz	1, 5	+25°C	-	3	$pA/\sqrt{Hz}$
Gain Bandwidth Product	GBWP	V_O = 100mV, f_o = 10kHz	1	+25°C	70	-	MHz
		V_O = 100mV, f_o = 1MHz	1	+25°C	70	-	MHz
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	+25°C	630	-	kHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 2kΩ, C_L = 50pF	1	-55°C to +125°C	+10	-	V/V
Rise & Fall Time	T_R	V_{OUT} = 0V to +200mV	1, 4	+25°C	-	60	ns
	T_F	V_{OUT} = 0V to -200mV	1, 4	+25°C	-	60	ns
Overshoot	+OS	V_{OUT} = 0V to +200mV	1	+25°C	-	40	%
	+OS	V_{OUT} = 0V to +200mV	1	+25°C	-	40	%
Output Resistance	R_{OUT}	Open Loop	1	+25°C	-	150	Ω
Quiescent Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	180	mW

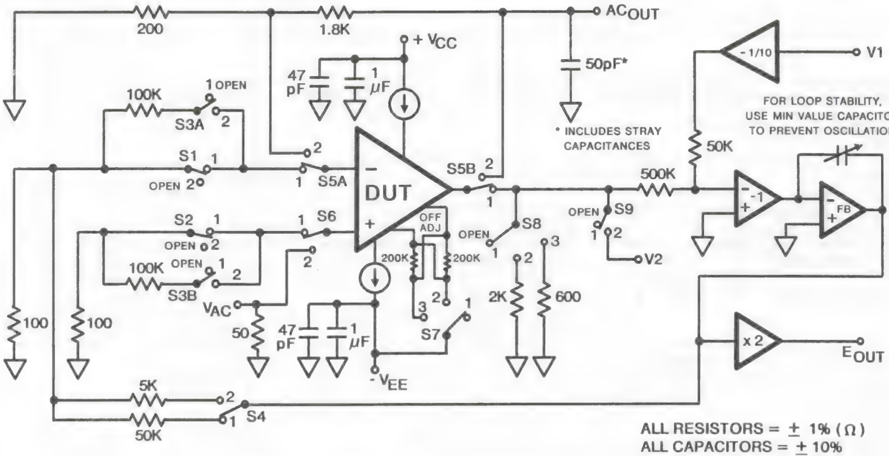
NOTES:
1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).
3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)
4. Measured between 10% and 90% points.
5. Input Noise Voltage Density and Input Noise Current Density is sample tested on every lot.
6. Offset adjustment range is [$V_{IO\ (Measured)}$ ± 1mV] minimum referred to output. This test is for functionality only to assure adjustment through 0V.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6
Group A Test Requirements	1, 2, 3, 4, 5, 6
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

Test Circuit (Applies To Tables 1, 2 And 3)

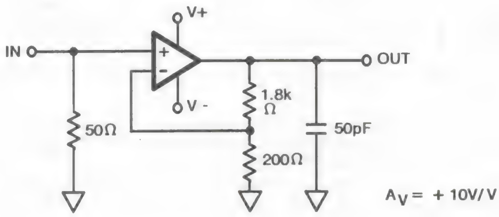


ALL RESISTORS = ± 1% (Ω)
ALL CAPACITORS = ± 10%

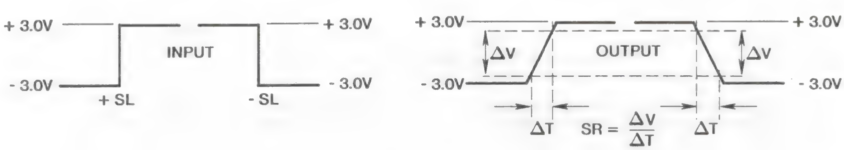
For Detailed Information, Refer to HA-5111/883 Test Tech Brief

Test Waveforms

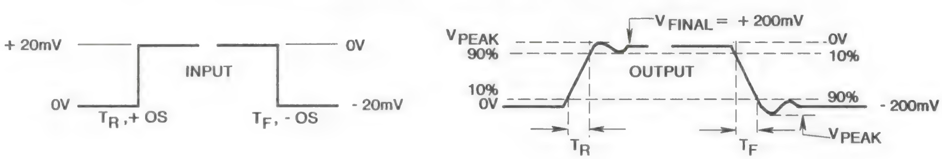
SIMPLIFIED TEST CIRCUIT (Applies To Tables 2 And 3)



SLEW RATE WAVEFORMS



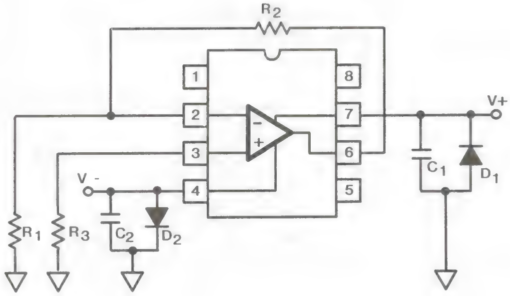
OVERSHOOT, RISE/FALL TIME WAVEFORMS



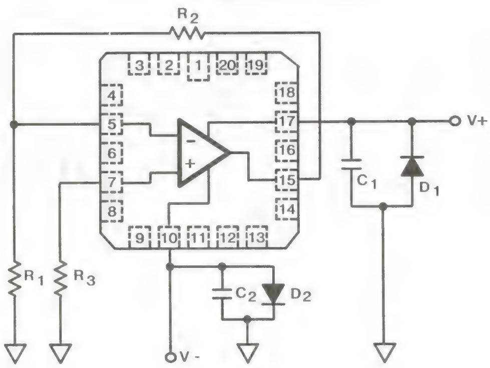
Note: Measured on both positive and negative transitions.
Capacitance at compensation pin should be minimized.

Burn-In Circuits

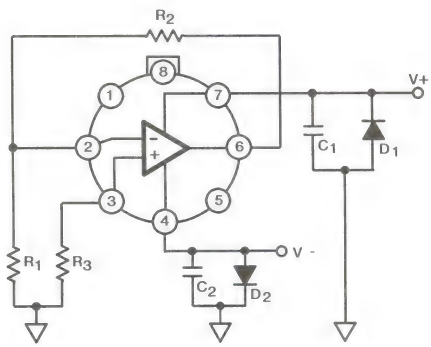
HA7-5111/883 CERAMIC DIP



HA4-5111/883 CERAMIC LCC



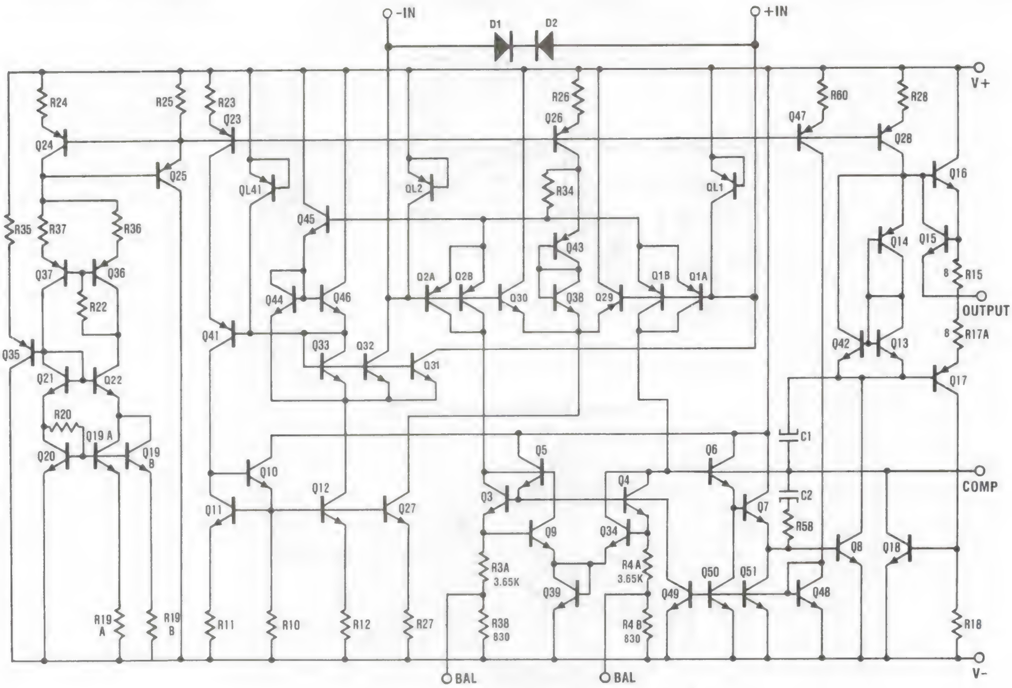
HA2-5111/883 (TO-99) METAL CAN



NOTES:

$R_1 = R_3 = 1k\Omega$, ±5%, 1/4W (Min)
$R_2 = 10k\Omega$, ±5%, 1/4W (Min)
$C_1 = C_2 = 0.01\mu F$/Socket (Min) or $0.1\mu F$/Row (Min)
$D_1 = D_2$ = IN4002 or Equivalent/Board
$|(V+) - (V-)| = 30V$

Schematic Diagram



Die Characteristics

DIE DIMENSIONS:
68.9 x 69.3 x 19 mils
(1750 x 1760 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$1.38 \times 10^5 A/cm^2$ at 30mA

SUBSTRATE POTENTIAL (POWERED UP): V-

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

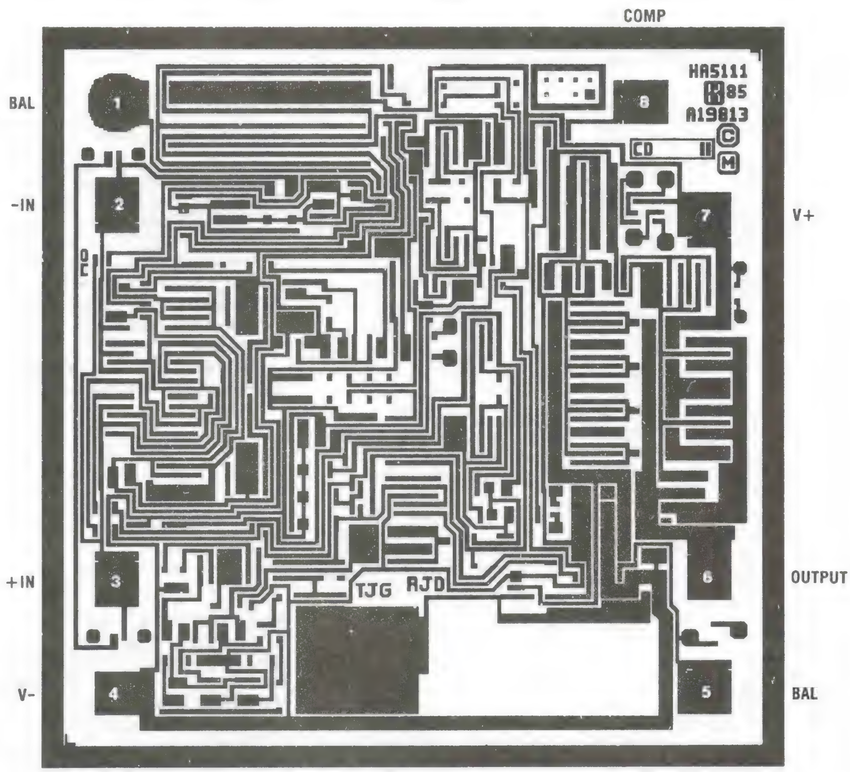
TRANSISTOR COUNT: 54

PROCESS: HFSB Bipolar Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)
Metal Can — 420°C (Max)

Metallization Mask Layout

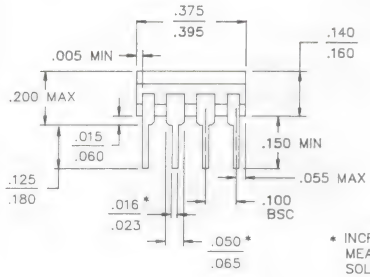
HA-5111/883

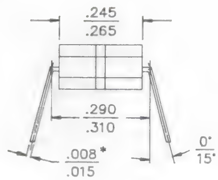


NOTE: Pin Numbers Correspond to Ceramic Mini-DIP and Metal Can Packages Only.

Packaging †

8 PIN CERAMIC DIP

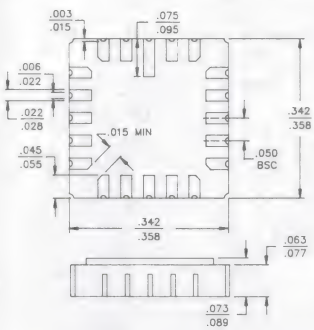




* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

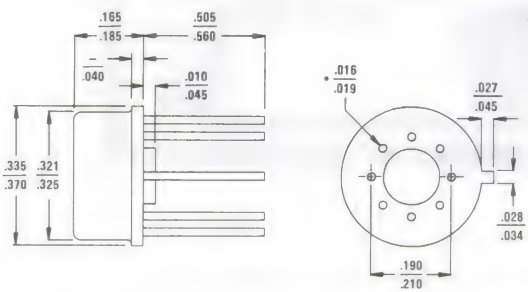
LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-4

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Ceramic, 90% Al_2O_3
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

8 PIN TO-99 METAL CAN



LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
Material: No Seal Material
Temperature: Room Temperature
Method: Resistance Weld
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic Bonded
COMPLIANT OUTLINE: 38510 A-1

*Dimension Maximum Limits Are Increased by 0.003 inches for Solder Dip Finish

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

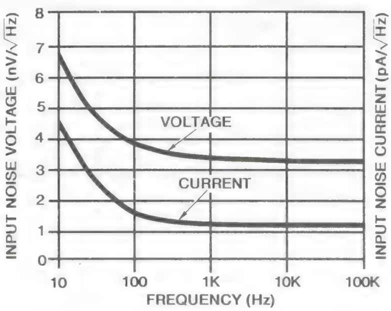
† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

Low Noise, High Performance Uncompensated Operational Amplifier

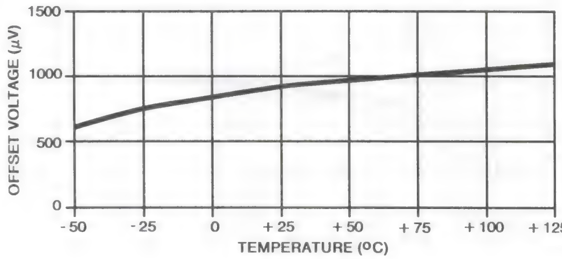
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $V\pm = \pm15V$, $T_A = +25^oC$

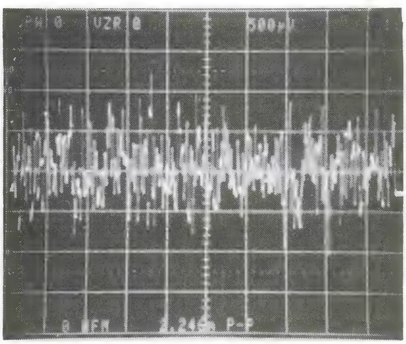
HA-5111 NOISE SPECTRUM



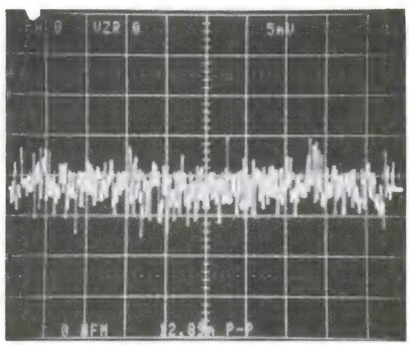
OFFSET VOLTAGE vs. TEMPERATURE



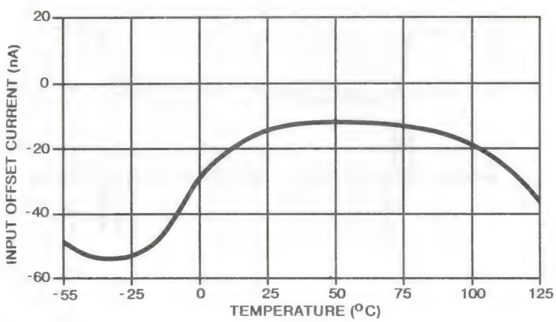
PEAK-TO-PEAK NOISE 0.1Hz TO 10Hz
$A_V = 25{,}000$, $V_{CC} = \pm15V$
($0.09\mu V_{p-p}$ RTI)



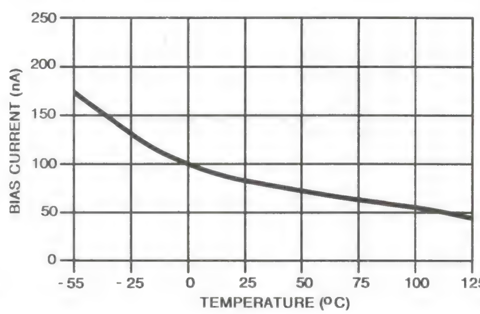
PEAK-TO-PEAK TOTAL NOISE 0.1Hz TO 1MHz
$A_V = 25{,}000$, $V_{CC} = \pm15V$
($12.89mV_{p-p}$ RTO or $0.52\mu V_{p-p}$ RTI)



INPUT OFFSET CURRENT vs. TEMPERATURE



INPUT BIAS CURRENT vs. TEMPERATURE

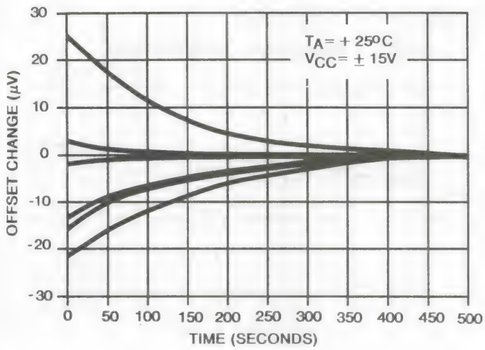


DESIGN INFORMATION (Continued)

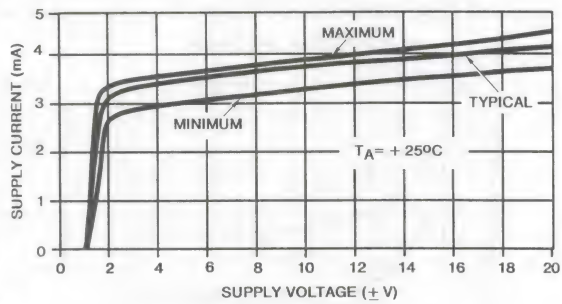
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: V± = ±15V, T_A = +25°C

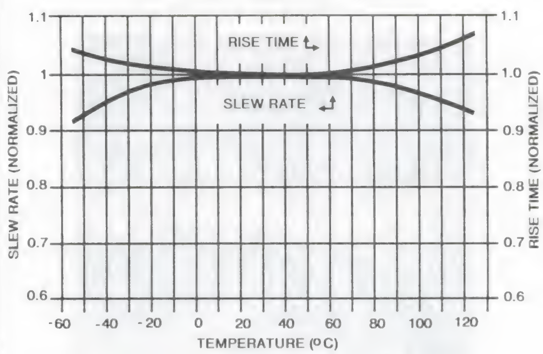
INPUT OFFSET WARMUP DRIFT vs. TIME
(Normalized to Zero Final Value)
(Six Representative Units)



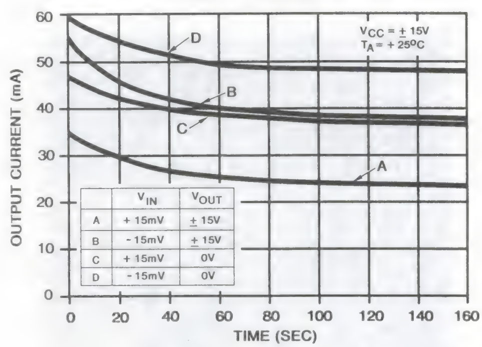
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SLEW RATE/RISE TIME vs. TEMPERATURE
R_L = 2K, C_L = 50pF, V_{CC} = ±15V

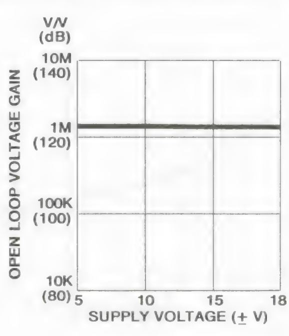


SHORT CIRCUIT CURRENT vs. TIME

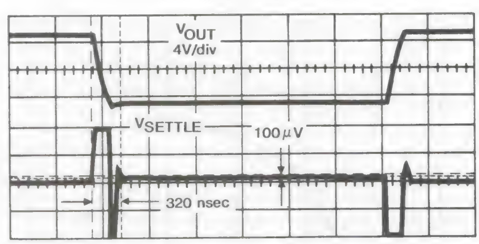


	V_{IN}	V_{OUT}
A	+ 15mV	± 15V
B	- 15mV	± 15V
C	+ 15mV	0V
D	- 15mV	0V

D.C. OPEN LOOP VOLTAGE GAIN vs. SUPPLY VOLTAGE



HA-5111 SETTLING WAVEFORM
1.5ms/DIV.



DESIGN INFORMATION (Continued)

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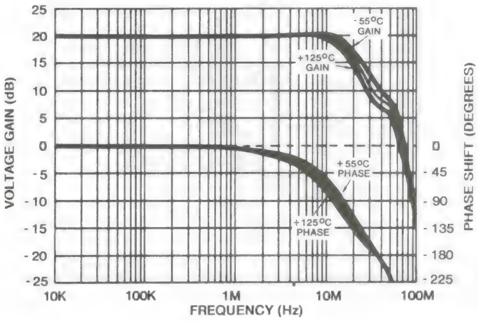
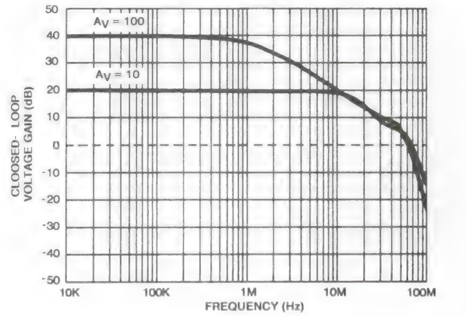
Typical Performance Curves Unless Otherwise Specified: $V\pm = \pm 15V$, $T_A = +25^oC$

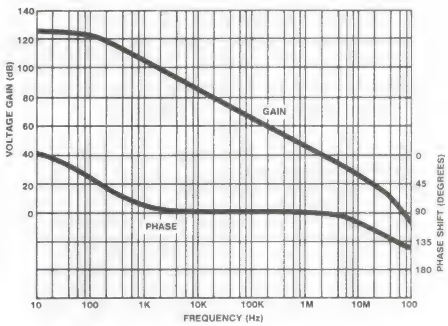
HA-5111 CLOSED LOOP GAIN AND PHASE AT HIGH AND LOW TEMPERATURE
(Typical Response of One Amplifier)
$V_{CC} = \pm 15V$, $A_V = 10V/V$, $R_L = 2K$, $C_L = 50pF$



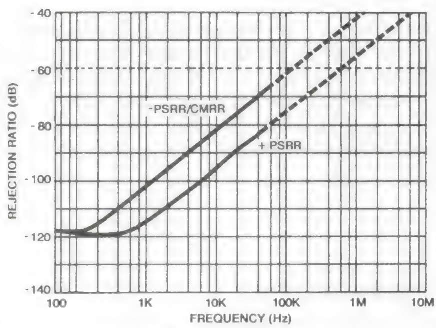
HA-5111 CLOSED LOOP VOLTAGE GAIN vs. FREQUENCY AT DIFFERENT CLOSED LOOP GAINS
$T_A = +25^oC$, $V_{CC} = \pm 15V$, $A_V = 100$, $10V/V$, $R_L = 2K$, $C_L = 50pF$



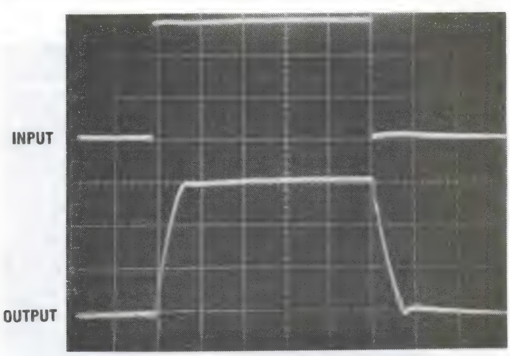
OPEN LOOP GAIN/PHASE vs. FREQUENCY



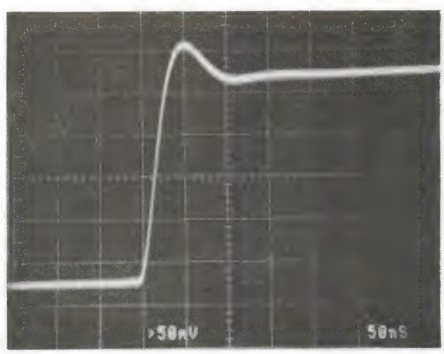
HA-5111 REJECTION RATIOS vs. FREQUENCY
$T_A = +25^oC$, $V_{CC} = \pm 15V$



SLEW RATE WAVEFORM
$V_{OUT} = \pm 3V$, $A_V = +10$, $R_L = 2k\Omega$, $C_L = 50pF$
Timescale = 200ns/Div., Scale: Input = 0.2V/Div., Output = 2V/Div.



SMALL SIGNAL WAVEFORM
Rise Time and Overshoot
$V_{OUT} = 0V$ to $+200mV$, $A_V = +10$, $R_L = 2K$, $C_L = 50pF$
Timescale = 50ns/Div.



DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Applications Information

OPERATION AT ±5V SUPPLY

The HA-5111 performs well at V_{CC} = ±5V exhibiting typical characteristics as listed below:

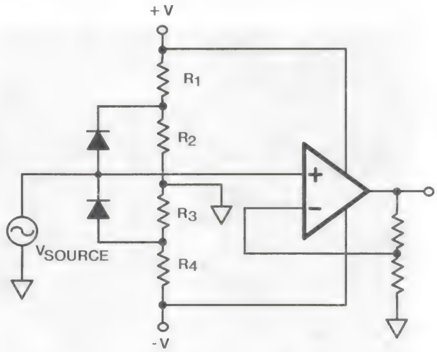
I_{CC}	3.7	mA
V_{IO}	0.5	mV
I_{BIAS}	56	nA
A_{VOL} (V_O = ±3V)	106	KV/V
V_{OUT}	3.7	V
I_{OUT}	13	mA
CMRR (ΔV_{CM} = ±2.5V)	90	dB
PSRR (ΔV_{CC} = 0.5V)	90	dB
GBW (5111)	100	MHz
Slew Rate (5111)	40	V/µs

INPUT PROTECTION

The HA-5111 has built-in back-to-back protection diodes which will limit the differential input voltage to approximately 7V. If the HA-5111 will be used in conditions where that voltage may be exceeded, then current limiting resistors must be used. No more than 25mA should be allowed to flow in the HA-5111 input.

OUTPUT SATURATION

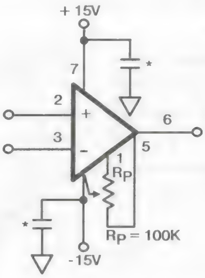
When an operational amplifier is overdriven, output devices can saturate and and sometimes take a long time to recover. Saturation can be avoided (sometimes) by using circuits such as:



If saturation cannot be avoided the HA-5111 recovers from a 25% overdrive in about 6.5µs (see photo).

OFFSET ADJUSTMENT

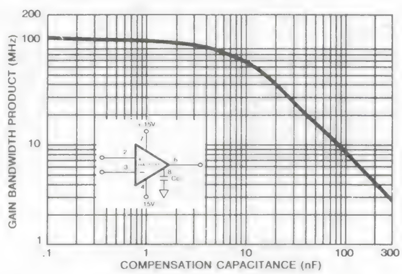
The following is the recommended V_{IO} adjust configuration:



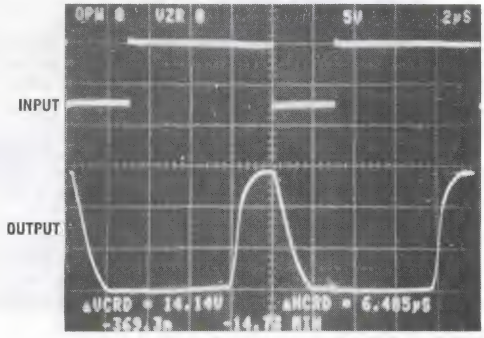
* Proper decoupling is always recommended, 0.1µF high quality capacitors should be at or vary near the device's supply pins.

COMPENSATION

An external compensation capacitor can be used with the HA-5111 connected between pin 8 and ground (or V-, V+ not recommended). A plot of gain bandwidth product vs. compensation capacitor has been included as a design aid. The capacitor should be a high frequency type mounted near the device leads to minimize parasitics.



Top: Input
Bottom: Output, 5V/Div., 2µs/Div.



Output is overdriven negative, recovers after 6µs.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_L = 2kΩ, C_L = 50pF, A_{VCL} = 10V/V Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMITS	UNITS
Offset Voltage	V_{CM} = 0V	+25°C	0.8	Table 1	mV
Offset Voltage Average Drift	Versus Temperature	-55°C to +125°C	3	7	μV/°C
Offset Current Average Drift	Versus Temperature	-55°C to +125°C	100	250	pA/°C
Input Bias Current	V_{CM} = 0V	+25°C	65	Table 1	nA
Input Offset Current	V_{CM} = 0V	+25°C	35	Table 1	nA
Differential Input Resistance	V_{CM} = 0V	+25°C	500	Table 3	kΩ
Peak-to-Peak Noise Voltage at Various Bandwidths	0.1Hz to 10Hz	+25°C	0.09	Table 3	$μV_{p-p}$
	0.1Hz to 100Hz	+25°C	0.14	0.3	$μV_{p-p}$
	0.1Hz to 1kHz	+25°C	0.47	1.0	$μV_{p-p}$
	10Hz to 1MHz	+25°C	2.76	4.0	$μV_{p-p}$
Input Noise Voltage Density	f_o = 10Hz	+25°C	5.4	9	$nV/\sqrt{Hz}$
	f_o = 100Hz	+25°C	3.4	5.5	$nV/\sqrt{Hz}$
	f_o = 1kHz	+25°C	3.2	Table 3	$nV/\sqrt{Hz}$
Input Noise Current Density	f_o = 10Hz	+25°C	6	20	$pA/\sqrt{Hz}$
	f_o = 100Hz	+25°C	1.5	5	$pA/\sqrt{Hz}$
	f_o = 1kHz	+25°C	0.52	Table 3	$pA/\sqrt{Hz}$
Large Signal Voltage Gain	V_{OUT} = ±10V	-55°C	400K	Table 1	V/V
		+25°C	1M	Table 1	V/V
		+125°C	1M	Table 1	V/V
Slew Rate	V_{OUT} = ±5V	-55°C to +125°C	±60	±40	V/μs
Full Power Bandwidth	Note 2, V_{peak} = 10V	-55°C to +125°C	1.6	0.63	MHz
Rise and Fall Times	V_{OUT} = ±200mV	-55°C to +125°C	30	80	ns
Overshoot	V_{OUT} = ±200mV	-55°C to +125°C	20	45	%
Settling Time	To 0.1% for 10V Step	+25°C	0.5	1.0	μs
	To 0.01% for 10V Step	+25°C	0.6	1.5	μs
Output Short Circuit Current	t <10 Seconds, V_{OUT} = ±15V	+25°C	±35	±50	mA
Output Resistance	Open Loop	+25°C	110	Table 3	Ω
Supply Current	No Load	+25°C	4.3	Table 1	mA
Minimum Supply Voltage	Functional Operation Only, Other Parameters Will Vary	+25°C	±4	±5	V

HARRIS

HA-5112/883

Dual, Low Noise, High Performance Uncompensated Operational Amplifier

January 1989

Features

- **This Circuit is Processed In Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- Low Input Noise Voltage Density @ 1kHz ... 6nV/$\sqrt{Hz}$ Max, 4.3nV/$\sqrt{Hz}$ Typ
- High Slew Rate ... 12V/μs Min, 20V/μs Typ
- Wide Gain Bandwidth Product ($A_{VCL} \geq 10$) .. 60MHz
- Low Offset Voltage Drift ... 3μV/°C Typ
- High Open Loop Gain (Full Temp.) ... 100kV/V Min, 250kV/V Typ
- High CMRR/PSRR (Full Temp.) ... 86dB Min, 100dB Typ
- Low Offset Voltage Drift ... 3μV/°C Typ
- No Crossover Distortion
- Standard Dual Pinout

Applications

- High Quality Audio Preamplifiers
- High Q Active Filters
- Low Noise Function Generators
- Low Distortion Oscillators
- Low Noise Comparators

Description

Low noise and high performance are key words describing the dual, uncompensated HA-5112/883. This general purpose amplifier offers an array of dynamic specifications including 12V/μs slew rate (min), and 60MHz gain-bandwidth-product for $A_{VCL} \geq 10$. Complementing these outstanding parameters is a very low noise specification of 6nV/$\sqrt{Hz}$ at 1kHz (max).

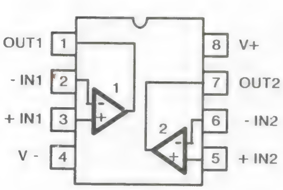
Fabricated using the Harris standard high frequency D.I. process, these operational amplifiers also offer excellent input specifications such as 2.5mV (max) offset voltage and 75nA (max) offset current. Complementing these specifications are 100dB (min) open loop gain and 100dB channel separation (typ). The HA-5112/883 also consumes a very modest amount of supply power (180mW/package).

This impressive combination of features make this amplifier ideally suited for designs ranging from audio amplifiers and active filters to the most demanding signal conditioning and instrumentation circuits.

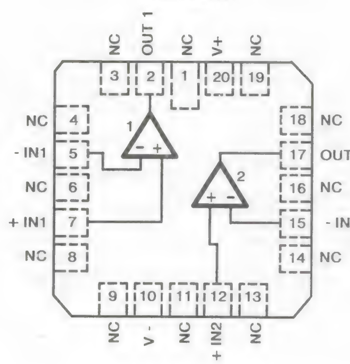
This dual operational amplifier is available with industry standard pinouts allowing for immediate interchangeability with most other dual operational amplifiers. HA-5112/883 is available in an 8 pin Ceramic Mini-DIP, 20 pin LCC and an 8 pin Metal Can (TO-99).

Pinouts

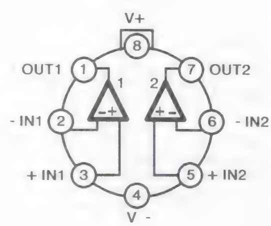
HA7-5112/883 (CERAMIC MINI-DIP)
TOP VIEW



HA4-5112/883 (CERAMIC LCC)
TOP VIEW



HA2-5112/883 (METAL CAN)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage 7V
Voltage at Either Input Terminal .... V+ to V-
Peak Output Current .... Indefinite
(One Amplifier Shorted to Ground)
Junction Temperature (T_J) .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... <2000V
Lead Temperature (Soldering 10 sec) .... +275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	121°C/W	39°C/W
Ceramic LCC Package	74°C/W	20°C/W
Metal Can Package	101°C/W	30°C/W

Package Power Dissipation at +75°C for $T_J \le$ +175°C
Ceramic DIP Package 820mW
Ceramic LCC Package 1.36W
Metal Can Package 1W

Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 8.2mW/°C
Ceramic LCC Package .... 13.6mW/°C
Metal Can Package .... 10mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±5V to ±15V
$V_{INcm} \le 1/2$ (V+ - V-)
$R_L \ge 2k\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	V_{CM} = 0V	1	+25°C	-2.0	2.0	mV
			2, 3	+125°C, -55°C	-2.5	2.5	mV
Input Bias Current	$+I_B$	V_{CM} = 0V, $+R_S$ = 10kΩ, $-R_S$ = 100Ω	1	+25°C	-200	200	nA
			2, 3	+125°C, -55°C	-325	325	nA
	$-I_B$	V_{CM} = 0V, $+R_S$ = 100Ω, $-R_S$ = 10kΩ	1	+25°C	-200	200	nA
			2, 3	+125°C, -55°C	-325	325	nA
Input Offset Current	I_{IO}	V_{CM} = 0V, $+R_S$ = 10kΩ, $-R_S$ = 10kΩ	1	+25°C	-75	75	nA
			2, 3	+125°C, -55°C	-125	125	nA
Common Mode Range	+CMR	V+ = 3V, V- = -27V	1	+25°C	+12	-	V
			2, 3	+125°C, -55°C	+12	-	V
	-CMR	V+ = 27V, V- = -3V	1	+25°C	-	-12	V
			2, 3	+125°C, -55°C	-	-12	V
Large Signal Voltage Gain	$+A_{VOL}$	V_{OUT} = 0V and +10V, R_L = 2kΩ	4	+25°C	100	-	kV/V
			5, 6	+125°C, -55°C	100	-	kV/V
	$-A_{VOL}$	V_{OUT} = 0V and -10V, R_L = 2kΩ	4	+25°C	100	-	kV/V
			5, 6	+125°C, -55°C	100	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔV_{CM} = +5V, +V = +10V, -V = -20V, V_{OUT} = -5V	1	+25°C	86	-	dB
			2, 3	+125°C, -55°C	86	-	dB
	-CMRR	ΔV_{CM} = -5V, +V = +20V, -V = -10V, V_{OUT} = +5V	1	+25°C	86	-	dB
			2, 3	+125°C, -55°C	86	-	dB

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Voltage Swing	$+V_{OUT1}$	$R_L = 2k\Omega$	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	$-V_{OUT1}$	$R_L = 2k\Omega$	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
	$+V_{OUT2}$	$R_L = 10k\Omega$	1	+25°C	12	-	V
			2, 3	+125°C, -55°C	12	-	V
	$-V_{OUT2}$	$R_L = 10k\Omega$	1	+25°C	-	-12	V
			2, 3	+125°C, -55°C	-	-12	V
Output Current	$+I_{OUT}$	$V_{OUT} = -5V$	1	+25°C	10	-	mA
			2, 3	+125°C, -55°C	10	-	mA
	$-I_{OUT}$	$V_{OUT} = +5V$	1	+25°C	-	-10	mA
			2, 3	+125°C, -55°C	-	-10	mA
Quiescent Power Supply Current	$+I_{CC}$	$V_{OUT} = 0V$	1	+25°C	-	5	mA
		$I_{OUT} = 0mA$	2, 3	+125°C, -55°C	-	6	mA
	$-I_{CC}$	$V_{OUT} = 0V$ $I_{OUT} = 0mA$	1	+25°C	-5	-	mA
			2, 3	+125°C, -55°C	-6	-	mA
Power Supply Rejection Ratio	+PSRR	$\Delta V_{SUP} = 10V$ +V = +10V, -V = -15V +V = +20V, -V = -15V	1	+25°C	86	-	dB
			2, 3	+125°C, -55°C	86	-	dB
	-PSRR	$\Delta V_{SUP} = 10V$ +V = +15V, -V = -10V +V = +15V, -V = -20V	1	+25°C	86	-	dB
			2, 3	+125°C, -55°C	86	-	dB

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

This Table Intentionally Left Blank. See A.C. Parameters on Table 3.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_{VCL} = 10V/V Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Differential Input Resistance	R_{IN}	V_{CM} = 0V	1	+25°C	250	-	kΩ
Input Noise Voltage	E_n	R_S = 20Ω, f_o = 1000Hz	1	+25°C	-	6	$nV/\sqrt{Hz}$
Input Noise Current	I_n	R_S = 2MΩ, f_o = 1000Hz	1	+25°C	-	3	$pA/\sqrt{Hz}$
Gain Bandwidth Product	GBWP	V_O = 200mV, f_o = 10kHz	1	+25°C	40	-	MHz
		V_O = 200mV, f_o = 1MHz	1	+25°C	60	-	MHz
Slew Rate	+SR	V_{OUT} = -5V to +5V	1	+25°C	12	-	V/µs
	-SR	V_{OUT} = +5V to -5V	1	+25°C	12	-	V/µs
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	+25°C	191	-	kHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 2kΩ, C_L = 50pF	1	-55°C to +125°C	10	-	V/V
Rise & Fall Time	T_R	V_{OUT} = 0V to +200mV	1, 4	+25°C	-	100	ns
	T_F	V_{OUT} = 0V to -200mV	1, 4	+25°C	-	100	ns
Overshoot	+OS	V_{OUT} = 0V to +200mV	1	+25°C	-	40	%
	-OS	V_{OUT} = 0V to -200mV	1	+25°C	-	40	%
Output Resistance	R_{OUT}	Open Loop	1	+25°C	-	150	Ω
Quiescent Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	180	mW
Channel Separation	CS	R_S = 1kΩ, A_{VCL} = 100V/V, V_{IN} = 100mV_{RMS} @ 10kHz Referred to Input	1	+25°C	90	-	dB

NOTES: 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).

3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)

4. Measured between 10% and 90% points.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

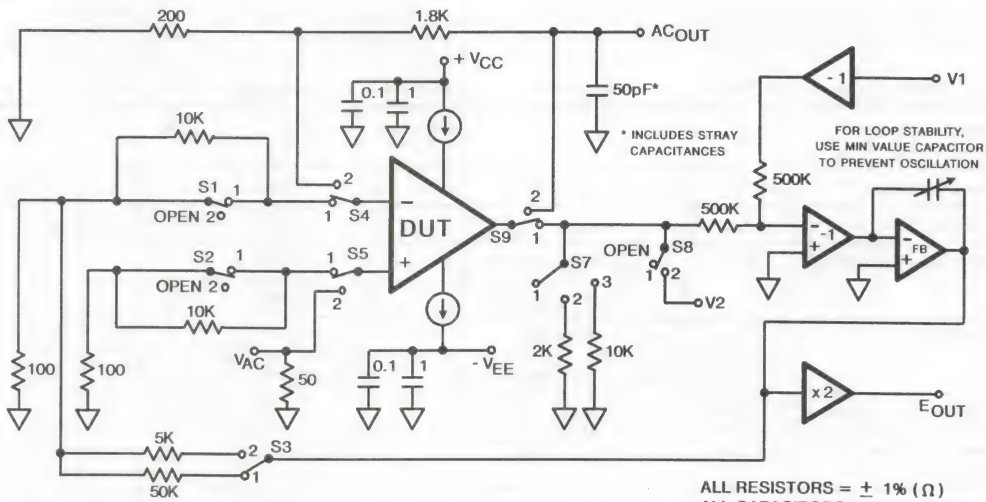
MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6
Group A Test Requirements	1, 2, 3, 4, 5, 6
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

3

OP AMPs & COMPARATORS

Test Circuit (Applies To Table 1)

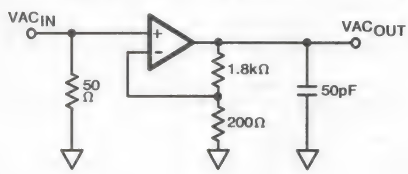


ALL RESISTORS = ± 1% (Ω)
ALL CAPACITORS = ± 10% (μF)
DUT = 1/2 OF HA - 5112/883

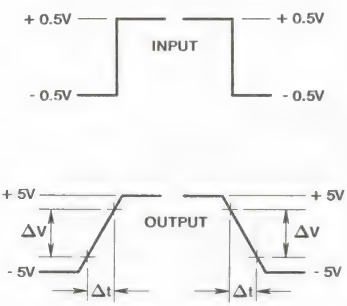
ONE OF TWO TEST LOOPS FOR THE HA - 5112/883 DUT

Test Waveforms

SIMPLIFIED TEST CIRCUIT (Applies To Table 3)

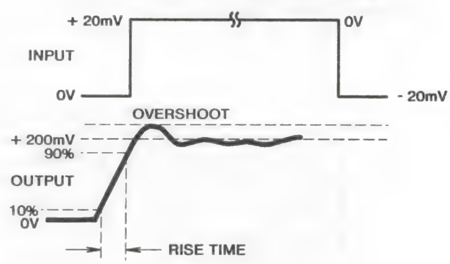


SLEW RATE WAVEFORM



$$\pm \text{S.R.} = \frac{\Delta V}{\Delta t}$$

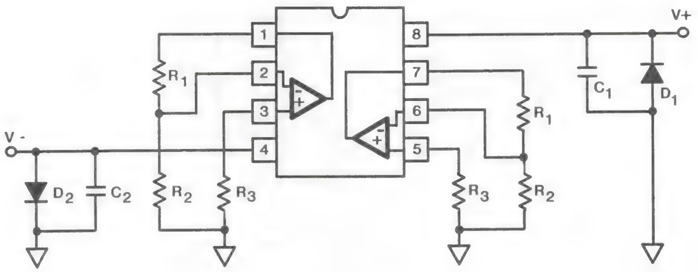
TRANSIENT RESPONSE WAVEFORM



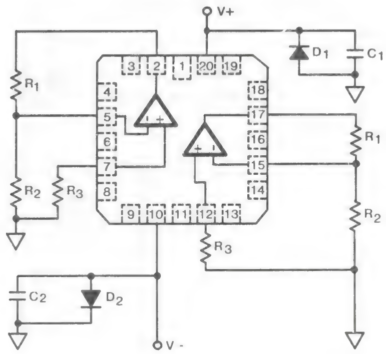
NOTE: Measured on both positive and negative transitions.

Burn-In Circuits

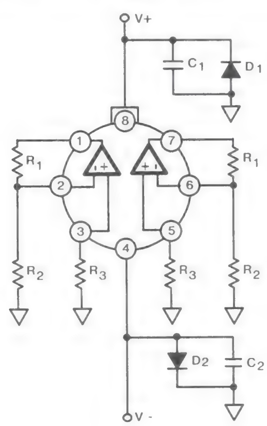
HA7-5112/883 CERAMIC DIP



HA4-5112/883 CERAMIC LCC



HA2-5112/883 (TO-99) METAL CAN



NOTES:

R_1 = 10kΩ, ±5%, 1/4W (Min)

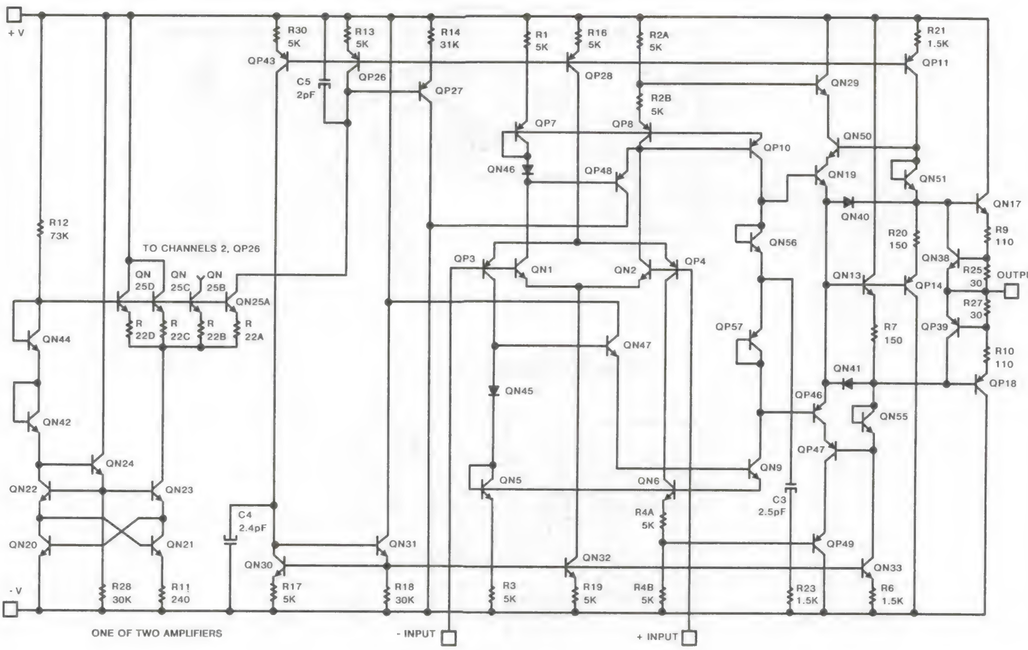
$R_2 = R_3$ = 1kΩ, ±5%, 1/4W (Min)

$C_1 = C_2$ = 0.01μF/Socket (Min) or 0.1μF/Row, (Min)

$D_1 = D_2$ = IN4002 or Equivalent/Board

$|(V+) - (V-)|$ = 30V

Schematic Diagram (½ HA-5112/883)



Die Characteristics

DIE DIMENSIONS:
98.4 x 67.3 x 19 mils
(2500 x 1710 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$1.43 \times 10^5 A/cm^2$ at 10mA

SUBSTRATE POTENTIAL (POWERED UP):
Unbiased

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

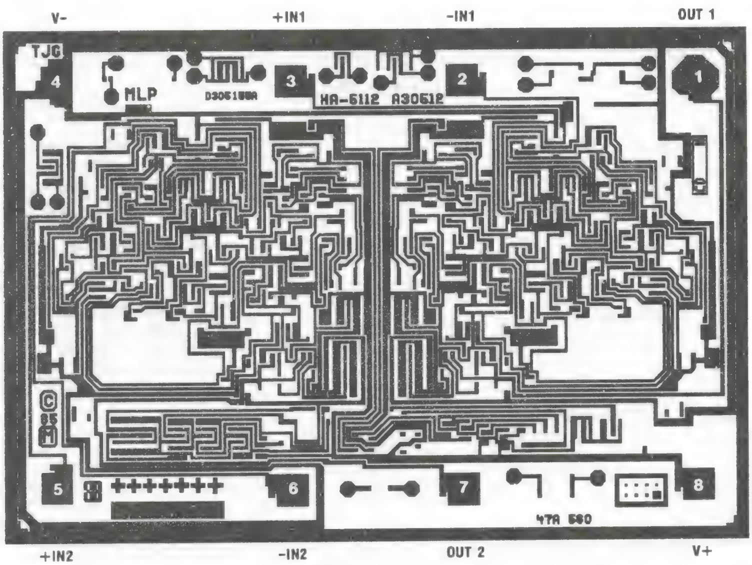
TRANSISTOR COUNT: 93

PROCESS: HFSB Linear Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)
Metal Can — 420°C (Max)

Metallization Mask Layout

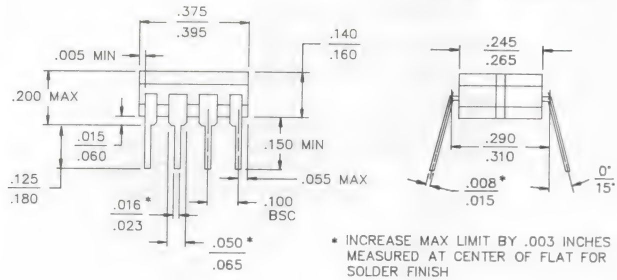
HA-5112/883



NOTE: Pin Numbers Correspond to Mini-DIP and Metal Can Packages Only.

Packaging †

8 PIN CERAMIC DIP

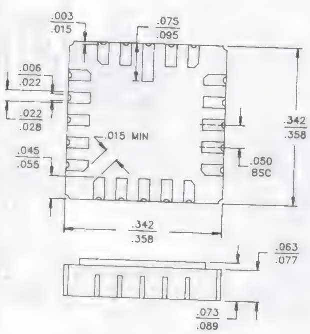


LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
- Material: Glass Frit
- Temperature: 450°C ± 10°C
- Method: Furnace Seal

INTERNAL LEAD WIRE:
- Material: Aluminum
- Diameter: 1.25 Mil
- Bonding Method: Ultrasonic

COMPLIANT OUTLINE: 38510 D-4

20 PAD CERAMIC LCC

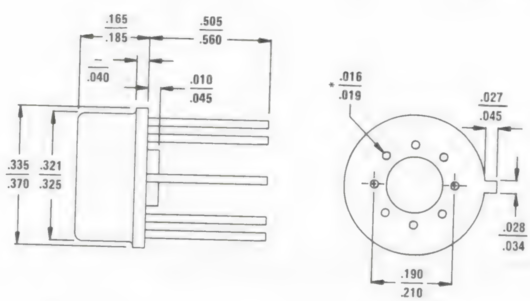


PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Ceramic, 90% Al_2O_3
PACKAGE SEAL:
- Material: Gold/Tin (80/20)
- Temperature: 320°C ± 10°C
- Method: Furnace Braze

INTERNAL LEAD WIRE:
- Material: Aluminum
- Diameter: 1.25 Mil
- Bonding Method: Ultrasonic

COMPLIANT OUTLINE: 38510 C-2

8 PIN TO-99 METAL CAN



LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
- Material: No Seal Material
- Temperature: Room Temperature
- Method: Resistance Weld

INTERNAL LEAD WIRE:
- Material: Aluminum
- Diameter: 1.25 Mil
- Bonding Method: Ultrasonic Bonded

COMPLIANT OUTLINE: 38510 A-1

*Dimension Maximum Limits Are Increased by 0.003 inches for Solder Dip Finish

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

HA-5112

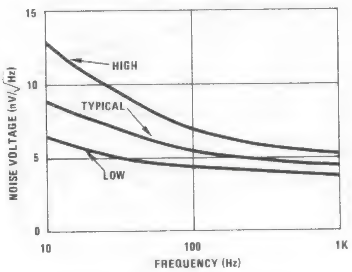
DESIGN INFORMATION

Dual, Low Noise, High Performance Uncompensated Operational Amplifier

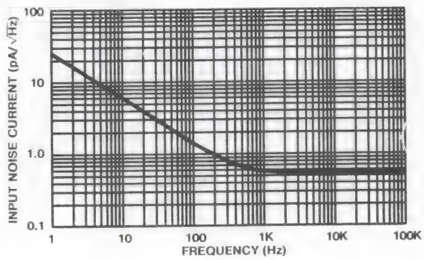
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

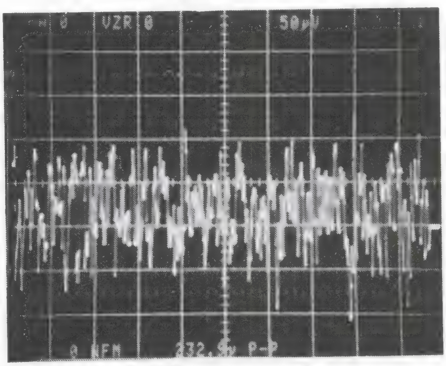
INPUT NOISE VOLTAGE DENSITY
$V_{CC} = \pm15V$, $T_A = +25^oC$



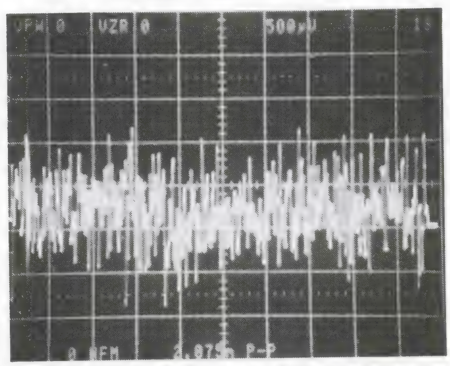
INPUT NOISE CURRENT DENSITY
$V_{CC} = \pm15V$, $T_A = +25^oC$



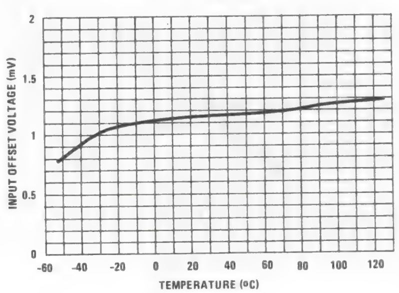
0.1Hz TO 10Hz NOISE
$V_{CC} = \pm15V$, $T_A = +25^oC$
50μV/Div., 1s/Div., A_V = 1000V/V
Input Noise = $0.232\mu V_{p-p}$



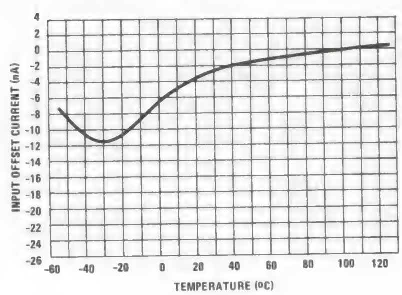
0.1Hz TO 1MHz NOISE
$V_{CC} = \pm15V$, $T_A = +25^oC$
500μV/Div., 1s/Div., A_V = 1000V/V
Total Output Noise = $2.075\mu V_{p-p}$



V_{IO} vs. TEMPERATURE
$V_{CC} = \pm15V$



I_{IO} vs. TEMPERATURE
$V_{CC} = \pm15V$



DESIGN INFORMATION (Continued)

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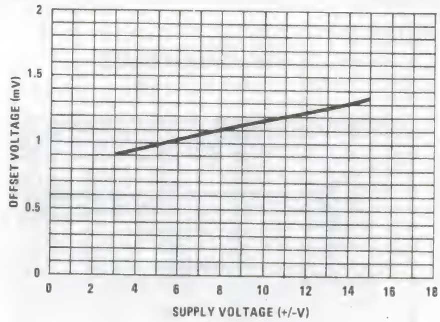
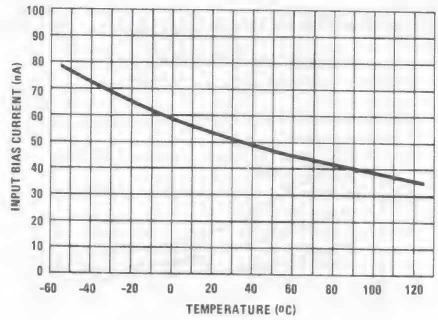
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

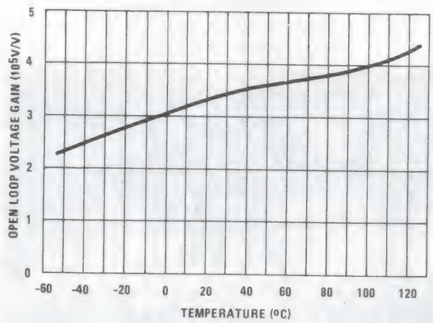
V_{IO} vs. V_{CC}
$T_A = +25^oC$



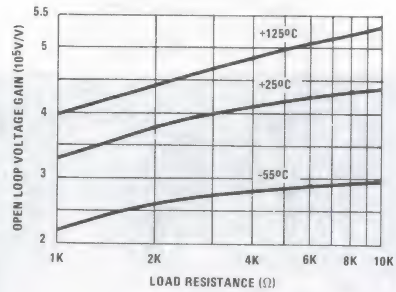
I_{BIAS} vs. TEMPERATURE
$V_{CC} = \pm15V$



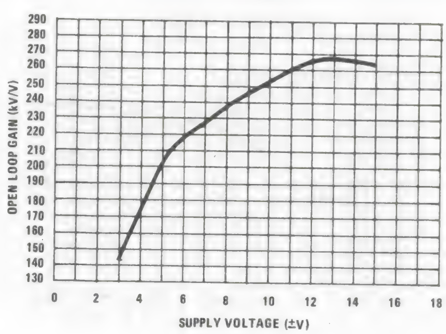
A_{VOL} vs. TEMPERATURE
$VCC = \pm15V$, $\Delta V_O = \pm10V$, $R_L = 2K$



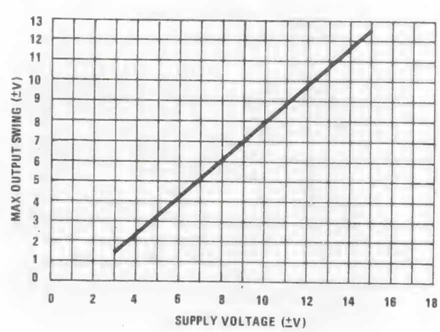
A_{VOL} vs. LOAD RESISTANCE
$V_O = \pm10V$, $V_{CC} = \pm15V$, $T_A = +25^oC$



A_{VOL} vs. V_{CC}
$T_A = +25^oC$, $R_L = 2K$



V_{OUT} vs. V_{CC}
$T_A = +25^oC$, $R_L = 2K$



DESIGN INFORMATION (Continued)

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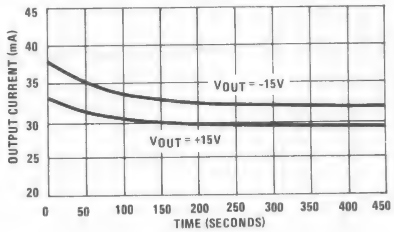
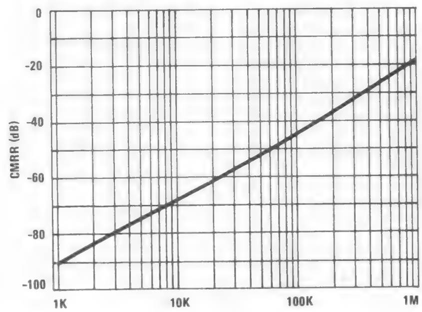
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

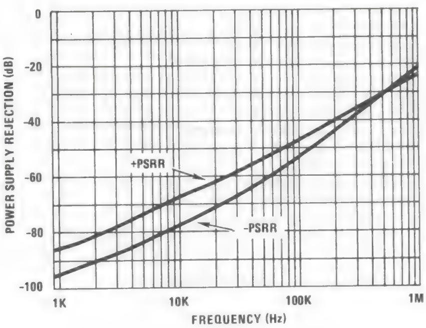
OUTPUT SHORT-CIRCUIT CURRENT vs. TIME
$V_{CC} = \pm 15V$, $T_A = +25^oC$



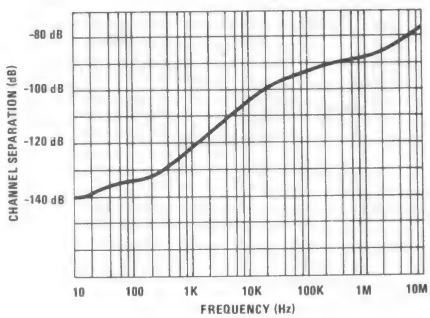
CMRR vs. FREQUENCY



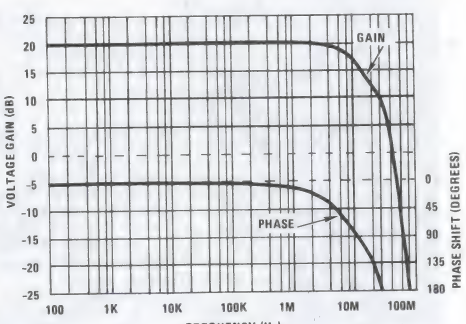
PSRR vs. FREQUENCY



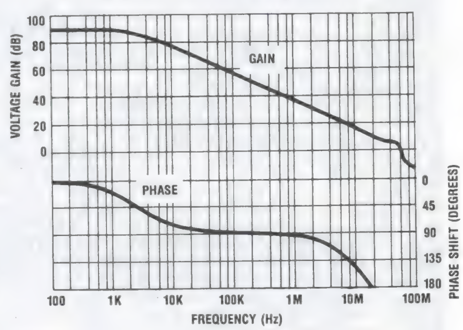
CHANNEL SEPARATION vs. FREQUENCY
10Hz ≤ f ≤ 10MHz



HA-5112 FREQUENCY RESPONSE
$A_{VCL} = 10$, $T_A = +25^oC$, $R_L = 2K$, $C_L = 50pF$



OPEN-LOOP GAIN vs. FREQUENCY
$V_{CC} = \pm 15V$, $R_L = 2K$, $C_L = 50pF$, $T_A = +25^oC$



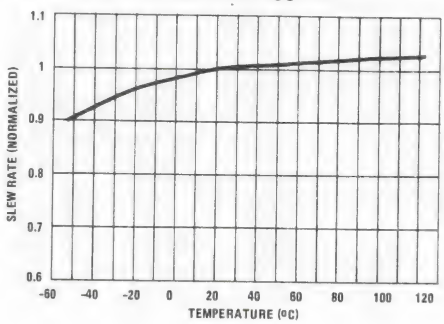
3
OP AMPs & COMPARATORS

DESIGN INFORMATION (Continued)

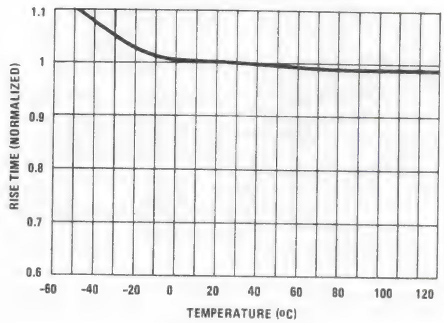
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

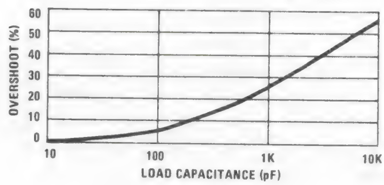
SLEW RATE vs.TEMPERATURE
$R_L = 2K$, $C_L = 50pF$, $V_{CC} = \pm15V$



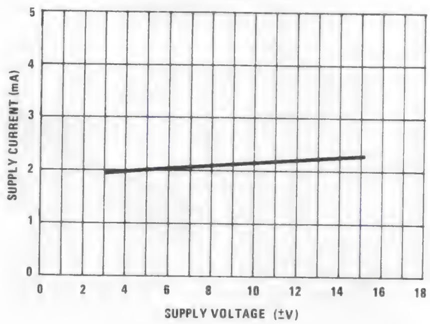
RISE TIME vs. TEMPERATURE
$R_L = 2K$, $C_L = 50pF$, $V_{CC} = \pm15V$



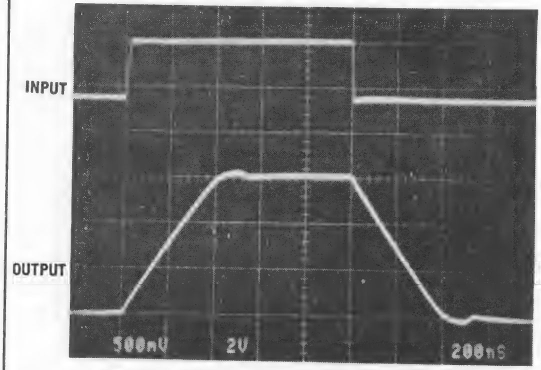
SMALL SIGNAL OVERSHOOT vs. C_{LOAD}
$R_L = 2K$, $T_A = +25^oC$, $V_{CC} = \pm15V$



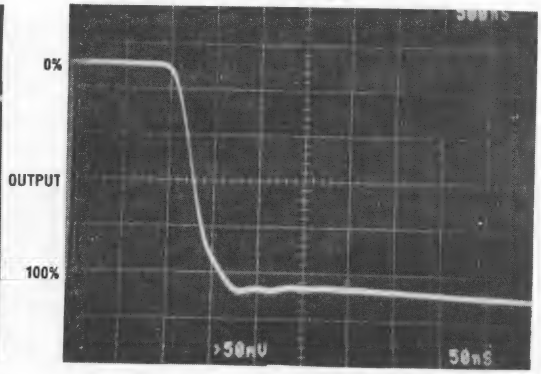
I_{CC} vs. V_{CC}
$T_A = +25^oC$, $I_{OUT} = 0mA$



LARGE SIGNAL RESPONSE
$V_{OUT} = \pm3V$, $A_V = 10$, $R_L = 2K$, $C_L = 50pF$
Input = 500mV/Div., Output = 2V/Div., Timescale = 200ns/Div.



SMALL SIGNAL RESPONSE
V_{OUT} = 0V to -200mV for Fall Time & -Overshoot
$A_V = 10$, $R_L = 2K$, $C_L = 50pF$, Timescale = 50ns/Div.



DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_L = 2kΩ, C_L = 50pF, A_{VCL} = 10V/V Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMITS	UNITS
Offset Voltage	V_{CM} = 0V	+25°C	0.8	Table 1	mV
Offset Voltage Average Drift	Versus Temperature	-55°C to +125°C	3	7	μV/°C
Offset Current Average Drift	Versus Temperature	-55°C to +125°C	100	250	pA/°C
Input Bias Current	V_{CM} = 0V	+25°C	50	Table 1	nA
Input Offset Current	V_{CM} = 0V	+25°C	25	Table 1	nA
Differential Input Resistance	V_{CM} = 0V	+25°C	500	Table 3	kΩ
Input Noise Voltage Density	f_O = 10Hz	+25°C	10.3	14	$nV/\sqrt{Hz}$
	f_O = 100Hz	+25°C	5.6	8	$nV/\sqrt{Hz}$
	f_O = 1kHz	+25°C	4.3	Table 3	$nV/\sqrt{Hz}$
Input Noise Current Density	f_O = 10Hz	+25°C	6	15	$pA/\sqrt{Hz}$
	f_O = 100Hz	+25°C	1.5	5	$pA/\sqrt{Hz}$
	f_O = 1kHz	+25°C	0.52	Table 3	$pA/\sqrt{Hz}$
Large Signal Voltage Gain	V_{OUT} = ±10V	-55°C	200	Table 1	kV/V
		+25°C	300	Table 1	kV/V
		+125°C	400	Table 1	kV/V
Slew Rate	V_{OUT} = ±5V	-55°C to +125°C	±20	±10	V/μs
Full Power Bandwidth	Note 2, V_{peak} = 10V	-55°C to +125°C	318	159	kHz
Rise and Fall Times	V_{OUT} = ±200mV	-55°C to +125°C	48	130	ns
Overshoot	V_{OUT} = ±200mV	-55°C to +125°C	30	50	%
Settling Time	To 0.1% for 10V Step	+25°C	0.6	1	μs
	To 0.01% for 10V Step	+25°C	1.2	2	μs
Output Short Circuit Current	To <10 Seconds, V_{OUT} = ±15V	+25°C	±35	±50	mA
Output Resistance	Open Loop	+25°C	110	Table 3	Ω
Channel Separation	f = 10kHz	+25°C	108	Table 3	dB
Supply Current	No Load	+25°C	2.4	Table 1	mA
Minimum Supply Voltage	Functional Operation Only, Other Parameters Will Vary	+25°C	±4	±5	V

HARRIS

HA-5114/883

Low Noise, High Performance Operational Amplifier

January 1989

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Low Input Noise Voltage Density @ 1kHz.. 6nV/$\sqrt{Hz}$ Max**
  4.3nV/$\sqrt{Hz}$ Typ
- **High Slew Rate .... 12V/μs Min**
  20V/μs Typ
- **Wide Gain Bandwidth Product ($A_{VCL} \geq 10$) .. 60MHz Typ**
- **High Open Loop Gain (Full Temp) ...... 100kV/V Min**
  250kV/V Typ
- **High CMRR, PSRR (Full Temp).............. 86dB Min**
  100dB Typ
- **Low Offset Voltage Drift .... 3μV/°C Typ**
- **No Crossover Distortion**
- **Standard Quad Pinout**

Applications

- **High Quality Audio Preamplifiers**
- **High Q Active Filters**
- **Low Noise Function Generators**
- **Low Distortion Oscillators**
- **Low Noise Comparators**

Description

Low noise and high performance are key words describing the quad, uncompensated HA-5114/883. This general purpose amplifier offers an array of dynamic specifications including 12V/μs slew rate (min), and 60MHz gain-bandwidth-product for $A_{VCL} \geq 10$. Complementing these outstanding parameters is a very low noise specification of 6nV/$\sqrt{Hz}$ at 1kHz (max).

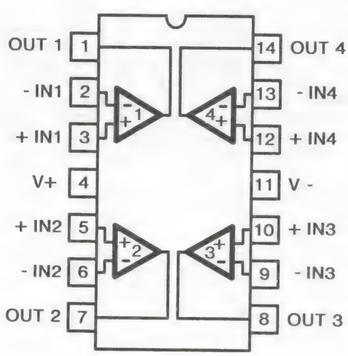
Fabricated using the Harris standard high frequency D.I. process, these operational amplifiers also offer excellent input specifications such as 2.5mV (max) offset voltage and 75nA (max) offset current. Complementing these specifications are 100dB (min) open loop gain and 100 dB channel separation (typ). Economically, HA-5114/883 also consumes a very modest amount of power (225mW/package), while also saving board space and cost.

This impressive combination of features make this amplifier ideally suited for designs ranging from audio amplifiers and active filters to the most demanding signal conditioning and instrumentation circuits.

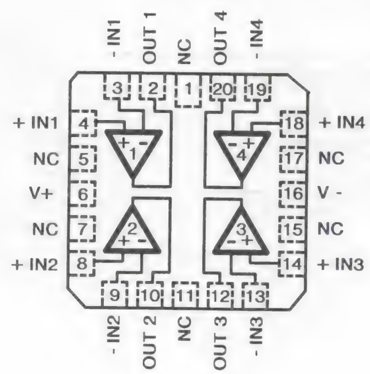
This quad operational amplifier is available with industry standard pinouts allowing for immediate interchangeability with most other quad operational amplifiers. The HA-5114/883 is available in a 14 pin Ceramic DIP and a 20 pin Ceramic LCC package.

Pinouts

HA1-5114/883 (CERAMIC DIP)
TOP VIEW



HA4-5114/883 (METAL CAN)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage 7V
Voltage at Either Input Terminal .... V+ to V-
Peak Output Current .... Indefinite
(One Amplifier Shorted to Ground)
Junction Temperature (T_J) .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... <2000V
Lead Temperature (Soldering 10 sec) .... +275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	78°C/W	18°C/W
Ceramic LCC Package	76°C/W	19°C/W

Package Power Dissipation Limit at +75°C for $T_J \leq$ +175°C
Ceramic DIP Package 1.29mW
Ceramic LCC Package 1.32W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 12.9mW/°C
Ceramic LCC Package .... 13.1mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±5V to ±15V
$V_{INcm} \leq 1/2$ (V+ - V-)
$R_L \geq 2k\Omega$

3

OP AMPs & COMPARATORS

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	V_{CM} = 0V	1	+25°C	-2.5	2.5	mV
			2, 3	+125°C, -55°C	-3.0	3.0	mV
Input Bias Current	$+I_B$	V_{CM} = 0V $+R_S$ = 10kΩ $-R_S$ = 100Ω	1	+25°C	-200	200	nA
			2, 3	+125°C, -55°C	-325	325	nA
	$-I_B$	V_{CM} = 0V $+R_S$ = 100Ω $-R_S$ = 10kΩ	1	+25°C	-200	200	nA
			2, 3	+125°C, -55°C	-325	325	nA
Input Offset Current	I_{IO}	V_{CM} = 0V $+R_S$ = 10kΩ $-R_S$ = 10kΩ	1	+25°C	-75	75	nA
			2, 3	+125°C, -55°C	-125	125	nA
Common Mode Range	+CMR	V+ = 3V V- = -27V	1	+25°C	+12	-	V
			2, 3	+125°C, -55°C	+12	-	V
	-CMR	V+ = 27V V- = -3V	1	+25°C	-	-12	V
			2, 3	+125°C, -55°C	-	-12	V
Large Signal Voltage Gain	$+A_{VOL}$	V_{OUT} = 0V and +10V R_L = 2kΩ	4	+25°C	100	-	kV/V
			5, 6	+125°C, -55°C	100	-	kV/V
	$-A_{VOL}$	V_{OUT} = 0V and -10V R_L = 2kΩ	4	+25°C	100	-	kV/V
			5, 6	+125°C, -55°C	100	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔV_{CM} = +5V +V = +10V -V = -20V V_{OUT} = -5V	1	+25°C	86	-	dB
			2, 3	+125°C, -55°C	86	-	dB
	-CMRR	ΔV_{CM} = -5V +V = +20V -V = -10V V_{OUT} = +5V	1	+25°C	86	-	dB
			2, 3	+125°C, -55°C	86	-	dB

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Voltage Swing	$+V_{OUT1}$	R_L = 2kΩ	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	$-V_{OUT1}$	R_L = 2kΩ	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
	$+V_{OUT2}$	R_L = 10kΩ	1	+25°C	12	-	V
			2, 3	+125°C, -55°C	12	-	V
	$-V_{OUT2}$	R_L = 10kΩ	1	+25°C	-	-12	V
			2, 3	+125°C, -55°C	-	-12	V
Output Current	$+I_{OUT}$	V_{OUT} = -5V	1	+25°C	10	-	mA
			2, 3	+125°C, -55°C	10	-	mA
	$-I_{OUT}$	V_{OUT} = +5V	1	+25°C	-	-10	mA
			2, 3	+125°C, -55°C	-	-10	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V	1	+25°C	-	6.5	mA
		I_{OUT} = 0mA	2, 3	+125°C, -55°C	-	7.5	mA
	$-I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-6.5	-	mA
			2, 3	+125°C, -55°C	-7.5	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = 10V +V = +10V, -V = -15V +V = +20V, -V = -15V	1	+25°C	86	-	dB
			2, 3	+125°C, -55°C	86	-	dB
	-PSRR	ΔV_{SUP} =10V +V = +15V, -V = -10V +V = +15V, -V = -20V	1	+25°C	86	-	dB
			2, 3	+125°C, -55°C	86	-	dB

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

This Table Intentionally Left Blank. See A.C. Parameters on Table 3.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_{VCL} = 10V/V Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Differential Input Resistance	R_{IN}	V_{CM} = 0V	1	+25°C	250	-	kΩ
Input Noise Voltage	E_n	R_S = 20Ω, f_o = 1000Hz	1	+25°C	-	6	nV/√Hz
Input Noise Current	I_n	R_S = 2MΩ, f_o = 1000Hz	1	+25°C	-	3	pA/√Hz
Gain Bandwidth Product	GBWP	V_O = 200mV, f_o = 10kHz	1	+25°C	40	-	MHz
		V_O = 200mV, f_o = 1MHz	1	+25°C	60	-	MHz
Slew Rate	+SR	V_{OUT} = -5V to +5V	1	+25°C	12	-	V/µs
	-SR	V_{OUT} = +5V to -5V	1	+25°C	12	-	V/µs
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	+25°C	191	-	kHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 2kΩ, C_L = 50pF	1	-55°C to +125°C	10	-	V/V
Rise & Fall Time	T_R	V_{OUT} = 0V to +200mV	1, 4	+25°C	-	100	ns
	T_F	V_{OUT} = 0V to -200mV	1, 4	+25°C	-	100	ns
Overshoot	+OS	V_{OUT} = 0V to +200mV	1	+25°C	-	40	%
	-OS	V_{OUT} = 0V to -200mV	1	+25°C	-	40	%
Output Resistance	R_{OUT}	Open Loop	1	+25°C	-	150	Ω
Quiescent Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	225	mW
Channel Separation	CS	R_S = 1kΩ, A_{VCL} = 100V/V, V_{IN} = 100mV_{RMS} @ 10kHz Referred to Input	1	+25°C	90	-	dB

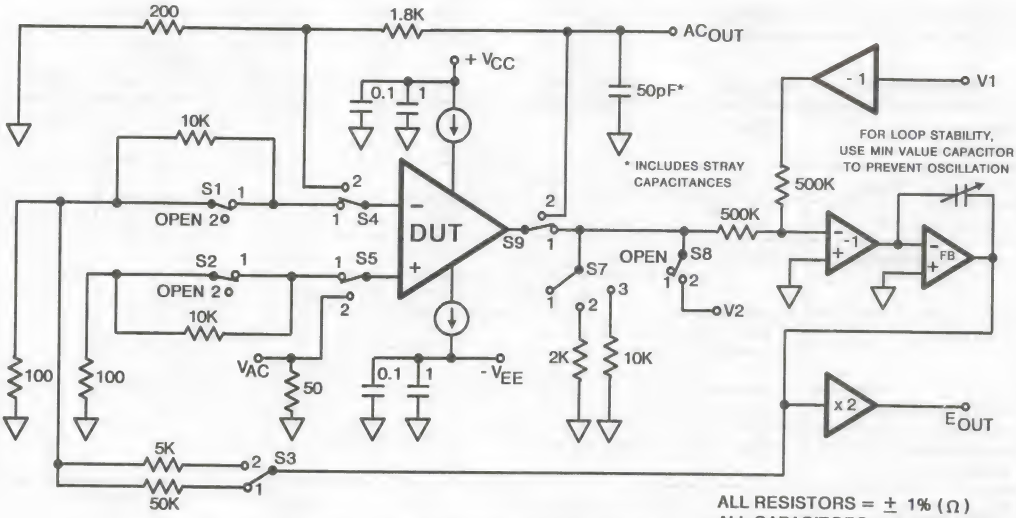
NOTES:
1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).
3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)
4. Measured between 10% and 90% points.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6
Group A Test Requirements	1, 2, 3, 4, 5, 6
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

Test Circuit

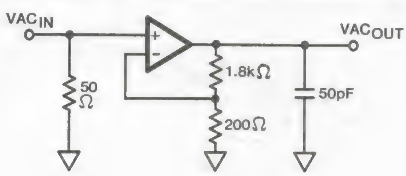


ONE OF FOUR TEST LOOPS FOR THE HA - 5114/ 883

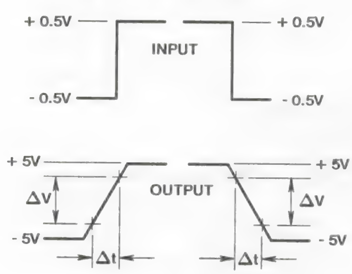
ALL RESISTORS = ± 1% (Ω)
ALL CAPACITORS = ± 10% (μF)
DUT = 1/4 OF HA - 5114/ 883

Test Waveforms

SIMPLIFIED TEST CIRCUIT (Applies To Table 3)

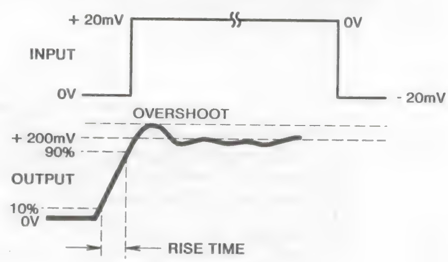


SLEW RATE WAVEFORM



$$\pm \text{S.R.} = \frac{\Delta V}{\Delta t}$$

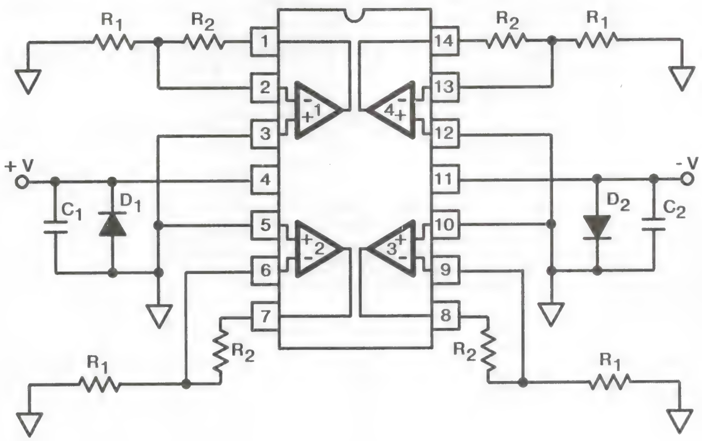
TRANSIENT RESPONSE WAVEFORM



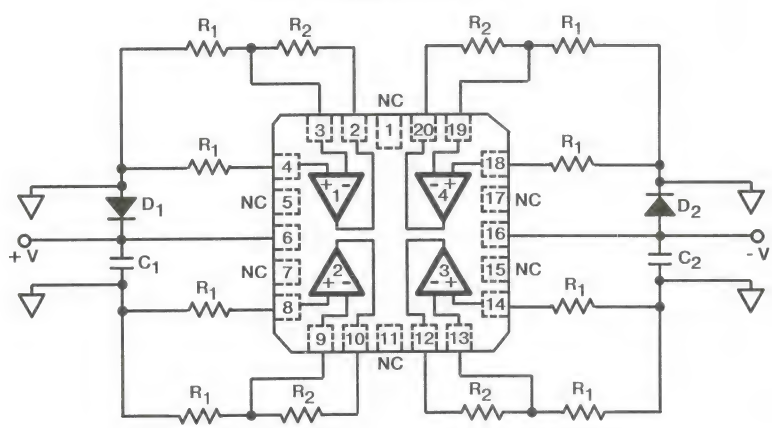
NOTE: Measured on both positive and negative transitions.

Burn-In Circuits

HA7-5114/883 CERAMIC DIP



HA4-5114/883 CERAMIC LCC



NOTES:

R_1 = 1kΩ, 5%, 1/4W (Per Socket) (Min)

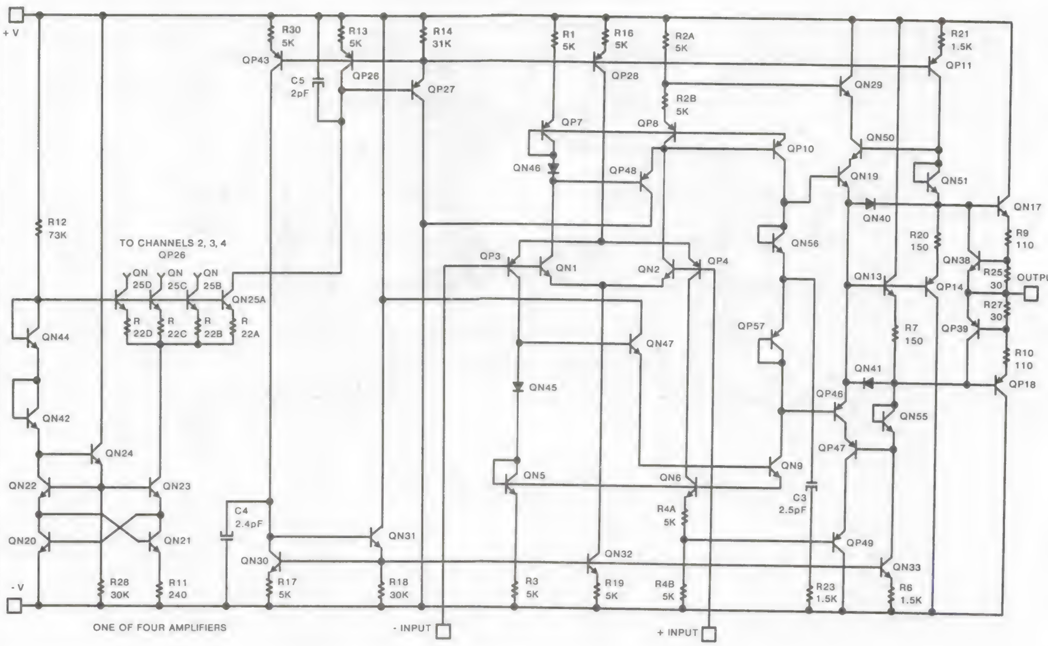
R_2 = 10kΩ, 5%, 1/4W/Socket (Min)

$C_1 = C_2$ = 0.01μF/Socket (Min) or 0.1μF/Row (Min)

$D_1 = D_2$ = IN4002 or Equivalent (Per Board)

$|(V+) - (V-)|$ = 30V

Schematic Diagram (1/4 HA-5114/883)



ONE OF FOUR AMPLIFIERS

Die Characteristics

DIE DIMENSIONS:
99.6 x 95.3 x 19 mils
(2530 x 2420 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
1.43 x 10^5A/cm^2 at 10mA

SUBSTRATE POTENTIAL (POWERED UP):
Unbiased

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

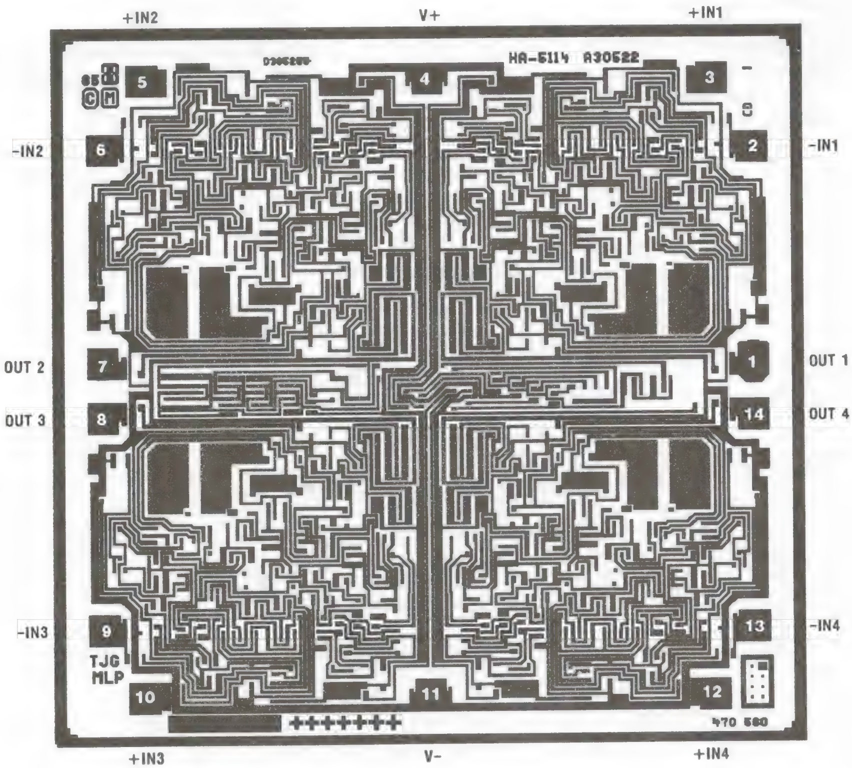
TRANSISTOR COUNT: 175

PROCESS: HFSB Linear Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

Metallization Mask Layout

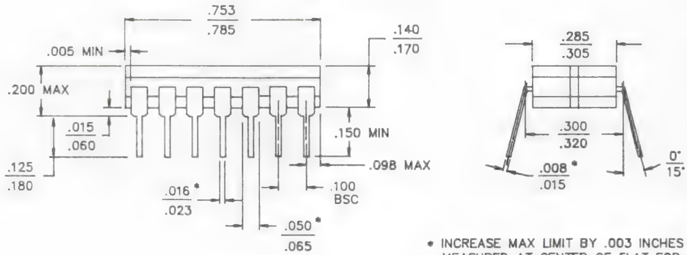
HA-5114/883



NOTE: Pad Numbers Correspond to 14 Lead Ceramic DIIP Package Only.

Packaging†

14 PIN CERAMIC DIP

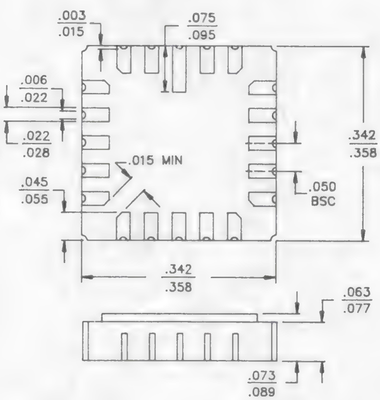


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-1

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

HA-5114

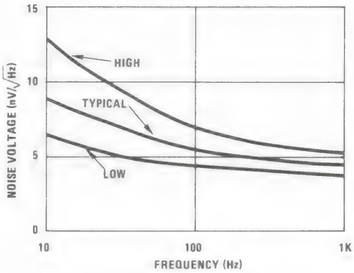
DESIGN INFORMATION

Low Noise, High Performance Operational Amplifier

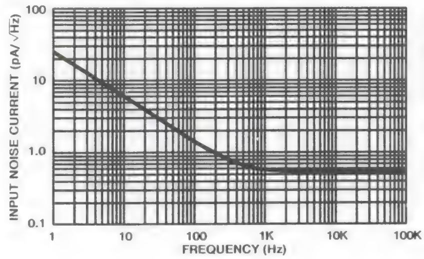
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

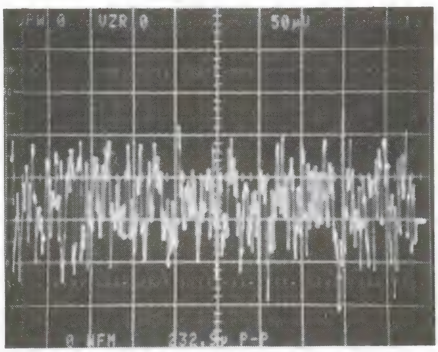
INPUT NOISE VOLTAGE DENSITY
$V_{CC} = \pm15V$, $T_A = +25^oC$



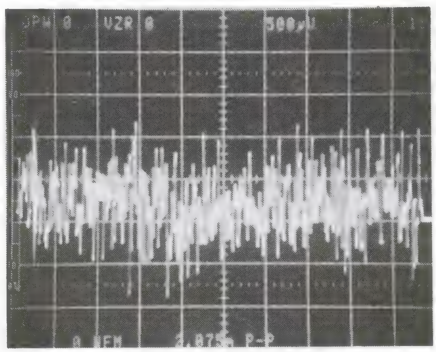
INPUT NOISE CURRENT DENSITY
$V_{CC} = \pm15V$, $T_A = +25^oC$



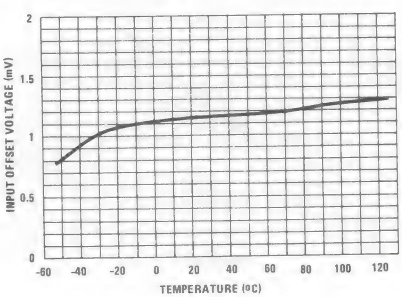
0.1Hz TO 10Hz NOISE
$V_{CC} = \pm15V$, $T_A = +25^oC$
50µV/Div., 1s/Div., $A_V = 1000V/V$
Input Noise = $0.232\mu V_{p-p}$



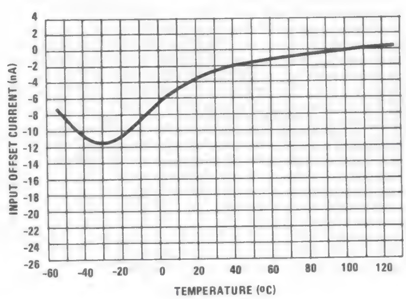
0.1Hz TO 1MHz NOISE
$V_{CC} = \pm15V$, $T_A = +25^oC$
500µV/Div., 1s/Div., $A_V = 1000V/V$
Total Output Noise = $2.075\mu V_{p-p}$



V_{IO} vs. TEMPERATURE
$V_{CC} = \pm15V$



I_{IO} vs. TEMPERATURE
$V_{CC} = \pm15V$



3
OP AMPs & COMPARATORS

DESIGN INFORMATION (Continued)

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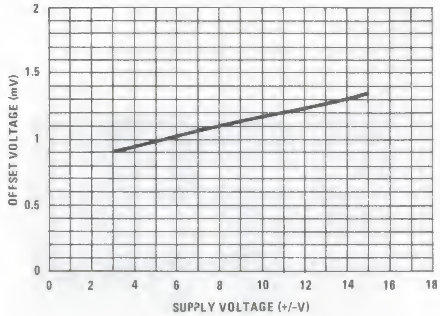
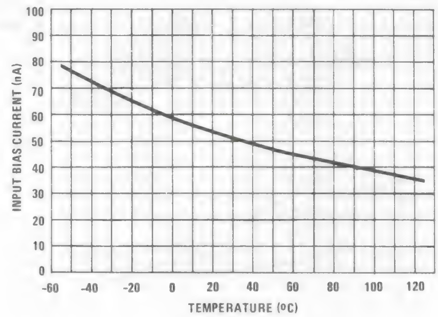
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

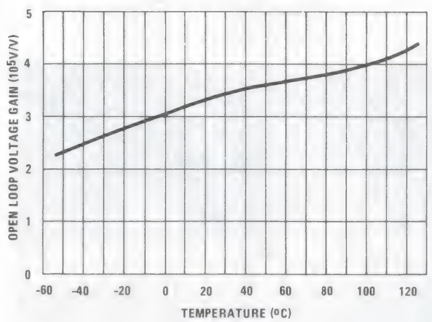
V_{IO} vs. V_{CC}
$T_A = +25^oC$



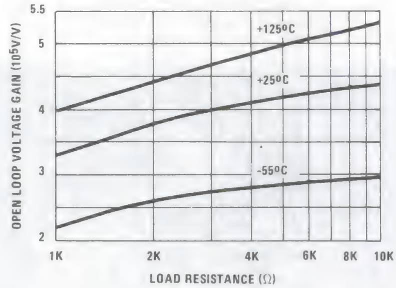
I_{BIAS} vs. TEMPERATURE
$V_{CC} = \pm15V$



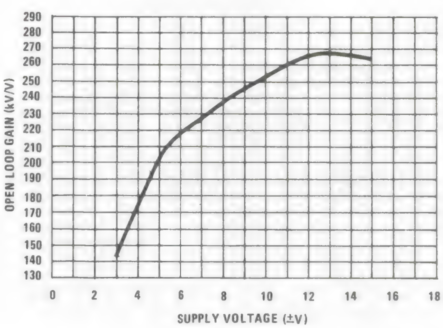
A_{VOL} vs. TEMPERATURE
$VCC = \pm15V$, $\Delta V_O = \pm10V$, $R_L = 2k\Omega$



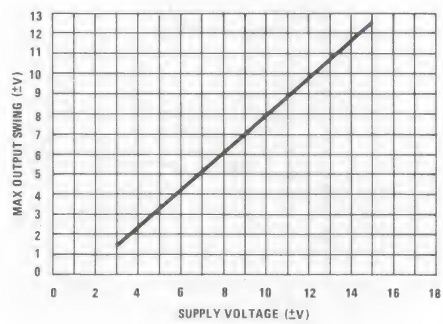
A_{VOL} vs. LOAD RESISTANCE
$V_O = \pm10V$, $V_{CC} = \pm15V$, $T_A = +25^oC$



A_{VOL} vs. V_{CC}
$T_A = +25^oC$, $R_L = 2k\Omega$



V_{OUT} vs. V_{CC}
$T_A = +25^oC$, $R_L = 2k\Omega$



DESIGN INFORMATION (Continued)

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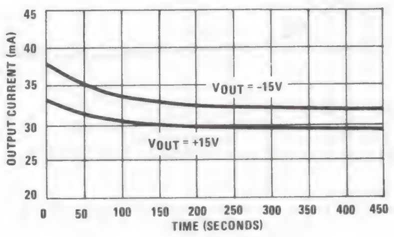
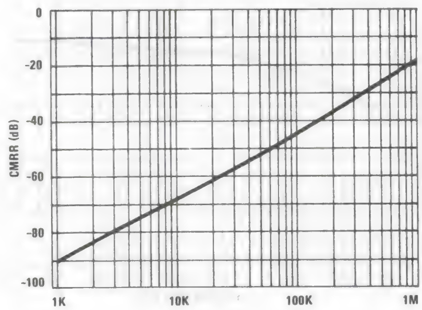
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

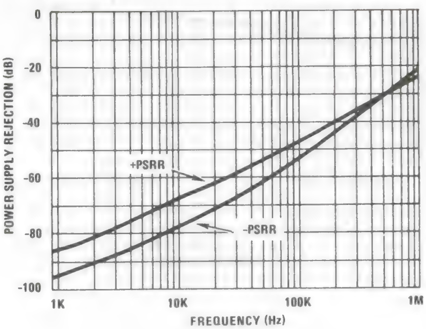
OUTPUT SHORT-CIRCUIT CURRENT vs. TIME
$V_{CC} = \pm15V$, $T_A = +25^oC$



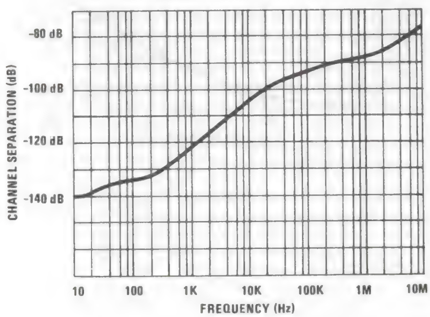
CMRR vs. FREQUENCY



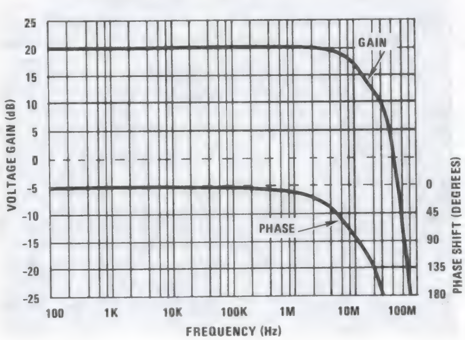
PSRR vs. FREQUENCY



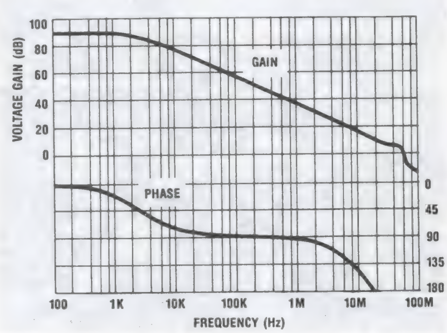
CHANNEL SEPARATION vs. FREQUENCY
$10Hz \leq f \leq 10MHz$



HA-5114 FREQUENCY RESPONSE
$A_{VCL} = 10$, $T_A = +25^oC$, $R_L = 2k\Omega$, $C_L = 50pF$



OPEN-LOOP GAIN vs. FREQUENCY
$V_{CC} = \pm15V$, $R_L = 2k\Omega$, $C_L = 50pF$, $T_A = +25^oC$



DESIGN INFORMATION (Continued)

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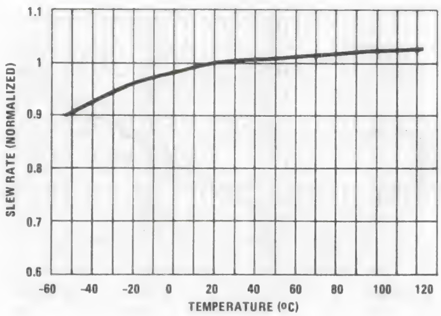
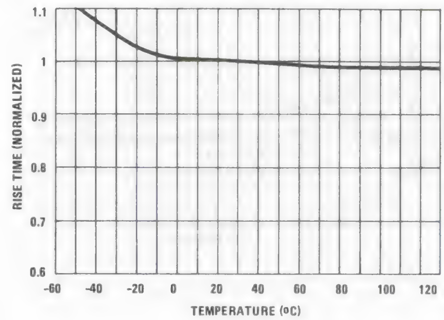
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

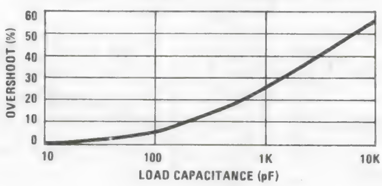
SLEW RATE vs.TEMPERATURE
$R_L = 2K$, $C_L = 50pF$, $V_{CC} = \pm15V$



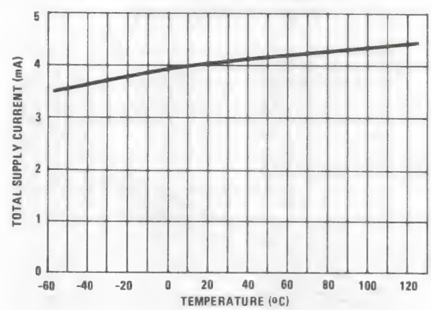
RISE TIME vs. TEMPERATURE
$R_L = 2K$, $C_L = 50pF$, $V_{CC} = \pm15V$



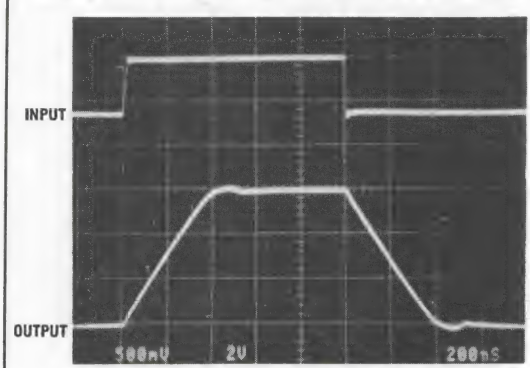
SMALL SIGNAL OVERSHOOT vs. C_{LOAD}
$R_L = 2K$, $T_A = +25^oC$, $V_{CC} = \pm15V$



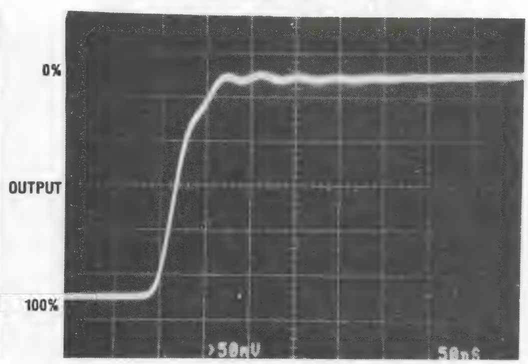
I_{CC} vs. TEMPERATURE
$T_A = +25^oC$, $V_{CC} = \pm15V$, $I_{OUT} = 0mA$



LARGE SIGNAL RESPONSE
$V_{OUT} = \pm3V$, $A_V = +10$, $R_L = 2k\Omega$, $C_L = 50pF$
Input = 500mV/Div., Output = 2V/Div., Timescale = 200ns/Div.



SMALL SIGNAL RESPONSE
V_{OUT} = 0V to +200mV for Rise Time & +Overshoot
$A_V = +10$, $R_L = 2k\Omega$, $C_L = 50pF$, Timescale = 50ns/Div.



DESIGN INFORMATION (Continued)

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TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_L = 2kΩ, C_L = 50pF, A_{VCL} = 10V/V Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMITS	UNITS
Offset Voltage	V_{CM} = 0V	+25°C	0.8	Table 1	mV
Offset Voltage Average Drift	Versus Temperature	-55°C to +125°C	3	7	μV/°C
Offset Current Average Drift	Versus Temperature	-55°C to +125°C	100	250	pA/°C
Input Bias Current	V_{CM} = 0V	+25°C	50	Table 1	nA
Input Offset Current	V_{CM} = 0V	+25°C	25	Table 1	nA
Differential Input Resistance	V_{CM} = 0V	+25°C	500	Table 3	kΩ
Input Noise Voltage Density	f_O = 10Hz	+25°C	10.3	14	$nV/\sqrt{Hz}$
	f_O = 100Hz	+25°C	5.6	8	$nV/\sqrt{Hz}$
	f_O = 1kHz	+25°C	4.3	Table 3	$nV/\sqrt{Hz}$
Input Noise Current Density	f_O = 10Hz	+25°C	6	15	$pA/\sqrt{Hz}$
	f_O = 100Hz	+25°C	1.5	5	$pA/\sqrt{Hz}$
	f_O = 1kHz	+25°C	0.52	Table 3	$pA/\sqrt{Hz}$
Large Signal Voltage Gain	V_{OUT} = ±10V	-55°C	200	Table 1	kV/V
		+25°C	300	Table 1	kV/V
		+125°C	400	Table 1	kV/V
Slew Rate	V_{OUT} = ±5V	-55°C to +125°C	±20	±10	V/μs
Full Power Bandwidth	Note 2, V_{peak} = 10V	-55°C to +125°C	318	159	kHz
Rise and Fall Times	V_{OUT} = ±200mV	-55°C to +125°C	48	130	ns
Overshoot	V_{OUT} = ±200mV	-55°C to +125°C	30	50	%
Settling Time	To 0.1% for 10V Step	+25°C	0.6	1	μs
	To 0.01% for 10V Step	+25°C	1.2	2	μs
Output Short Circuit Current	To <10 Seconds, V_{OUT} = ±15V	+25°C	±35	±50	mA
Output Resistance	Open Loop	+25°C	110	Table 3	Ω
Channel Separation	f = 10kHz	+25°C	108	Table 3	dB
Supply Current	No Load	+25°C	4.2	Table 1	mA
Minimum Supply Voltage	Functional Operation Only, Other Parameters Will Vary	+25°C	±4	±5	V

HARRIS

HA-5127/883

Ultra-Low Noise, Precision Operational Amplifier

January 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- High Slew Rate .... 7V/μs (Min)
- Wide Unity Gain Bandwidth .... 5MHz (Min)
- Low Noise Voltage (@1kHz)....... 4.5nV/$\sqrt{Hz}$ (Max)
- Low Offset Voltage .... 100μV (Max)
- Low Offset Drift With Temperature .. 1.8μV/°C (Max)
- High CMRR............................ 100dB (Min)
- High Voltage Gain .... 700kV/V (Min)

Applications

- High Speed Signal Conditioners
- Wide Bandwidth Instrumentation Amplifiers
- Low Level Transducer Amplifiers
- Fast, Low Level Voltage Comparators
- Highest Quality Audio Preamplifiers
- Pulse/RF Amplifiers

Description

The HA-5127/883 monolithic operational amplifier features an excellent combination of precision D.C. and wideband high speed characteristics. Utilizing the Harris D.I. technology and advanced processing techniques, this unique design unites low noise precision instrumentation performance with high speed, wideband capability.

This amplifier's impressive list of features include low V_{OS}, wide gain-bandwidth, high open loop gain, and high CMRR. Additionally, this flexible device operates over a wide supply range while consuming only 120mW of power.

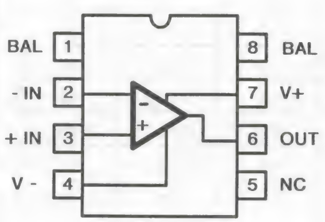
Using the HA-5127/883 allows designers to minimize errors while maximizing speed and bandwidth.

This device is ideally suited for low level transducer signal amplifer circuits. Other applications which can utilize the HA-5127/883's qualities include instrumentation amplifiers, pulse or RF amplifiers, audio preamplifiers, and signal conditioning circuits.

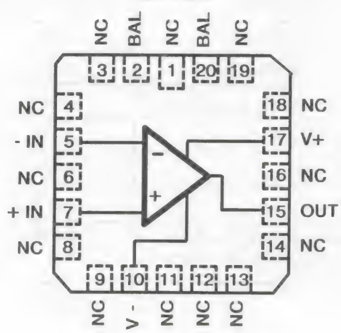
This device can easily be used as a design enhancement by directly replacing the 725, OP-25, OP-06, OP-07, OP-27 and OP-37. The HA-5127/883 is available in TO-99 Metal Can, Ceramic 8 Pin Mini-DIP, and 20 Pin LCC packages.

Pinouts

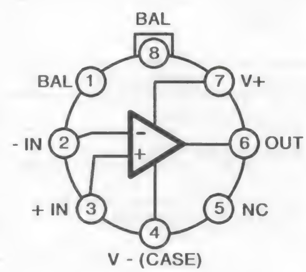
HA7-5127/883 (CERAMIC MINI-DIP)
TOP VIEW



HA4-5127/883 (CERAMIC LCC)
TOP VIEW



HA2-5127/883 (METAL CAN)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 44V
Differential Input Voltage (Note 6) 0.7V
Voltage at Either Input Terminal .... V+ to V-
Input Current 25mA
Differential Output Current .... Full Short Circuit Protection
Junction Temperature (T_J) .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... < 2000V
Lead Temperature (Soldering 10 sec) .... +275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	82°C/W	25°C/W
Ceramic LCC Package	84°C/W	25°C/W
Metal Can Package	98°C/W	30°C/W

Package Power Dissipation Limit at +75°C for $T_J \leq$ +175°C
Ceramic DIP Package 1.22W
Ceramic LCC Package 1.19W
Metal Can Package 1.02W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 12.2mW/°C
Ceramic LCC Package .... 11.9mW/°C
Metal Can Package .... 10.2mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±15V
$V_{INcm} \leq$ 1/2 (V+ - V-)
$R_L \geq 600\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, $R_{SOURCE} = 50\Omega$, $R_{LOAD} = 100k\Omega$, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	V_{CM} = 0V	1	+25°C	-100	100	µV
			2, 3	+125°C, -55°C	-300	300	µV
Input Bias Current	I_B	V_{CM} = 0V R_S = 10kΩ, 50Ω $\left(\frac{\lvert +I_B\rvert + \lvert -I_B\rvert}{2}\right)$	1	+25°C	-	80	nA
			2, 3	+125°C, -55°C	-	150	nA
Input Offset Current	I_{IO}	V_{CM} = 0V $+R_S$ = 10kΩ $-R_S$ = 10kΩ	1	+25°C	-75	75	nA
			2, 3	+125°C, -55°C	-135	135	nA
Common Mode Range	+CMR	V+ = 4.7V V- = -25.3V	1	+25°C	10.3	-	V
			2, 3	+125°C, -55°C	10.3	-	V
	-CMR	V+ = 25.3V V- = -4.7V	1	+25°C	-	-10.3	V
			2, 3	+125°C, -55°C	-	-10.3	V
Large Signal Voltage Gain	$+A_{VOL}$	V_{OUT} = 0V and +10V R_L = 2kΩ	4	+25°C	700	-	kV/V
			5, 6	+25°C, -55°C	300	-	kV/V
	$-A_{VOL}$	V_{OUT} = 0V and -10V R_L = 2kΩ	4	+25°C	700	-	kV/V
			5, 6	+125°C, -55°C	300	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔV_{CM} = +11V	1	+25°C	100	-	dB
		ΔV_{CM} = +10V	2, 3	+125°C, -55°C	100	-	dB
	-CMRR	ΔV_{CM} = -11V	1	+25°C	100	-	dB
		ΔV_{CM} = -10V	2, 3	+125°C, -55°C	100	-	dB

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 100kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Voltage Swing	$+V_{OUT1}$	R_L = 2kΩ	4	+25°C	11.5	-	V
			5, 6	+125°C, -55°C	11.5	-	V
	$-V_{OUT1}$	R_L = 2kΩ	4	+25°C	-	-11.5	V
			5, 6	+125°C, -55°C	-	-11.5	V
	$+V_{OUT2}$	R_L = 600Ω	4	+25°C	10	-	V
	$-V_{OUT2}$	R_L = 600Ω	4	+25°C	-	-10	V
Output Current	$+I_{OUT}$	V_{OUT} = -10V	4	+25°C	16.5	-	mA
	$-I_{OUT}$	V_{OUT} = +10V	4	+25°C	-	-16.5	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V	1	+25°C	-	4	mA
		I_{OUT} = 0mA	2, 3	+125°C, -55°C	-	4	mA
	$-I_{CC}$	V_{OUT} = 0V	1	+25°C	-4	-	mA
		I_{OUT} = 0mA	2, 3	+125°C, -55°C	-4	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = 14V	1	+25°C	86	-	dB
		ΔV_{SUP} = 13.5V	2, 3	+125°C, -55°C	86	-	dB
	-PSRR	ΔV_{SUP} = 14V	1	+25°C	86	-	dB
		ΔV_{SUP} = 13.5V	2, 3	+125°C, -55°C	86	-	dB
Offset Voltage Adjustment	$+V_{IO}Adj$	Note 5	1	+25°C	V_{IO} -1	-	mV
			2, 3	+125°C, -55°C	V_{IO} -1	-	mV
	$-V_{IO}Adj$	Note 5	1	+25°C	V_{IO} +1	-	mV
			2, 3	+125°C, -55°C	V_{IO} +1	-	mV

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 2kΩ, C_{LOAD} =50pF, A_{VCL} = +1V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Slew Rate	+SR	V_{OUT} = -3V to +3V	7	+25°C	7	-	V/μs
	-SR	V_{OUT} = +3V to -3V	7	+25°C	7	-	V/μs
Rise & Fall Time	T_R	V_{OUT} = 0 to +200mV 10% $\leq T_R \leq$ 90%	7	+25°C	-	150	ns
	T_F	V_{OUT} = 0 to -200mV 10% $\leq T_F \leq$ 90%	7	+25°C	-	150	ns
Overshoot	+OS	V_{OUT} = 0 to +200mV	7	+25°C	-	40	%
	-OS	V_{OUT} = 0 to -200mV	7	+25°C	-	40	%

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_V = +1V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	MAX	UNITS
Average Offset Voltage Drift	$V_{IO}TC$	V_{CM} = 0V	1	-55°C to +125°C	-	1.8	μV/°C
Differential Input Resistance	R_{IN}	V_{CM} = 0V	1	+25°C	0.8	-	MΩ
Low Frequency Peak-to-Peak Noise	E_{np-p}	0.1Hz to 10Hz	1	+25°C	-	0.25	μV_{p-p}
Input Noise Voltage Density	E_n	R_S = 20Ω, f_o = 10Hz	1, 4	+25°C	-	8.0	$nV/\sqrt{Hz}$
		R_S = 20Ω, f_o = 100Hz	1, 4	+25°C	-	5.6	$nV/\sqrt{Hz}$
		R_S = 20Ω, f_o = 1kHz	1, 4	+25°C	-	4.5	$nV/\sqrt{Hz}$
Input Noise Current Density	I_n	R_S = 2MΩ, f_o = 10Hz	1,4	+25°C	-	4.0	$pA/\sqrt{Hz}$
		R_S = 2MΩ, f_o = 100Hz	1, 4	+25°C	-	2.3	$pA/\sqrt{Hz}$
		R_S = 2MΩ, f_o = 1kHz	1, 4	+25°C	-	0.6	$pA/\sqrt{Hz}$
Unity Gain Bandwidth	UGBW	V_O = 100mV	1	+25°C	5	-	MHz
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	+25°C	111	-	kHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 2kΩ, C_L = 50pF	1	-55°C to +125°C	±1	-	V/V
Settling Time	T_S	To 0.1% for a 10V Step	1	+25°C	-	2	μs
Output Resistance	R_{OUT}	Open Loop	1	+25°C	-	100	Ω
Quiescent Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	120	mW

NOTES: 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).

3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)

4. Input Noise Voltage Density and Input Noise Current Density is sample tested on every lot.

5. Offset adjustment range is [V_{IO} (Measured) ± 1mV] minimum referred to output. This test is for functionality only to assure adjustment through 0V.

6. For differential input voltages greater than 0.7V, the input current must be limited to 25mA to protect the back-to-back input diodes.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

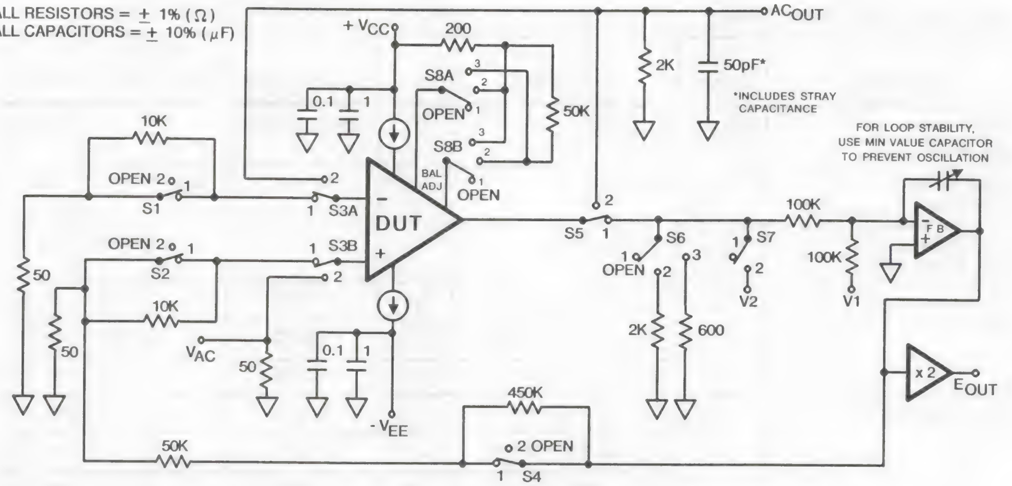
MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6, 7
Group A Test Requirements	1, 2, 3, 4, 5, 6, 7
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

The Subgroup assignments of the parameters in these tables were patterned after Mil-M-38510/135, with the exception of V_{IO}, which is Subgroups 1, 2, and 3.

Test Circuit (Applies to Tables 1 and 2)

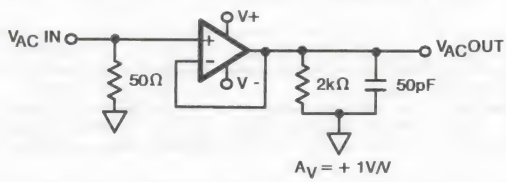
ALL RESISTORS = ± 1% (Ω)
ALL CAPACITORS = ± 10% (μF)



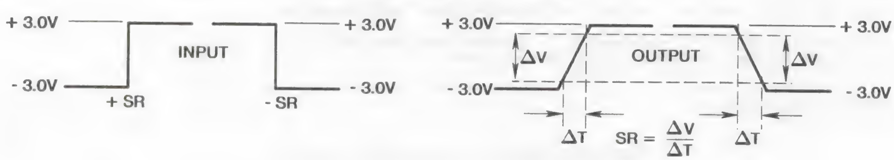
For Op-Amp Test Circuits and Conditions, Refer to the Harris Tech Brief "HA-5127 Op-Amp Test Methods".

Test Waveforms

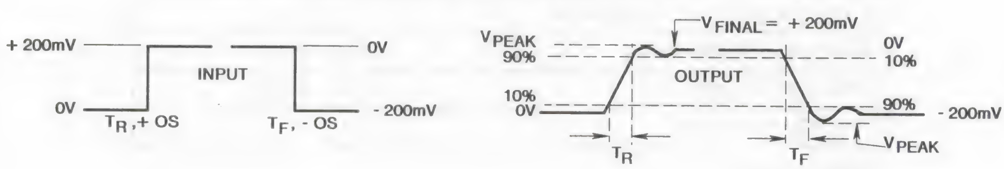
SIMPLIFIED TEST CIRCUIT (Applies to Table 2)



SLEW RATE WAVEFORM



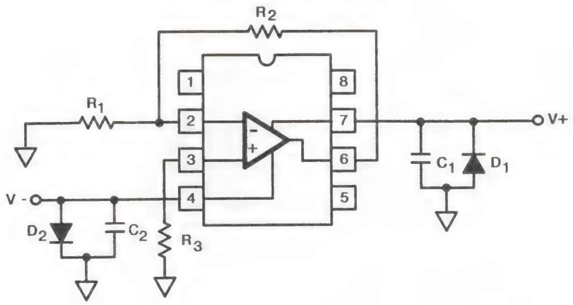
TRANSIENT RESPONSE WAVEFORM



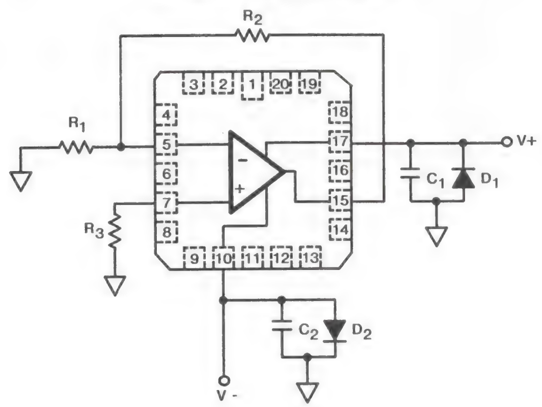
NOTE: Measured on Both positive and negative transitions.

Burn-In Circuits

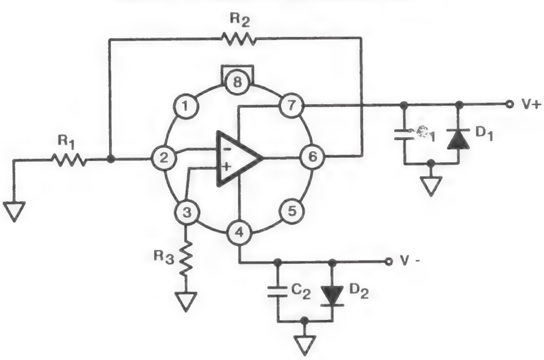
HA7-5127/883 CERAMIC DIP



HA4-5127/883 CERAMIC LCC



HA2-5127/883 (TO-99) METAL CAN



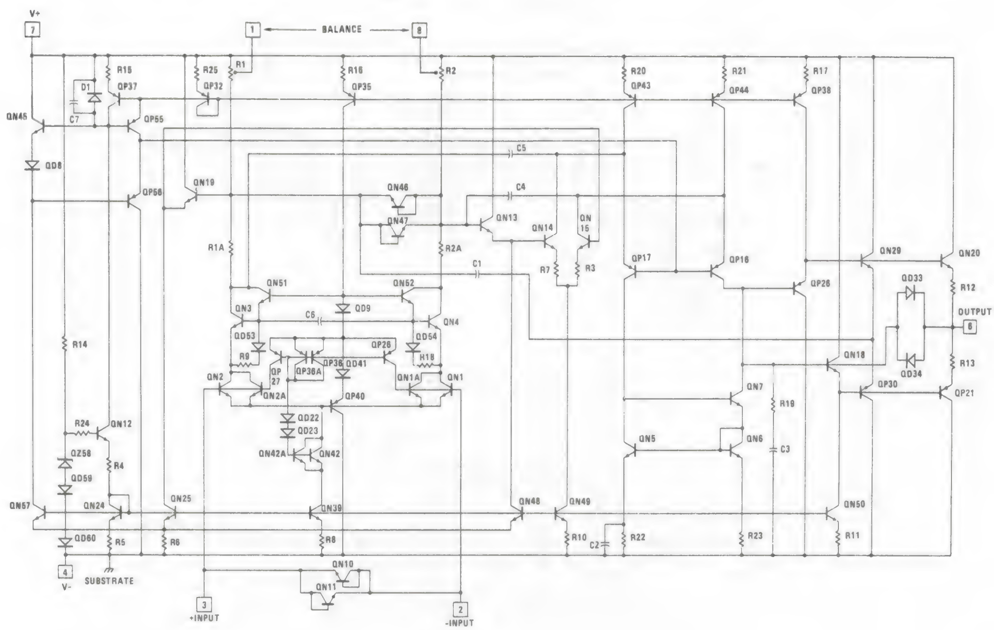
NOTES:

R_1 = R3 = 1kΩ ±5%, 1/4W (Min)
R_2 = 10kΩ ±5%, 1/4W (Min)
C_1 = C_2 = 0.01μF/ per Socket (Min) or 0.1μF/per Row (Min)
D_1 = D_2 = IN4002 or Equivalent/Board
$|(V+) - (V-)| = 30V$

3

OP AMPs & COMPARATORS

Schematic Diagram



Die Characteristics

DIE DIMENSIONS:
104.3 x 65 x 19 mils
(2650 x 1650 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$3.6 \times 10^5 A/cm^2$ @15mA
This device meets Glassivation Integrity Test requirement per Mil-Std-883 Method 2021 and Mil-M-38510 paragraph 3.5.5.4.

SUBSTRATE POTENTIAL (Powered Up): V-

GLASSIVATION:
Type: Silox
Thickness: 7kÅ ± 0.7kÅ

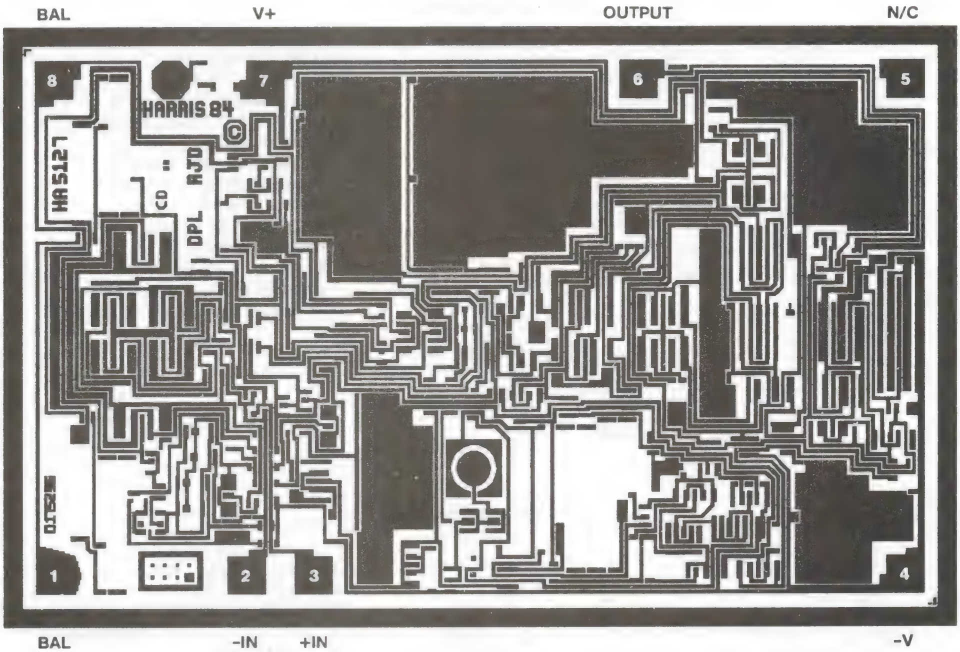
TRANSISTOR COUNT: 63

PROCESS: HFHB Bipolar Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)
Metal Can — 420°C (Max)

Metallization Mask Layout

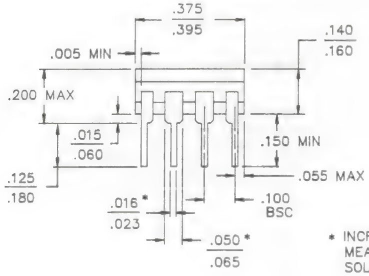
HA-5127/883

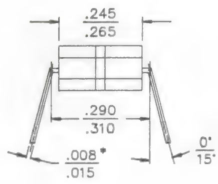


NOTE: Pin Numbers Correspond to 8 Pin Metal Can and Mini-DIP Package Only.

Packaging †

8 PIN CERAMIC DIP

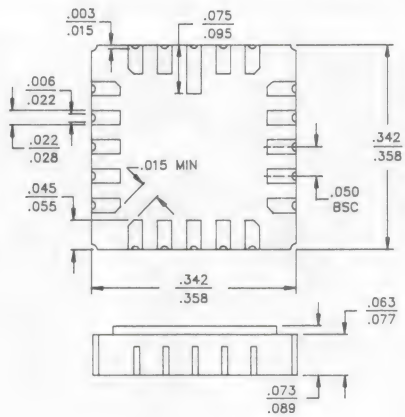




* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

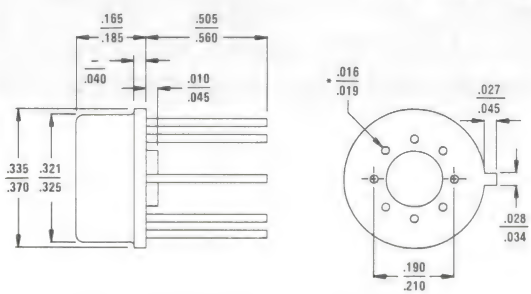
LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-4

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Ceramic, 90% Al_2O_3
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

8 PIN TO-99 METAL CAN



LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
Material: No Seal Material
Temperature: Room Temperature
Method: Resistance Weld
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic Bonded
COMPLIANT OUTLINE: 38510 A-1

*Dimension Maximum Limits Are Increased by 0.003 inches for Solder Dip Finish

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

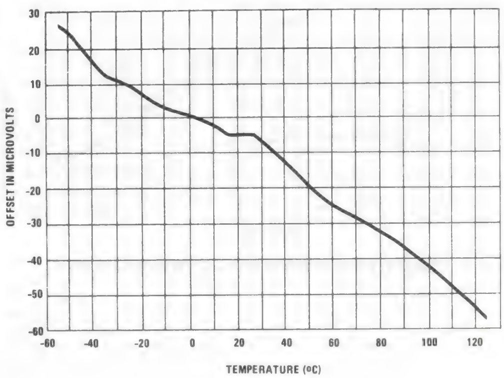
DESIGN INFORMATION

Ultra-Low Noise, Precision Operational Amplifier

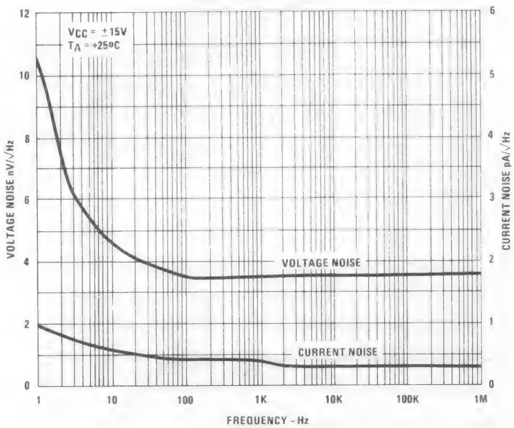
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

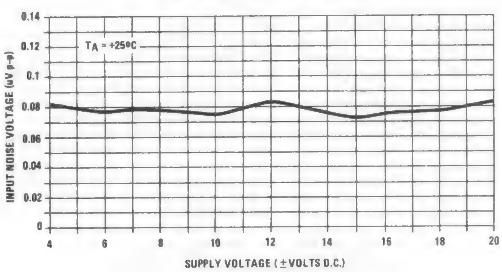
OFFSET VOLTAGE TYPICAL DRIFT vs. TEMPERATURE



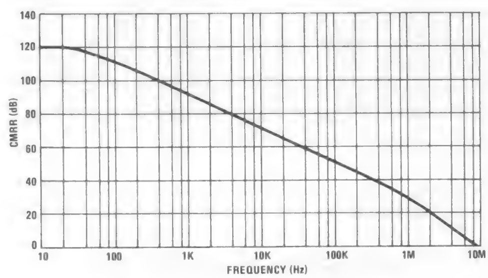
NOISE CHARACTERISTICS



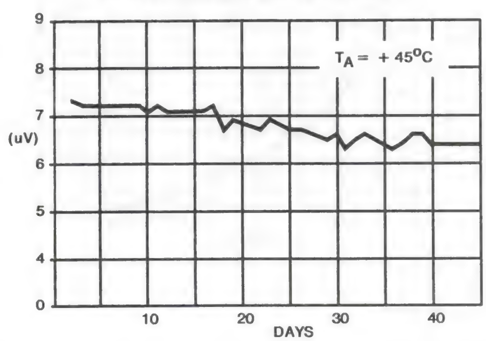
NOISE vs. SUPPLY VOLTAGE



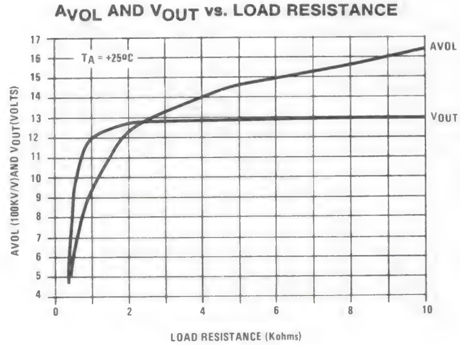
CMRR vs. FREQUENCY



OFFSET VOLTAGE DRIFT vs. TIME



A_{VOL} AND V_{OUT} vs. LOAD RESISTANCE



3

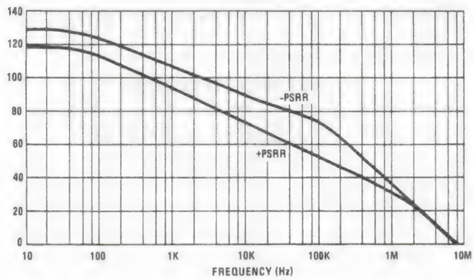
OP AMPs & COMPARATORS

DESIGN INFORMATION (Continued)

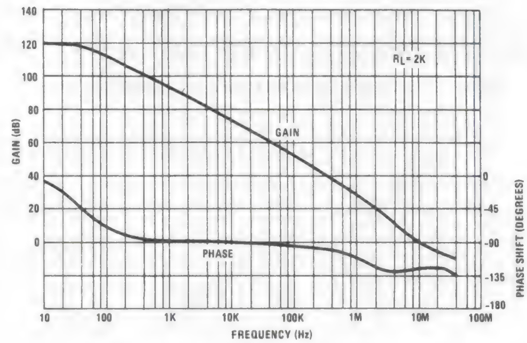
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

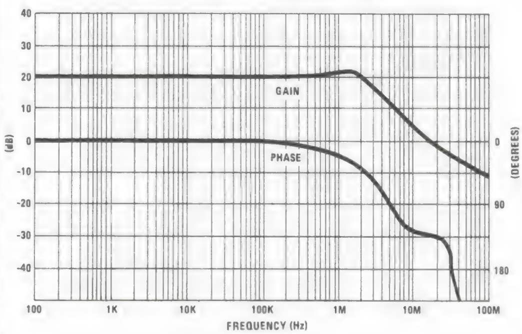
PSRR vs. FREQUENCY



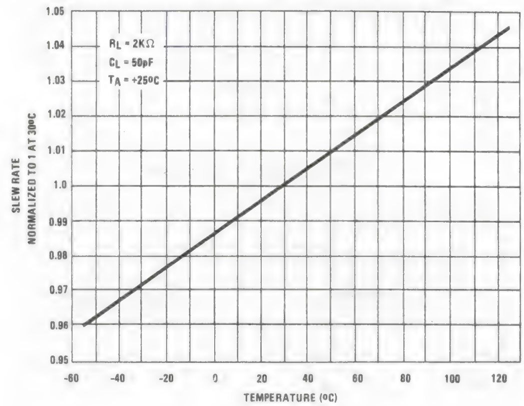
OPEN LOOP GAIN AND PHASE vs. FREQUENCY



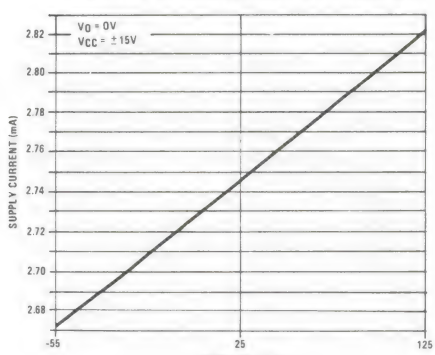
CLOSED LOOP GAIN AND PHASE vs. FREQUENCY



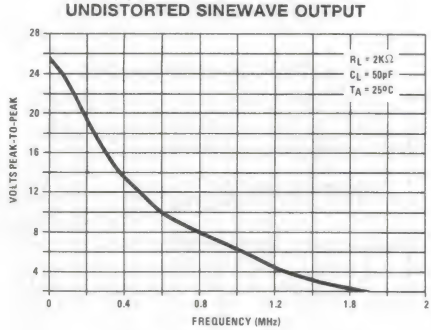
NORMALIZED SLEW RATE vs. TEMPERATURE



SUPPLY CURRENT vs. TEMPERATURE



V_{OUT} MAX vs. FREQUENCY UNDISTORTED SINEWAVE OUTPUT



DESIGN INFORMATION (Continued)

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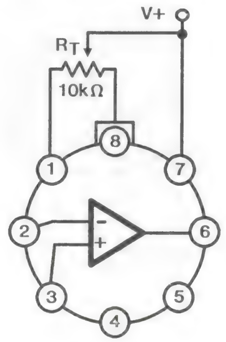
Typical Performance Information Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

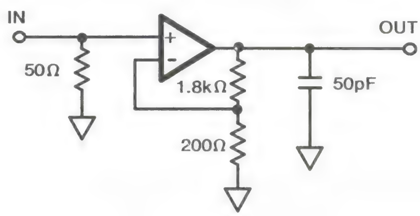
SUGGESTED OFFSET VOLTAGE ADJUSTMENT



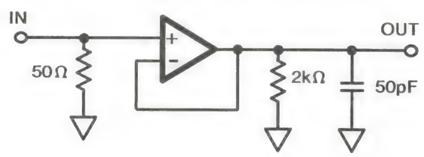
Tested Offset Adjustment Range is $|V_{OS} + mV|$ minimum referred to output. Typical Range is ±4mV with R_T = 10kΩ.

LARGE AND SMALL SIGNAL RESPONSE

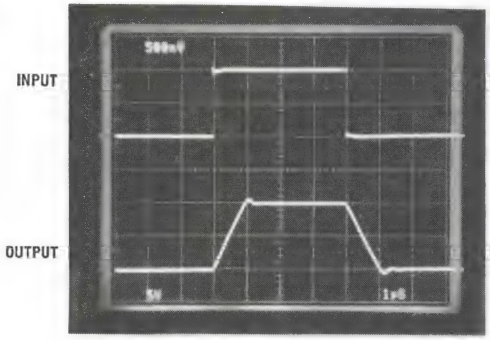
LARGE SIGNAL TEST CIRCUIT USED FOR PHOTO BELOW



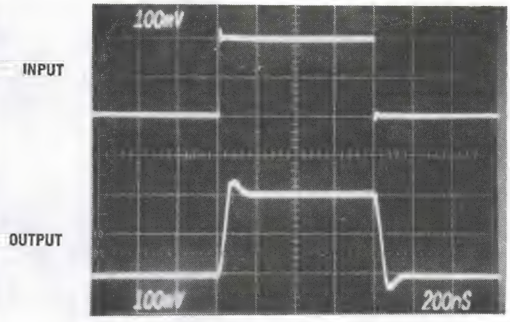
SMALL SIGNAL TEST CIRCUIT USED FOR PHOTO BELOW



MEASURED LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 0.5V/Div.)
(Volts: Output = 5V/Div.)
Horizontal Scale: (Time: 1μs/Div.)



MEASURED SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 100mV/Div)
(Volts: Output = 100mV/Div.)
Horizontal Scale: (Time: 200ns/Div.)



3 OP AMPs & COMPARATORS

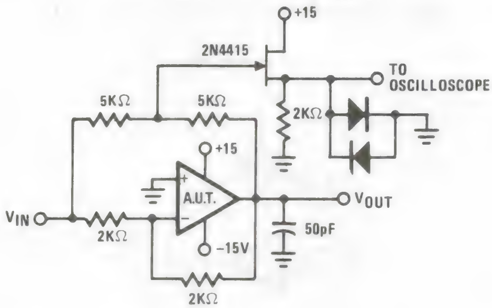
DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Information

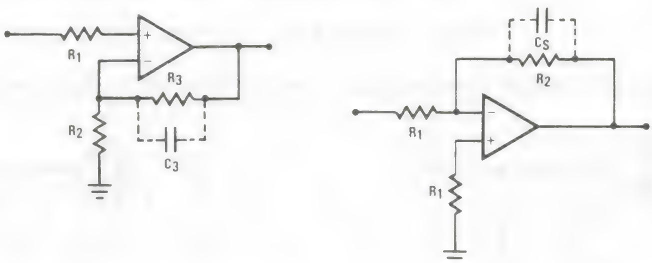
Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

SETTLING TIME TEST CIRCUIT



- $A_V = -1$
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional. HP5082-2810 recommended.

SUGGESTED STABILITY CIRCUITS



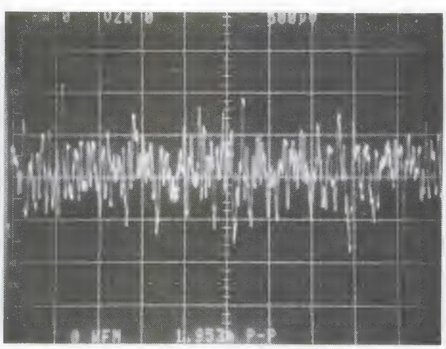
Low resistances are preferred for low noise applications as a 1kΩ resistor has $4nV/\sqrt{Hz}$ of thermal noise. Total resistances of greater than 10kΩ on either input can reduce stability. In most high resistance applications, a few picofarads of capacitance across the feedback resistor will improve stability.

0.1Hz TO 10Hz NOISE WITH A_{VCL}= 25,000V/V

Horizontal Scale = 1sec/Div.

Vertical Scale = 0.002μV/Div.

$0.08\mu V_{p-p}$ RTI



DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_L = 2kΩ, C_L = 50pF, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage	V_{CM} = 0V	+25°C	30	Table 1	μV
		Full	70	Table 1	μV
Offset Voltage Drift	Versus Temperature	Full	0.4	Table 3	μV/°C
	Versus Time	+45°C	0.71	1.5	μV/Month
Bias Current	V_{CM} = 0V	+25°C	±15	Table 1	nA
		Full	±35	Table 1	nA
Differential Input Resistance		+25°C	6	Table 3	MΩ
Input Noise Voltage	f_O = 10Hz	+25°C	4.4	Table 3	$nV/\sqrt{Hz}$
	f_O = 100Hz	+25°C	3.4	Table 3	$nV/\sqrt{Hz}$
	f_O = 1kHz	+25°C	3.2	Table 3	$nV/\sqrt{Hz}$
Input Noise Current	f_O = 10Hz	+25°C	1.7	Table 3	$pA/\sqrt{Hz}$
	f_O = 100Hz	+25°C	1.0	Table 3	$pA/\sqrt{Hz}$
	f_O = 1kHz	+25°C	0.4	Table 3	$pA/\sqrt{Hz}$
Voltage Gain	V_{OUT} = ±10V	+25°C	1.8	Table1	MV/V
		Full	1.2	Table 1	MV/V
CMRR	ΔV = ±10V	Full	126	Table 1	dB
PSRR	V_S = ±4 to ±18V	Full	110	Table 1	dB
Slew Rate	V_{OUT} = ±5V, $A_V \geq 1$	+25°C	10	Table 2	V/μs
Overshoot	V_{OUT} = ±200mV	+25°C	20	Table 2	%
Settling Time	10V to 0.1%	+25°C	1.5	Table 3	μs
	10V to 0.01%	+25°C	1.8	2.3	μs
Minimum Supply Voltage	Functional Operation Only. Other Parameters Will Vary.	+25°C	±4	±5	V

HARRIS

HA-5134/883

Precision Quad Operational Amplifier

January 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low Offset Voltage (+25°C) .... 200μV (Max)
  (Full Temp.) .... 350μV (Max)
- Low Offset Voltage Drift @ Temp. ...... 2μV/°C (Max)
- Offset Voltage Match (Full Temp.) ...... 350μV (Max)
- High Channel Separation (+25°C)...... 120dB (Min)
- Low Noise (f ≥ 100Hz) .... 10nV/$\sqrt{Hz}$ (Max)
- Wide Bandwidth .... 4MHz (Typ)
- High CMRR/PSRR (+25°C)............. 100dB (Min)
- High Voltage Gain (+25°C)............1.2MV/V (Min)
- Dielectric Isolation

Applications

- Instrumentation Amplifiers
- State-Variable Filters
- Precision Integrators
- Threshold Detectors
- Precision Data Acquisition Systems
- Low-Level Transducer Amplifiers

Description

The HA-5134/883 is a precision quad operational amplifier that is pin compatible with the OP-400, LT1014, OP11, RM4156, and LM148 as well as the HA-4741/883. Each amplifier features guaranteed maximum values for offset voltage of 350μV, offset voltage drift of 2μV/°C (max), and offset current of 75nA over the full military temperature range while CMRR/PSRR is guaranteed greater than 94dB and open loop gain is guaranteed above 750K V/V from -55°C to +125°C. Room temperature specifications exceed these values such as an offset voltage matching specifications between channels of 200μV (max) at +25°C.

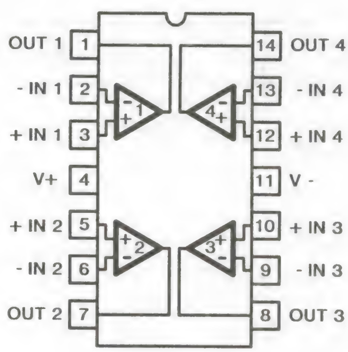
Precision performance of the HA-5134/883 is enhanced by a noise voltage density of 7nV/$\sqrt{Hz}$ at 1kHz (Typ), noise current density of 2pA/$\sqrt{Hz}$ at 1kHz and channel separation of 120dB (min). Each of the four unity gain stable amps on the quad are electrically isolated, having only supply lines in common and are fabricated using Dielectric Isolation to insure quality performance in the most demanding applications.

The HA-5134/883 is ideal for compact circuits such as instrumentation amplifiers, state-variable filters, and low-level transducer amplifiers. Other applications include precision data acquisition systems, precision integrators, and accurate threshold detectors in designs where board space is a limitation.

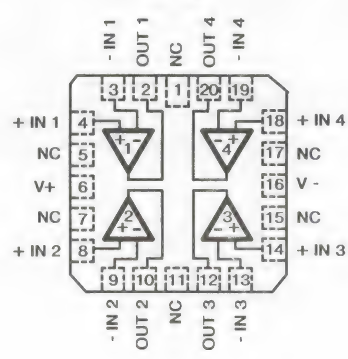
The HA-5134/883 has guaranteed operation from -55°C to +125°C and can be ordered in the 14 pin Ceramic DIP or 20 pad Ceramic LCC Package.

Pinouts

HA1-5134/883 (CERAMIC DIP)
TOP VIEW



HA4-5134/883 (CERAMIC LCC)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage 6V
Voltage at Either Input Terminal .... V+ to V-
Input Current 25mA
Output Current .... Full Short Circuit Protection
Output Current Duration ....Indefinite
(One Amplifier Shorted to Ground)
Junction Temperature................................ +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... <2000V
Lead Temperature (Soldering 10 sec)...................... 275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	75°C/W	16°C/W
Ceramic LCC Package	76°C/W	19°C/W

Package Power Dissipation Limit at +75°C for $T_J \leq$ +175°C
Ceramic DIP Package 1.33W
Ceramic LCC Package................................ 1.32W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 13.3mW/°C
Ceramic LCC Package........................... 13.2mW/°C

Recommended Operating Conditions

Operating Temperature Range ....-55°C to +125°C
Operating Supply Voltage .... ±15V
$V_{INcm} \leq$ 1/2 (V+ - V-)
$R_L \geq$ 2kΩ

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 100kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	V_{CM} = 0V	1	+25°C	-200	200	µV
			2, 3	+125°C, -55°C	-350	350	µV
Offset Voltage Match	ΔV_{IO}	$\lvert V_{IO}$ (Max) $- V_{IO}$ (Min)$\rvert$	1	+125°C	-	200	µV
			2, 3	+125°C, -55°C	-	350	µV
Input Bias Current	+IB	VCM = 0V $+R_S$ = 10kΩ $-R_S$ = 50Ω	1	+125°C	-50	50	nA
			2, 3	+125°C, -55°C	-75	75	nA
	$-I_B$	V_{CM} = 0V $+R_S$ = 50Ω $-R_S$ = 10kΩ	1	+25°C	-50	50	nA
			2, 3	+125°C, -55°C	-75	75	nA
Input Offset Current	I_{IO}	V_{CM} = 0V $+R_S$ = 10kΩ $-R_S$ = 10kΩ	1	+25°C	-50	50	nA
			2, 3	+125°C, -55°C	-75	75	nA
Common Mode Range	+CMR	V+ = 5V V- = -25V	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	-CMR	V+ = 25V V- = -5V	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
Large Signal Voltage Gain	$+A_{VOL}$	V_{OUT} = 0V and +10V R_L = 2kΩ	4	+25°C	1200	-	kV/V
			5, 6	+125°C, -55°C	750	-	kV/V
	$-A_{VOL}$	V_{OUT} = 0V and -10V R_L = 2kΩ	4	+25°C	1200	-	kV/V
			5, 6	+125°C, -55°C	750	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔV_{CM} = 10V +V = +5V -V = -25V V_{OUT} = -10V	1	+25°C	100	-	dB
			2, 3	+125°C, -55°C	94	-	dB
	-CMRR	ΔV_{CM} = 10V +V = +25V -V = -5V V_{OUT} = +10V	1	+25°C	100	-	dB
			2, 3	+125°C, -55°C	94	-	dB

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 100kΩ, V_{OUT} = 0V, Unless Otherwise Specified

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Voltage Swing	$+V_{OUT1}$	$R_L = 2k\Omega$	4	+25°C	12	-	V
			5, 6	+125°C, -55°C	12	-	V
	$-V_{OUT1}$	$R_L = 2k\Omega$	4	+25°C	-	-12	V
			5, 6	+125°C, -55°C	-	-12	V
Output Current	$+I_{OUT}$	$V_{OUT} = -10V$	4	+25°C	16	-	mA
			5, 6	+125°C, -55°C	10	-	mA
	$-I_{OUT}$	$V_{OUT} = +10V$	4	+25°C	-	-16	mA
			5, 6	+125°C, -55°C	-	-10	mA
Quiescent Power Supply Current	$+I_{CC}$	$V_{OUT} = 0V$ $I_{OUT} = 0mA$	1	+25°C	-	6.8	mA
			2, 3	+125°C, -55°C	-	8	mA
	$+I_{CC}$	$V_{OUT} = 0V$ $I_{OUT} = 0mA$	1	+25°C	-	6.8	mA
			2, 3	+125°C, -55°C	-	8	mA
Power Supply Rejection Ratio	+PSRR	$\Delta V_{SUP} = 10V$ +V = +20V, -V = -15V +V = +10V, -V = -15V	1	+25°C	100	-	dB
			2, 3	+125°C, -55°C	94	-	dB
	-PSRR	$\Delta V_{SUP} = -10V$ +V = +15V, -V = -20V +V = +15V, -V = -10V	1	+25°C	100	-	dB
			2, 3	+125°C, -55°C	94	-	dB

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_{VCL} = +1V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Slew Rate	+SR	V_{OUT} = -3V to +3V	7	+25°C	.75	-	V/µs
	-SR	V_{OUT} = +3V to -3V	7	+25°C	.75	-	V/µs
Rise & Fall Time	T_R	V_{OUT} = 0 to +200mV $10\% \leq T_R \leq 90\%$	7	+25°C	-	400	ns
	T_F	V_{OUT} = 0 to -200mV $10\% \leq T_F \leq 90\%$	7	+25°C	-	400	ns
Overshoot	+OS	V_{OUT} = 0 to +200mV	7	+25°C	-	40	%
	-OS	V_{OUT} = 0 to -200mV	7	+25°C	-	40	%

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Average Offset Voltage Drift	$V_{IO}TC$	V_{CM} = 0V	1	-55°C to +125°C	-	2	μV/°C
Differential Input Resistance	R_{IN}	V_{CM} = 0V	1	+25°C	20	-	MΩ
Low Frequency Peak-to-Peak Noise	E_{np-p}	0.1Hz to 10Hz	1	+25°C	-	0.25	$μV_{p-p}$
Input Noise Voltage Density	E_n	R_S = 20Ω, f_o = 1kHz	1, 5	+25°C	-	10	$nV/\sqrt{Hz}$
Input Noise Current Density	I_n	R_S = 2MΩ, f_o = 1kHz	1, 5	+25°C	-	2	$pA/\sqrt{Hz}$
Gain Bandwidth Product	GBWP	V_O = 200mV, $f_o \geq$ 100kHz	1	+25°C	3	-	MHz
Unity Gain Bandwidth	UGBW	V_O = 200mV	1	+25°C	3	-	MHz
Slew Rate	±SR	V_{OUT} = -3V to +3V And V_{OUT} = +3V to -3V	1	+25°C to +125°C	0.75	-	V/μs
			1	-55°C	0.6	-	V/μs
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	+25°C	12	-	kHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 2kΩ, C_L = 50pF	1	-55°C to +125°C	+1	-	V/V
Rise & Fall Time	T_R	V_{OUT} = 0V to +200mV	1, 4	-55°C to +125°C	-	400	ns
	T_F	V_{OUT} = 0V to -200mV	1, 4	-55°C to +125°C	-	400	ns
Overshoot	+OS	V_{OUT} = 0V to +200mV	1	-55°C to +125°C	-	40	%
	-OS	V_{OUT} = 0V to -200mV	1	-55°C to +125°C	-	40	%
Output Resistance	R_{OUT}	Open Loop	1	+25°C	-	86	Ω
Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	240	mW
Channel Separation (A.C.)	CS (A.C)	V_{IN} = $1V_{p-p}$ f_o = 100Hz	1	+25°C	120	-	dB
		V_{IN} = $1V_{p-p}$ f_o = 10kHz	1	+25°C	120	-	dB
Channel Separation (D.C.)	CS (D.C.)	V_O = ±10V ($20V_{p-p}$) Delta $V_{IO} \leq$ 20μV	1	+25°C	120	-	dB

NOTES:
1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).
3. Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)
4. Measured between 10% and 90% points.
5. Input Noise Voltage Density and Input Noise Current Density is sample tested on every lot.
6. Offset adjustment range is [$V_{IO\ (Measured)}$ ± 1mV] minimum referred to output. This test is for functionality only to assure adjustment through 0V.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

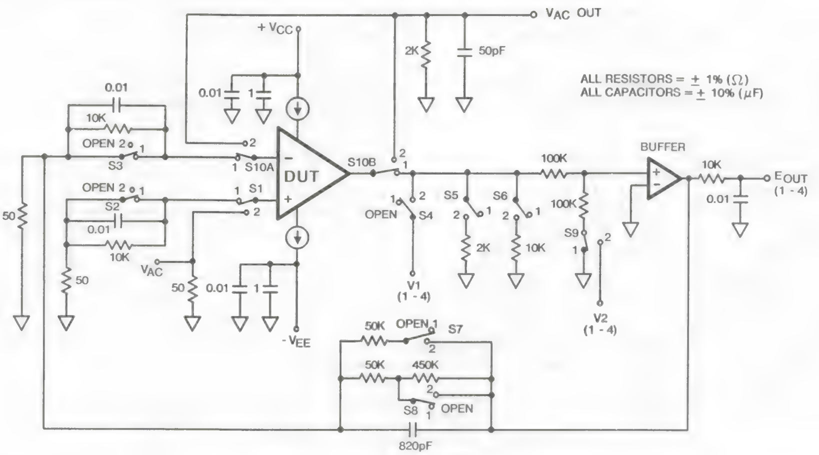
MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6, 7
Group A Test Requirements	1, 2, 3, 4, 5, 6, 7
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

3

OP AMPs & COMPARATORS

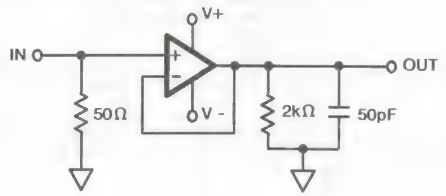
Test Circuit (Applies to Tables 1, 2 and 3)



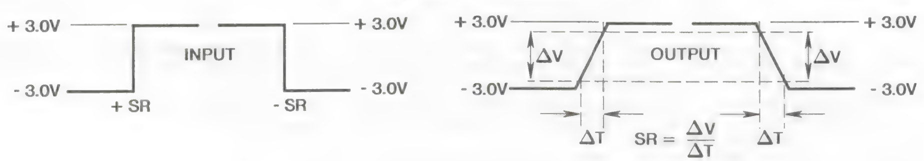
For Op-Amp Test Circuits and Conditions, Refer to the Harris Tech Brief "HA-5134/883 Op-Amp Test Methods".
One of Four Circuits for Quad D.U.T.

Test Waveforms

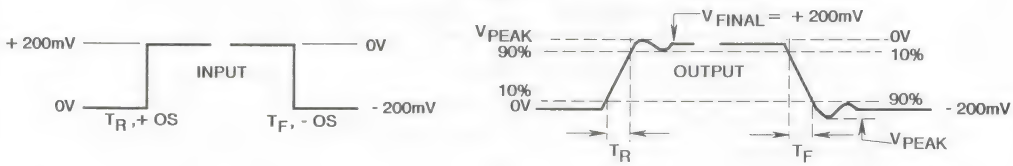
SIMPLIFIED TEST CIRCUIT (Applies to Tables 2 and 3)



SLEW RATE WAVEFORM



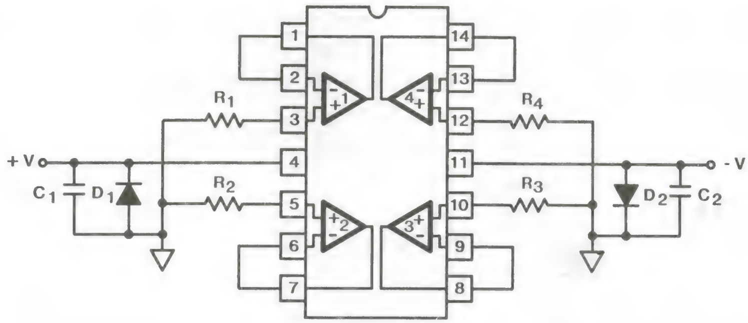
TRANSIENT RESPONSE WAVEFORM



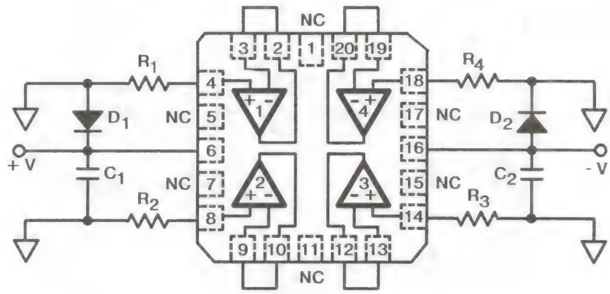
NOTE: Measured on Both positive and negative transitions.

Burn-In Circuits

HA1-5134/883 CERAMIC DIP



HA4-5134/883 CERAMIC LCC



NOTES:

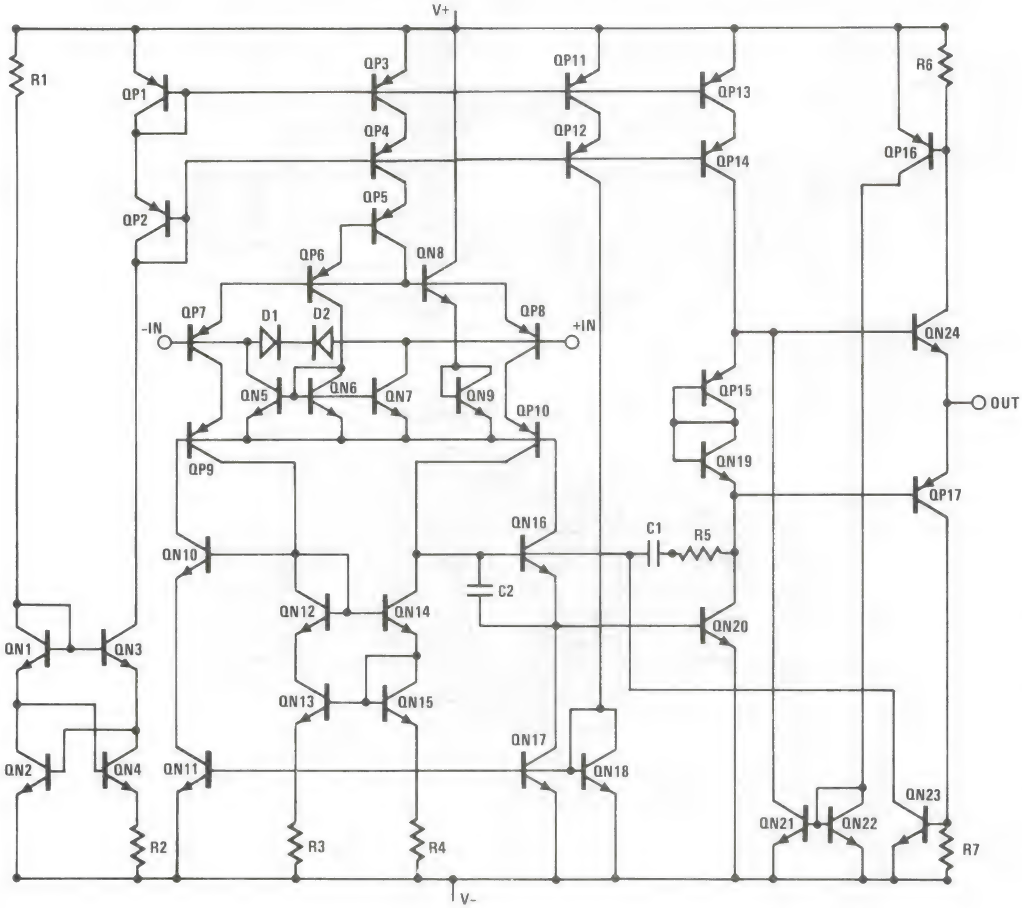
$R_1 = R_2 = R_3 = R_4 = 1M\Omega \pm 5\%$, 1/4W (Min)

$C_1 = C_2 = 0.01\mu F$/ per Socket (Min) or $0.1\mu F$/per Row (Min)

$D_1 = D_2$ = IN4002 or Equivalent/Board

$|(V+) - (V-)| = 30V$

Schematic Diagram (1/4 of HA-5134/883)



Die Characteristics

DIE DIMENSIONS:
89.4 x 113 x 19 mils
(2270 x 2870 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$2.65 \times 10^5 A/cm^2$ @ 33.4mA
This device meets Glassivation Integrity Test requirement per Mil-Std-883 Method 2021 and Mil-M-38510 paragraph 3.5.5.4.

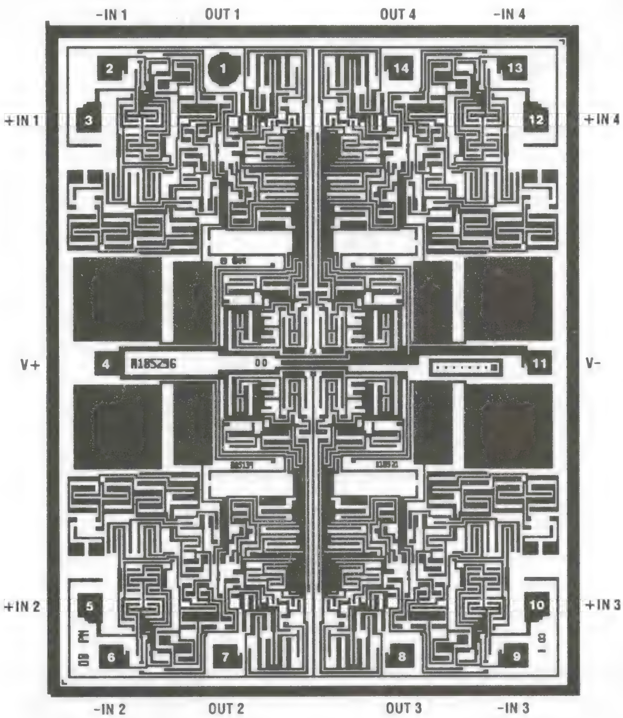
SUBSTRATE POTENTIAL (Powered Up):
Unbiased

GLASSIVATION:
Type: Silox
Thickness: 14kÅ ± 1kÅ

TRANSISTOR COUNT: 160
PROCESS: HFHB Bipolar Dielectric Isolation
DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

Metallization Mask Layout

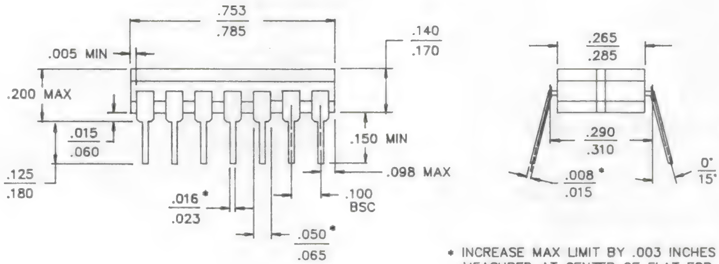
HA-5134/883



NOTE: Pin Numbers Correspond to DIP Package Only.

Packaging†

14 PIN CERAMIC DIP

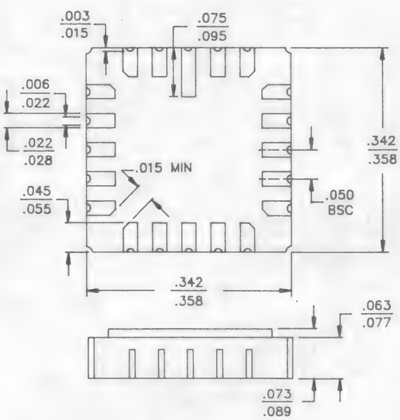


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-1

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

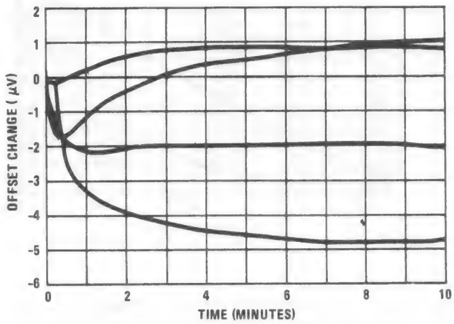
DESIGN INFORMATION

Precision Quad Operational Amplifier

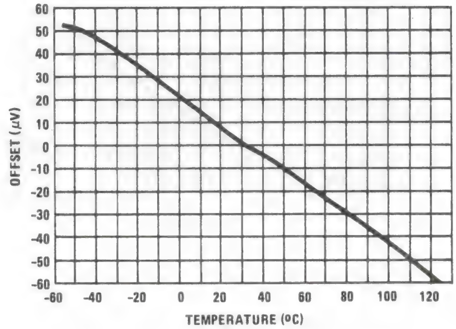
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V\pm = \pm 15V$

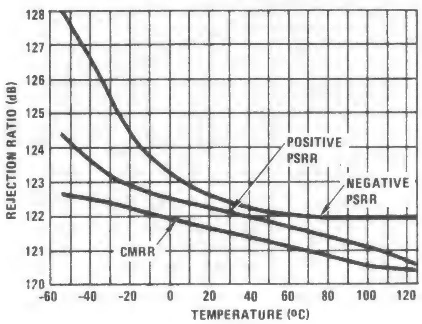
V_{IO} WARMUP DRIFT
$T_A = +25^oC$, $V_{CC} = \pm 15V$



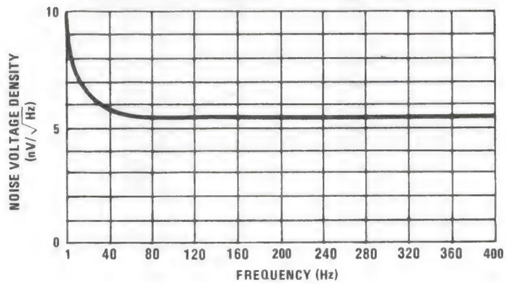
INPUT OFFSET VOLTAGE vs. TEMPERATURE



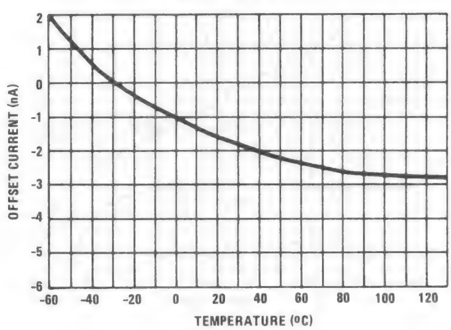
REJECTION RATIOS vs. TEMPERATURE
$V_{CC} = \pm 5V$ to $\pm 20V$, $V_{CM} = \pm 10V$



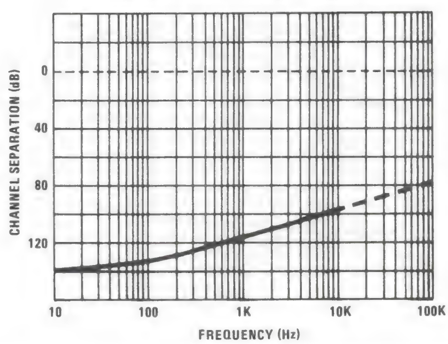
NOISE VOLTAGE DENSITY vs. FREQUENCY



OFFSET CURRENT vs. TEMPERATURE
$A_{CI} = 1$, $V_{CC} = \pm 15V$



CHANNEL SEPARATION vs. FREQUENCY



DESIGN INFORMATION (Continued)

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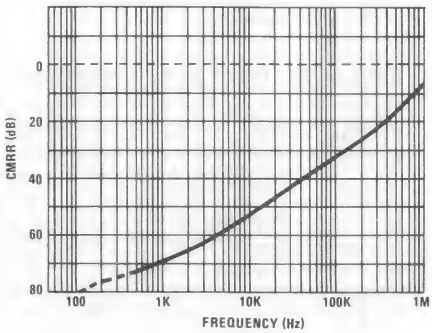
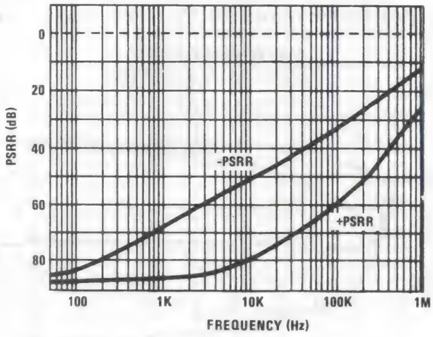
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V\pm = \pm 15V$

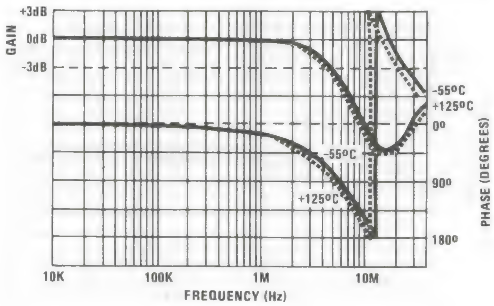
CMRR vs. FREQUENCY



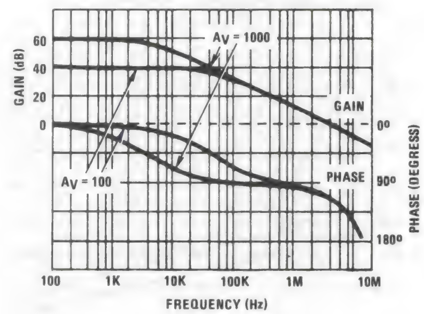
PSRR vs. FREQUENCY



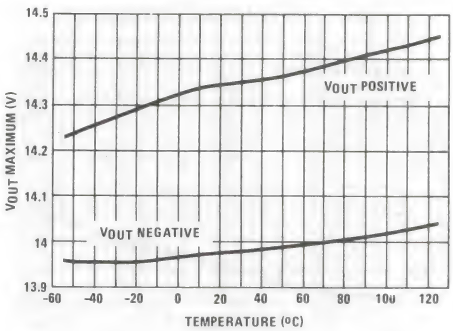
CLOSED LOOP FREQUENCY RESPONSE vs. TEMPERATURE



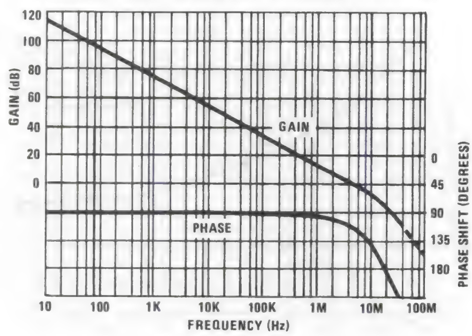
CLOSED LOOP GAIN/PHASE vs. FREQUENCY
$T_A = +25^oC$, $V_{CC} = +15V$



MAXIMUM OUTPUT VOLTAGE vs. TEMPERATURE
$R_{LOAD} = 2K$, $A_V = 1000$, $V_{IN} = \pm 2V$



OPEN LOOP GAIN AND PHASE vs. FREQUENCY



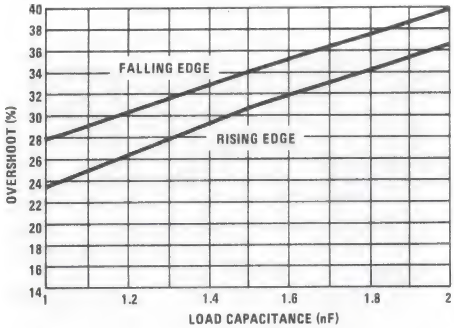
DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

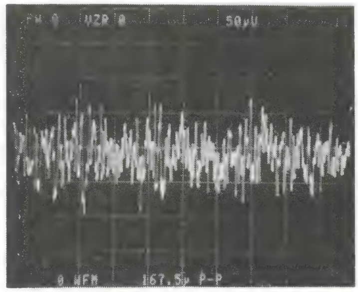
OVERSHOOT vs. C_{LOAD}

$V_{CC} = \pm15V$, $T_A = +25^oC$, $A_V = +1$, $V_{OUT} = 200mV$



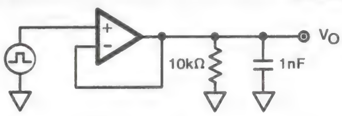
PEAK-TO-PEAK NOISE 0.1Hz to 10Hz

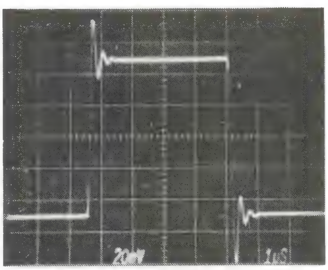
$T_A = +25^oC$, $V_{CC} = \pm15V$, $A_V = 1000$



$e_{np-p} = 0.167\mu V_{p-p}$, $0.05\mu V$/Div., 1s/Div.

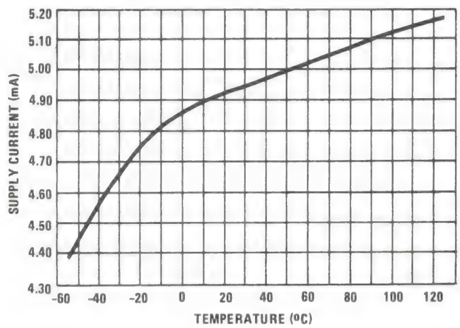
SMALL SIGNAL TRANSIENT RESPONSE C_{LOAD} = 1nF





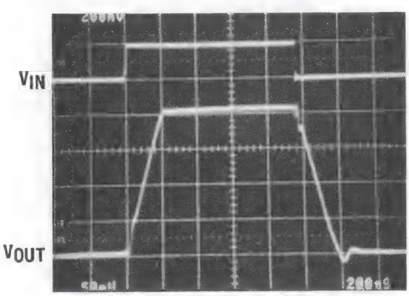
$T_A = +25^oC$, $V_{CC} = \pm15V$,
$A_V = +1$, $R_L = 10k\Omega$, 20mV/Div., 1µs/Div.

SUPPLY CURRENT vs. TEMPERATURE



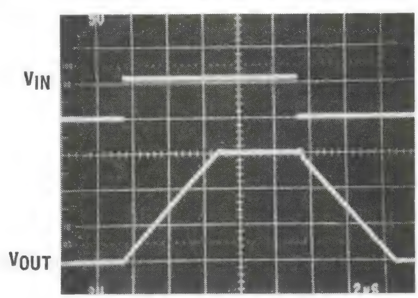
MEASURED SMALL SIGNAL RESPONSE ($A_V = +1$)

$T_A = +25^oC$, $V_{CC} = \pm15V$, $A_V = +1$, $R_L = 2k\Omega$, $C_L = 50pF$
In Scale = 200mV/Div., Out Scale = 50mV/Div.
Time Scale = 200ns/Div.



MEASURED LARGE SIGNAL RESPONSE (±3V)

$T_A = +25^oC$, $V_{CC} = \pm15V$, $A_V = +1$, $R_L = 2k\Omega$, $C_L = 50pF$
In Scale = 5V/Div., Out Scale = 2V/Div., Time Scale = 2µs/Div.

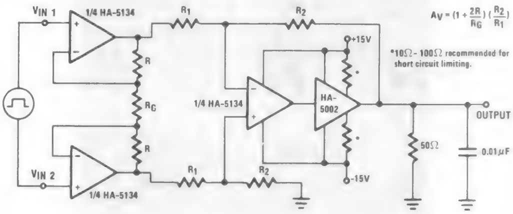


DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

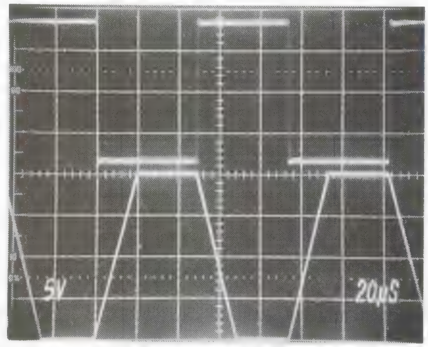
Applications Information

APPLICATION CIRCUIT #1: INSTRUMENTATION AMPLIFIER WITH POWER OUTPUT

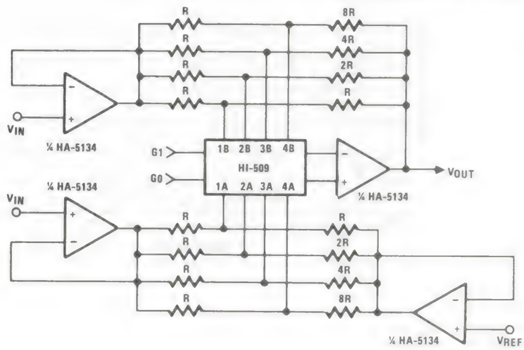


NOTE: When driving heavy loads the HA-5002 may contribute to thermal errors. Proper thermal shielding is recommended.

TRANSIENT RESPONSE OF APPLICATION CIRCUIT #1
$V_{OUT} = \pm 10V$, $R_{LOAD} = 50\Omega$
$C_{LOAD} = 0.01\mu F$, $A_V = 3$, $V_{CC} = \pm 15V$
Top: Input, 2V/Div., 20µs/Div.
Bottom: Output, 5V/Div., 20µs/Div.



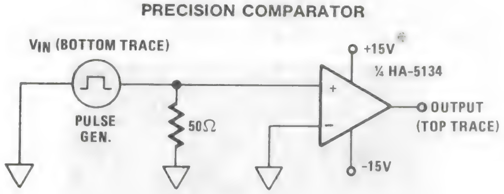
APPLICATION CIRCUIT #2: PROGRAMMABLE GAIN AMPLIFIER



G_1	G_0	A_V
0	0	-1
0	1	-2
1	0	-4
1	1	-8

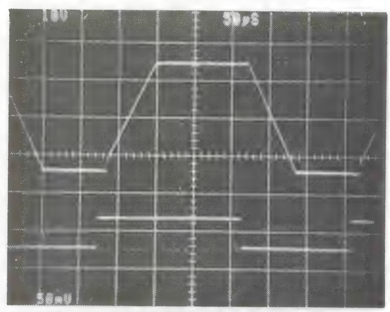
High A_{VOL} of HA-5134 reduces gain error.
Gain Error ≃ 0.004% @ $A_V = 8$

APPLICATION CIRCUIT #3: PRECISION COMPARATOR



NOTE: If differential input voltages greater than 6V are present, input current must be limited to less than 25mA.

COMPARATOR RESPONSE WAVEFORMS
Horizontal: 50µs/Div.
$V_{IN} = \pm 25mV$, $V_{OUT} = \pm 14V$



DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_L = 2kΩ, C_L = 50pF, A_V = +1V/V, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage	V_{CM} = 0V	+25°C	50	Table 1	µV
		Full	75	Table 1	µV
Average Offset Voltage Drift	Versus Temperature	Full	0.3	Table 3	µV/°C
Bias Current	V_{CM} = 0V	+25°C	±10	Table 1	nA
		Full	±20	Table 1	nA
Offset Current	V_{CM} = 0V	+25°C	10	Table 1	nA
		Full	15	Table 1	nA
Average Offset Current Drift	Versus Temperature	Full	50	100	pA/°C
Differential Input Resistance		+25°C	30	Table 3	MΩ
Input Noise Voltage	0.1Hz to 10Hz	+25°C	0.2	Table 3	µVp-p
Input Noise Voltage Density	f_O = 10Hz	+25°C	10	-	$nV/\sqrt{Hz}$
	f_O = 100Hz	+25°C	7.5	-	$nV/\sqrt{Hz}$
	f_O = 1kHz	+25°C	7	Table 3	$nV/\sqrt{Hz}$
Input Noise Current Density	f_O = 10Hz	+25°C	3	-	$pA/\sqrt{Hz}$
	f_O = 100Hz	+25°C	1.5	-	$pA/\sqrt{Hz}$
	f_O = 1kHz	+25°C	1	Table 3	$pA/\sqrt{Hz}$
Open Loop Voltage Gain	V_{OUT} = ±10V	+25°C	5	Table 1	MV/V
Unity Gain Bandwidth	Small Signal ($V_{OUT} \leq$ ±100mV)	+25°C	5	Table 3	MHz
Output Voltage Swing		Full	±13.5	Table 1	V
Output Current		+25°C	20	Table 1	mA
Channel Separation	V_{OUT} = ±10V	+25°C	136	Table 3	dB
Rise/Fall Time	V_{OUT} = +200mV, -200mV	+25°C	200	Table 2	ns
Overshoot	V_{OUT} = +200mV, -200mV	+25°C	10	Table 2	%
Slew Rate	Large Signal	+25°C	1	Table 2	V/µs
Settling Time	10V Step to 0.01%	+25°C	13	20	µs
Supply Current	Unload Output	+25°C	5.2	Table 1	mA
PSRR, CMRR		+25°C	125	Table 1	dB

General Considerations

1. **POWER SUPPLY DECOUPLING:** Although not absolutely necessary, it is recommended that all power supply lines be decoupled with 0.01µF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.
2. **CONSIDERATIONS FOR PROTOTYPING:** The following list of recommendations are suggested for prototyping.
   - Resolving low level signals requires minimizing leakage currents caused by external circuitry. Use of quality insulating materials, thorough cleaning of insulating surfaces and implementation of moisture barriers when required is suggested.
   - Error voltages generated by thermocouples formed between dissimilar metals in the presence of temperature gradients should be minimized. Isolation of low level circuitry from heat generating components is recommended.
   - Shielded cable input leads, guard rings and shield drivers are recommended for the most critical applications.

HA-5135/883

January 1989

Precision Operational Amplifier

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low Offset Drift .... 0.4μV/°C (Max)
- Low Offset Voltage .... 75μV (Max)
- High Gain ....120dB(1MV/V) (Min)
- High CMRR............................ 106dB (Min)
- High PSRR ....94dB (Min)
- Low Supply Current .... 1.7mA (Max)
- Low Noise Voltage Density @1kHz .. $9nV/\sqrt{Hz}$ (Max)
- Low Noise Current Density @1kHz .. $0.4pA/\sqrt{Hz}$ (Max)

Applications

- High Gain Instrumentation
- Precision Data Acquisition
- Precision Integrators
- Biomedical Amplifiers
- Precision Threshold Detectors

Description

The HA-5135/883 is a precision operational amplifier manufactured using a combination of key technological advancements to provide outstanding input characteristics.

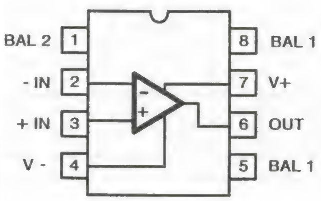
A high Beta input stage is combined with laser trimming, dielectric isolation, and matching techniques to produce 75μV (Max) input offset voltage and 0.4μV/°C (Max) input offset voltage average drift. Other features enhanced by this process include $9nV/\sqrt{Hz}$ (Typ). Input Noise Voltage, 4nA Input Bias Current (Max) and 120dB Open Loop Gain (Min).

These features coupled with 106dB CMRR and 94dB PSRR make HA-5135/883 an ideal device for precision D.C. instrumentation amplifiers. Excellent input characteristics in conjunction with 0.6MHz (Min) bandwidth and 0.5V/μs (Min) slew rate, makes this amplifier extremely useful for precision integrator and biomedical amplifier designs. These amplifiers are also well suited for precision data acquisition and for accurate threshold detector applications.

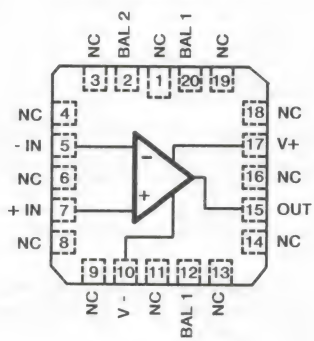
HA-5135/883 is packaged in an 8 pin (TO-99) Metal Can, an 8 lead Ceramic Mini-DIP, and a 20 pin Ceramic LCC package and is compatible with many existing op amp configurations. All packages are specified for -55°C to +125°C operation.

Pinouts

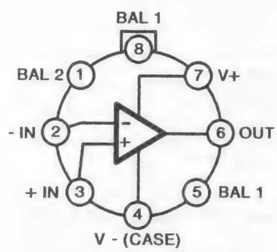
HA7-5135/883 (CERAMIC DIP)
TOP VIEW



HA4-5135/883 (CERAMIC LCC)
TOP VIEW



HA2-5135/883 (METAL CAN)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage (Note 6) 15V
Voltage at Either Input Terminal .... V+ to V-
Input Current 25mA
Output Current .... Full Short Circuit Protection
Junction Temperature (T_J) .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... < 2000V
Lead Temperature (Soldering 10 sec) .... +275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	82°C/W	25°C/W
Ceramic LCC Package	74°C/W	22°C/W
Metal Can Package	96°C/W	29°C/W

Package Power Dissipation Limit at +75°C for $T_J \leq$ +175°C
Ceramic DIP Package 1.22mW
Ceramic LCC Package 1.36W
Metal Can Package 1.04W

Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 12.2mW/°C
Ceramic LCC Package .... 13.6mW/°C
Metal Can Package .... 10.4mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±15V
$V_{INcm} \leq 1/2$ (V+ - V-)
$R_L \geq 600\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, $R_{SOURCE} = 50\Omega$, $R_{LOAD} = 100k\Omega$, $V_{OUT} = 0V$, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	$V_{CM} = 0V$	1	+25°C	-75	75	µV
			2, 3	+125°C, -55°C	-130	130	µV
Input Bias Current	I_B	$V_{CM} = 0V$ $+R_S = 10k\Omega, 50\Omega$ $\left(\frac{\lvert +I_B \rvert + \lvert -I_B \rvert}{2}\right)$	1	+25°C	-4	4	nA
			2, 3	+125°C, -55°C	-6	6	nA
Input Offset Current	I_{IO}	$V_{CM} = 0V$ $+R_S = 10k\Omega$ $-R_S = 10k\Omega$	1	+25°C	-4	4	nA
			2, 3	+125°C, -55°C	-5.5	5.5	nA
Common Mode Range	+CMR	V+ = 3V V- = -27V	1	+25°C	12	-	V
			2, 3	+125°C, -55°C	12	-	V
	-CMR	V+ = 27V V- = -3V	1	+25°C	-	-12	V
			2, 3	+125°C, -55°C	-	-12	V
Large Signal Voltage Gain	$+A_{VOL}$	V_{OUT} = 0V and +10V $R_L = 2k\Omega$	4	+25°C	120	-	dB
			5, 6	+25°C, -55°C	120	-	dB
	$-A_{VOL}$	V_{OUT} = 0V and -10V $R_L = 2k\Omega$	4	+25°C	120	-	dB
			5, 6	+125°C, -55°C	120	-	dB
Common Mode Rejection Ratio	+CMRR	ΔV_{CM} = +10V +V = +5V -V = -25V ΔV_{CM} = -10V	1	+25°C	106	-	dB
			2, 3	+125°C, -55°C	106	-	dB
	-CMRR	ΔV_{CM} = -10V +V = +25V -V = -5V ΔV_{CM} = +10V	1	+25°C	106	-	dB
			2, 3	+125°C, -55°C	106	-	dB

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 100kΩ, V_{OUT} = 0V, Unless Otherwise Specified

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Output Voltage Swing	$+V_{OUT1}$	R_L = 600Ω	4	+25°C	10	-	V
			5, 6	+125°C, -55°C	10	-	V
	$-V_{OUT1}$	R_L = 600Ω	4	+25°C	-	-10	V
			5, 6	+125°C, -55°C	-	-10	V
Output Current	$+I_{OUT}$	V_{OUT} = -10V	4	+25°C	15	-	mA
	$-I_{OUT}$	V_{OUT} = +10V	4	+25°C	-	-15	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-	1.7	mA
			2, 3	+125°C, -55°C	-	1.7	mA
	$-I_{CC}$	I_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-1.7	-	mA
			2, 3	+125°C, -55°C	-1.7	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = 10V +V = +5V, -V = -15V +V = +15V, -V = -15V	1	+25°C	94	-	dB
			2, 3	+125°C, -55°C	94	-	dB
	-PSRR	ΔV_{SUP} = 10V +V = +15V, -V = -5V +V = +15V, -V = -15V	1	+25°C	94	-	dB
			2, 3	+125°C, -55°C	94	-	dB
Offset Voltage Adjustment	$+V_{IO}Adj$	Note 5	1	+25°C	V_{IO} - 1	-	mV
			2, 3	+125°C, -55°C	V_{IO} - 1	-	mV
	$-V_{IO}Adj$	Note 5	1	+25°C	V_{IO} +1	-	mV
			2, 3	+125°C, -55°C	V_{IO} + 1	-	mV

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_{VCL} = +1V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Slew Rate	+SR	V_{OUT} = -3V to +3V V_{IN} S.R. $\leq$ 25V/μs	7	+25°C	0.5	-	V/μs
	-SR	V_{OUT} = +3V to -3V V_{IN} S.R. $\leq$ 25V/μs	7	+25°C	0.5	-	V/μs

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_V = +1V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Average Offset Voltage Drift	$V_{IO}TC$	V_{CM} = 0V	1	-55°C to +125°C	-	1.3	μV/°C
Differential Input Resistance	R_{IN}	V_{CM} = 0V	1	+25°C	20	-	MΩ
Average Offset Current Drift	$I_{IO}TC$	Versus Temperature V_{CM} = 0V	1	-55°C to +125°C	-	40	pA/°C
Average Bias Current Drift	I_BTC	Versus Temperature V_{CM} = 0V	1	-55°C to +125°C	-	40	pA/°C
Input Noise Voltage Density	E_n	R_S = 20Ω, f_o = 1kHz	1	+25°C	-	11	nV/√Hz
Input Noise Current Density	I_n	R_S = 2MΩ, f_o = 1kHz	1	+25°C	-	0.4	pA/√Hz
Unity Gain Bandwidth	UGBW	V_{OUT} = ±100mV, f_o @ -3dB	1	+25°C	600	-	kHz
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	+25°C	8	-	kHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 2kΩ, C_L = 50pF	1	-55°C to +125°C	+1	-	V/V
Output Resistance	R_{OUT}	Open Loop	1	+25°C	-	80	Ω
Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	51	mW

NOTES:
1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).
3. Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)
4. Measured between 10% and 90% points.
5. Offset adjustment range is [V_{IO} (Measured) ± 1mV] minimum referred to output. This test is for functionality only to assure adjustment through 0V.
6. The input stage has series 1kΩ resistors along with back to back diodes. This allows large differential input voltage protection at a slight increase to noise voltage.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6, 7
Group A Test Requirements	1, 2, 3, 4, 5, 6, 7
Groups C & D Endpoints	1

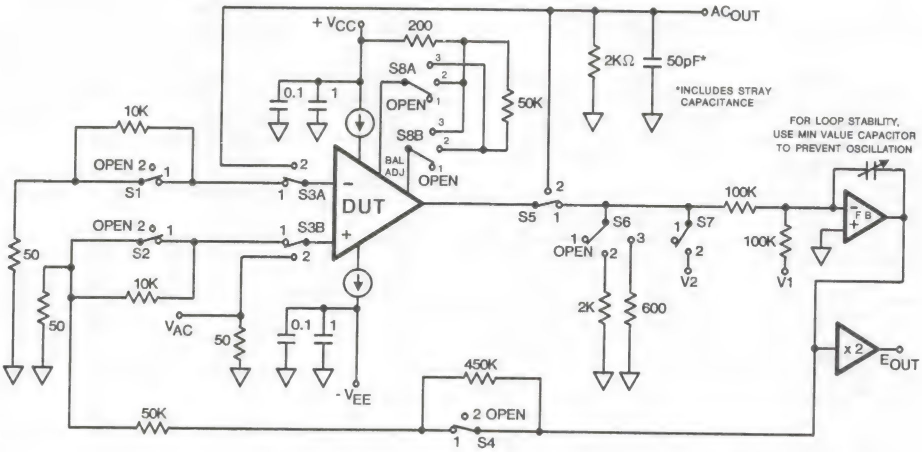
* PDA applies to Subgroup 1 only.

The Subgroup assignments of the parameters in these tables were patterned after Mil-M-38510/135, except for V_{IO} which is Subgroup 1, 2, and 3.

3

OP AMPs & COMPARATORS

Test Circuit (Applies to Tables 1 and 2)

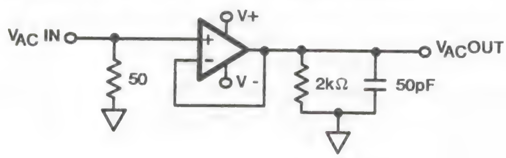


ALL RESISTORS = ± 1% (Ω)
ALL CAPACITORS = ± 10% (μF)

For Op-Amp Test Circuits and Conditions, Refer to the Harris Tech Brief "HA-5135 Op-Amp Test Methods".

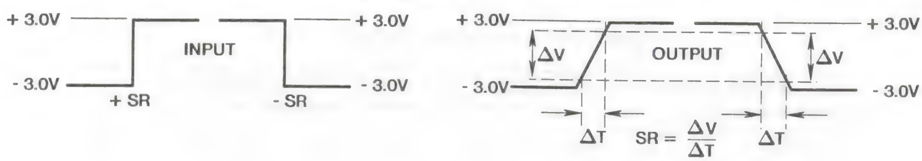
Test Waveforms

SIMPLIFIED TEST CIRCUIT (Applies to Tables 2 and 3)

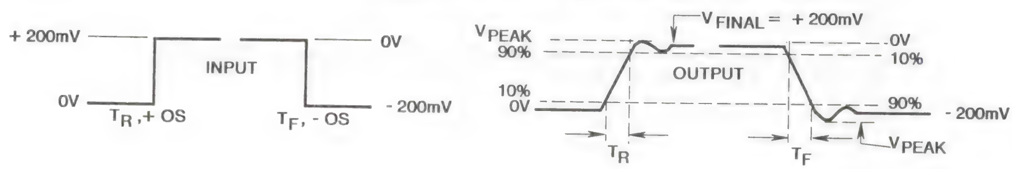


$A_V = +1V/V$

SLEW RATE WAVEFORM



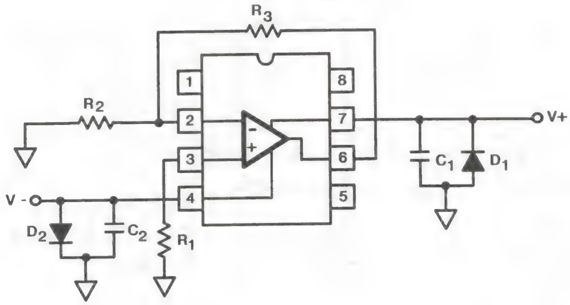
TRANSIENT RESPONSE WAVEFORM



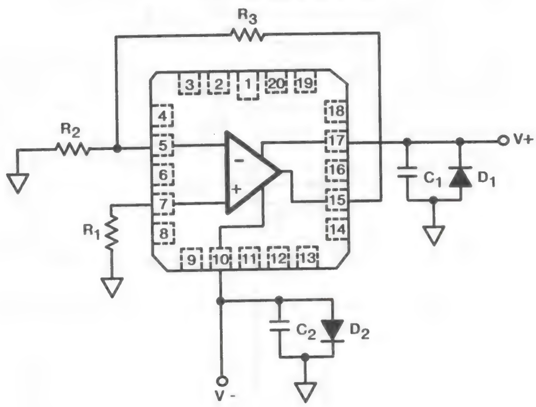
NOTE: Measured on Both positive and negative transitions.

Burn-In Circuits

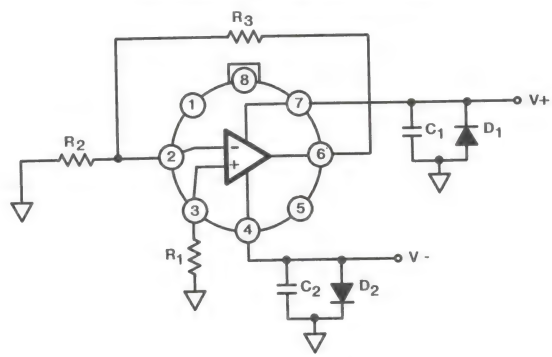
HA7-5135/883 CERAMIC DIP



HA4-5135/883 CERAMIC LCC



HA2-5135/883 (TO-99) METAL CAN



NOTES:

$R_1 = R_2 = 1k\Omega \pm 5\%$, 1/4W (Min)

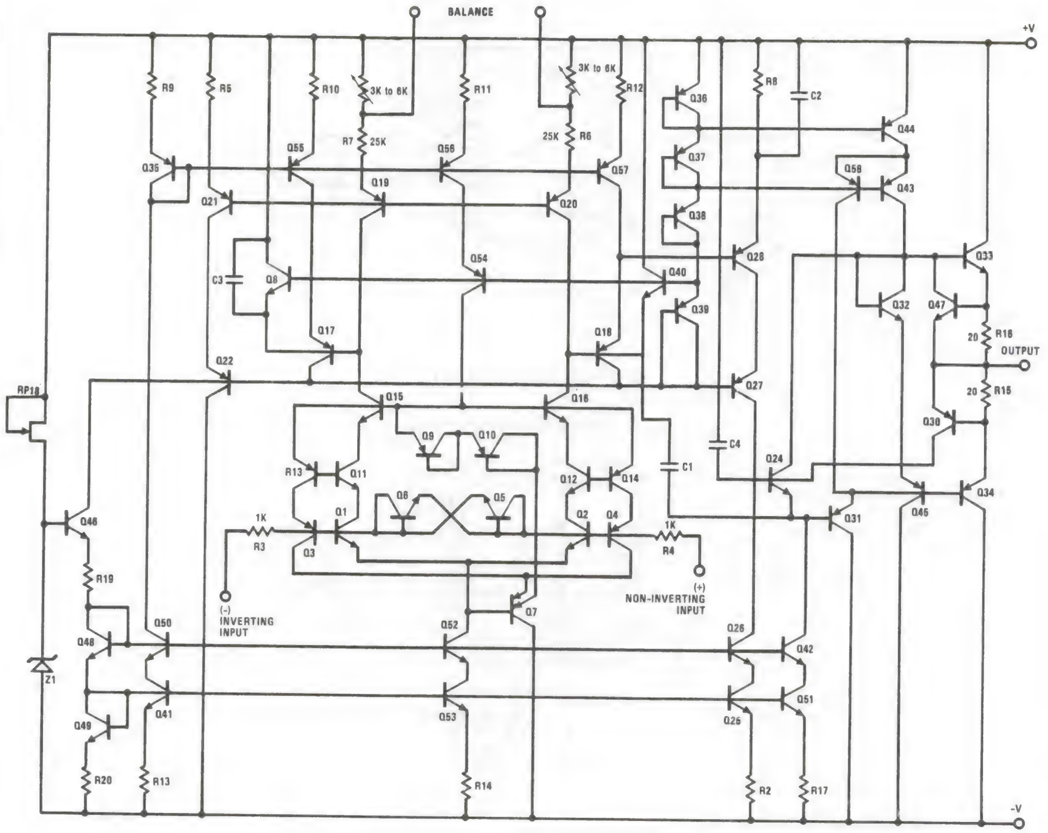
$R_3 = 10k\Omega \pm 5\%$, 1/4W (Min)

$C_1 = C_2 = 0.01\mu F$ per Socket (Min) or $0.1\mu F$ per Row (Min)

$D_1 = D_2 =$ IN4002 or Equivalent/Board

$|(V+) - (V-)| = 30V$

Schematic Diagram



Die Characteristics

DIE DIMENSIONS:
107.3 x 65 x 19 mils
(2720 x 1660 x 483 µm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$3.57 \times 10^5 A/cm^2$ @15mA
This device meets Glassivation Integrity Test requirement per Mil-Std-883 Method 2021 and Mil-M-38510 paragraph 3.5.5.4.

SUBSTRATE POTENTIAL (Powered Up): V-

GLASSIVATION:
Type: Silox
Thickness: 9.5kÅ ± 2.5kÅ

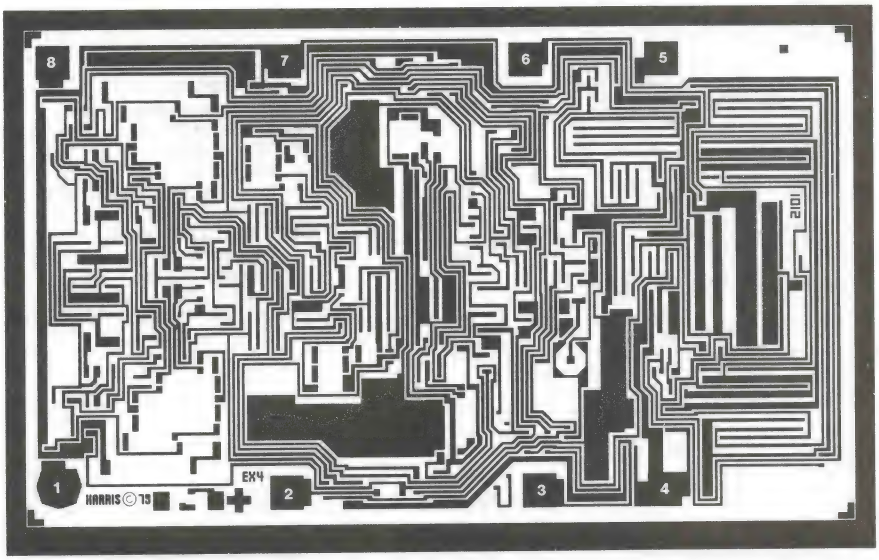
TRANSISTOR COUNT: 57

PROCESS: HFHB Bipolar Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)
Metal Can — 420°C (Max)

Metallization Mask Layout

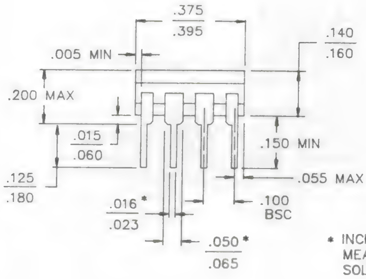
HA-5135/883

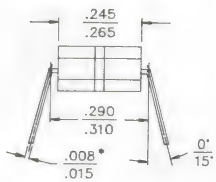


NOTE: Pin Numbers Correspond to 8 Pin Metal Can and Mini-DIP Package Only.

Packaging †

8 PIN CERAMIC DIP

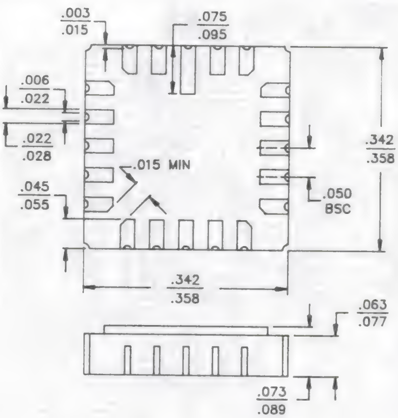




* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

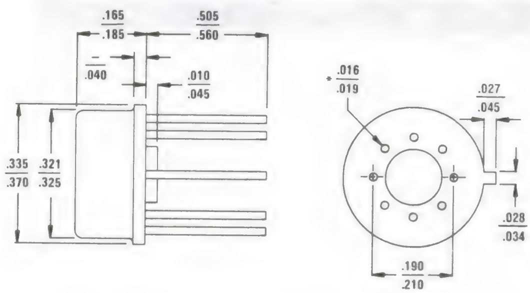
LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-4

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Ceramic, 90% Al_2O_3
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

8 PIN TO-99 METAL CAN



LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
Material: No Seal Material
Temperature: Room Temperature
Method: Resistance Weld
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic Bonded
COMPLIANT OUTLINE: 38510 A-1

*Dimension Maximum Limits Are Increased by 0.003 inches for Solder Dip Finish

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

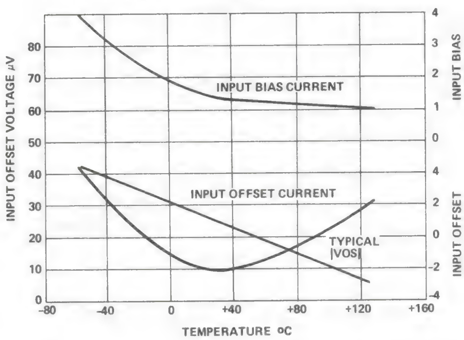
DESIGN INFORMATION

Precision Operational Amplifier

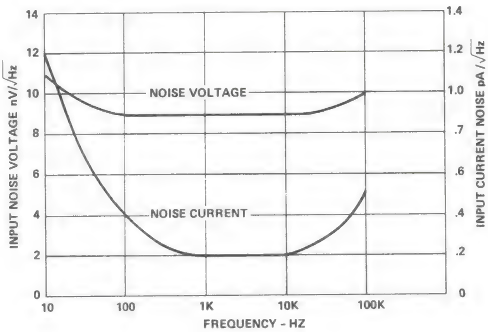
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

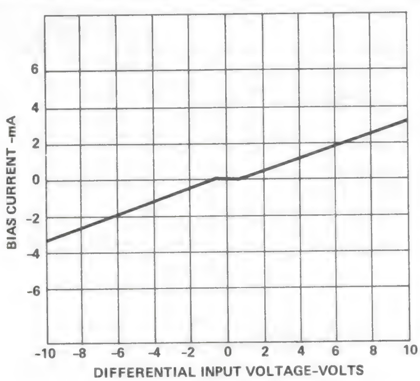
INPUT OFFSET VOLTAGE, INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



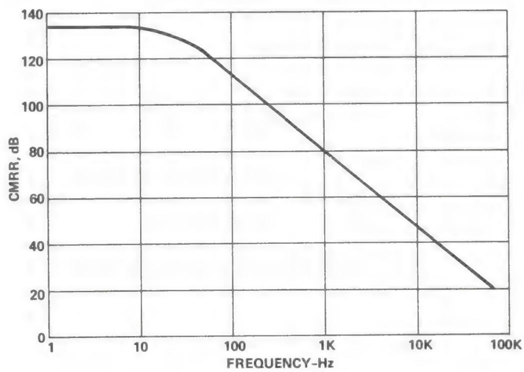
INPUT-NOISE vs. FREQUENCY



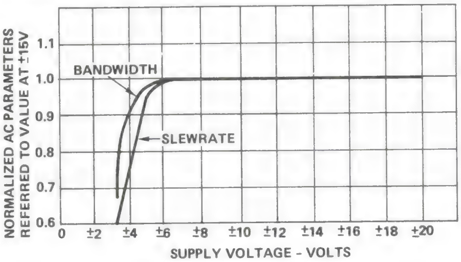
INPUT BIAS CURRENT vs. DIFFERENTIAL INPUT VOLTAGE



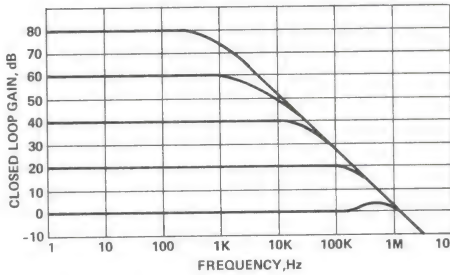
CMRR vs. FREQUENCY



NORMALIZED A.C. PARAMETERS vs. SUPPLY VOLTAGE



CLOSED LOOP FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS



DESIGN INFORMATION (Continued)

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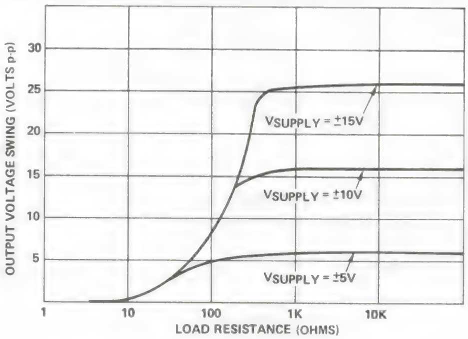
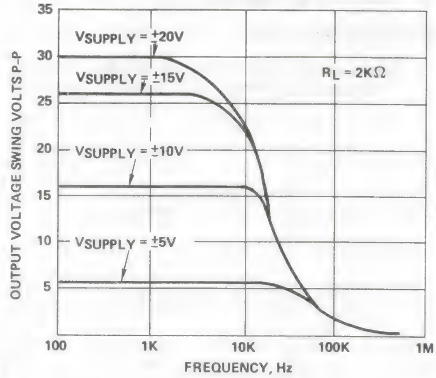
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

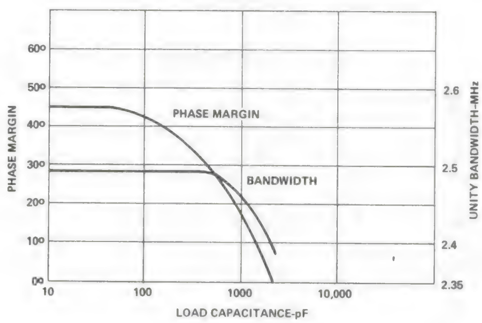
MAXIMUM OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE AND SUPPLY VOLTAGE



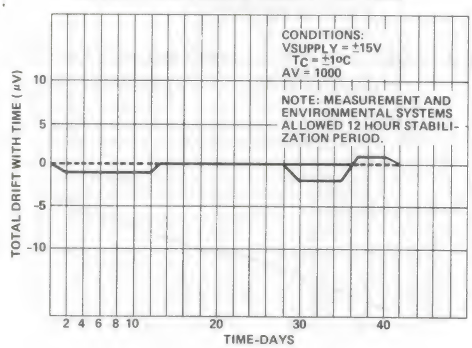
OUTPUT VOLTAGE SWING vs. FREQUENCY AND SUPPLY VOLTAGE



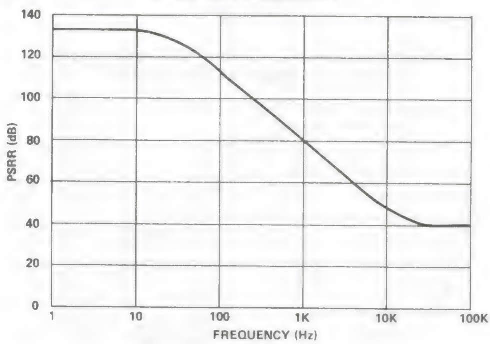
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN vs. LOAD CAPACITANCE



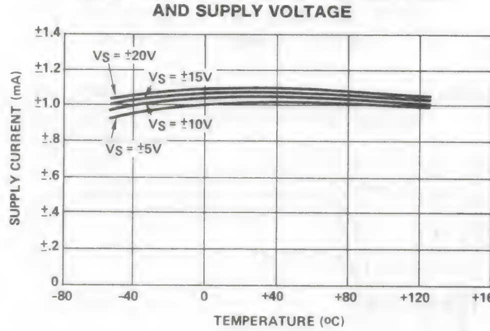
OFFSET VOLTAGE STABILITY vs. TIME



PSRR vs. FREQUENCY



POWER SUPPLY CURRENT vs. TEMPERATURE AND SUPPLY VOLTAGE



DESIGN INFORMATION (Continued)

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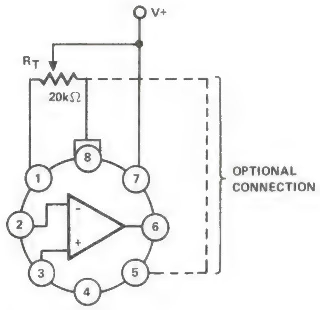
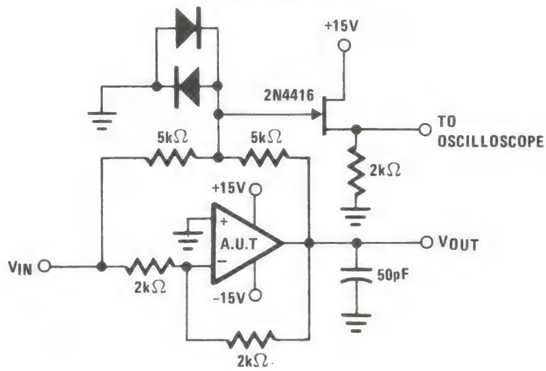
Typical Performance Information Unless Otherwise Specified: $T_A = +25^oC$, $V\pm = \pm15V$

OFFSET NULLING CONNECTIONS



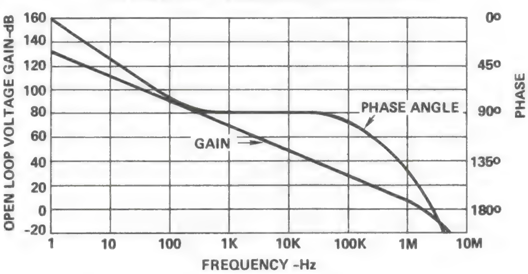
Although R_T is shown equal to 20K, other values such as 50K, 100K and 1M may be used. Range of adjustment is approximately ±2.5mV. V_{OS} TC of the amplifier is optimized at minimal V_{OS}. Tested Offset Adjustment is $|V_{OS} + 1mV|$ minimum referred to output.

SETTLING TIME CIRCUIT

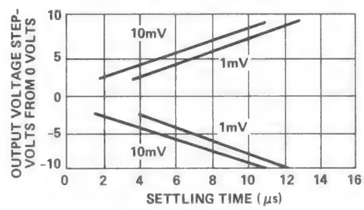


- $A_V = -1$
- Feedback and summing resistors should be 0.1%
- Clippong diodes are optional. HP5082-2810.

OPEN LOOP FREQUENCY RESPONSE

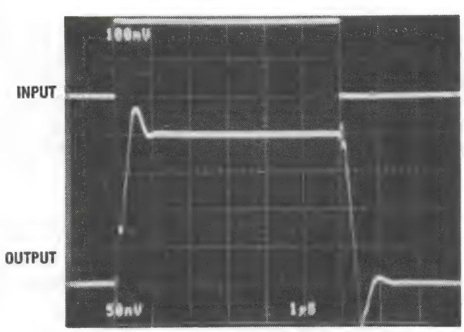


SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



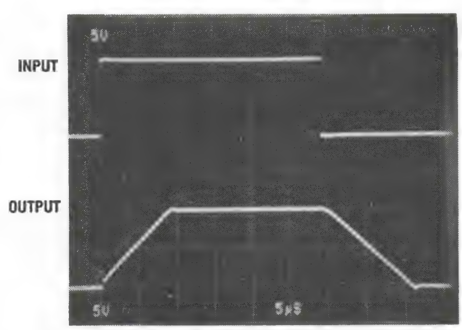
MEASURED SMALL SIGNAL RESPONSE

Input Scale: (Volts: 100mV/Div.)
Output Scale: (Volts: 50mV/Div.)
Time Scale: (1μs/Div.)



MEASURED LARGE SIGNAL RESPONSE

Vertical Scale: (Volts: 5V/Div)
Horizontal Scale: (Time: 5μs/Div.)



DESIGN INFORMATION (Continued)

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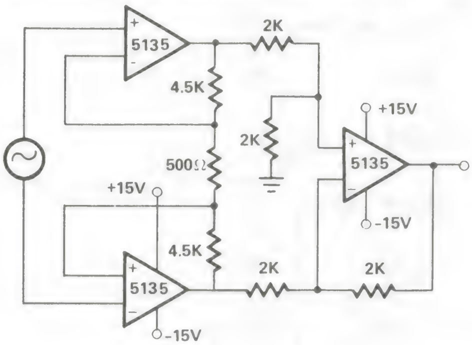
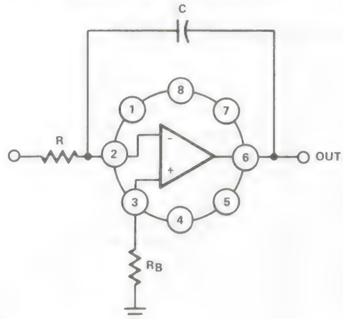
Typical Application Information Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

PRECISION INSTRUMENTATION AMPLIFIER (A_V = 100)

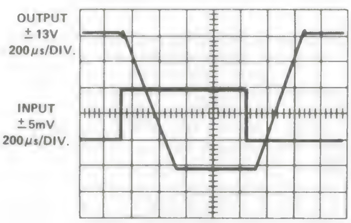


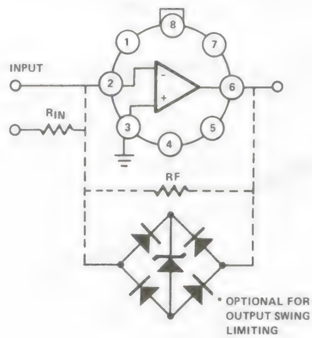
PRECISION INTEGRATOR



The excellent inputs and gain characteristics of HA-5135/883 are well suited for precision integrator applications. Accurate integration over seven decades of frequency using HA-5135/883, virtually nullifies the need for more expensive chopper-type amplifiers.

ZERO CROSSING DETECTOR





Low V_{OS} coupled with high open loop Gain, high CMRR and high PSRR make HA-5135/883 ideally suited for precision detector applications.

Applying the HA-5135 Operational Amplifiers

1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with 0.01µF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.
2. CONSIDERATIONS FOR PROTOTYPING: The following list of recommendations are suggested for prototyping.
   - Resolving low level signals requires minimizing leakage currents caused by external circuitry. Use of quality insulating materials thorough cleaning of insulating surfaces and implementation of moisture barriers when required is suggested.
   - Error voltages generated by thermocouples formed between dissimilar metals in the presence of temperature gradients should be minimized. Isolation of low level circuity from heat generating components is recommended.
   - Shielded cable input leads, guard rings and shield drivers are recommended for the most critical applications.
3. When driving large capacitive loads (> 500pF), as small value resistor (≈ 50Ω) should be connected in series with output and inside the feedback loop.
4. OFFSET VOLTAGE ADJUSTMENT: A 20kΩ balance potentiometer is recommended if offset nulling is required. However, other potentiometer values such as 10kΩ, 50kΩ and 100kΩ may be used. The minimum adjustment range for given values is ±2mV.
5. SATURATION RECOVER: Input and output saturation recovery time is negligible in most applications. However, care should be exercised to avoid exceeding the absolute maximum ratings of the device.
6. DIFFERENTIAL INPUT VOLTAGES: Inputs are shunted with back-to-back diodes and series current limiting resistors for overvoltage protection. The bias currents will increase when a differential voltage of 0.7 volts is exceeded. Refer to the "Bias current versus differential input curve.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_L = 2K, C_L = 50pF, A_V = +1V/V, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage	V_{CM} = 0V	+25°C	10	Table 1	µV
		Full	50	Table 1	µV
Offset Voltage Drift	Versus Temperature	Full	0.4	Table 3	µV/°C
Bias Current	V_{CM} = 0V	+25°C	1	Table 1	nA
		Full	3	Table 1	nA
Bias Current Drift	Versus Temperature	Full	0.02	Table 3	nA/°C
Offset Current Drift	Versus Temperature	Full	0.02	Table 3	nA/°C
Differential Input Resistance		+25°C	30	Table 3	MΩ
Input Noise Voltage Density	f_O = 1Hz	+25°C	15	25	$nV/\sqrt{Hz}$
	f_O = 10Hz	+25°C	13	18	$nV/\sqrt{Hz}$
	f_O = 100Hz	+25°C	10	13	$nV/\sqrt{Hz}$
	f_O = 1kHz	+25°C	9	Table 3	$nV/\sqrt{Hz}$
Input Noise Current Density	f_O = 1Hz	+25°C	1.5	4	$pA/\sqrt{Hz}$
	f_O = 10Hz	+25°C	0.4	1	$pA/\sqrt{Hz}$
	f_O = 100Hz	+25°C	0.2	0.5	$pA/\sqrt{Hz}$
	f_O = 1kHz	+25°C	0.14	Table 3	$pA/\sqrt{Hz}$
Low Frequency P-P Noise Voltage	0.1Hz to 10Hz	+25°C	0.4	0.6	µVp-p
Voltage Gain	V_{OUT} = ±10V R_L = 2KΩ	+25°C	10	Table 1	MV/V
		Full	5	Table 1	MV/V
CMRR	ΔV = ±10V	Full	120	Table 1	dB
PSRR	ΔV_S = ±5 to ±20V	Full	130	Table 1	dB
Slew Rate	V_{OUT} = ±5V	+25°C	0.8	Table 2	V/µs
Settling Time	10V Step to 0.1%	+25°C	11	15	µs
Rise/Fall Time	V_{OUT} = ±200mV	+25°C	340	500	ns
Overshoot	V_{OUT} = ±200mV	+25°C	15	30	%
Supply Current	No Load	Full	1	Table 1	mA
Minimum Supply Voltage	Functional Operation Only. Other Parameters Will Vary.	+25°C	±5	±6	V

3

OP AMPs & COMPARATORS

HARRIS

HA-5137/883

January 1989

Ultra-Low Noise, Precision Wideband Operational Amplifier

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **High Slew Rate .... 14V/μs (Min)**
- **Wide Gain Bandwidth ($A_V \geq 5$) .... 60MHz (Min)**
- **Low Noise (@1kHz)............... 4.5nV/$\sqrt{Hz}$ (Max)**
- **Low Offset Voltage .... 100μV (Max)**
- **Low Offset Drift With Temperature .. 1.8μV/°C (Max)**
- **High CMRR............................ 100dB (Min)**
- **High Voltage Gain .... 700kV/V (Min)**

Applications

- **High Speed Signal Conditioners**
- **Wide Bandwidth Instrumentation Amplifiers**
- **Low Level Transducer Amplifiers**
- **Fast, Low Level Voltage Comparators**
- **Highest Quality Audio Preamplifiers**
- **Pulse/RF Amplifiers**

Description

The HA-5137/883 monolithic operational amplifier features an suburb combination of precision D.C. and wideband high speed characteristics. Utilizing the Harris D.I. technology and advanced processing techniques, this unique design unites low noise precision instrumentation performance with high speed, wideband capability.

This amplifier's impressive list of features include low V_{OS}, wide gain-bandwidth, high open loop gain, and high CMRR. Additionally, this flexible device operates over a wide supply range while consuming only 120mW of power.

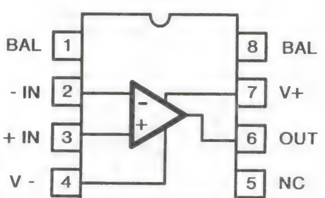
Using the HA-5137/883 allows designers to minimize errors while maximizing speed and bandwidth in applications requiring gains greater than five.

This device is ideally suited for low level transducer signal amplifer circuits. Other applications which can utilize the HA-5137/883's qualities include instrumentation amplifiers, pulse or RF amplifiers, audio preamplifiers, and signal conditioning circuits.

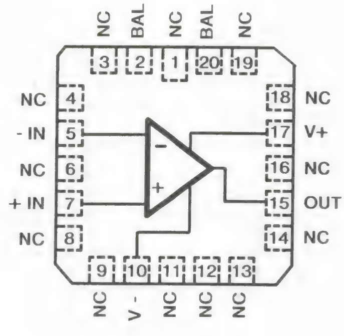
This device can easily be used as a design enhancement by directly replacing the 725, OP-25, OP-06, OP-07, OP-27 and OP-37 where gains are greater than five. The HA-5137/883 is available in TO-99 Metal Can, Ceramic 8 Pin Mini-DIP, and 20 Pin Ceramic LCC packages.

Pinouts

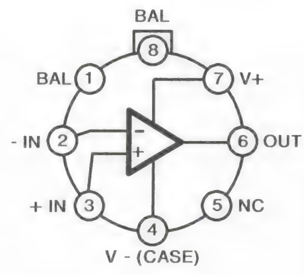
HA7-5137/883 (CERAMIC MINI-DIP)
TOP VIEW



HA4-5137/883 (CERAMIC LCC)
TOP VIEW



HA2-5137/883 (METAL CAN)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 44V
Differential Input Voltage (Note 6) 0.7V
Voltage at Either Input Terminal .... V+ to V-
Input Current 25mA
Differential Output Current .... Full Short Circuit Protection
Junction Temperature (T_J) .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... < 2000V
Lead Temperature (Soldering 10 sec) .... +275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	82°C/W	25°C/W
Ceramic LCC Package	84°C/W	25°C/W
Metal Can Package	98°C/W	30°C/W

Package Power Dissipation Limit at +75°C for $T_J \leq$ +175°C
Ceramic DIP Package 1.22W
Ceramic LCC Package 1.19W
Metal Can Package 1.02W

Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 12.2mW/°C
Ceramic LCC Package .... 11.9mW/°C
Metal Can Package .... 10.2mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±15V
$V_{INcm} \leq 1/2 (V+ - V-)$
$R_L \geq 600\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, $R_{SOURCE} = 50\Omega$, $R_{LOAD} = 100k\Omega$, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	V_{CM} = 0V	1	+25°C	-100	100	µV
			2, 3	+125°C, -55°C	-300	300	µV
Input Bias Current	I_B	V_{CM} = 0V, $R_S = 10k\Omega, 50\Omega$, $\left(\frac{\lvert +I_B\rvert + \lvert -I_B\rvert}{2}\right)$	1	+25°C	-	80	nA
			2, 3	+125°C, -55°C	-	150	nA
Input Offset Current	I_{IO}	V_{CM} = 0V, $+R_S = 10k\Omega$, $-R_S = 10k\Omega$	1	+25°C	-75	75	nA
			2, 3	+125°C, -55°C	-135	135	nA
Common Mode Range	+CMR	V+ = 4.7V, V- = -25.3V	1	+25°C	10.3	-	V
			2, 3	+125°C, -55°C	10.3	-	V
	-CMR	V+ = 25.3V, V- = -4.7V	1	+25°C	-	-10.3	V
			2, 3	+125°C, -55°C	-	-10.3	V
Large Signal Voltage Gain	$+A_{VOL}$	V_{OUT} = 0V and +10V, $R_L = 2k\Omega$	4	+25°C	700	-	kV/V
			5, 6	+25°C, -55°C	300	-	kV/V
	$-A_{VOL}$	V_{OUT} = 0V and -10V, $R_L = 2k\Omega$	4	+25°C	700	-	kV/V
			5, 6	+125°C, -55°C	300	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔV_{CM} = +11V	1	+25°C	100	-	dB
		ΔV_{CM} = +10V	2, 3	+125°C, -55°C	100	-	dB
	-CMRR	ΔV_{CM} = -11V	1	+25°C	100	-	dB
		ΔV_{CM} = -10V	2, 3	+125°C, -55°C	100	-	dB

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

3
OP AMPs & COMPARATORS

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 100kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Voltage Swing	$+V_{OUT1}$	R_L = 2kΩ	4	+25°C	11.5	-	V
			5, 6	+125°C, -55°C	11.5	-	V
	$-V_{OUT1}$	R_L = 2kΩ	4	+25°C	-	-11.5	V
			5, 6	+125°C, -55°C	-	-11.5	V
	$+V_{OUT2}$	R_L = 600Ω	4	+25°C	10	-	V
	$-V_{OUT2}$	R_L = 600Ω	4	+25°C	-	-10	V
Output Current	$+I_{OUT}$	V_{OUT} = -10V	4	+25°C	16.5	-	mA
	$-I_{OUT}$	V_{OUT} = +10V	4	+25°C	-	-16.5	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V	1	+25°C	-	4	mA
		I_{OUT} = 0mA	2, 3	+125°C, -55°C	-	4	mA
	$-I_{CC}$	V_{OUT} = 0V	1	+25°C	-4	-	mA
		I_{OUT} = 0mA	2, 3	+125°C, -55°C	-4	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = 14V +V = +4V, -V = -15V +V = +18V, -V = -15V	1	+25°C	86	-	dB
			2, 3	+125°C, -55°C	86	-	dB
	-PSRR	ΔV_{SUP} = 14V +V = +15V, -V = -4V +V = +15V, -V = -18V	1	+25°C	86	-	dB
			2, 3	+125°C, -55°C	86	-	dB
Offset Voltage Adjustment	$+V_{IO}Adj$	Note 5	1	+25°C	V_{IO} -1	-	mV
			2, 3	+125°C, -55°C	V_{IO} -1	-	mV
	$-V_{IO}Adj$	Note 5	1	+25°C	V_{IO} +1	-	mV
			2, 3	+125°C, -55°C	V_{IO} +1	-	mV

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 2kΩ, C_{LOAD} =50pF, A_{VCL} = +10V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Slew Rate	+SR	V_{OUT} = -4V to +4V	7	+25°C	14	-	V/µs
	-SR	V_{OUT} = +4V to -4V	7	+25°C	14	-	V/µs
Rise & Fall Time	T_R	V_{OUT} = 0 to +200mV 10% ≤ T_R ≤ 90%	7	+25°C	-	100	ns
	T_F	V_{OUT} = 0 to -200mV 10% ≤ T_F ≤ 90%	7	+25°C	-	100	ns
Overshoot	+OS	V_{OUT} = 0 to +200mV	7	+25°C	-	40	%
	-OS	V_{OUT} = 0 to -200mV	7	+25°C	-	40	%

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_V = +5V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Average Offset Voltage Drift	$V_{IO}TC$	V_{CM} = 0V	1	-55°C to +125°C	-	1.8	μV/°C
Differential Input Resistance	R_{IN}	V_{CM} = 0V	1	+25°C	0.8	-	MΩ
Low Frequency Peak-to-Peak Noise	E_{np-p}	0.1Hz to 10Hz	1	+25°C	-	0.25	μV_{p-p}
Input Noise Voltage Density	E_n	R_S = 20Ω, f_O = 10Hz	1, 4	+25°C	-	8.0	$nV/\sqrt{Hz}$
		R_S = 20Ω, f_O = 100Hz	1, 4	+25°C	-	5.6	$nV/\sqrt{Hz}$
		R_S = 20Ω, f_O = 1kHz	1, 4	+25°C	-	4.5	$nV/\sqrt{Hz}$
Input Noise Current Density	I_n	R_S = 2MΩ, f_O = 10Hz	1,4	+25°C	-	4.0	$pA/\sqrt{Hz}$
		R_S = 2MΩ, f_O = 100Hz	1, 4	+25°C	-	2.3	$pA/\sqrt{Hz}$
		R_S = 2MΩ, f_O = 1kHz	1, 4	+25°C	-	0.6	$pA/\sqrt{Hz}$
Gain Bandwidth Product	GBWP	V_O = 100mV, f_O = 10kHz	1	+25°C	60	-	MHz
		V_O = 100mV, f_O = 1MHz	1	+25°C	43	-	MHz
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	+25°C	220	-	kHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 2kΩ, C_L = 50pF	1	-55°C to +125°C	±5	-	V/V
Settling Time	T_S	To 0.1% for a 10V Step	1	+25°C	-	1.5	μs
Output Resistance	R_{OUT}	Open Loop	1	+25°C	-	100	Ω
Quiescent Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	120	mW

NOTES: 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).

3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)

4. Input Noise Voltage Density and Input Noise Current Density is sample tested on every lot.

5. Offset adjustment range is [V_{IO} (Measured) ± 1mV] minimum referred to output. This test is for functionality only to assure adjustment through 0V.

6. For differential input voltages greater than 0.7V, the input current must be limited to 25mA to protect the back-to-back input diodes.

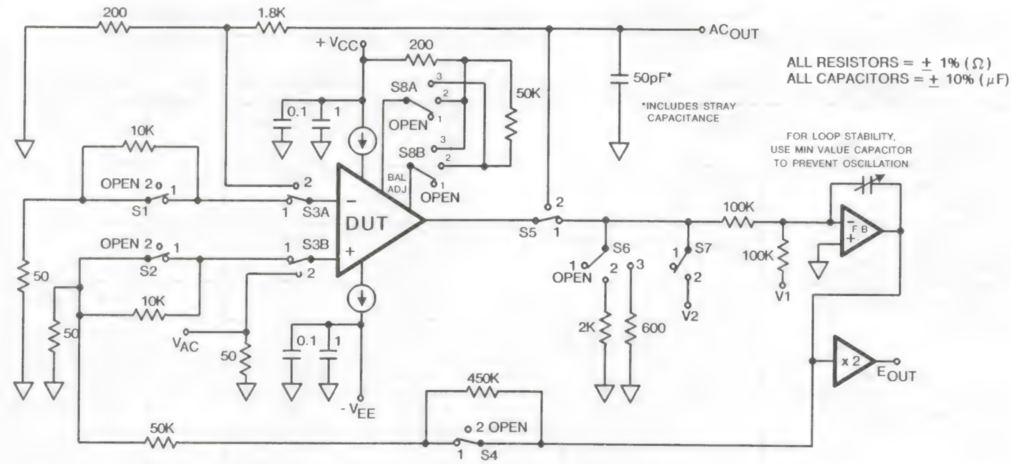
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6, 7
Group A Test Requirements	1, 2, 3, 4, 5, 6, 7
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

The Subgroup assignments of the parameters in these tables were patterned after Mil-M-38510/135, with the exception of V_{IO}, which is Subgroups 1, 2, and 3.

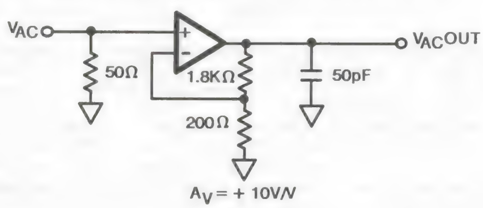
Test Circuit (Applies to Tables 1 and 2)



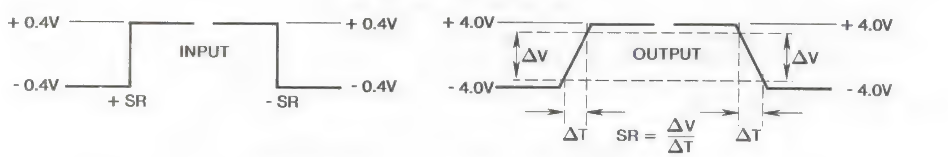
For Op-Amp Test Circuits and Conditions, Refer to the Harris Tech Brief "HA-5137 Op-Amp Test Methods". The HA-5137/883 is A.C. Tested (Table 2) at $A_V = +10V/V$. Stability at a Gain of +5 is Tested for Table 3.

Test Waveforms

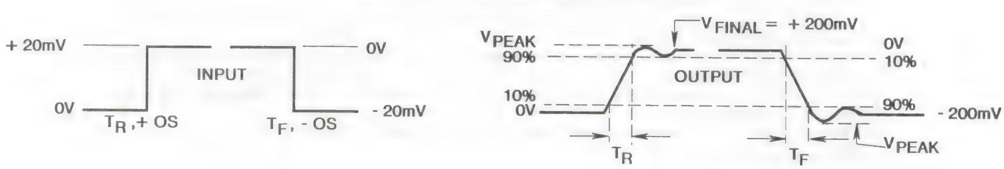
SIMPLIFIED TEST CIRCUIT (Applies to Table 2)



SLEW RATE WAVEFORM



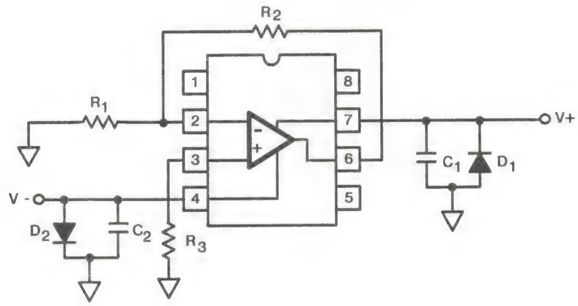
TRANSIENT RESPONSE WAVEFORM



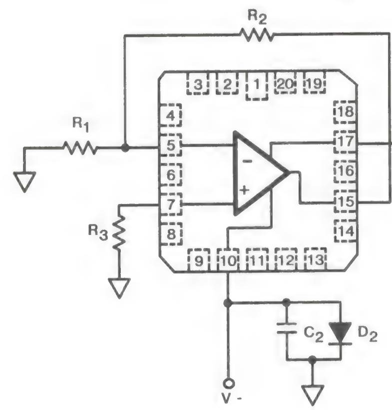
NOTE: Measured on Both positive and negative transitions.

Burn-In Circuits

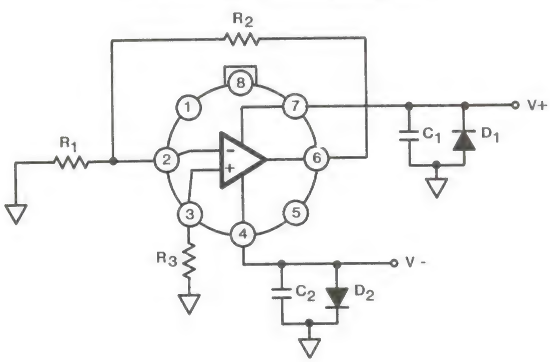
HA7-5137/883 CERAMIC DIP



HA4-5137/883 CERAMIC LCC



HA2-5137/883 (TO-99) METAL CAN

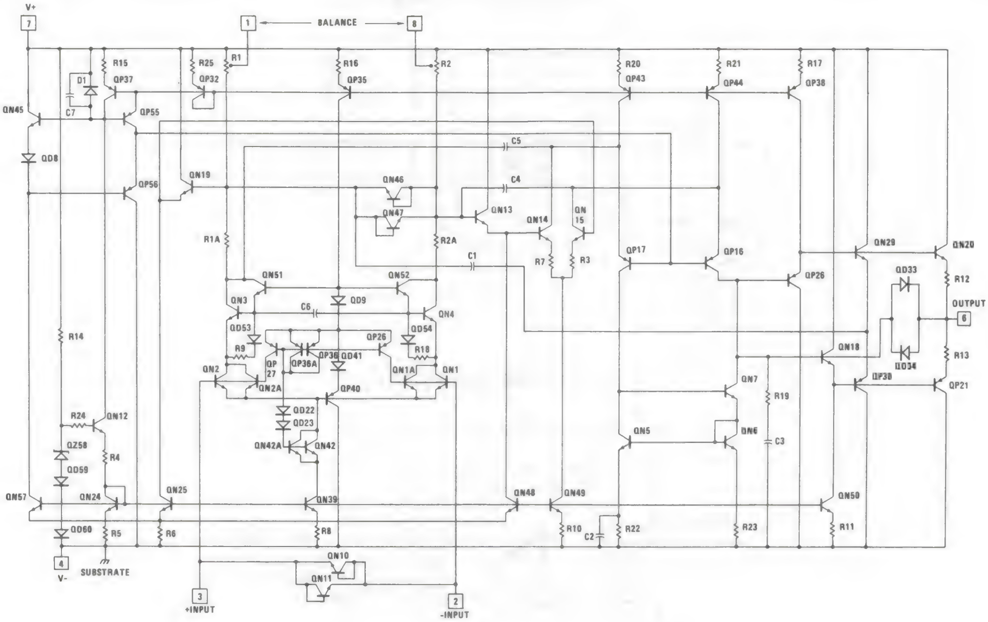


NOTES:

R_1 = R3 = 1kΩ ±5%, 1/4W (Min)
R_2 = 10kΩ ±5%, 1/4W (Min)
$C_1 = C_2$ = 0.01µF/ per Socket (Min) or 0.1µF/per Row (Min)
$D_1 = D_2$ = IN4002 or Equivalent/Board
$|(V+) - (V-)|$ = 30V

3 OP AMPs & COMPARATORS

Schematic Diagram



Die Characteristics

DIE DIMENSIONS:
104.3 x 65 x 19 mils
(2650 x 1650 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$3.6 \times 10^5 A/cm^2$ @15mA
This device meets Glassivation Integrity Test requirement per Mil-Std-883 Method 2021 and Mil-M-38510 paragraph 3.5.5.4.

SUBSTRATE POTENTIAL (Powered Up): V-

GLASSIVATION:
Type: Silox
Thickness: 7kÅ ± 0.7kÅ

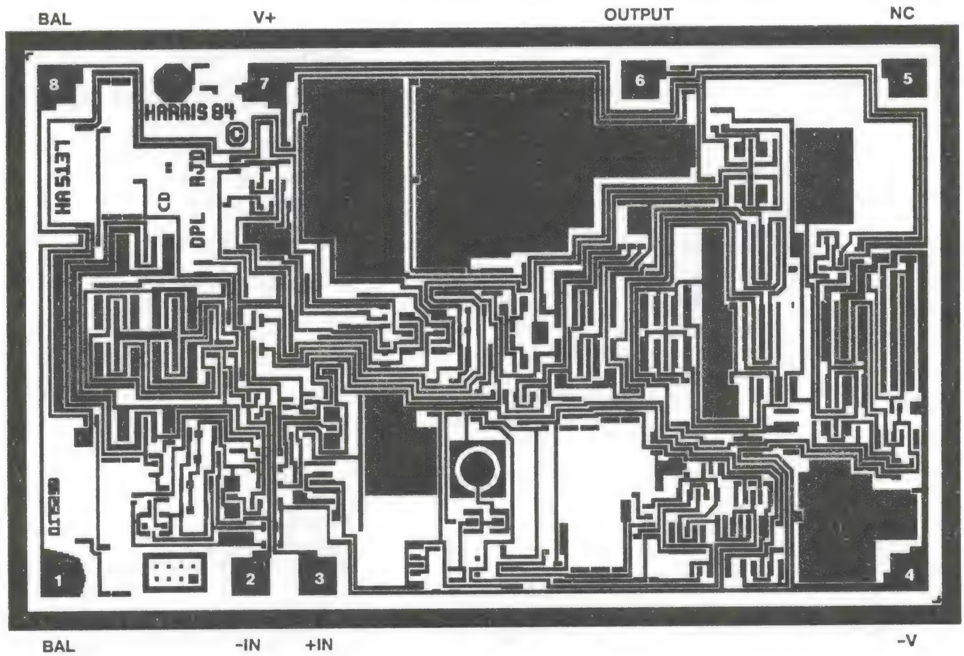
TRANSISTOR COUNT: 63

PROCESS: HFHB Bipolar Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)
Metal Can — 420°C (Max)

Metallization Mask Layout

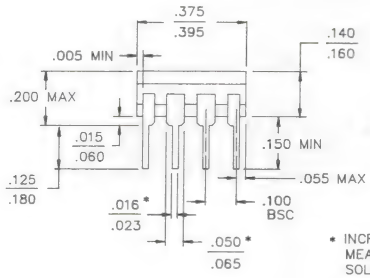
HA-5137/883

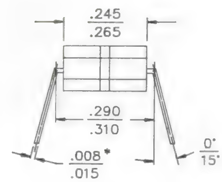


NOTE: Pin Numbers Correspond to 8 Pin Metal Can and Mini-DIP Package Only.

Packaging †

8 PIN CERAMIC DIP

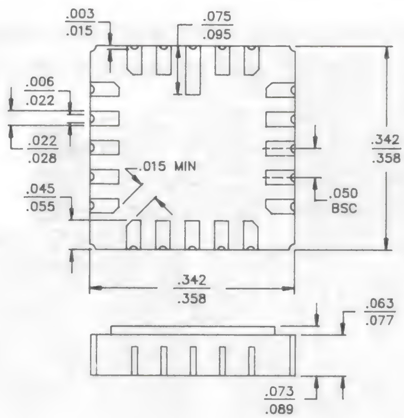




* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

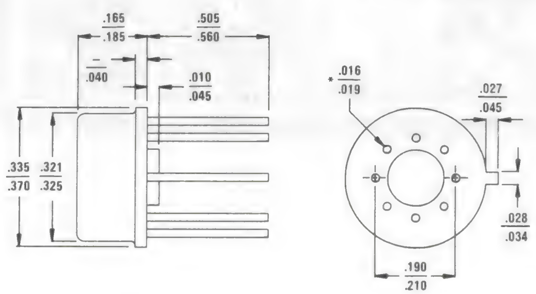
LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-4

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Ceramic, 90% Al_2O_3
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

8 PIN TO-99 METAL CAN



*Dimension Maximum Limits Are Increased by 0.003 inches for Solder Dip Finish

LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
Material: No Seal Material
Temperature: Room Temperature
Method: Resistance Weld
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic Bonded
COMPLIANT OUTLINE: 38510 A-1

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HA-5137

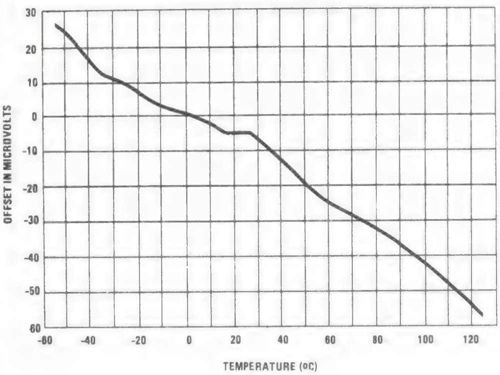
DESIGN INFORMATION

Ultra-Low Noise, Precision Wideband Operational Amplifier

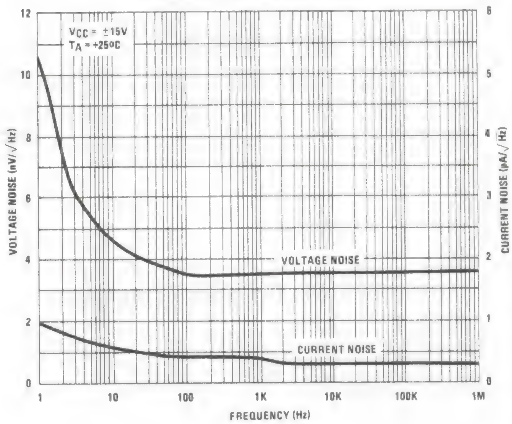
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

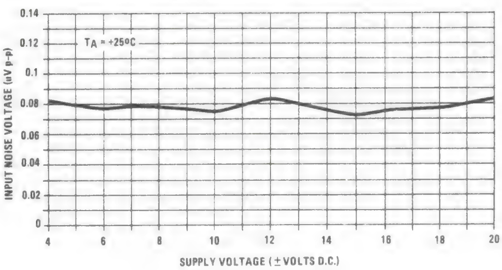
OFFSET VOLTAGE TYPICAL DRIFT vs. TEMPERATURE



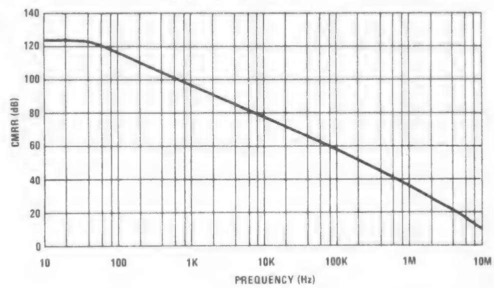
NOISE CHARACTERISTICS



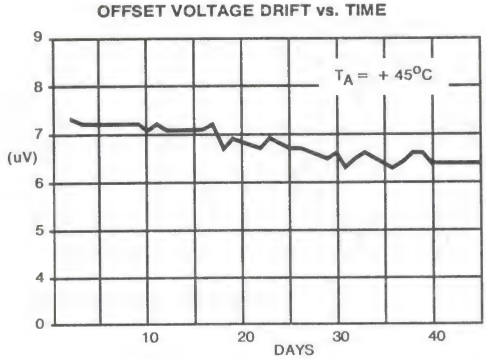
NOISE vs. SUPPLY VOLTAGE



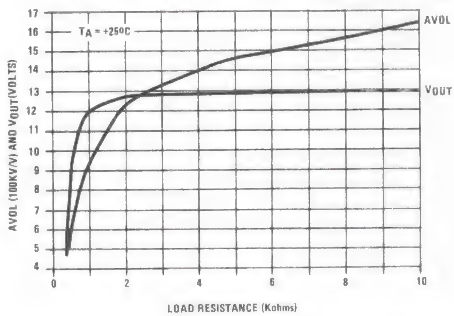
CMRR vs. FREQUENCY



OFFSET VOLTAGE DRIFT vs. TIME



A_{VOL} AND V_{OUT} vs. LOAD RESISTANCE



DESIGN INFORMATION (Continued)

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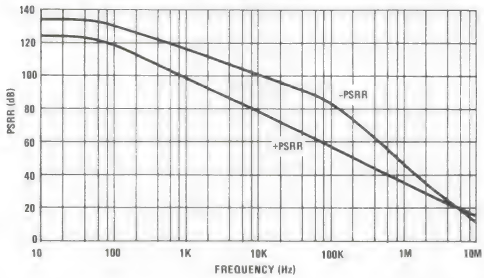
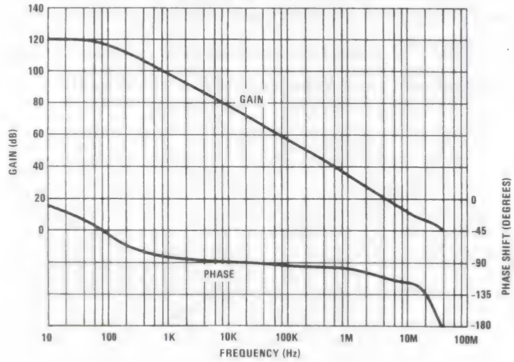
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

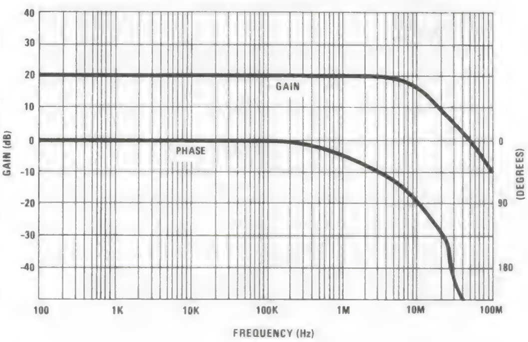
PSRR vs. FREQUENCY



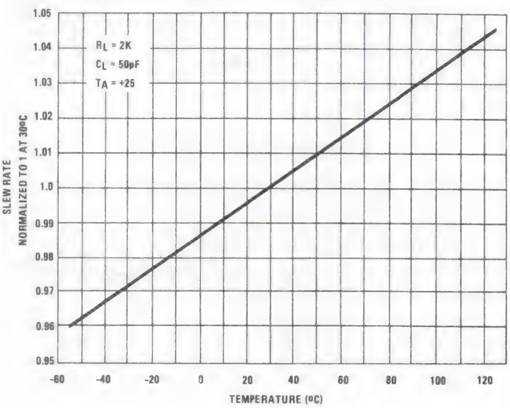
OPEN LOOP GAIN AND PHASE vs. FREQUENCY



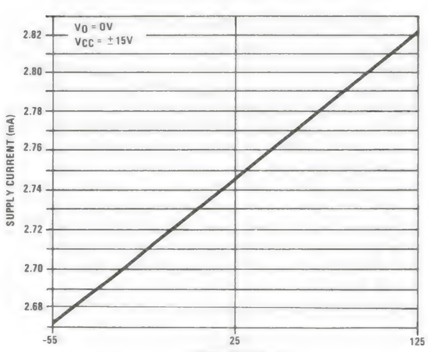
CLOSED LOOP GAIN AND PHASE vs. FREQUENCY



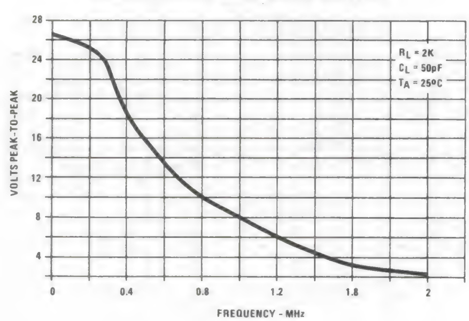
NORMALIZED SLEW RATE vs. TEMPERATURE



SUPPLY CURRENT vs. TEMPERATURE



V_{OUT} MAX vs. FREQUENCY
UNDISTORTED SINEWAVE OUTPUT



DESIGN INFORMATION (Continued)

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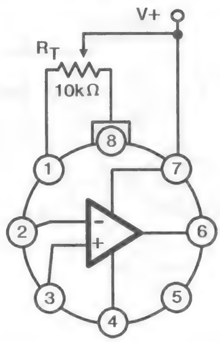
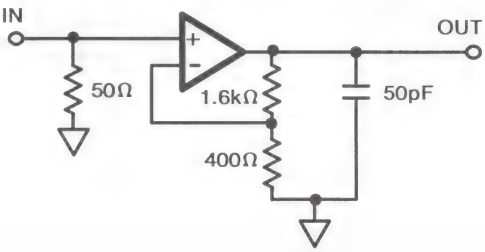
Typical Performance Information Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

SUGGESTED OFFSET VOLTAGE ADJUSTMENT



Tested Offset Adjustment Range is $|V_{OS} + mV|$ minimum referred to output. Typical Range is ±4mV with R_T = 10kΩ.

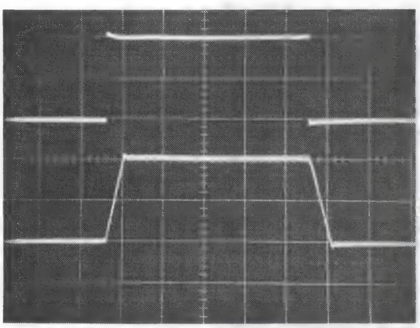
LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT
($A_V = +5$)



MEASURED LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 1V/Div.)
(Volts: Output = 5V/Div.)
Horizontal Scale: (Time: 1µs/Div.)

INPUT

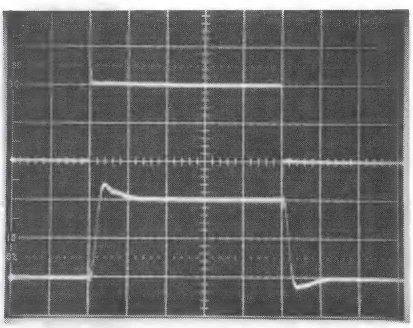
OUTPUT



MEASURED SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 20mV/Div)
(Volts: Output = 100mV/Div.)
Horizontal Scale: (Time: 100ns/Div.)

INPUT

OUTPUT



3

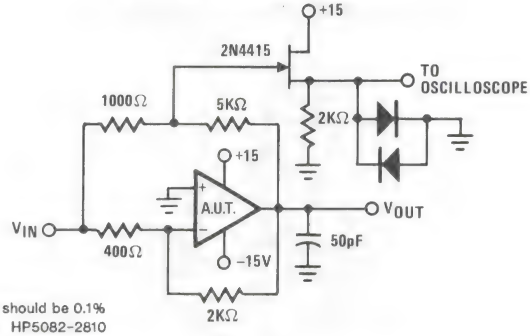
OP AMPs & COMPARATORS

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

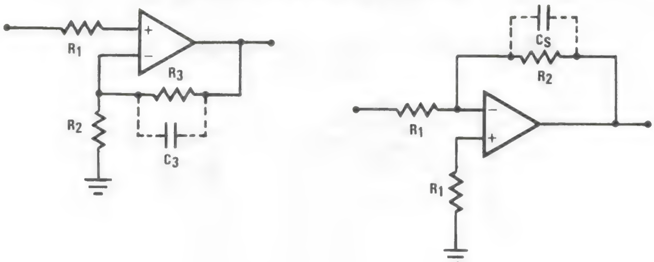
Typical Performance Information Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

SETTLING TIME TEST CIRCUIT



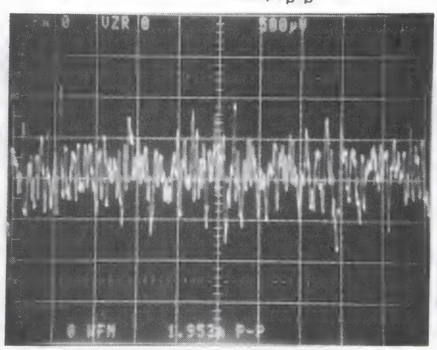
- $A_V = -5$
- Feedback and summing resistors should be 0.1%
- Clipping diodes are optional. HP5082-2810 recommended

SUGGESTED STABILITY CIRCUITS



Low resistances are preferred for low noise applications as a 1kΩ resistor has $4nV/\sqrt{Hz}$ of thermal noise. Total resistances of greater than 10kΩ on either input can reduce stability. In most high resistance applications, a few picofarads of capacitance across the feedback resistor will improve stability.

0.1Hz TO 10Hz NOISE WITH A_{VCL}= 25,000V/V
Horizontal Scale = 1sec/Div.
Vertical Scale = 0.002µV/Div.
$0.08\mu V_{p-p}$ RTI



DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_L = 2kΩ, C_L = 50pF, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage	V_{CM} = 0V	+25°C	30	Table 1	μV
		Full	70	Table 1	μV
Offset Voltage Drift	Versus Temperature	Full	0.4	Table 3	μV/°C
	Versus Time	+45°C	0.71	1.5	μV/Month
Bias Current	V_{CM} = 0V	+25°C	±15	Table 1	nA
		Full	±35	Table 1	nA
Differential Input Resistance		+25°C	6	Table 3	MΩ
Input Noise Voltage	f_O = 10Hz	+25°C	4.4	Table 3	$nV/\sqrt{Hz}$
	f_O = 100Hz	+25°C	3.4	Table 3	$nV/\sqrt{Hz}$
	f_O = 1kHz	+25°C	3.2	Table 3	$nV/\sqrt{Hz}$
Input Noise Current	f_O = 10Hz	+25°C	1.7	Table 3	$pA/\sqrt{Hz}$
	f_O = 100Hz	+25°C	1.0	Table 3	$pA/\sqrt{Hz}$
	f_O = 1kHz	+25°C	0.4	Table 3	$pA/\sqrt{Hz}$
Voltage Gain	V_{OUT} = ±10V	+25°C	1.8	Table1	MV/V
		Full	1.2	Table 1	MV/V
CMRR	ΔV = ±10V	Full	126	Table 1	dB
PSRR	V_S = ±4 to ±18V	Full	110	Table 1	dB
Slew Rate	V_{OUT} = ±5V	+25°C	20	Table 2	V/μs
Overshoot	V_{OUT} = ±200mV	+25°C	20	Table 2	%
Settling Time	10V to 0.1%	+25°C	1.0	Table 3	μs
	10V to 0.01%	+25°C	1.3	1.8	μs
Minimum Supply Voltage	Functional Operation Only. Other Parameters Will Vary.	+25°C	±4	±5	V

HARRIS HA-5141/883

Single, Ultra-Low Power Operational Amplifier

January 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low Supply Current @ V_S = +5V . . (+25°C) 80µA (Max) (Full) 100µA (Max)
- Wide Supply Voltage Range . . . . Single 3V to 30V or Dual ±1.5 to ±15V
- High Slew Rate . . . . +S.R. 0.8V/µs (Min) 1.5V/µs (Typ)
- High Gain . . . . 20kV/V (Min) 75kV/V (Typ)
- Low Noise (1kHz) . . . . 20nV/$\sqrt{Hz}$ (Typ)
- 100% Tested at ±15V and 0V, +5V Power Supplies
- Unity Gain Stable
- Dielectric Isolation

Applications

- Portable Instruments
- Meter Amplifiers
- Telephone Headsets
- Microphone Amplifiers
- Instrumentation
- For Further Design Ideas See App. Note 544

Description

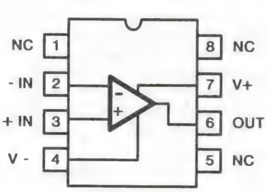
The HA-5141/883 single, ultra-low power operational amplifier provide AC and DC performance characteristics similar to, or better than most general purpose amplifiers while only drawing 1/30 of the supply current of most general purpose amplifiers. This amplifier is well suited to applications which require low power dissipation and good electrical characteristics.

The HA-5141/883 provides accurate signal processing by virtue of their low input offset voltage (6mV), low input bias current (100nA), high open loop gain (20kV/V) and low noise (20nV/$\sqrt{Hz}$). These characteristics coupled with a 1.5V/µs slew rate and a 24kHz bandwidth make the HA-5141/883 ideal for use in low power instrumentation, audio amplifier and active filter designs. The wide range of supply voltages (3V to 30V) also allow these amplifier and active filter designs. The wide range of supply voltages (3V to 30V) also allow these amplifiers to be very useful in low voltage battery powered equipment.

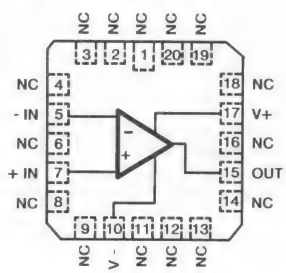
The HA-5141/883 offers tested specifications at both single ended levels (0V, +5V) and dual supplies (±15V). Packaging is offered in the Ceramic Mini-DIP, 20 pad Ceramic LCC or 8 pin (TO-99) Metal Can, and operation is specified at the full military -55°C to +125°C temperature range.

Pinouts

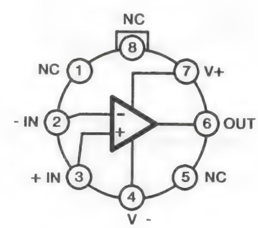
HA7-5141/883 (CERAMIC MINI-DIP)
TOP VIEW



HA4-5141/883 (CERAMIC LCC)
TOP VIEW



HA2-5141/883 (METAL CAN)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage 7V
Voltage at Either Input Terminal .... V+ to V-
Output Current .... Full Short Circuit Protection
Output Current Duration .... Indefinite, One Amplifier Shorted to Ground
Junction Temperature (T_J) .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... <2000V
Lead Temperature (Soldering 10 sec) .... +275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	83°C/W	28°C/W
Ceramic LCC Package	74°C/W	20°C/W
Metal Can Package	149°C/W	45°C/W

Package Power Dissipation Limit at +75°C For $T_J \leq$ +175°C
- Ceramic DIP Package 1.21W
- Ceramic LCC Package 1.34W
- Metal Can Package 670mW

Package Power Dissipation Derating Factor Above +75°C
- Ceramic DIP Package .... 12.1mW/°C
- Ceramic LCC Package .... 13.4mW/°C
- Metal Can Package .... 6.7mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±1.5V to ±15V or 3V to 30V
$V_{INcm} \leq 1/2$ (V+ - V-)
$R_L \geq 50k\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $R_{SOURCE} = 100\Omega$, $R_{LOAD} = 500k\Omega$, V_{OUT} = 0V, Unless Otherwise Specified.
Subscript 1 Refers to Supply Voltages ($\pm V_S$) = ±15V, Subscript 2 Refers to $+V_S$ = 5.0V, $-V_S$ = 0.0V.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO1}	V_{CM} = 0V	1	+25°C	-6	6	mV
			2, 3	+125°C, -55°C	-8	8	mV
	V_{IO2}	V_{CM} = 0V, V_{OUT} = 1.4V	1	+25°C	-6	6	mV
			2, 3	+125°C, -55°C	-8	8	mV
Input Bias Current	$+I_{B1}$	V_{CM} = 0V, $+R_S = 10k\Omega$, $-R_S = 100\Omega$	1	+25°C	-100	100	nA
			2, 3	+125°C, -55°C	-125	125	nA
	$-I_{B1}$	V_{CM} = 0V, $+R_S = 100\Omega$, $-R_S = 10k\Omega$	1	+25°C	-100	100	nA
			2, 3	+125°C, -55°C	-125	125	nA
	$+I_{B2}$	V_{CM} = 0V, V_{OUT} = 1.4V, $+R_S = 10k\Omega$, $-R_S = 100\Omega$	1	+25°C	-100	100	nA
			2, 3	+125°C, -55°C	-125	125	nA
	$-I_{B2}$	V_{CM} = 0V, V_{OUT} = 1.4V, $+R_S = 100\Omega$, $-R_S = 10k\Omega$	1	+25°C	-100	100	nA
			2, 3	+125°C, -55°C	-125	125	nA
Input Offset Current	I_{IO1}	V_{CM} = 0V, $+R_S = 10k\Omega$, $-R_S = 10k\Omega$	1	+25°C	-10	10	nA
			2, 3	+125°C, -55°C	-20	20	nA
	I_{IO2}	V_{CM} = 0V, V_{OUT} = 1.4V, $+R_S = 10k\Omega$, $-R_S = 10k\Omega$	1	+25°C	-10	10	nA
			2, 3	+125°C, -55°C	-20	20	nA
Common Mode Range	$+CMR_1$	V+ = 5V, V- = -25V	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	$-CMR_1$	V+ = 25V, V- = -5V	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
	$+CMR_2$	V+ = 5V to 2V, V- = 0V to -3V, V_{OUT} = 1.4V to -1.6V	1	+25°C	0 to 3	-	V
			2, 3	+125°C, -55°C	0 to 3	-	V

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: $R_{SOURCE} = 100\Omega$, $R_{LOAD} = 500k\Omega$, $V_{OUT} = 0V$, Unless Otherwise Specified.
Subscript 1 Refers to Supply Voltages ($\pm V_S$) = $\pm 15V$; Subscript 2 Refers to $+V_S = 5.0V$, $-V_S = 0.0V$.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Large Signal Voltae Gain	$+A_{VOL1}$	V_{OUT} = 0V and 10V, $R_L = 50k\Omega$	4	$+25^oC$	20	-	kV/V
			5, 6	$+125^oC, -55^oC$	15	-	kV/V
	$-A_{VOL1}$	V_{OUT} = 0V and -10V, $R_L = 50k\Omega$	4	$+25^oC$	20	-	kV/V
			5, 6	$+125^oC, -55^oC$	15	-	kV/V
	$+A_{VOL2}$	V_{OUT} = 1.4V and 2.5V, $R_L = 50k\Omega$	4	$+25^oC$	20	-	kV/V
			5, 6	$+125^oC, -55^oC$	15	-	kV/V
Common Mode Rejection Ratio	$+CMRR_1$	ΔV_{CM} = 10V, +V = 5V, -V = -25V, V_{OUT} = -10V	1	$+25^oC$	77	-	dB
			2, 3	$+125^oC, -55^oC$	77	-	dB
	$-CMRR_1$	ΔV_{CM} = 10V, +V = 25V, -V = -5V, V_{OUT} = 10V	1	$+25^oC$	77	-	dB
			2, 3	$+125^oC, -55^oC$	77	-	dB
	$+CMRR_2$	ΔV_{CM} = 0V to 3V, +V = 2V, -V = -3V, V_{OUT} = -3V	1	$+25^oC$	77	-	dB
			2, 3	$+125^oC, -55^oC$	77	-	dB
Output Voltage Swing	$+V_{OUT1}$	$R_L = 50k\Omega$	1	$+25^oC$	10	-	V
			2, 3	$+125^oC, -55^oC$	10	-	V
	$-V_{OUT1}$	$R_L = 50k\Omega$	1	$+25^oC$	-	-10	V
			2, 3	$+125^oC, -55^oC$	-	-10	V
	$+V_{OUT2}$	$R_L = 50k\Omega$, Terminated at 2.5V	1	$+25^oC$	3.8	-	V
			2, 3	$+125^oC, -55^oC$	3.5	-	V
	$-V_{OUT2}$	$R_L = 50k\Omega$, Terminated at 2.5V	1	$+25^oC$	-	1	V
			2, 3	$+125^oC, -55^oC$	-	1.2	V
Quiescent Power Supply Current	$+I_{CC1}$	V_{OUT} = 0V, I_{OUT} = 0mA	1	$+25^oC$	-	150	μA
			2, 3	$+125^oC, -55^oC$	-	200	μA
	$-I_{CC1}$	V_{OUT} = 0V, I_{OUT} = 0mA	1	$+25^oC$	-150	-	μA
			2, 3	$+125^oC, -55^oC$	-200	-	μA
	$+I_{CC2}$	V_{OUT} = 1.4V, I_{OUT} = 0mA	1	$+25^oC$	-	80	μA
			2, 3	$+125^oC, -55^oC$	-	100	μA
Power Supply Rejection Ratio	$+PSRR_1$	ΔV_{SUP} = 10V, +V = 10V, -V = -15V, +V = 20V, -V = -15V	1	$+25^oC$	77	-	dB
			2, 3	$+125^oC, -55^oC$	77	-	dB
	$-PSRR_1$	ΔV_{SUP} = 10V, +V = 15V, -V = -10V, +V = 15V, -V = -20V	1	$+25^oC$	77	-	dB
			2, 3	$+125^oC, -55^oC$	77	-	dB
	$+PSRR_2$	ΔV_{SUP} = 10V, +V = 5V, -V = 0V, +V = 15V, -V = 0V	1	$+25^oC$	77	-	dB
			2, 3	$+125^oC, -55^oC$	77	-	dB

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $R_{SOURCE} = 50\Omega$, $R_{LOAD} = 50k\Omega$, $C_{LOAD} = 50pF$, $V_{OUT} = 0V$, Unless Otherwise Specified.
Subscript 1 Refers to Supply Voltages ($\pm V_S$) = $\pm 15V$; Subscript 2 Refers to $+V_S = 5.0V$, $-V_S = 0.0V$.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Slew Rate	$+SR_1$	$V_{OUT} = -3V$ to $3V$ V_{IN} S.R. $\leq 10V/\mu s$ @ $A_V = 1$	4	+25°C	0.8	-	V/µs
	$-SR_1$	$V_{OUT} = 3V$ to $-3V$ V_{IN} S.R. $\leq 10V/\mu s$ @ $A_V = 1$	4	+25°C	0.8	-	V/µs
	$+SR_2$	$V_{OUT} = 0V$ to $3V$ V_{IN} S.R. $\leq 10V/\mu s$ @ $A_V = 1$	4	+25°C	0.8	-	V/µs
	$-SR_2$	$V_{OUT} = 3V$ to $0V$ V_{IN} S.R. $\leq 10V/\mu s$ @ $A_V = 1$	4	+25°C	0.8	-	V/µs

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $R_{SOURCE} = 50\Omega$, $R_{LOAD} = 50k\Omega$, $C_{LOAD} = 50pF$, $A_V = 1V/V$, Unless Otherwise Specified.
Subscript 1 Refers to Supply Voltages ($\pm V_S$) = $\pm 15V$; Subscript 2 Refers to $+V_S = 5.0V$, $-V_S = 0.0V$.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Full Power Bandwidth	$FPBW_1$	$V_{PEAK} = 10V$	1, 2	+25°C	12.7	-	kHz
	$FPBW_2$	$V_{PEAK} = 1.1V$ $V_{Ref} = 2.5V$	1, 2	+25°C	115.8	-	kHz
Minimum Closed Loop Stable Gain	CLSG	$R_L = 50k\Omega$, $C_L = 50pF$	1	-55°C to +125°C	1	-	V/V
Quiecent Power Consumption	PC_1	$V_{OUT} = 0V$, $I_{OUT} = 0mA$	1, 3	-55°C to +125°C	-	6	mW
	PC_2	$V_{OUT} = 1.4V$, $I_{OUT} = 0mA$	1, 3	-55°C to +125°C	-	0.5	mW

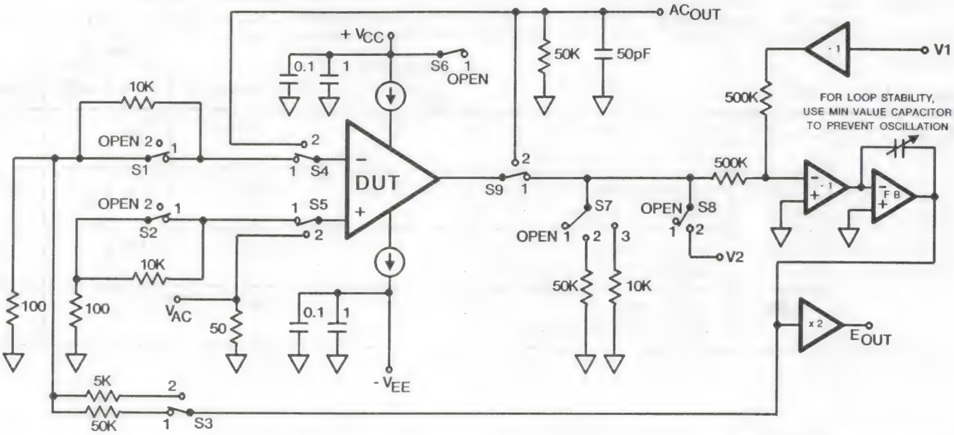
NOTES:
1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Full Power Bandwidth guarantee based on Slew Rate measurement using $FPBW = \text{Slew Rate}/(2\pi V_{PEAK})$.
3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6
Group A Test Requirements	1, 2, 3, 4, 5, 6
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

Test Circuit (Applies to Tables 1 and 2)

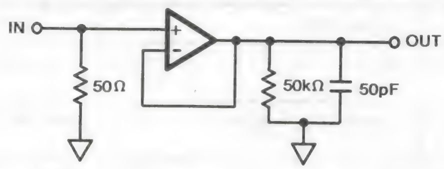


ALL RESISTORS = ± 1% (Ω)
ALL CAPACITORS = ± 10% (μF)

For Detailed Information, Refer to HA-5141/883 Test Tech Brief

Test Waveforms

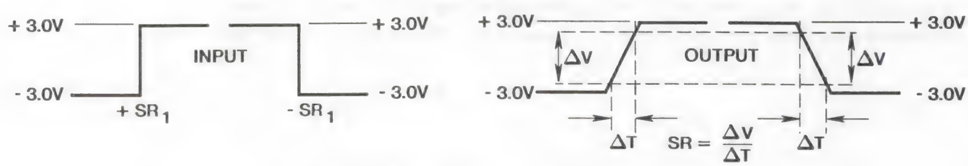
SIMPLIFIED TEST CIRCUIT (Applies to Table 2)



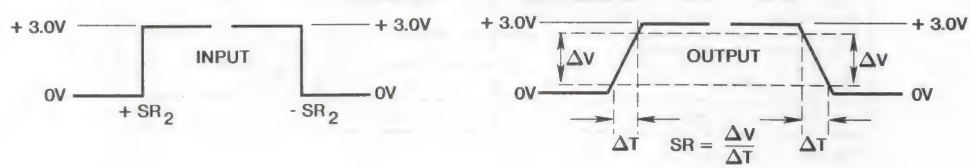
NOTE: $\pm V_{SUPPLY}$ ($\pm V_S$) Tested with ±15V and 0V, +5V. V_{IN} Slew Rate Maintained with Less Than 10V/μs Input for Voltage Follower Configuration.

SLEW RATE WAVEFORMS, A_V = 1V/V

$\pm V_{SUPPLY} = \pm 15V$

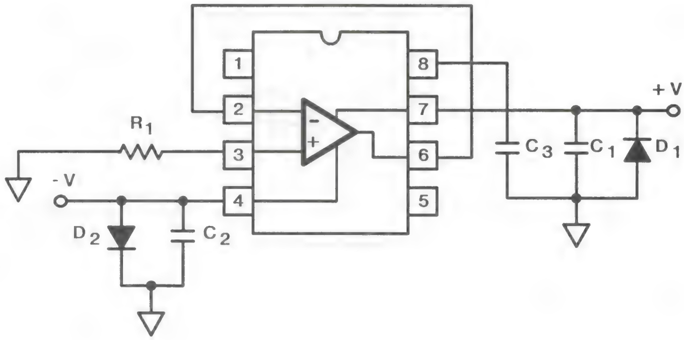


$+V_{SUPPLY} = 5V$, $-V_{SUPPLY} = 0V$

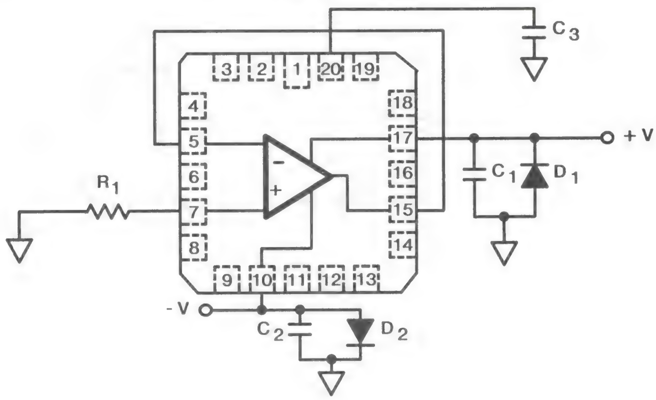


Burn-In Circuits

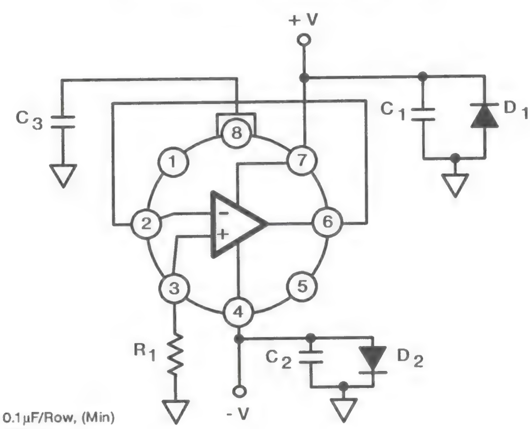
HA7-5141/883 CERAMIC DIP



HA4-5141/883 CERAMIC LCC



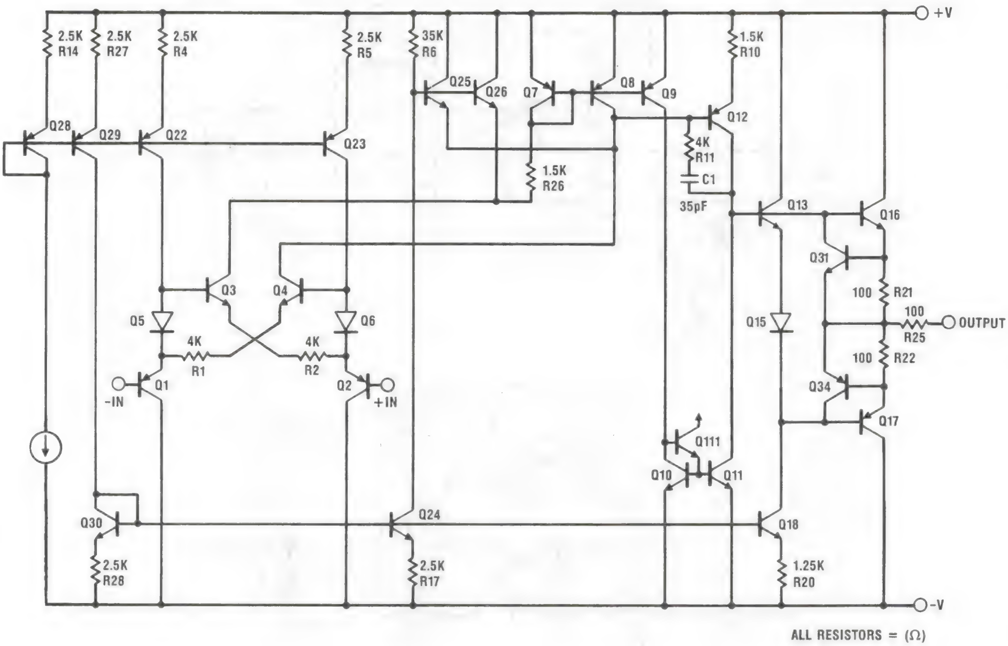
HA2-5141/883 TO-99 METAL CAN



NOTES:

R_1 = 1MΩ, ±5%, 1/4W (Min)
$C_1 = C_2$ = 0.01μF/Socket (Min) or 0.1μF/Row, (Min)
C_3 = 0.01μF/Socket, 10% (Not Required)
$D_1 = D_2$ = IN4002 or Equivalent/Board
$|(V+) - (V-)|$ = 30V

Schematic Diagram



Die Characteristics

DIE DIMENSIONS:
53.1 x 58.7 x 19 mils
(1350 x 1490 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$0.6 \times 10^5 A/cm^2$ @ 2.5mA

SUBSTRATE POTENTIAL (Powered Up): V-

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

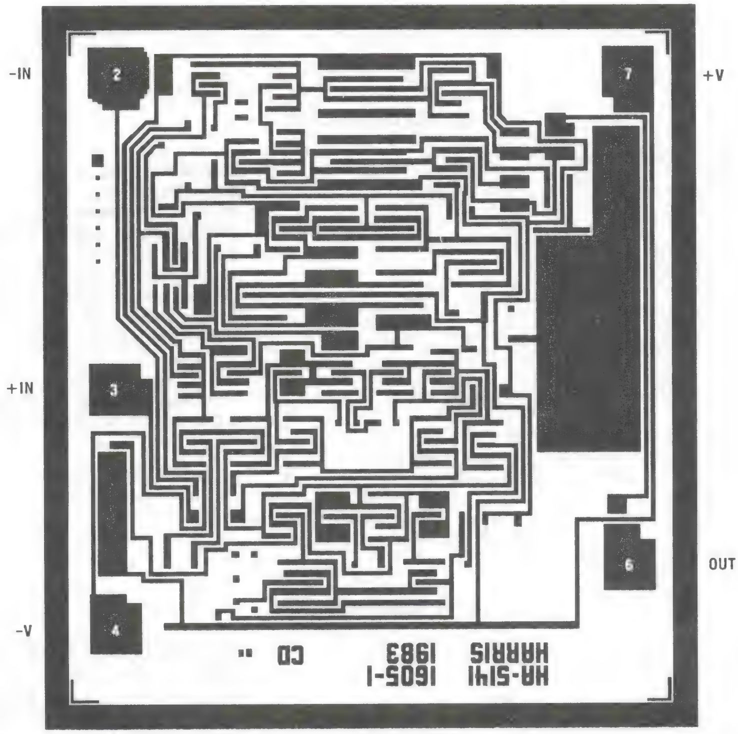
TRANSISTOR COUNT: 36

PROCESS: HFSB Bipolar/JFET Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)
Metal Can — 420°C (Max)

Metallization Mask Layout

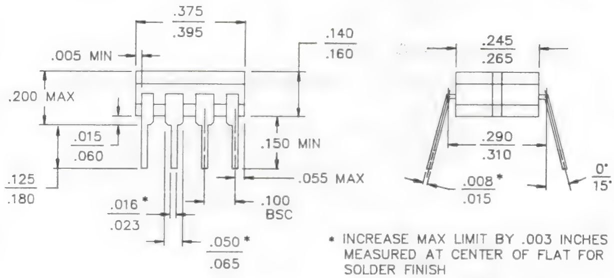
HA-5141/883



NOTE: Pad Numbers Refer to 8 Pin Ceramic Mini-DIP or Metal Can Package Pinouts Only.

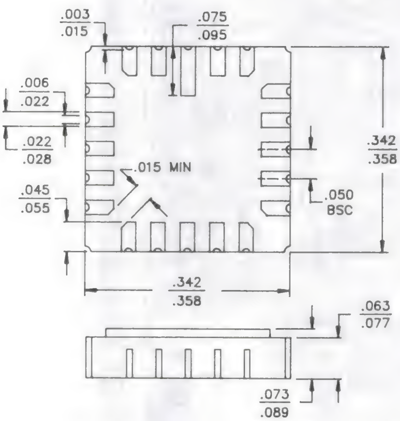
Packaging †

8 PIN CERAMIC DIP



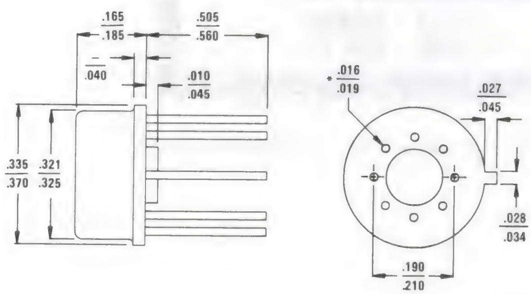
LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-4

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Ceramic, 90% Al_2O_3
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

8 PIN TO-99 METAL CAN



LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
Material: No Seal Material
Temperature: Room Temperature
Method: Resistance Weld
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic Bonded
COMPLIANT OUTLINE: 38510 A-1

*Dimension Maximum Limits Are Increased by 0.003 inches for Solder Dip Finish

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

HA-5141

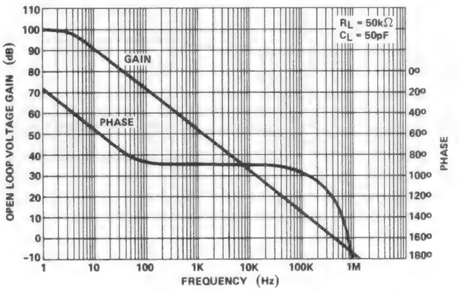
DESIGN INFORMATION

Single, Ultra-Low Power Operational Amplifier

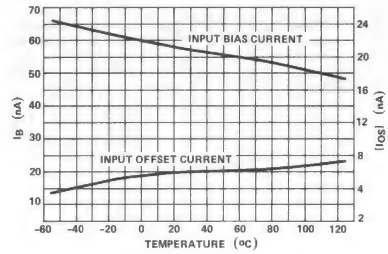
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

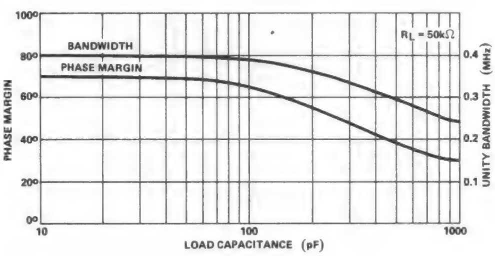
OPEN LOOP FREQUENCY RESPONSE



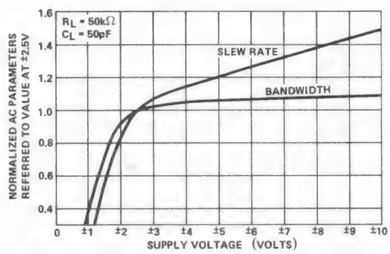
INPUT OFFSET CURRENT AND BIAS CURRENT vs. TEMPERATURE



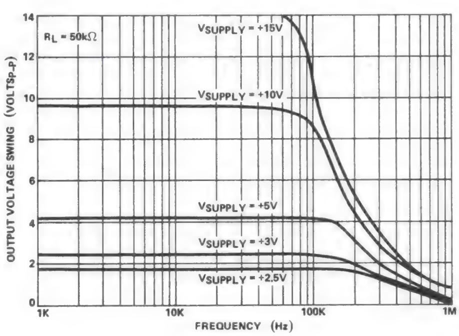
BANDWIDTH AND PHASE MARGIN vs. LOAD CAPACITANCE



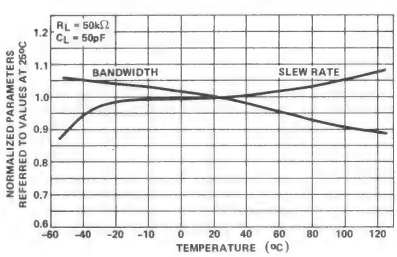
NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING vs. FREQUENCY AND SINGLE SUPPLY VOLTAGE



NORMALIZED AC PARAMETERS vs. TEMPERATURE

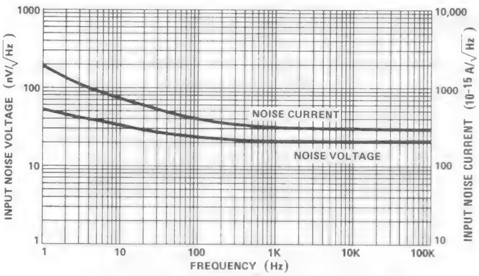


DESIGN INFORMATION (Continued)

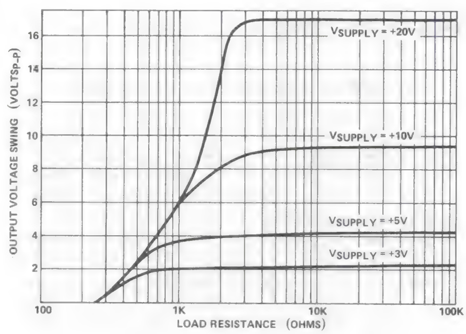
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

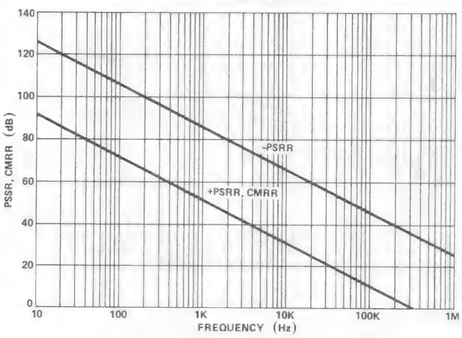
INPUT NOISE vs. FREQUENCY



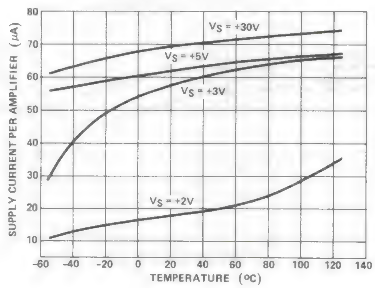
MAXIMUM OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE AND SINGLE SUPPLY VOLTAGE



PSRR AND CMRR vs. FREQUENCY



POWER SUPPLY CURRENT vs. TEMPERATURE AND SINGLE SUPPLY VOLTAGE

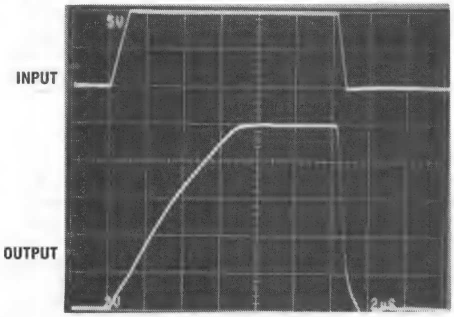


DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

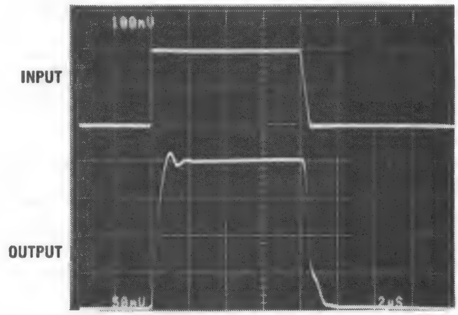
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

MEASURED LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 5V/Div.; Output = 2V/Div.)
Horizontal Scale: (Time: 2µs/Div.)



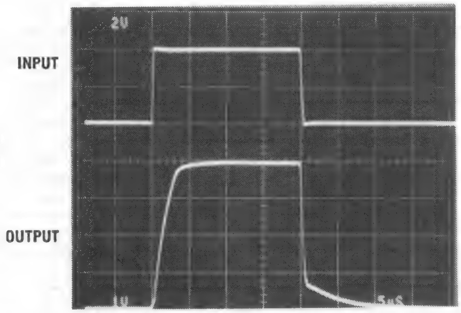
$+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$

MEASURED SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 100mV/Div.; Output = 50mV/Div.)
Horizontal Scale: (Time: 2µs/Div.)



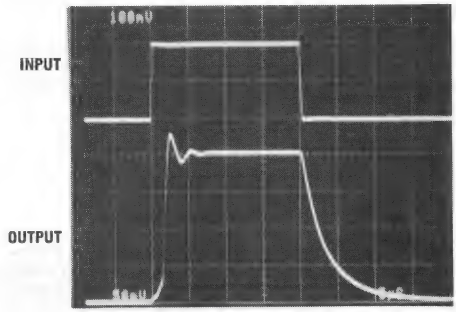
$+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$

MEASURED LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 2V/Div.; Output = 1V/Div.)
Horizontal Scale: (Time: 5µs/Div.)



$+V_{SUPPLY} = +5V$, $-V_{SUPPLY} = 0V$

MEASURED SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 100mV/Div.; Output = 50mV/Div.)
Horizontal Scale: (Time: 5µs/Div.)



$+V_{SUPPLY} = +5V$, $-V_{SUPPLY} = 0V$

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = 0V, 5 to ±15V, R_L = 50kΩ, C_L = 50pF, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage	V_{CM} = 0V	Full	0.5	Table 1	mV
Offset Voltage Drift	Versus Temperature	Full	3	6	μV/°C
Bias Current	V_{CM} = 0V	+25°C, +125°C	50	Table 1	nA
		-55°C	75	Table 1	nA
Offset Current	V_{CM} = 0V	Full	5	Table 1	nA
Differential Input Resistance		+25°C	0.6	0.4	MΩ
Input Noise Voltage	f_O = 10Hz	+25°C	40	80	$nV/\sqrt{Hz}$
	f_O = 100Hz	+25°C	30	60	$nV/\sqrt{Hz}$
	f_O = 1kHz	+25°C	20	40	$nV/\sqrt{Hz}$
Input Noise Current	f_O = 10Hz	+25°C	0.7	1	$pA/\sqrt{Hz}$
	f_O = 100Hz	+25°C	0.25	0.8	$pA/\sqrt{Hz}$
	f_O = 1kHz	+25°C	0.2	0.5	$pA/\sqrt{Hz}$
Large Signal Voltage Gain	R_L = 50kΩ	+25°C, +125°C	75K	Table 1	V/V
		-55°C	30K	Table 1	V/V
CMRR		Full	105	Table 1	dB
PSRR		Full	100	Table 1	dB
Unity Gain Bandwidth	f @ -3dB	+25°C	400	300	kHz
+ Slew Rate	V_S = 0V, 5V	-55°C	1	0.6	V/μs
	V_S = 0V, 5V to ±15V	+25°C, +125°C	1.5	0.8	V/μs
- Slew Rate	V_S = 0V, 5V to ±15V	Full	15	0.8	V/μs
+ I_{OUT}		+25°C, +125°C	2	0.4	mA
		-55°C	0.8	0.4	mA
- I_{OUT}		-55°C, +25°C	-7.5	-6	mA
		+125°C	-4.5	-3.5	mA
Rise Time	V_S = ±15V, V_O = 200mV	Full	0.8	1.5	μs
Fall Time	V_S = ±15V, V_O = -200mV	Full	0.9	1.5	μs
Overshoot	V_S = ±15V, V_O = ±200mV	Full	5	10	%
Supply Current	V_S = 0V, 5V	+25°C	64	Table 1	μA
	V_S = ±15V	+25°C	70	Table 1	μA

HARRIS

HA-5142/883

Dual, Ultra-Low Power Operational Amplifier

January 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low Supply Current @ V_S = +5V . . (+25°C) 160μA (Max) (Full) 200μA (Max)
- Wide Supply Voltage Range . . . . Single 3V to 30V or Dual ±1.5 to ±15V
- High Slew Rate . . . . +S.R. 0.8V/μs (Min) 1.5V/μs (Typ)
- High Gain . . . . 20kV/V (Min) 75kV/V (Typ)
- Low Noise (1kHz) . . . . 20nV/$\sqrt{Hz}$ (Typ)
- 100% Tested at ±15V and 0V, +5V Power Supplies
- Unity Gain Stable
- Dielectric Isolation

Applications

- Portable Instruments
- Meter Amplifiers
- Telephone Headsets
- Microphone Amplifiers
- Instrumentation
- For Further Design Ideas See App. Note 544

Description

The HA-5142/883 dual, ultra-low power operational amplifier provide AC and DC performance characteristics similar to, or better than most general purpose amplifiers while only drawing 1/30 of the supply current of most general purpose amplifiers. This amplifier is well suited to applications which require low power dissipation and good electrical characteristics.

The HA-5142/883 provides accurate signal processing by virtue of their low input offset voltage (6mV), low input bias current (100nA), high open loop gain (20kV/V) and low noise (20nV/$\sqrt{Hz}$). These characteristics coupled with a 1.5V/μs slew rate and a 24kHz bandwidth make the HA-5142/883 ideal for use in low power instrumentation, audio amplifier and active filter designs. The wide range of supply voltages (3V to 30V) also allow these amplifier and active filter designs. The wide range of supply voltages (3V to 30V) also allow these amplifiers to be very useful in low voltage battery powered equipment.

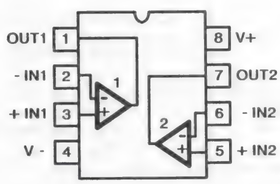
The HA-5142/883 offers tested specifications at both single ended levels (0V, +5V) and dual supplies (±15V). Packaging is offered in the Ceramic Mini-DIP, 20 pad Ceramic LCC or 8 pin (TO-99) Metal Can, and operation is specified at the full military -55°C to +125°C temperature range.

3

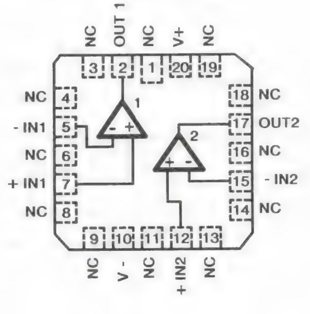
OP AMPs & COMPARATORS

Pinouts

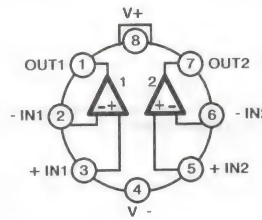
HA7-5142/883 (CERAMIC MINI-DIP)
TOP VIEW



HA4-5142/883 (CERAMIC LCC)
TOP VIEW



HA2-5142/883 (METAL CAN)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage 7V
Voltage at Either Input Terminal .... V+ to V-
Output Current .... Full Short Circuit Protection
Output Current Duration .... Indefinite, One Amplifier Shorted to Ground
Junction Temperature (T_J) .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... <2000V
Lead Temperature (Soldering 10 sec) .... +275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	82°C/W	26°C/W
Ceramic LCC Package	74°C/W	20°C/W
Metal Can Package	111°C/W	33°C/W

Package Power Dissipation Limit at +75°C For $T_J \leq$ +175°C
Ceramic DIP Package 1.22W
Ceramic LCC Package 1.35W
Metal Can Package 670mW
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 12.2mW/°C
Ceramic LCC Package .... 13.5mW/°C
Metal Can Package .... 6.7mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±1.5V to ±15V or 3V to 30V
$V_{INcm} \leq 1/2$ (V+ - V-)
$R_L \geq 50k\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $R_{SOURCE} = 100\Omega$, $R_{LOAD} = 500k\Omega$, V_{OUT} = 0V, Unless Otherwise Specified.
Subscript 1 Refers to Supply Voltages ($\pm V_S$) = ±15V, Subscript 2 Refers to $+V_S$ = 5.0V, $-V_S$ = 0.0V.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO1}	V_{CM} = 0V	1	+25°C	-6	6	mV
			2, 3	+125°C, -55°C	-8	8	mV
	V_{IO2}	V_{CM} = 0V V_{OUT} = 1.4V	1	+25°C	-6	6	mV
			2, 3	+125°C, -55°C	-8	8	mV
Input Bias Current	$+I_{B1}$	V_{CM} = 0V $+R_S = 10k\Omega$ $-R_S = 100\Omega$	1	+25°C	-100	100	nA
			2, 3	+125°C, -55°C	-125	125	nA
	$-I_{B1}$	V_{CM} = 0V $+R_S = 100\Omega$ $-R_S = 10k\Omega$	1	+25°C	-100	100	nA
			2, 3	+125°C, -55°C	-125	125	nA
	$+I_{B2}$	V_{CM} = 0V, V_{OUT} = 1.4V $+R_S = 10k\Omega$ $-R_S = 100\Omega$	1	+25°C	-100	100	nA
			2, 3	+125°C, -55°C	-125	125	nA
	$-I_{B2}$	V_{CM} = 0V, V_{OUT} = 1.4V $+R_S = 100\Omega$ $-R_S = 10k\Omega$	1	+25°C	-100	100	nA
			2, 3	+125°C, -55°C	-125	125	nA
Input Offset Current	I_{IO1}	V_{CM} = 0V $+R_S = 10k\Omega$ $-R_S = 10k\Omega$	1	+25°C	-10	10	nA
			2, 3	+125°C, -55°C	-20	20	nA
	I_{IO2}	V_{CM} = 0V, V_{OUT} = 1.4V $+R_S = 10k\Omega$ $-R_S = 10k\Omega$	1	+25°C	-10	10	nA
			2, 3	+125°C, -55°C	-20	20	nA
Common Mode Range	$+CMR_1$	V+ = 5V V- = -25V	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	$-CMR_1$	V+ = 25V V- = -5V	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
	$+CMR_2$	V+ = 5V to 2V V- = 0V to -3V V_{OUT} = 1.4V to -1.6V	1	+25°C	0 to 3	-	V
			2, 3	+125°C, -55°C	0 to 3	-	V

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.
Subscript 1 Refers to Supply Voltages ($\pm V_S$) = ±15V; Subscript 2 Refers to $+V_S$ = 5.0V, $-V_S$ = 0.0V.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Large Signal Voltae Gain	$+A_{VOL1}$	V_{OUT} = 0V and 10V R_L = 50kΩ	4	+25°C	20	-	kV/V
			5, 6	+125°C, -55°C	15	-	kV/V
	$-A_{VOL1}$	V_{OUT} = 0V and -10V R_L = 50kΩ	4	+25°C	20	-	kV/V
			5, 6	+125°C, -55°C	15	-	kV/V
	$+A_{VOL2}$	V_{OUT} = 1.4V and 2.5V R_L = 50kΩ	4	+25°C	20	-	kV/V
			5, 6	+125°C, -55°C	15	-	kV/V
Common Mode Rejection Ratio	$+CMRR_1$	ΔV_{CM} = 10V +V = 5V -V = -25V V_{OUT} = -10V	1	+25°C	77	-	dB
			2, 3	+125°C, -55°C	77	-	dB
	$-CMRR_1$	ΔV_{CM} = 10V +V = 25V -V = -5V V_{OUT} = 10V	1	+25°C	77	-	dB
			2, 3	+125°C, -55°C	77	-	dB
	$+CMRR_2$	ΔV_{CM} = 0V to 3V +V = 2V -V = -3V V_{OUT} = -3V	1	+25°C	77	-	dB
			2, 3	+125°C, -55°C	77	-	dB
Output Voltage Swing	$+V_{OUT1}$	R_L = 50kΩ	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	$-V_{OUT1}$	R_L = 50kΩ	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
	$+V_{OUT2}$	R_L = 50kΩ Terminated at 2.5V	1	+25°C	3.8	-	V
			2, 3	+125°C, -55°C	3.5	-	V
	$-V_{OUT2}$	R_L = 50kΩ Terminated at 2.5V	1	+25°C	-	1	V
			2, 3	+125°C, -55°C	-	1.2	V
Quiescent Power Supply Current (Both Amplifiers)	$+I_{CC1}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-	300	μA
			2, 3	+125°C, -55°C	-	400	μA
	$-I_{CC1}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-300	-	μA
			2, 3	+125°C, -55°C	-400	-	μA
	$+I_{CC2}$	V_{OUT} = 1.4V I_{OUT} = 0mA	1	+25°C	-	160	μA
			2, 3	+125°C, -55°C	-	200	μA
Power Supply Rejection Ratio	$+PSRR_1$	ΔV_{SUP} = 10V +V = 10V, -V = -15V +V = 20V, -V = -15V	1	+25°C	77	-	dB
			2, 3	+125°C, -55°C	77	-	dB
	$-PSRR_1$	ΔV_{SUP} = 10V +V = 15V, -V = -10V +V = 15V, -V = -20V	1	+25°C	77	-	dB
			2, 3	+125°C, -55°C	77	-	dB
	$+PSRR_2$	ΔV_{SUP} = 10V +V = 5V, -V = 0V +V = 15V, -V = 0V	1	+25°C	77	-	dB
			2, 3	+125°C, -55°C	77	-	dB
Channel Separation	±CS	R_L = 50kΩ	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: R_{SOURCE} = 50Ω, R_{LOAD} = 50kΩ, C_{LOAD} = 50pF, V_{OUT} = 0V, Unless Otherwise Specified.
Subscript 1 Refers to Supply Voltages (±V_S) = ±15V; Subscript 2 Refers to +V_S = 5.0V, -V_S = 0.0V.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Slew Rate	$+SR_1$	V_{OUT} = -3V to 3V V_{IN} S.R. ≤ 10V/µs @ A_V = 1	4	+25°C	0.8	-	V/µs
	$-SR_1$	V_{OUT} = 3V to -3V V_{IN} S.R. ≤ 10V/µs @ A_V = 1	4	+25°C	0.8	-	V/µs
	$+SR_2$	V_{OUT} = 0V to 3V V_{IN} S.R. ≤ 10V/µs @ A_V = 1	4	+25°C	0.8	-	V/µs
	$-SR_2$	V_{OUT} = 3V to 0V V_{IN} S.R. ≤ 10V/µs @ A_V = 1	4	+25°C	0.8	-	V/µs

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: R_{SOURCE} = 50Ω, R_{LOAD} = 50kΩ, C_{LOAD} = 50pF, A_V = 1V/V, Unless Otherwise Specified.
Subscript 1 Refers to Supply Voltages (±V_S) = ±15V; Subscript 2 Refers to +V_S = 5.0V, -V_S = 0.0V.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Full Power Bandwidth	$FPBW_1$	V_{PEAK} = 10V	1, 2	+25°C	12.7	-	kHz
	$FPBW_2$	V_{PEAK} = 1.1V V_{Ref} = 2.5V	1, 2	+25°C	115.8	-	kHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 50kΩ, C_L = 50pF	1	-55°C to +125°C	1	-	V/V
Quiecent Power Consumption	PC_1	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	12	mW
	PC_2	V_{OUT} = 1.4V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	1	mW

NOTES: 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).

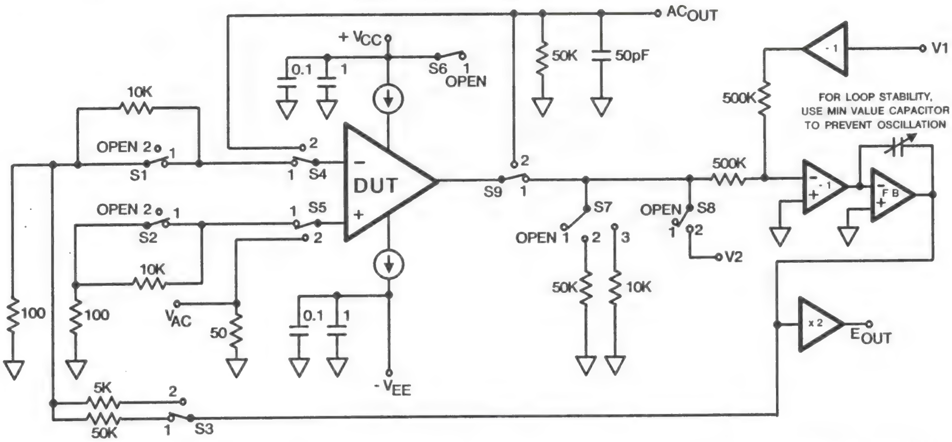
3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6
Group A Test Requirements	1, 2, 3, 4, 5, 6
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

Test Circuit (Applies to Tables 1 and 2)



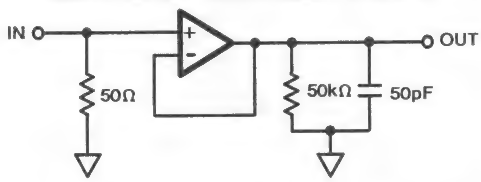
ONE OF TWO TEST LOOPS FOR THE HA - 5142/ 883

ALL RESISTORS = ± 1% (Ω)
ALL CAPACITORS = ± 10% (μF)

For Detailed Information, Refer to HA-5142/883 Test Tech Brief

Test Waveforms

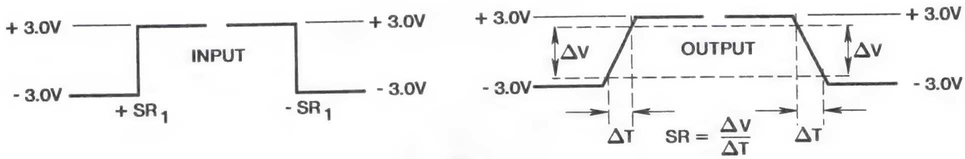
SIMPLIFIED TEST CIRCUIT (Applies to Table 2)



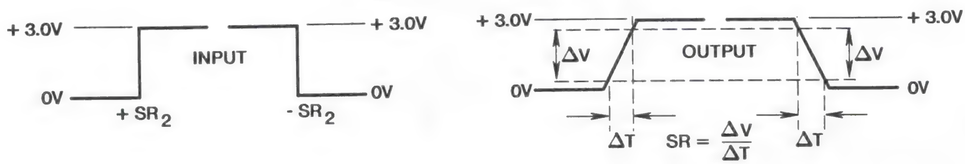
NOTE: $\pm V_{SUPPLY}$ ($\pm V_S$) Tested with ±15V and 0V, +5V. V_{IN} Slew Rate Maintained with Less Than 10V/μs Input for Voltage Follower Configuration.

SLEW RATE WAVEFORMS, A_V = 1V/V

$\pm V_{SUPPLY} = \pm 15V$

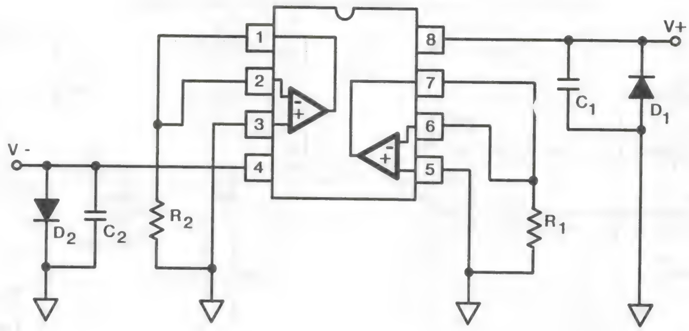


$+V_{SUPPLY}$ = 5V, $-V_{SUPPLY}$ = 0V

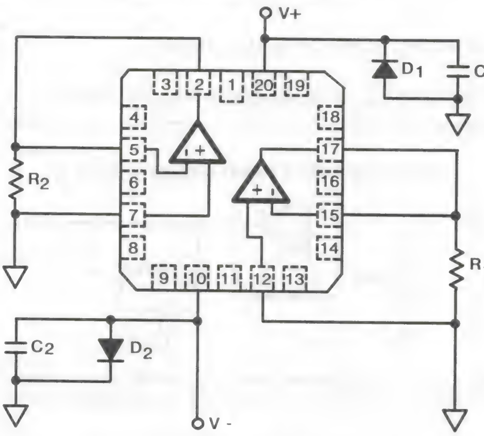


Burn-In Circuits

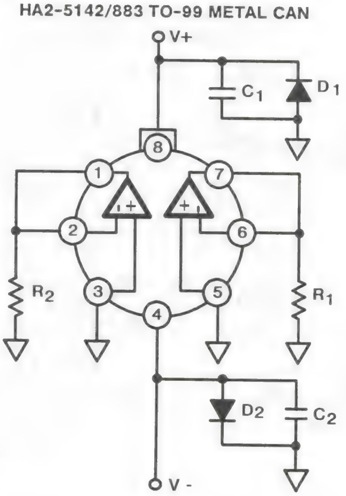
HA7-5142/883 CERAMIC DIP



HA4-5142/883 CERAMIC LCC



HA2-5142/883 TO-99 METAL CAN



NOTES:

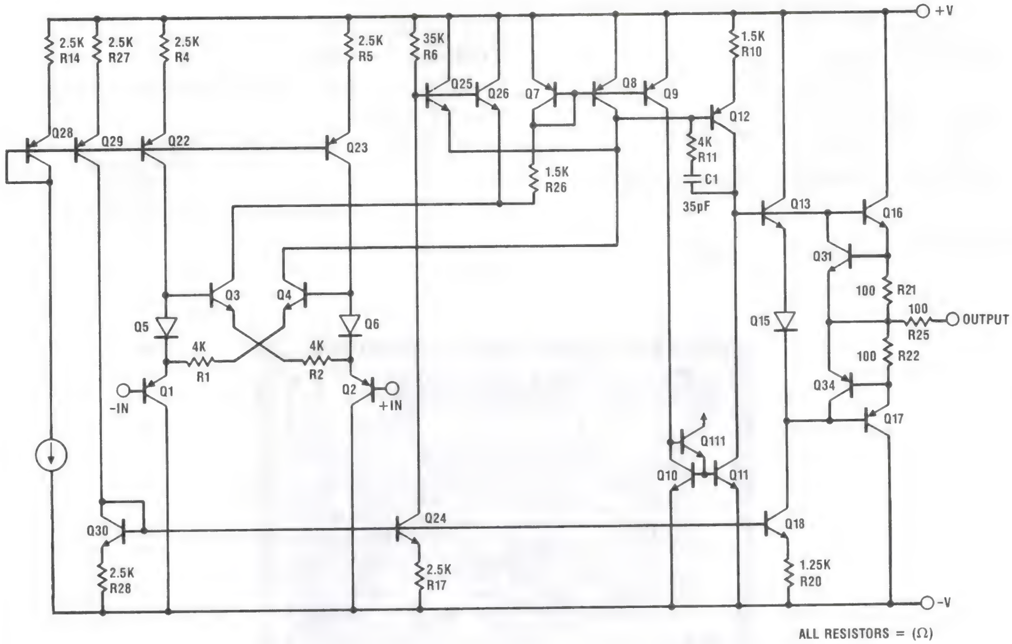
$R_1 = R_2 = 2k\Omega$, ±5%, 1/4W (Min)

$C_1 = C_2 = 0.01\mu F$/Socket (Min) or $0.1\mu F$/Row, (Min)

$D_1 = D_2$ = IN4002 or Equivalent/Board

$|(V+) - (V-)| = 30V$

Schematic Diagram (1/2 Of HA-5142/883)



Die Characteristics

DIE DIMENSIONS:
53.9 x 103.1 x 19 mils
(1370 x 2620 x 483 µm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$0.6 \times 10^5 A/cm^2$ @ 2.5mA

SUBSTRATE POTENTIAL (Powered Up): V-

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

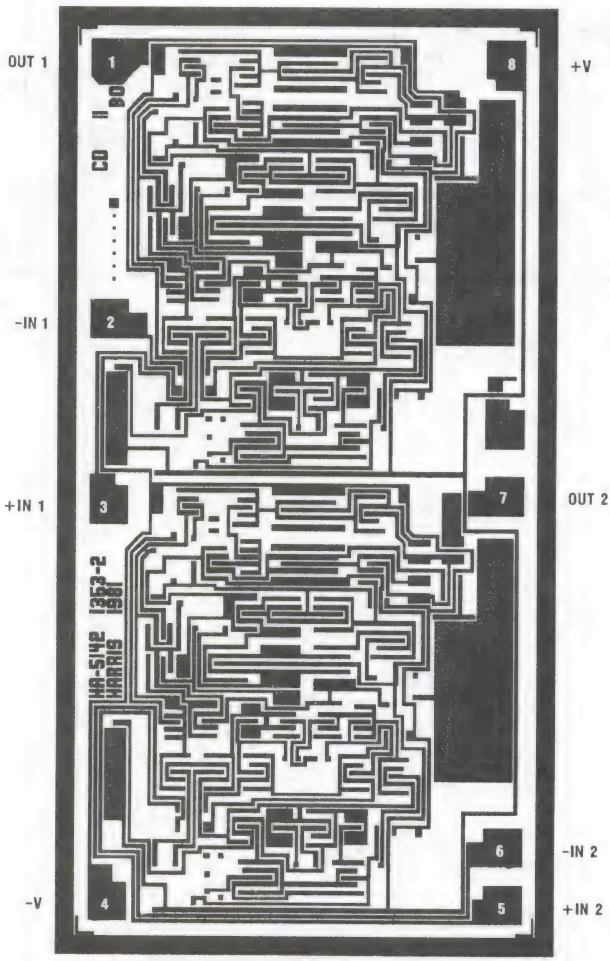
TRANSISTOR COUNT: 72

PROCESS: HFSB Bipolar/JFET Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)
Metal Can — 420°C (Max)

Metallization Mask Layout

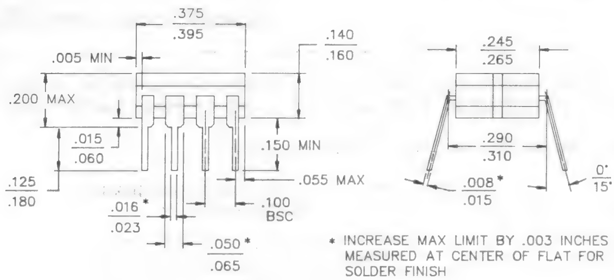
HA-5142/883



NOTE: Pad Numbers Refer to 8 Pin Ceramic Mini-DIP or Metal Can Package Pinouts Only.

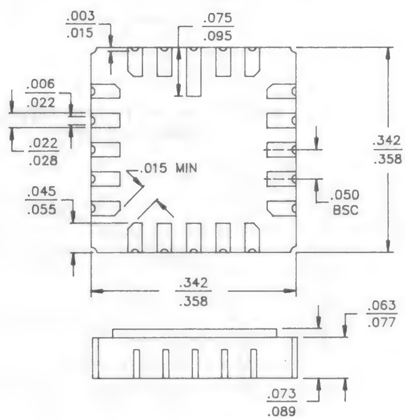
Packaging †

8 PIN CERAMIC DIP



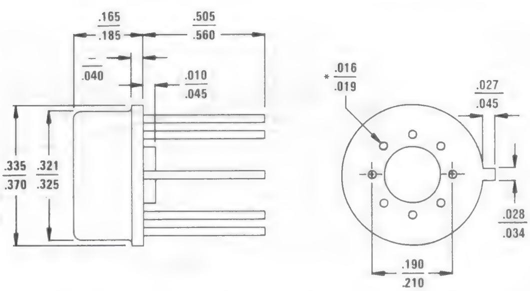
LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-4

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Ceramic, 90% Al_2O_3
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

8 PIN TO-99 METAL CAN



LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
Material: No Seal Material
Temperature: Room Temperature
Method: Resistance Weld
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic Bonded
COMPLIANT OUTLINE: 38510 A-1

*Dimension Maximum Limits Are Increased by 0.003 inches for Solder Dip Finish

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

HA-5142

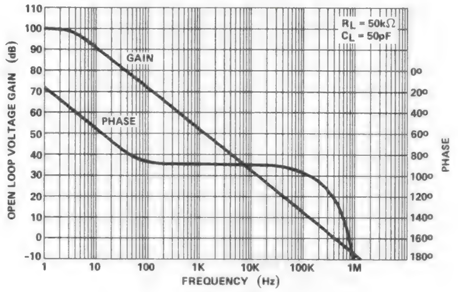
DESIGN INFORMATION

Dual, Ultra-Low Power Operational Amplifier

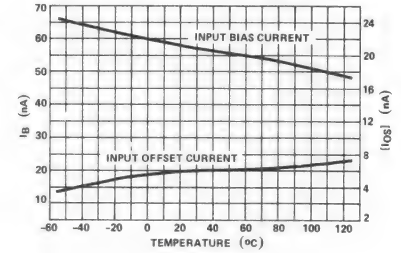
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

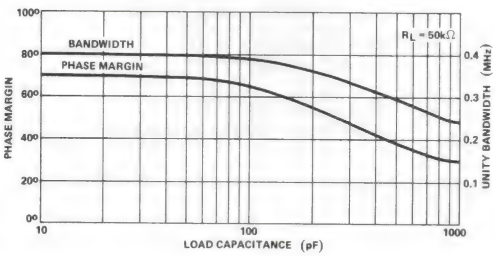
OPEN LOOP FREQUENCY RESPONSE



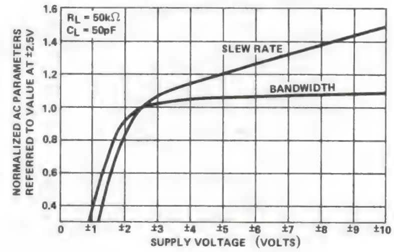
INPUT OFFSET CURRENT AND BIAS CURRENT vs. TEMPERATURE



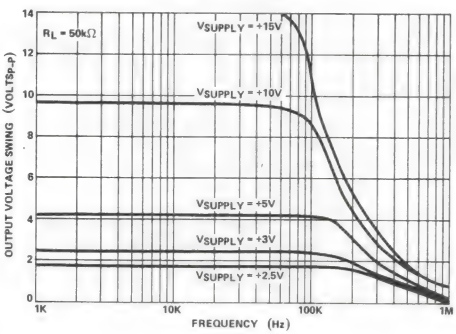
BANDWIDTH AND PHASE MARGIN vs. LOAD CAPACITANCE



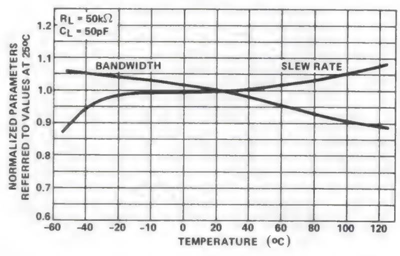
NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING vs. FREQUENCY AND SINGLE SUPPLY VOLTAGE



NORMALIZED AC PARAMETERS vs. TEMPERATURE

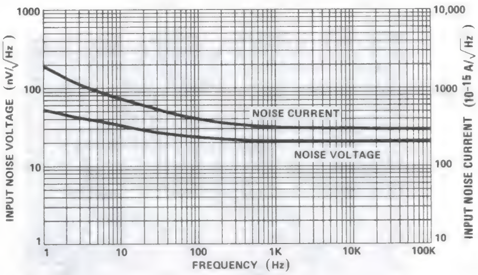


DESIGN INFORMATION (Continued)

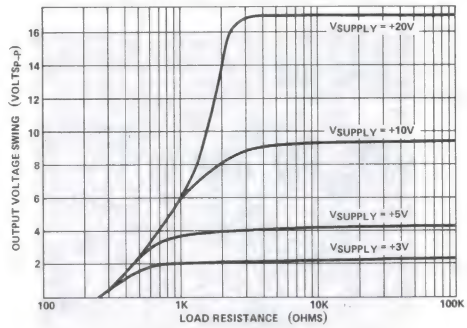
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

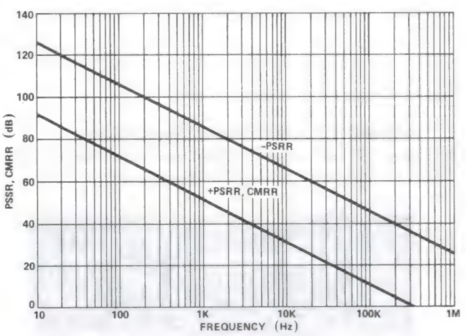
INPUT NOISE vs. FREQUENCY



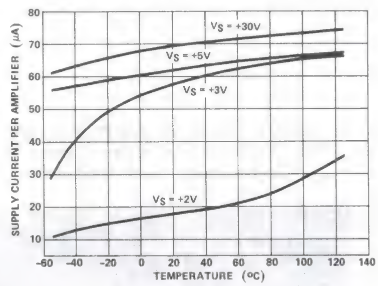
MAXIMUM OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE AND SINGLE SUPPLY VOLTAGE



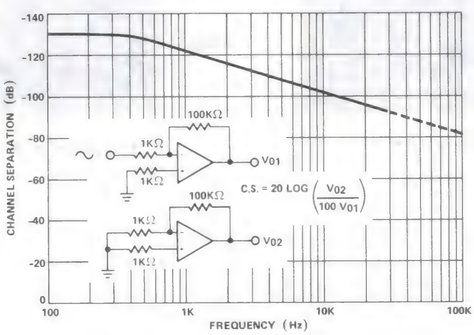
PSRR AND CMRR vs. FREQUENCY



POWER SUPPLY CURRENT vs. TEMPERATURE AND SINGLE SUPPLY VOLTAGE



CHANNEL SEPARATION vs. FREQUENCY



DESIGN INFORMATION (Continued)

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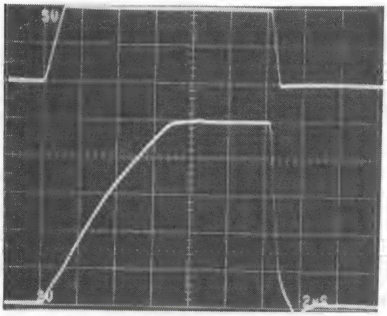
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

MEASURED LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 5V/Div.; Output = 2V/Div.)
Horizontal Scale: (Time: 2μs/Div.)

INPUT

OUTPUT

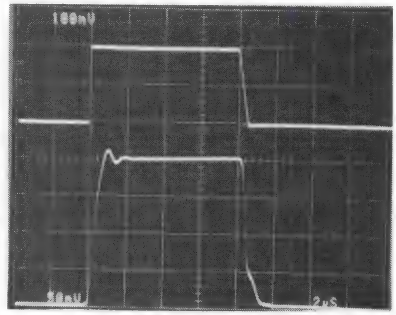


$+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$

MEASURED SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 100mV/Div.; Output = 50mV/Div.)
Horizontal Scale: (Time: 2μs/Div.)

INPUT

OUTPUT

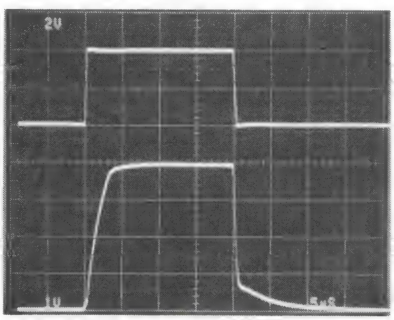


$+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$

MEASURED LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 2V/Div.; Output = 1V/Div.)
Horizontal Scale: (Time: 5μs/Div.)

INPUT

OUTPUT

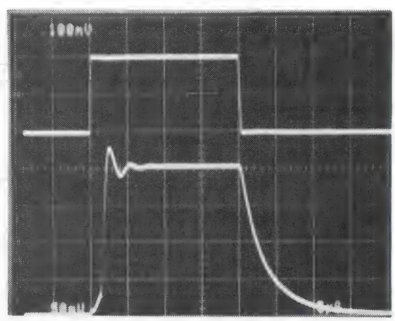


$+V_{SUPPLY} = +5V$, $-V_{SUPPLY} = 0V$

MEASURED SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 100mV/Div.; Output = 50mV/Div.)
Horizontal Scale: (Time: 5μs/Div.)

INPUT

OUTPUT



$+V_{SUPPLY} = +5V$, $-V_{SUPPLY} = 0V$

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = 0V, 5 to ±15V, R_L = 50kΩ, C_L = 50pF, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage	V_{CM} = 0V	Full	0.5	Table 1	mV
Offset Voltage Drift	Versus Temperature	Full	3	6	μV/°C
Bias Current	V_{CM} = 0V	+25°C, +125°C	50	Table 1	nA
		-55°C	75	Table 1	nA
Offset Current	V_{CM} = 0V	Full	5	Table 1	nA
Differential Input Resistance		+25°C	0.6	0.4	MΩ
Input Noise Voltage	f_O = 10Hz	+25°C	40	80	$nV/\sqrt{Hz}$
	f_O = 100Hz	+25°C	30	60	$nV/\sqrt{Hz}$
	f_O = 1kHz	+25°C	20	40	$nV/\sqrt{Hz}$
Input Noise Current	f_O = 10Hz	+25°C	0.7	1	$pA/\sqrt{Hz}$
	f_O = 100Hz	+25°C	0.25	0.8	$pA/\sqrt{Hz}$
	f_O = 1kHz	+25°C	0.2	0.5	$pA/\sqrt{Hz}$
Large Signal Voltage Gain	R_L = 50kΩ	+25°C, +125°C	75K	Table 1	V/V
		-55°C	30K	Table 1	V/V
CMRR		Full	105	Table 1	dB
PSRR		Full	100	Table 1	dB
Unity Gain Bandwidth	f @ -3dB	+25°C	400	300	kHz
+ Slew Rate	V_S = 0V, 5V	-55°C	1	0.6	V/μs
	V_S = 0V, 5V to ±15V	+25°C, +125°C	1.5	0.8	V/μs
- Slew Rate	V_S = 0V, 5V to ±15V	Full	15	0.8	V/μs
+ I_{OUT}		+25°C, +125°C	2	0.4	mA
		-55°C	0.8	0.4	mA
- I_{OUT}		-55°C, +25°C	-7.5	-6	mA
		+125°C	-4.5	-3.5	mA
Rise Time	V_S = ±15V, V_O = 200mV	Full	0.8	1.5	μs
Fall Time	V_S = ±15V, V_O = -200mV	Full	0.9	1.5	μs
Overshoot	V_S = ±15V, V_O = ±200mV	Full	5	10	%
Supply Current (Both Amplifiers)	V_S = 0V, 5V	+25°C	124	Table 1	μA
	V_S = ±15V	+25°C	140	Table 1	μA

HARRIS

HA-5144/883

Quad, Ultra-Low Power Operational Amplifier

January 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low Supply Current @ V_S = +5V . . (+25°C) 320μA (Max) (Full) 400μA (Max)
- Wide Supply Voltage Range . . . . Single 3V to 30V or Dual ±1.5 to ±15V
- High Slew Rate . . . . +S.R. 0.8V/μs (Min) 1.5V/μs (Typ)
- High Gain . . . . 20kV/V (Min) 75kV/V (Typ)
- Low Noise (1kHz) . . . . 20nV/$\sqrt{Hz}$ (Typ)
- 100% Tested at ±15V and 0V, +5V Power Supplies
- Unity Gain Stable
- Dielectric Isolation

Applications

- Portable Instruments
- Meter Amplifiers
- Telephone Headsets
- Microphone Amplifiers
- Instrumentation
- For Further Design Ideas See App. Note 544

Description

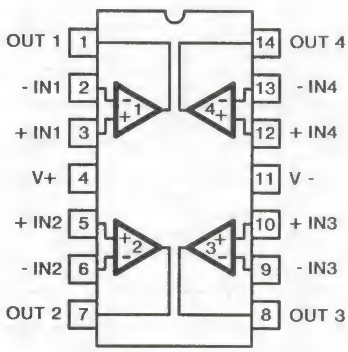
The HA-5144/883 quad, ultra-low power operational amplifier provide AC and DC performance characteristics similar to, or better than most general purpose amplifiers while only drawing 1/30 of the supply current of most general purpose amplifiers. This amplifier is well suited to applications which require low power dissipation and good electrical characteristics.

The HA-5144/883 provides accurate signal processing by virtue of their low input offset voltage (6mV), low input bias current (100nA), high open loop gain (20kV/V) and low noise (20nV/$\sqrt{Hz}$). These characteristics coupled with a 1.5V/μs slew rate and a 24kHz bandwidth make the HA-5144/883 ideal for use in low power instrumentation, audio amplifier and active filter designs. The wide range of supply voltages (3V to 30V) also allow these amplifier and active filter designs. The wide range of supply voltages (3V to 30V) also allow these amplifiers to be very useful in low voltage battery powered equipment.

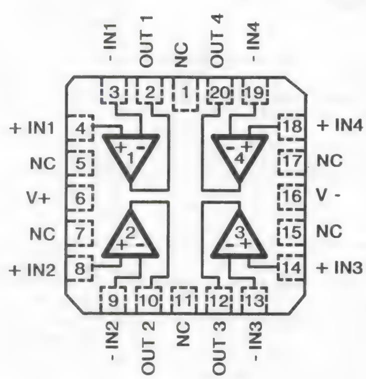
The HA-5144/883 offers tested specifications at both single ended levels (0V, +5V) and dual supplies (±15V). Packaging is offered in the 14 pin Ceramic DIP or 20 pad Ceramic LCC, and operation is specified at the full military -55°C to +125°C temperature range.

Pinouts

HA1-5144/883 (CERAMIC DIP)
TOP VIEW



HA4-5144/883 (CERAMIC LCC)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage 7V
Voltage at Either Input Terminal .... V+ to V-
Output Current .... Full Short Circuit Protection
Output Current Duration .... Indefinite, One Amplifier Shorted to Ground
Junction Temperature (T_J) .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... <2000V
Lead Temperature (Soldering 10 sec) .... +275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	75°C/W	17°C/W
Ceramic LCC Package	76°C/W	19°C/W

Package Power Dissipation Limit at +75°C For $T_J \leq$ +175°C
Ceramic DIP Package 1.33W
Ceramic LCC Package 1.32W

Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 13.3mW/°C
Ceramic LCC Package .... 13.2mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±1.5V to ±15V or 3V to 30V

$V_{INcm} \leq$ 1/2 (V+ - V-)
$R_L \geq$ 50kΩ

3

OP AMPs & COMPARATORS

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.
Subscript 1 Refers to Supply Voltages ($\pm V_S$) = ±15V, Subscript 2 Refers to $+V_S$ = 5.0V, $-V_S$ = 0.0V.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO1}	V_{CM} = 0V	1	+25°C	-6	6	mV
			2, 3	+125°C, -55°C	-8	8	mV
	V_{IO2}	V_{CM} = 0V V_{OUT} = 1.4V	1	+25°C	-6	6	mV
			2, 3	+125°C, -55°C	-8	8	mV
Input Bias Current	$+I_{B1}$	V_{CM} = 0V $+R_S$ = 10kΩ $-R_S$ = 100Ω	1	+25°C	-100	100	nA
			2, 3	+125°C, -55°C	-125	125	nA
	$-I_{B1}$	V_{CM} = 0V $+R_S$ = 100Ω $-R_S$ = 10kΩ	1	+25°C	-100	100	nA
			2, 3	+125°C, -55°C	-125	125	nA
	$+I_{B2}$	V_{CM} = 0V, V_{OUT} = 1.4V $+R_S$ = 10kΩ $-R_S$ = 100Ω	1	+25°C	-100	100	nA
			2, 3	+125°C, -55°C	-125	125	nA
	$-I_{B2}$	V_{CM} = 0V, V_{OUT} = 1.4V $+R_S$ = 100Ω $-R_S$ = 10kΩ	1	+25°C	-100	100	nA
			2, 3	+125°C, -55°C	-125	125	nA
Input Offset Current	I_{IO1}	V_{CM} = 0V $+R_S$ = 10kΩ $-R_S$ = 10kΩ	1	+25°C	-10	10	nA
			2, 3	+125°C, -55°C	-20	20	nA
	I_{IO2}	V_{CM} = 0V, V_{OUT} = 1.4V $+R_S$ = 10kΩ $-R_S$ = 10kΩ	1	+25°C	-10	10	nA
			2, 3	+125°C, -55°C	-20	20	nA
Common Mode Range	$+CMR_1$	V+ = 5V V- = -25V	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	$-CMR_1$	V+ = 25V V- = -5V	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
	$+CMR_2$	V+ = 5V to 2V V- = 0V to -3V V_{OUT} = 1.4V to -1.6V	1	+25°C	0 to 3	-	V
			2, 3	+125°C, -55°C	0 to 3	-	V

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: $R_{SOURCE} = 100\Omega$, $R_{LOAD} = 500k\Omega$, $V_{OUT} = 0V$, Unless Otherwise Specified.
Subscript 1 Refers to Supply Voltages ($\pm V_S$) = ±15V; Subscript 2 Refers to $+V_S = 5.0V$, $-V_S = 0.0V$.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Large Signal Voltae Gain	$+A_{VOL1}$	V_{OUT} = 0V and 10V $R_L = 50k\Omega$	4	+25°C	20	-	kV/V
			5, 6	+125°C, -55°C	15	-	kV/V
	$-A_{VOL1}$	V_{OUT} = 0V and -10V $R_L = 50k\Omega$	4	+25°C	20	-	kV/V
			5, 6	+125°C, -55°C	15	-	kV/V
	$+A_{VOL2}$	V_{OUT} = 1.4V and 2.5V $R_L = 50k\Omega$	4	+25°C	20	-	kV/V
			5, 6	+125°C, -55°C	15	-	kV/V
Common Mode Rejection Ratio	$+CMRR_1$	ΔV_{CM} = 10V +V = 5V -V = -25V V_{OUT} = -10V	1	+25°C	77	-	dB
			2, 3	+125°C, -55°C	77	-	dB
	$-CMRR_1$	ΔV_{CM} = 10V +V = 25V -V = -5V V_{OUT} = 10V	1	+25°C	77	-	dB
			2, 3	+125°C, -55°C	77	-	dB
	$+CMRR_2$	ΔV_{CM} = 0V to 3V +V = 2V -V = -3V V_{OUT} = -3V	1	+25°C	77	-	dB
			2, 3	+125°C, -55°C	77	-	dB
Output Voltage Swing	$+V_{OUT1}$	$R_L = 50k\Omega$	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	$-V_{OUT1}$	$R_L = 50k\Omega$	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
	$+V_{OUT2}$	$R_L = 50k\Omega$ Terminated at 2.5V	1	+25°C	3.8	-	V
			2, 3	+125°C, -55°C	3.5	-	V
	$-V_{OUT2}$	$R_L = 50k\Omega$ Terminated at 2.5V	1	+25°C	-	1	V
			2, 3	+125°C, -55°C	-	1.2	V
Quiescent Power Supply Current (All Four Amplifiers)	$+I_{CC1}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-	600	µA
			2, 3	+125°C, -55°C	-	800	µA
	$-I_{CC1}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-600	-	µA
			2, 3	+125°C, -55°C	-800	-	µA
	$+I_{CC2}$	V_{OUT} = 1.4V I_{OUT} = 0mA	1	+25°C	-	320	µA
			2, 3	+125°C, -55°C	-	400	µA
Power Supply Rejection Ratio	$+PSRR_1$	ΔV_{SUP} = 10V +V = 10V, -V = -15V +V = 20V, -V = -15V	1	+25°C	77	-	dB
			2, 3	+125°C, -55°C	77	-	dB
	$-PSRR_1$	ΔV_{SUP} = 10V +V = 15V, -V = -10V +V = 15V, -V = -20V	1	+25°C	77	-	dB
			2, 3	+125°C, -55°C	77	-	dB
	$+PSRR_2$	ΔV_{SUP} = 10V +V = 5V, -V = 0V +V = 15V, -V = 0V	1	+25°C	77	-	dB
			2, 3	+125°C, -55°C	77	-	dB
Channel Separation	±CS	$R_L = 50k\Omega$	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $R_{SOURCE} = 50\Omega$, $R_{LOAD} = 50k\Omega$, $C_{LOAD} = 50pF$, $V_{OUT} = 0V$, Unless Otherwise Specified.
Subscript 1 Refers to Supply Voltages ($\pm V_S$) = ±15V; Subscript 2 Refers to $+V_S = 5.0V$, $-V_S = 0.0V$.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Slew Rate	$+SR_1$	$V_{OUT} = -3V$ to $3V$ V_{IN} S.R. $\leq 10V/\mu s$ @ $A_V = 1$	4	+25°C	0.8	-	V/µs
	$-SR_1$	$V_{OUT} = 3V$ to $-3V$ V_{IN} S.R. $\leq 10V/\mu s$ @ $A_V = 1$	4	+25°C	0.8	-	V/µs
	$+SR_2$	$V_{OUT} = 0V$ to $3V$ V_{IN} S.R. $\leq 10V/\mu s$ @ $A_V = 1$	4	+25°C	0.8	-	V/µs
	$-SR_2$	$V_{OUT} = 3V$ to $0V$ V_{IN} S.R. $\leq 10V/\mu s$ @ $A_V = 1$	4	+25°C	0.8	-	V/µs

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $R_{SOURCE} = 50\Omega$, $R_{LOAD} = 50k\Omega$, $C_{LOAD} = 50pF$, $A_V = 1V/V$, Unless Otherwise Specified.
Subscript 1 Refers to Supply Voltages ($\pm V_S$) = ±15V; Subscript 2 Refers to $+V_S = 5.0V$, $-V_S = 0.0V$.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Full Power Bandwidth	$FPBW_1$	$V_{PEAK} = 10V$	1, 2	+25°C	12.7	-	kHz
	$FPBW_2$	$V_{PEAK} = 1.1V$ $V_{Ref} = 2.5V$	1, 2	+25°C	115.8	-	kHz
Minimum Closed Loop Stable Gain	CLSG	$R_L = 50k\Omega$, $C_L = 50pF$	1	-55°C to +125°C	1	-	V/V
Quiecent Power Consumption	PC_1	$V_{OUT} = 0V$, $I_{OUT} = 0mA$	1, 3	-55°C to +125°C	-	24	mW
	PC_2	$V_{OUT} = 1.4V$, $I_{OUT} = 0mA$	1, 3	-55°C to +125°C	-	2	mW

NOTES: 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).

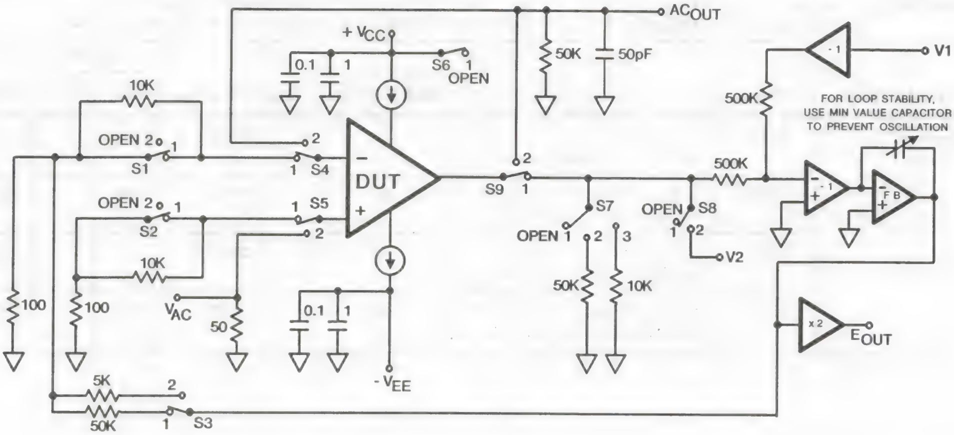
3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6
Group A Test Requirements	1, 2, 3, 4, 5, 6
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

Test Circuit (Applies to Tables 1 and 2)



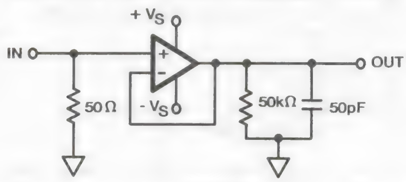
ONE OF FOUR TEST LOOPS FOR THE HA - 5144/ 883

ALL RESISTORS = ± 1% (Ω)
ALL CAPACITORS = ± 10% (μF)

For Detailed Information, Refer to HA-5144/883 Test Tech Brief

Test Waveforms

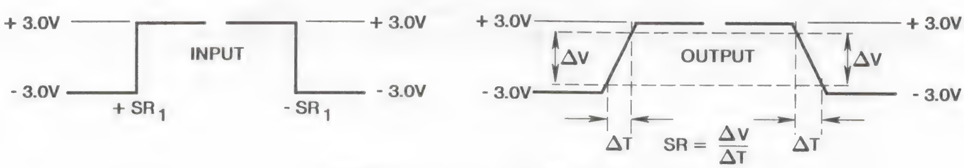
SIMPLIFIED TEST CIRCUIT (Applies to Table 2)



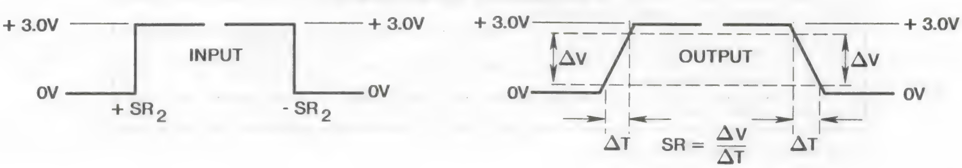
NOTE: $\pm V_{SUPPLY}$ ($\pm V_S$) Tested with ±15V and 0V, +5V. V_{IN} Slew Rate Maintained with Less Than 10V/μs Input for Voltage Follower Configuration.

SLEW RATE WAVEFORMS, A_V = 1V/V

$\pm V_{SUPPLY} = \pm 15V$

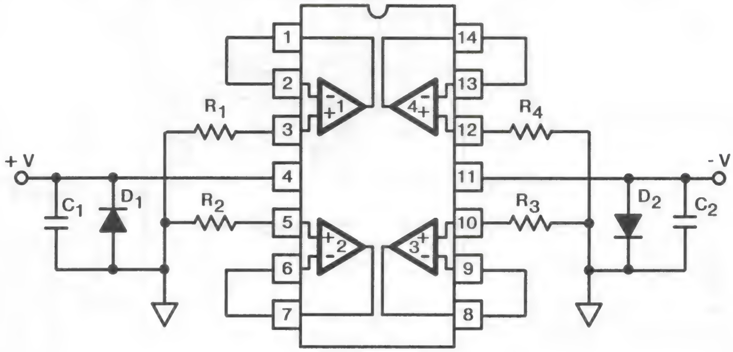


$+V_{SUPPLY} = 5V$, $-V_{SUPPLY} = 0V$

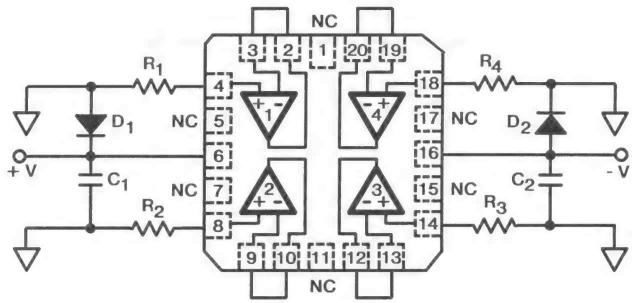


Burn-In Circuits

HA1-5144/883 CERAMIC DIP



HA4-5144/883 CERAMIC LCC



NOTES:

$R_1 = R_2 = R_3 = R_4 = 1M\Omega$, ±5%, 1/4W (Min)

$C_1 = C_2 = 0.01\mu F$/Socket (Min) or $0.1\mu F$/Row, (Min)

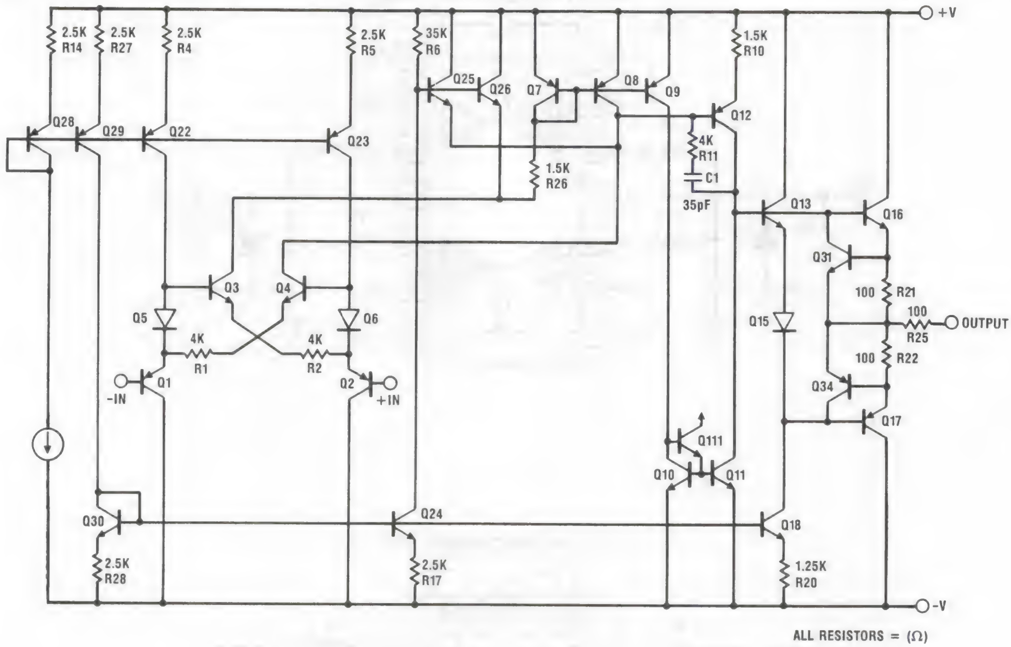
$D_1 = D_2$ = IN4002 or Equivalent/Board

$|(V+) - (V-)| = 30V$

3

OP AMPs & COMPARATORS

Schematic Diagram (1/4 Of HA-5144/883)



Die Characteristics

DIE DIMENSIONS:
95.7 x 101.6 x 19 mils
(2430 x 2580 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$0.45 \times 10^5 A/cm^2$ @ 2.5mA

SUBSTRATE POTENTIAL (Powered Up): V-

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

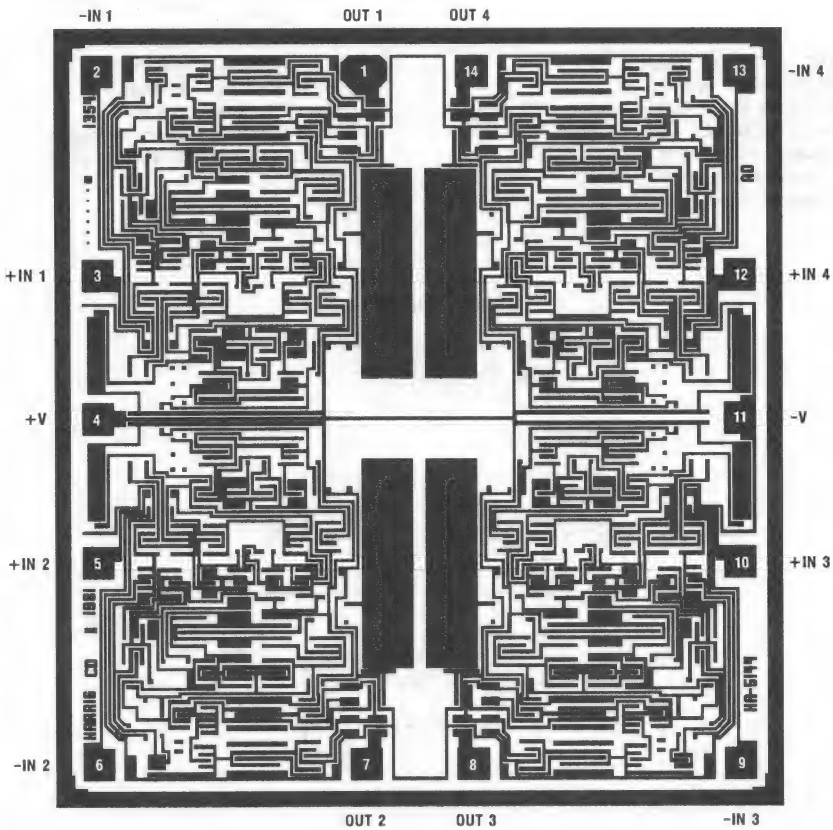
TRANSISTOR COUNT: 144

PROCESS: HFSB Bipolar/JFET Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

Metallization Mask Layout

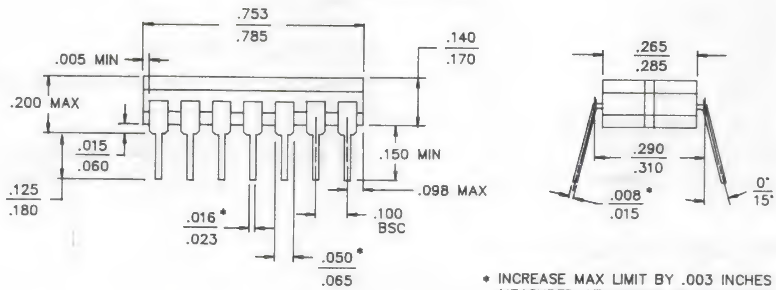
HA-5144/883



NOTE: Pad Numbers Refer to 14 Pin Ceramic DIP Package Pinout Only.

Packaging†

14 PIN CERAMIC DIP

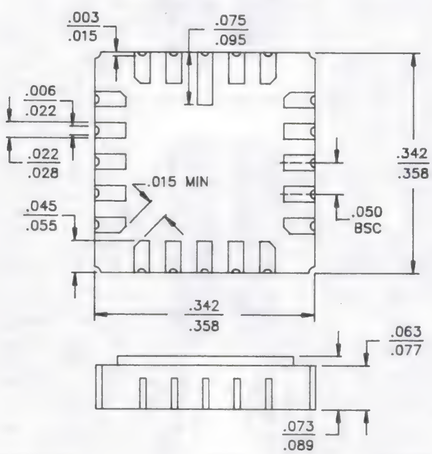


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-1

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

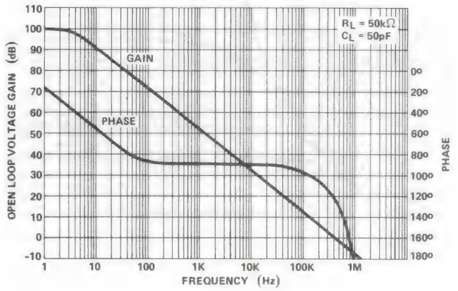
DESIGN INFORMATION

Quad, Ultra-Low Power Operational Amplifier

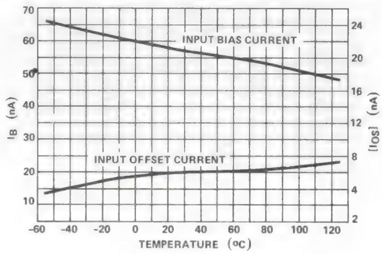
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

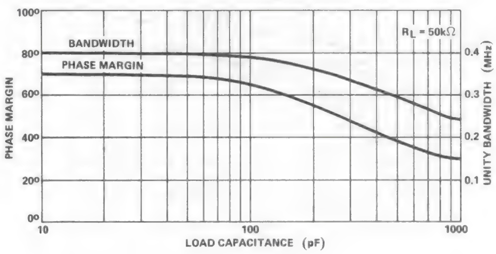
OPEN LOOP FREQUENCY RESPONSE



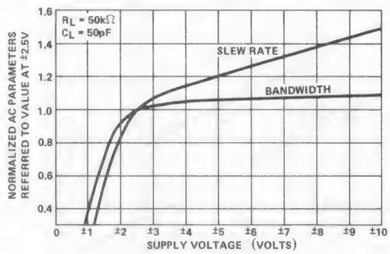
INPUT OFFSET CURRENT AND BIAS CURRENT vs. TEMPERATURE



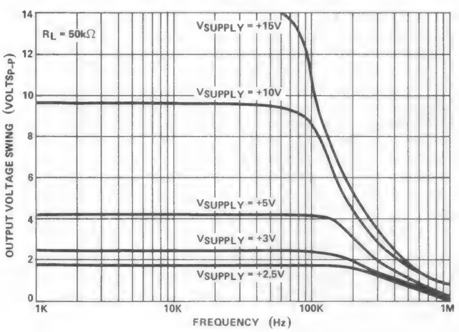
BANDWIDTH AND PHASE MARGIN vs. LOAD CAPACITANCE



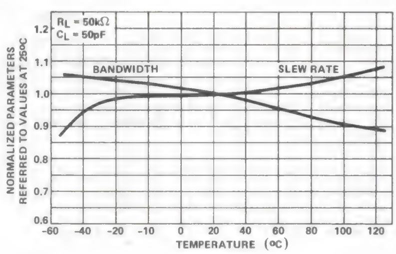
NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING vs. FREQUENCY AND SINGLE SUPPLY VOLTAGE



NORMALIZED AC PARAMETERS vs. TEMPERATURE



3

OP AMPs & COMPARATORS

DESIGN INFORMATION (Continued)

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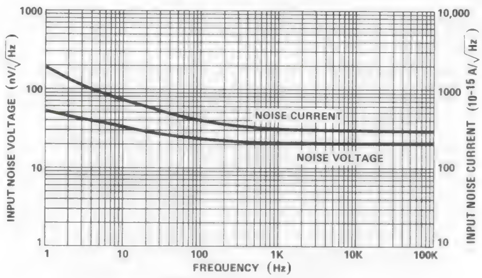
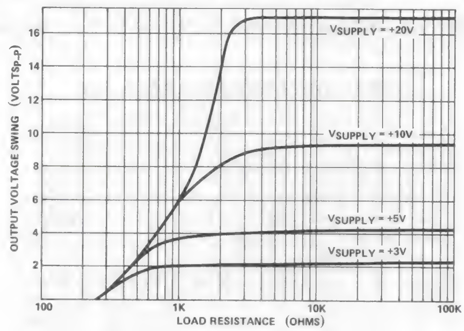
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

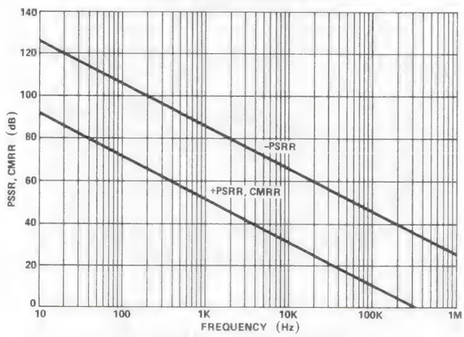
INPUT NOISE vs. FREQUENCY



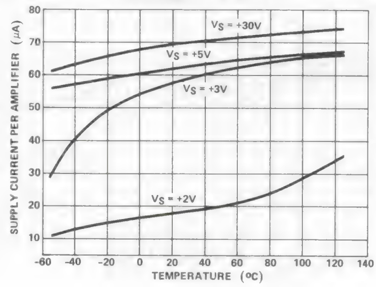
MAXIMUM OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE AND SINGLE SUPPLY VOLTAGE



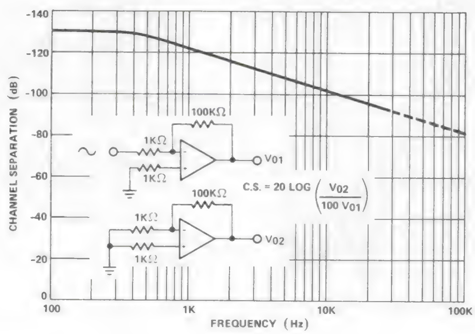
PSRR AND CMRR vs. FREQUENCY



POWER SUPPLY CURRENT vs. TEMPERATURE AND SINGLE SUPPLY VOLTAGE



CHANNEL SEPARATION vs. FREQUENCY



DESIGN INFORMATION (Continued)

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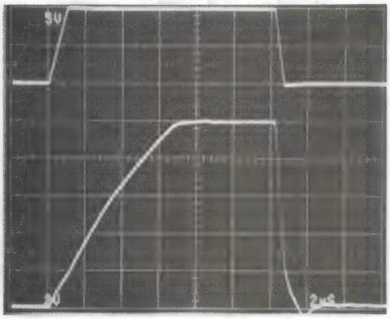
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

MEASURED LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 5V/Div.; Output = 2V/Div.)
Horizontal Scale: (Time: 2µs/Div.)

INPUT

OUTPUT

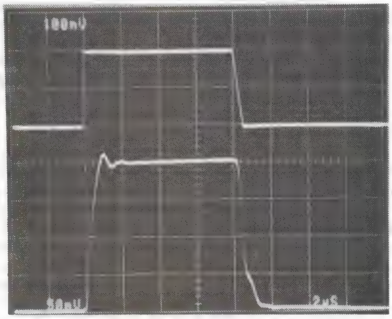


$+V_{SUPPLY} = +15V, -V_{SUPPLY} = -15V$

MEASURED SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 100mV/Div.; Output = 50mV/Div.)
Horizontal Scale: (Time: 2µs/Div.)

INPUT

OUTPUT

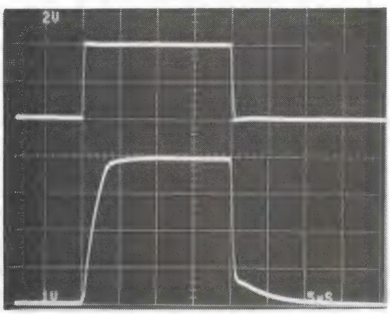


$+V_{SUPPLY} = +15V, -V_{SUPPLY} = -15V$

MEASURED LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 2V/Div.; Output = 1V/Div.)
Horizontal Scale: (Time: 5µs/Div.)

INPUT

OUTPUT

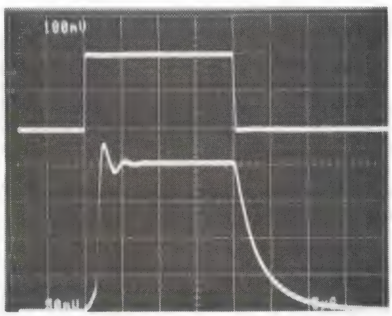


$+V_{SUPPLY} = +5V, -V_{SUPPLY} = 0V$

MEASURED SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 100mV/Div.; Output = 50mV/Div.)
Horizontal Scale: (Time: 5µs/Div.)

INPUT

OUTPUT



$+V_{SUPPLY} = +5V, -V_{SUPPLY} = 0V$

3

OP AMPs & COMPARATORS

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = 0V, 5 to ±15V, R_L = 50kΩ, C_L = 50pF, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage	V_{CM} = 0V	Full	0.5	Table 1	mV
Offset Voltage Drift	Versus Temperature	Full	3	6	μV/°C
Bias Current	V_{CM} = 0V	+25°C, +125°C	50	Table 1	nA
		-55°C	75	Table 1	nA
Offset Current	V_{CM} = 0V	Full	5	Table 1	nA
Differential Input Resistance		+25°C	0.6	0.4	MΩ
Input Noise Voltage	f_O = 10Hz	+25°C	40	80	$nV/\sqrt{Hz}$
	f_O = 100Hz	+25°C	30	60	$nV/\sqrt{Hz}$
	f_O = 1kHz	+25°C	20	40	$nV/\sqrt{Hz}$
Input Noise Current	f_O = 10Hz	+25°C	0.7	1	$pA/\sqrt{Hz}$
	f_O = 100Hz	+25°C	0.25	0.8	$pA/\sqrt{Hz}$
	f_O = 1kHz	+25°C	0.2	0.5	$pA/\sqrt{Hz}$
Large Signal Voltage Gain	R_L = 50kΩ	+25°C, +125°C	75K	Table 1	V/V
		-55°C	30K	Table 1	V/V
CMRR		Full	105	Table 1	dB
PSRR		Full	100	Table 1	dB
Unity Gain Bandwidth	f @ -3dB	+25°C	400	300	kHz
+ Slew Rate	V_S = 0V, 5V	-55°C	1	0.6	V/μs
	V_S = 0V, 5V to ±15V	+25°C, +125°C	1.5	0.8	V/μs
- Slew Rate	V_S = 0V, 5V to ±15V	Full	15	0.8	V/μs
+ I_{OUT}		+25°C, +125°C	2	0.4	mA
		-55°C	0.8	0.4	mA
- I_{OUT}		-55°C, +25°C	-7.5	-6	mA
		+125°C	-4.5	-3.5	mA
Rise Time	V_S = ±15V, V_O = 200mV	Full	0.8	1.5	μs
Fall Time	V_S = ±15V, V_O = -200mV	Full	0.9	1.5	μs
Overshoot	V_S = ±15V, V_O = ±200mV	Full	5	10	%
Supply Current (All Four Amplifiers)	V_S = 0V, 5V	+25°C	250	Table 1	μA
	V_S = ±15V	+25°C	300	Table 1	μA

HARRIS

HA-5147/883

Ultra-Low Noise, Precision, High Slew Rate Wideband Operational Amplifier

January 1989

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **High Slew Rate .... 28V/μs (Min)**
- **Wide Gain Bandwidth ($A_V \geq 10$) .... 100MHz (Min)**
- **Low Noise (@1kHz)............... 4.5nV/$\sqrt{Hz}$ (Max)**
- **Low Offset Voltage .... 100μV (Max)**
- **Low Offset Drift With Temperature .. 1.8μV/°C (Max)**
- **High CMRR............................ 100dB (Min)**
- **High Voltage Gain ....700V/mV (Min)**

Applications

- **High Speed Signal Conditioners**
- **Wide Bandwidth Instrumentation Amplifiers**
- **Low Level Transducer Amplifiers**
- **Fast, Low Level Voltage Comparators**
- **Highest Quality Audio Preamplifiers**
- **Pulse/RF Amplifiers**

Description

The HA-5147/883 monolithic operational amplifier features an unparalleled combination of precision D.C. and wideband high speed characteristics. Utilizing the Harris D.I. technology and advanced processing techniques, this unique design unites low noise precision instrumentation performance with high speed wideband capability.

This amplifier's impressive list of features include low V_{OS}, wide gain-bandwidth, high open loop gain, and high CMRR. Additionally, this flexible device operates over a wide supply range while consuming only 120mW of power.

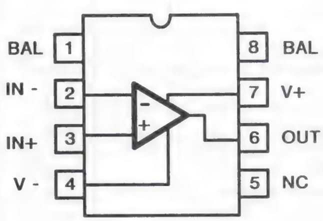
Using the HA-5147/883 allows designers to minimize errors while maximizing speed and bandwidth in applications requiring gains greater than ten.

This device is ideally suited for low level transducer signal amplifer circuits. Other applications which can utilize the HA-5147/883's qualities include instrumentation amplifiers, pulse or RF amplifiers, audio preamplifiers, and signal conditioning circuits.

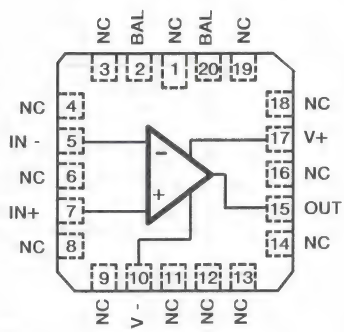
This device can easily be used as a design enhancement by directly replacing the 725, OP-25, OP-06, OP-07, OP-27 and OP-37 where gains are greater than ten. The HA-5147/883 is available in TO-99 Metal Can, Ceramic 8 Pin Mini-DIP, and 20 Pin Ceramic LCC packages.

Pinouts

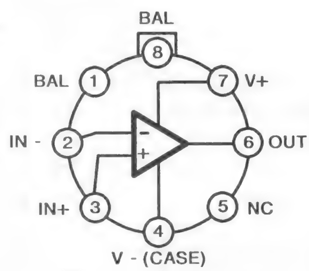
HA7-5147/883 (CERAMIC MINI-DIP)
TOP VIEW



HA4-5147/883 (CERAMIC LCC)
TOP VIEW



HA2-5147/883 (METAL CAN)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 44V
Differential Input Voltage (Note 6) 0.7V
Voltage at Either Input Terminal ...... V+ to V-
Input Current 25mA
Differential Output Current ...... Full Short Circuit Protection
Junction Temperature (T_J) ...... +175^{o}C
Storage Temperature Range ...... -65^{o}C to +150^{o}C
ESD Rating ...... < 2000V
Lead Temperature (Soldering 10 sec) ...... +275^{o}C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	82^{o}C/W	25^{o}C/W
Ceramic LCC Package	84^{o}C/W	25^{o}C/W
Metal Can Package	98^{o}C/W	30^{o}C/W

Package Power Dissipation Limit at +75^{o}C for $T_J \leq$ +175^{o}C
Ceramic DIP Package 1.22W
Ceramic LCC Package 1.19W
Metal Can Package 1.02W

Package Power Dissipation Derating Factor Above +75^{o}C
Ceramic DIP Package ...... 12.2mW/^{o}C
Ceramic LCC Package ...... 11.9mW/^{o}C
Metal Can Package ...... 10.2mW/^{o}C

Recommended Operating Conditions

Operating Temperature Range ...... -55^{o}C to +125^{o}C
Operating Supply Voltage ...... ±15V
$V_{INcm} \leq$ 1/2 (V+ - V-)
$R_L \geq 600\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, $R_{SOURCE} = 50\Omega$, $R_{LOAD} = 100k\Omega$, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	V_{CM} = 0V	1	+25^{o}C	-100	100	µV
			2, 3	+125^{o}C, -55^{o}C	-300	300	µV
Input Bias Current	I_B	V_{CM} = 0V $R_S = 10k\Omega, 50\Omega$ $\left(\frac{\lvert +I_B \rvert + \lvert -I_B \rvert}{2}\right)$	1	+25^{o}C	-	80	nA
			2, 3	+125^{o}C, -55^{o}C	-	150	nA
Input Offset Current	I_{IO}	V_{CM} = 0V $+R_S = 10k\Omega$ $-R_S = 10k\Omega$	1	+25^{o}C	-75	75	nA
			2, 3	+125^{o}C, -55^{o}C	-135	135	nA
Common Mode Range	+CMR	V+ = 4.7V V- = -25.3V	1	+25^{o}C	10.3	-	V
			2, 3	+125^{o}C, -55^{o}C	10.3	-	V
	-CMR	V+ = 25.3V V- = -4.7V	1	+25^{o}C	-	-10.3	V
			2, 3	+125^{o}C, -55^{o}C	-	-10.3	V
Large Signal Voltage Gain	$+A_{VOL}$	V_{OUT} = 0V and +10V $R_L = 2k\Omega$	4	+25^{o}C	700	-	kV/V
			5, 6	+25^{o}C, -55^{o}C	300	-	kV/V
	$-A_{VOL}$	V_{OUT} = 0V and -10V $R_L = 2k\Omega$	4	+25^{o}C	700	-	kV/V
			5, 6	+125^{o}C, -55^{o}C	300	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔV_{CM} = +11V	1	+25^{o}C	100	-	dB
		ΔV_{CM} = +10V	2, 3	+125^{o}C, -55^{o}C	100	-	dB
	-CMRR	ΔV_{CM} = -11V	1	+25^{o}C	100	-	dB
		ΔV_{CM} = -10V	2, 3	+125^{o}C, -55^{o}C	100	-	dB

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 100kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Output Voltage Swing	$+V_{OUT1}$	R_L = 2kΩ	4	+25°C	11.5	-	V
			5, 6	+125°C, -55°C	11.5	-	V
	$-V_{OUT1}$	R_L = 2kΩ	4	+25°C	-	-11.5	V
			5, 6	+125°C, -55°C	-	-11.5	V
	$+V_{OUT2}$	R_L = 600Ω	4	+25°C	10	-	V
	$-V_{OUT2}$	R_L = 600Ω	4	+25°C	-	-10	V
Output Current	$+I_{OUT}$	V_{OUT} = -10V	4	+25°C	16.5	-	mA
	$-I_{OUT}$	V_{OUT} = +10V	4	+25°C	-	-16.5	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V	1	+25°C	-	4	mA
		I_{OUT} = 0mA	2, 3	+125°C, -55°C	-	4	mA
	$-I_{CC}$	V_{OUT} = 0V	1	+25°C	-4	-	mA
		I_{OUT} = 0mA	2, 3	+125°C, -55°C	-4	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = 14V	1	+25°C	86	-	dB
		ΔV_{SUP} = 13.5V	2, 3	+125°C, -55°C	86	-	dB
	-PSRR	ΔV_{SUP} = 14V	1	+25°C	86	-	dB
		ΔV_{SUP} = 13.5V	2, 3	+125°C, -55°C	86	-	dB
Offset Voltage Adjustment	$+V_{IO}Adj$	Note 5	1	+25°C	V_{IO} -1	-	mV
			2, 3	+125°C, -55°C	V_{IO} -1	-	mV
	$-V_{IO}Adj$	Note 5	1	+25°C	V_{IO} +1	-	mV
			2, 3	+125°C, -55°C	V_{IO} +1	-	mV

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 2kΩ, C_{LOAD} =50pF, A_{VCL} = +10V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Slew Rate	+SR	V_{OUT} = -4V to +4V	7	+25°C	28	-	V/µs
	-SR	V_{OUT} = +4V to -4V	7	+25°C	28	-	V/µs
Rise & Fall Time	T_R	V_{OUT} = 0 to +200mV 10% ≤ T_R ≤ 90%	7	+25°C	-	50	ns
	T_F	V_{OUT} = 0 to -200mV 10% ≤ T_F ≤ 90%	7	+25°C	-	50	ns
Overshoot	+OS	V_{OUT} = 0 to +200mV	7	+25°C	-	40	%
	-OS	V_{OUT} = 0 to -200mV	7	+25°C	-	40	%

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_V = +10V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Average Offset Voltage Drift	$V_{IO}TC$	$V_{CM} = 0V$	1	-55°C to +125°C	-	1.8	μV/°C
Differential Input Resistance	R_{IN}	$V_{CM} = 0V$	1	+25°C	0.8	-	MΩ
Low Frequency Peak-to-Peak Noise	E_{np-p}	0.1Hz to 10Hz	1	+25°C	-	0.25	μV_{p-p}
Input Noise Voltage Density	E_n	$R_S = 20\Omega, f_o = 10Hz$	1, 4	+25°C	-	8.0	$nV/\sqrt{Hz}$
		$R_S = 20\Omega, f_o = 100Hz$	1, 4	+25°C	-	5.6	$nV/\sqrt{Hz}$
		$R_S = 20\Omega, f_o = 1kHz$	1, 4	+25°C	-	4.5	$nV/\sqrt{Hz}$
Input Noise Current Density	I_n	$R_S = 2M\Omega, f_o = 10Hz$	1,4	+25°C	-	4.0	$pA/\sqrt{Hz}$
		$R_S = 2M\Omega, f_o = 100Hz$	1, 4	+25°C	-	2.3	$pA/\sqrt{Hz}$
		$R_S = 2M\Omega, f_o = 1kHz$	1, 4	+25°C	-	0.6	$pA/\sqrt{Hz}$
Gain Bandwidth Product	GBWP	$V_O = 100mV, f_o = 10kHz$	1	+25°C	120	-	MHz
		$V_O = 100mV, f_o = 1MHz$	1	+25°C	100	-	MHz
Full Power Bandwidth	FPBW	$V_{PEAK} = 10V$	1, 2	+25°C	445	-	kHz
Minimum Closed Loop Stable Gain	CLSG	$R_L = 2k\Omega, C_L = 50pF$	1	-55°C to +125°C	±10	-	V/V
Settling Time	T_S	To 0.1% for a 10V Step	1	+25°C	-	600	μs
Output Resistance	R_{OUT}	Open Loop	1	+25°C	-	100	Ω
Quiescent Power Consumption	PC	$V_{OUT} = 0V, I_{OUT} = 0mA$	1, 3	-55°C to +125°C	-	120	mW

NOTES:
1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).
3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)
4. Input Noise Voltage Density and Input Noise Current Density is sample tested on every lot.
5. Offset adjustment range is [V_{IO} (Measured) ± 1mV] minimum referred to output. This test is for functionality only to assure adjustment through 0V.
6. For differential input voltages greater than 0.7V, the input current must be limited to 25mA to protect the back-to-back input diodes.

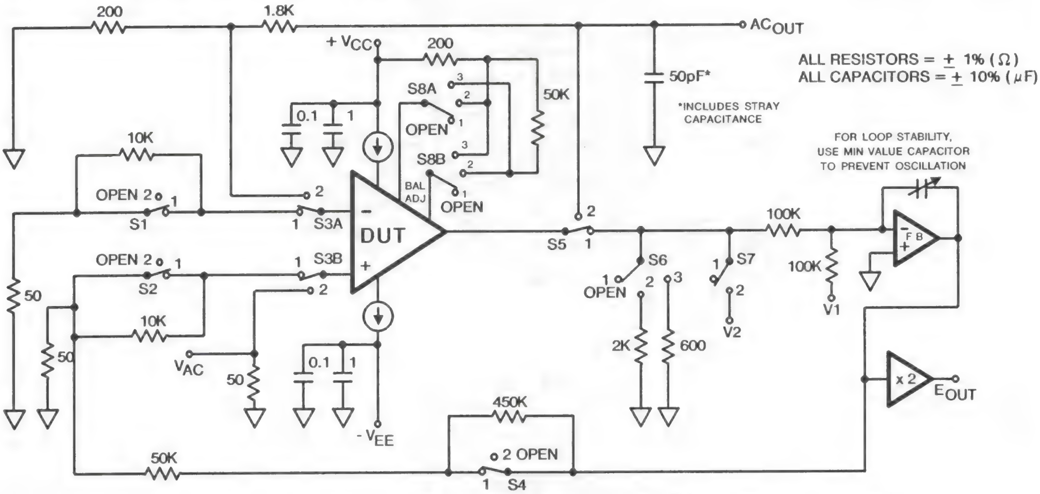
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6, 7
Group A Test Requirements	1, 2, 3, 4, 5, 6, 7
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

The Subgroup assignments of the parameters in these tables were patterned after Mil-M-38510/135, with the exception of V_{IO}, which is Subgroups 1, 2, and 3.

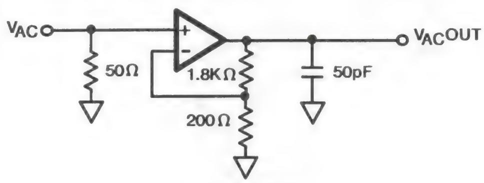
Test Circuit (Applies to Tables 1 and 2)



For Op-Amp Test Circuits and Conditions, Refer to the Harris Tech Brief "HA-5147 Op-Amp Test Methods". The HA-5147/883 is A.C. Tested (Table 2) at $A_V = +10V/V$.

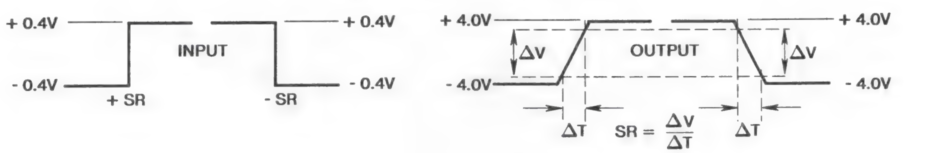
Test Waveforms

SIMPLIFIED TEST CIRCUIT (Applies to Table 2)

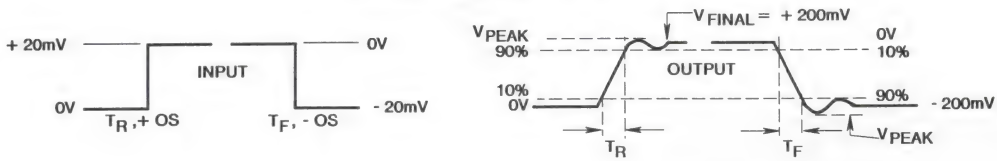


$A_V = +10V/V$

SLEW RATE WAVEFORM



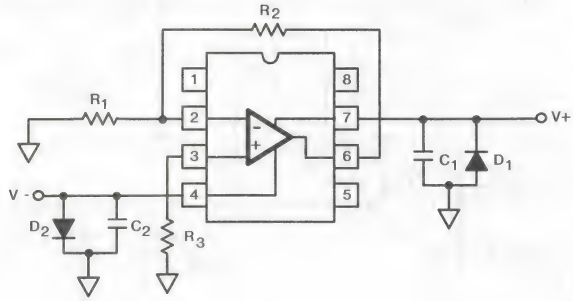
TRANSIENT RESPONSE WAVEFORM



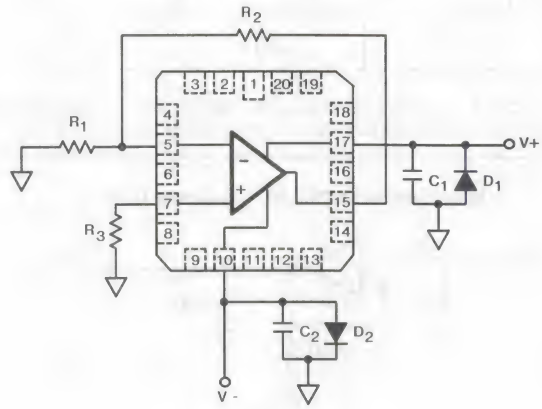
NOTE: Measured on Both positive and negative transitions.

Burn-In Circuits

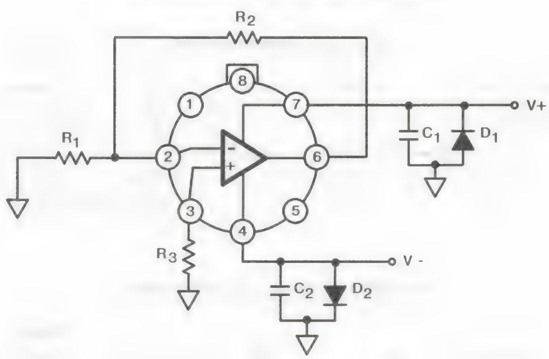
HA7-5147/883 CERAMIC DIP



HA4-5147/883 CERAMIC LCC

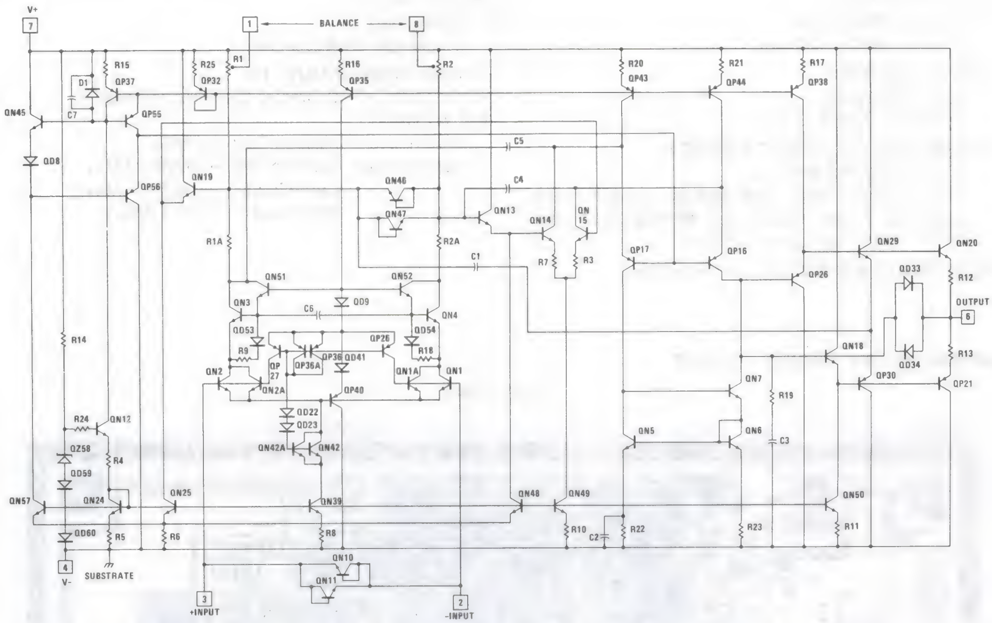


HA2-5147/883 (TO-99) METAL CAN



NOTES:
R_1 = R3 = 1kΩ, ±5%, 1/4W (Min)
R_2 = 10kΩ ±5%, 1/4W (Min)
C_1 = C_2 = 0.01μF/ per Socket (Min) or 0.1μF/Row (Min)
D_1 = D_2 = IN4002 or Equivalent/Board
$|(V+) - (V-)| = 30V$

Schematic Diagram



Die Characteristics

DIE DIMENSIONS:
104.3 x 65 x 19 mils
(2650 x 1650 x 483 µm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$3.6 \times 10^5 A/cm^2$ @15mA
This device meets Glassivation Integrity Test requirement per Mil-Std-883 Method 2021 and Mil-M-38510 paragraph 3.5.5.4.

SUBSTRATE POTENTIAL (Powered Up): V-

GLASSIVATION:
Type: Silox
Thickness: 7kÅ ± 0.7kÅ

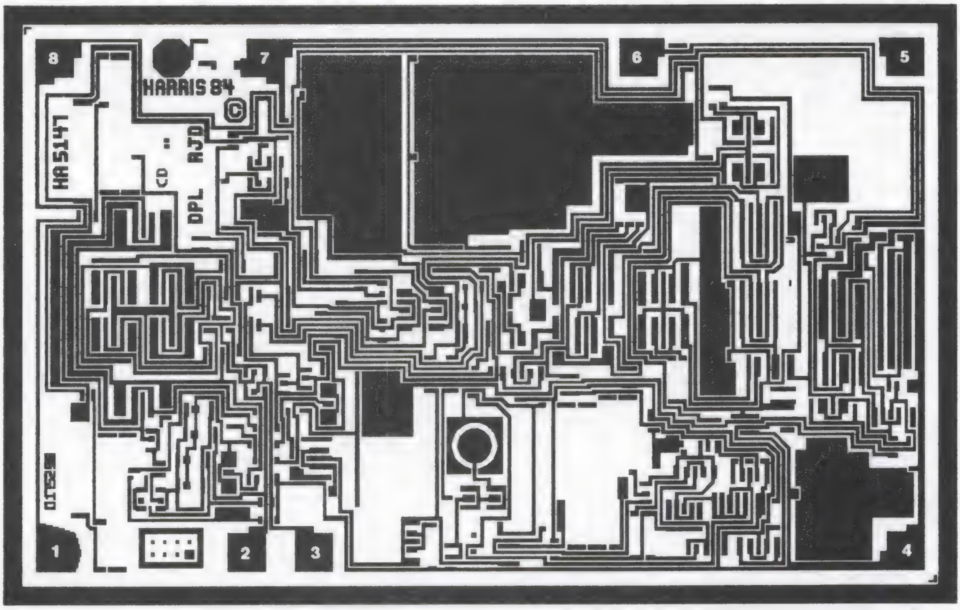
TRANSISTOR COUNT: 63

PROCESS: HFHB Bipolar Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)
Metal Can — 420°C (Max)

Metallization Mask Layout

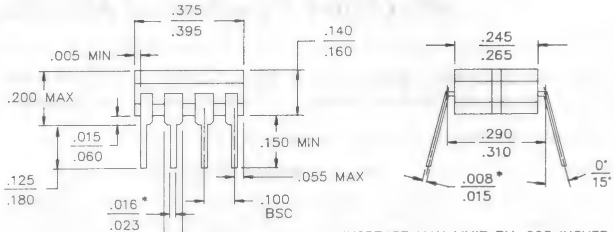
HA-5147/883



NOTE: Pin Numbers Correspond to 8 Pin Metal Can and Mini-DIP Package Only.

Packaging †

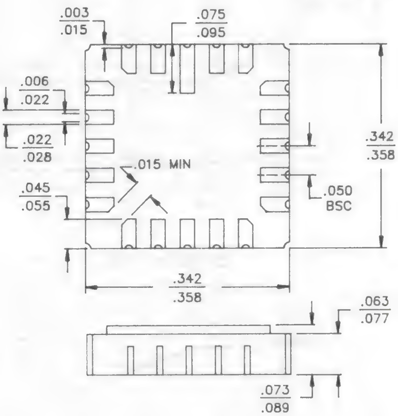
8 PIN CERAMIC DIP



* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

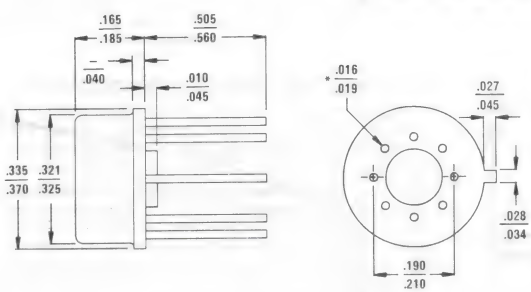
LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-4

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Ceramic, 90% Al_2O_3
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

8 PIN TO-99 METAL CAN



*Dimension Maximum Limits Are Increased by 0.003 inches for Solder Dip Finish

LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
Material: No Seal Material
Temperature: Room Temperature
Method: Resistance Weld
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic Bonded
COMPLIANT OUTLINE: 38510 A-1

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

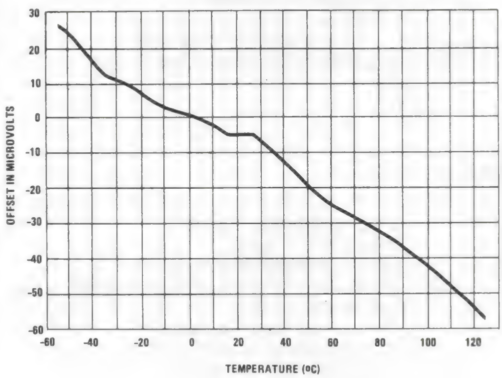
DESIGN INFORMATION

Ultra-Low Noise, Precision, High Slew Rate Wideband Operational Amplifier

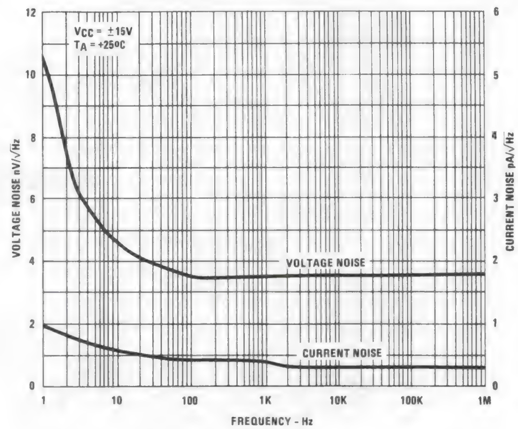
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

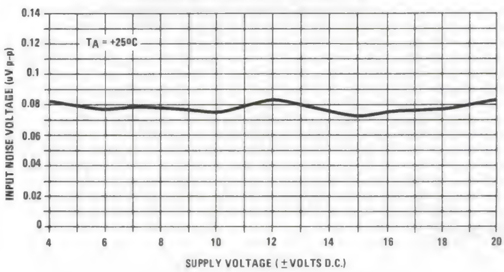
OFFSET VOLTAGE TYPICAL DRIFT vs. TEMPERATURE



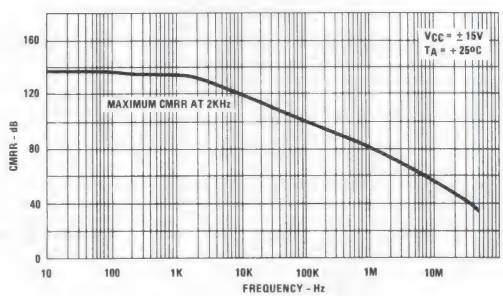
NOISE CHARACTERISTICS



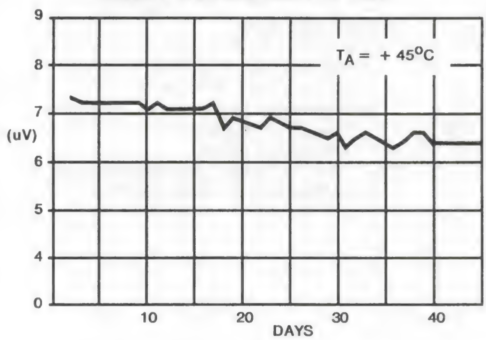
NOISE vs. SUPPLY VOLTAGE



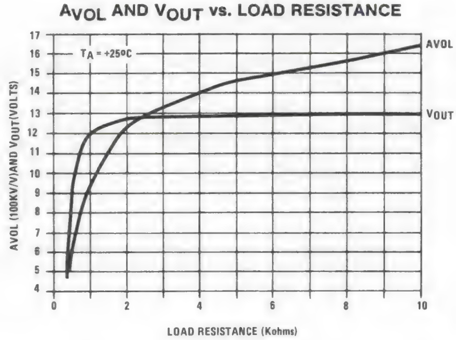
CMRR vs. FREQUENCY



OFFSET VOLTAGE DRIFT vs. TIME



A_{VOL} AND V_{OUT} vs. LOAD RESISTANCE



DESIGN INFORMATION (Continued)

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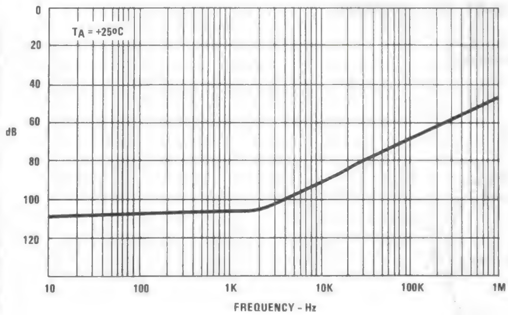
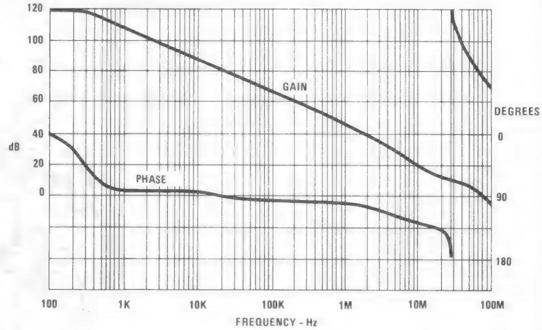
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

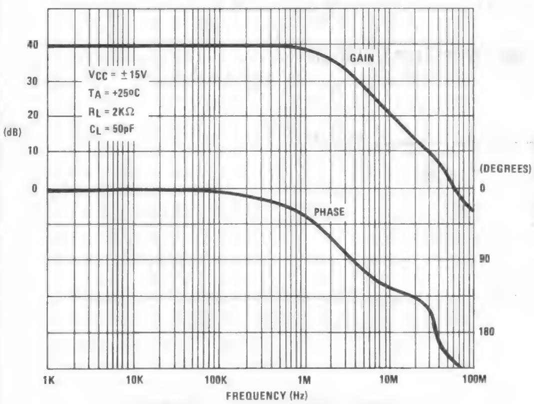
PSRR vs. FREQUENCY



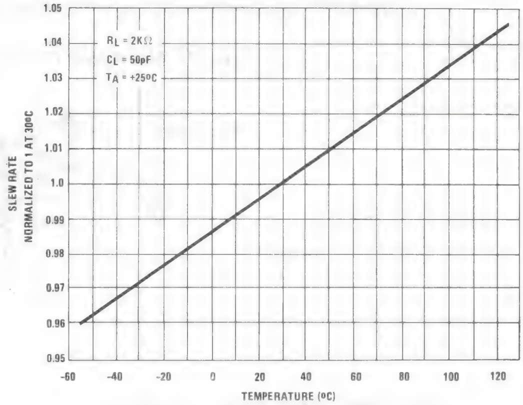
OPEN LOOP GAIN AND PHASE vs. FREQUENCY



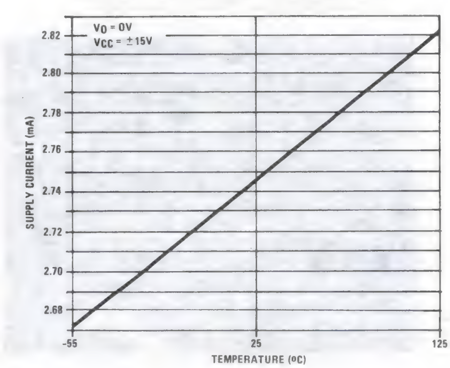
CLOSED LOOP GAIN AND PHASE vs. FREQUENCY



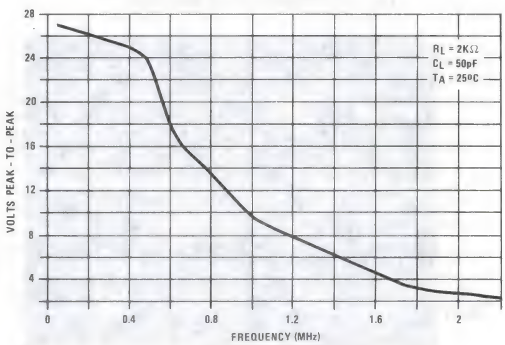
NORMALIZED SLEW RATE vs. TEMPERATURE



SUPPLY CURRENT vs. TEMPERATURE



VOUT MAX vs. FREQUENCY UNDISTORTED SINEWAVE OUTPUT



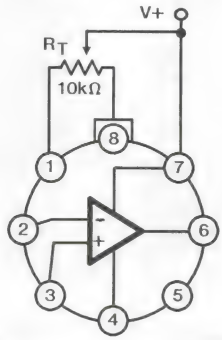
DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Information

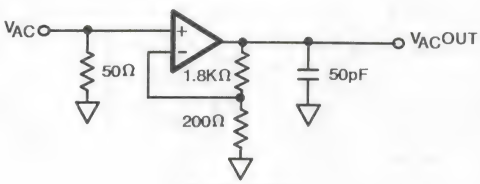
Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

SUGGESTED OFFSET VOLTAGE ADJUSTMENT



Tested Offset Adjustment Range is $|V_{OS} + mV|$ minimum referred to output. Typical Range is ±4mV with $R_T = 10k\Omega$.

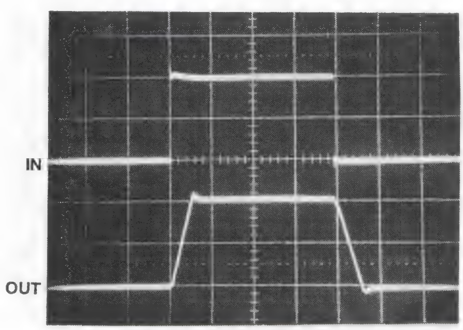
LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT



$A_V = +10V/V$

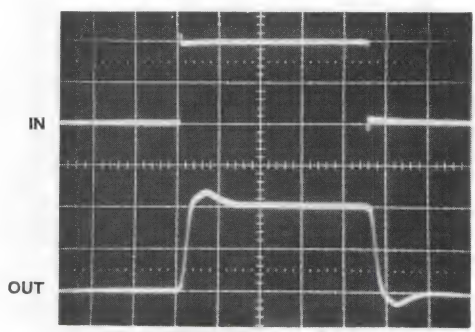
MEASURED LARGE SIGNAL RESPONSE

Vertical Scale: (Volts: Input = 0.5V/Div.)
(Volts: Output = 5V/Div.)
Horizontal Scale: (Time: 500ns/Div.)



MEASURED SMALL SIGNAL RESPONSE

Vertical Scale: (Volts: Input = 10mV/Div)
(Volts: Output = 100mV/Div.)
Horizontal Scale: (Time: 100ns/Div.)

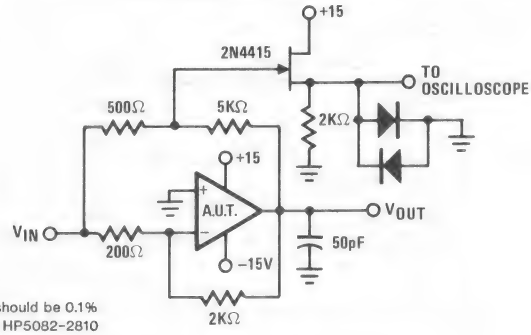


DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

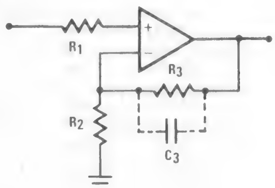
Typical Performance Information Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

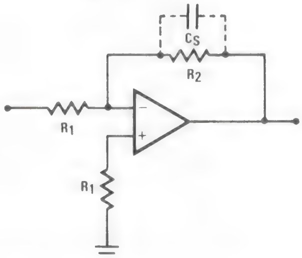
SETTLING TIME TEST CIRCUIT



- $A_V = -10$
- Feedback and summing resistors should be 0.1%
- Clipping diodes are optional. HP5082-2810 recommended

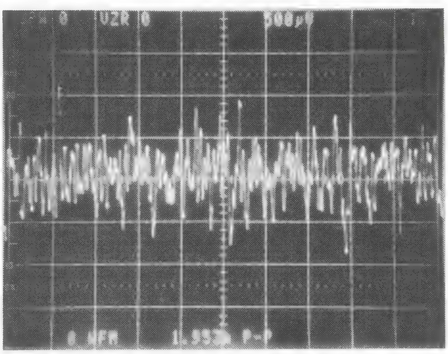
SUGGESTED STABILITY CIRCUITS





Low resistances are preferred for low noise applications as a 1kΩ resistor has $4nV/\sqrt{Hz}$ of thermal noise. Total resistances of greater than 10kΩ on either input can reduce stability. In most high resistance applications, a few picofarads of capacitance across the feedback resistor will improve stability.

0.1Hz TO 10Hz NOISE WITH A_{VCL}= 25,000V/V
Horizontal Scale = 1sec/Div.
Vertical Scale = 0.002µV/Div.
$0.08\mu V_{p-p}$ RTI



DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_L = 2kΩ, C_L = 50pF, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage	V_{CM} = 0V	+25°C	30	Table 1	μV
		Full	70	Table 1	μV
Offset Voltage Drift	Versus Temperature	Full	0.4	Table 3	μV/°C
	Versus Time	+45°C	0.71	1.5	μV/Month
Bias Current	V_{CM} = 0V	+25°C	±15	Table 1	nA
		Full	±35	Table 1	nA
Differential Input Resistance		+25°C	6	Table 3	MΩ
Input Noise Voltage	f_O = 10Hz	+25°C	4.4	Table 3	$nV/\sqrt{Hz}$
	f_O = 100Hz	+25°C	3.4	Table 3	$nV/\sqrt{Hz}$
	f_O = 1kHz	+25°C	3.2	Table 3	$nV/\sqrt{Hz}$
Input Noise Current	f_O = 10Hz	+25°C	1.7	Table 3	$pA/\sqrt{Hz}$
	f_O = 100Hz	+25°C	1.0	Table 3	$pA/\sqrt{Hz}$
	f_O = 1kHz	+25°C	0.4	Table 3	$pA/\sqrt{Hz}$
Voltage Gain	V_{OUT} = ±10V	+25°C	1.8	Table1	MV/V
		Full	1.2	Table 1	MV/V
CMRR	ΔV = ±10V	Full	126	Table 1	dB
PSRR	V_S = ±4 to ±18V	Full	110	Table 1	dB
Slew Rate	V_{OUT} = ±5V	+25°C	35	Table 2	V/μs
Overshoot	V_{OUT} = ±200mV	+25°C	20	Table 2	%
Settling Time	10V to 0.1%	+25°C	400	Table 3	ns
	10V to 0.01%	+25°C	800	1000	ns
Minimum Supply Voltage	Functional Operation Only. Other Parameters Will Vary.	+25°C	±4	±5	V

HARRIS

HA-5151/883

Single, Low Power Operational Amplifier

January 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low Supply Current .... 250μA (Max)
- Wide Supply Voltage Range .... Single 3V to 30V or Dual ±1.5 to ±15V
- High Slew Rate .... +S.R. 4V/μs (Min) 6V/μs (Typ)
- Low V_{OS} Drift (Over Full Temp) .... 3μV/°C (Typ)
- Low Noise (1kHz).................. 15nV/$\sqrt{Hz}$ (Typ)
- 100% Tested at ±15V and +5V Power Supplies
- Dielectric Isolation

Applications

- Portable Instruments
- Meter Amplifiers
- Telephone Headsets
- Microphone Amplifiers
- Remote Sensor/Transmitter
- Battery Powered Equipment
- For Further Design Ideas See App. Note 544

Description

The HA-5151/883 single operational amplifier is part of a family of dielectrically isolated bipolar amplifiers designed to provide excellent AC performance while drawing less than 250μA of supply current at +25°C. This unity gain stable amplifier is especially well suited for portable and lightweight equipment where available power is limited.

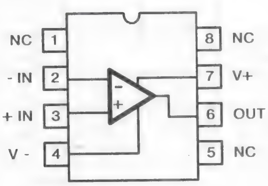
The HA-5151/883 combines superior low power AC performance with DC precision not usually found in general purpose amplifiers. The DC performance is centered around low input offset voltage (3mV), low offset voltage drift (3μV/°C), and low input bias current (250nA). This is combined with a very low input noise voltage of 15nV/$\sqrt{Hz}$ at 1kHz.

The AC performance of the HA-5151/883 surpasses that of typical low power amplifiers with 4V/μs slew rate and a full power bandwidth of 64kHz. This makes the HA-5151/883 an excellent choice for virtually all audio processing applications as well as remote sensor/ transmitter designs requiring both low power and high speed. The suitability of the HA-5151/883 for remote and low power operation is further enhanced by the wide range of supply voltages (±1.5V to ±15V) as well as single supply operation (3V to 30V).

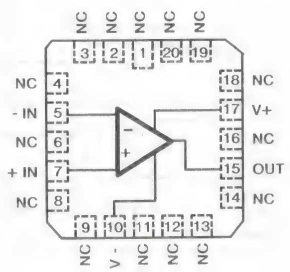
The HA-5151/883 is available in 8 pin Ceramic Mini-DIP, 20 pad Ceramic LCC or 8 pin (TO-99) Metal Can, and is interchangeable with most other operational amplifiers in their class.

Pinouts

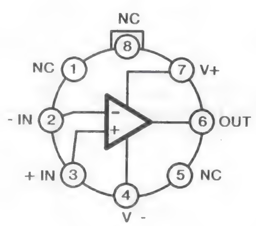
HA7-5151/883 (CERAMIC MINI-DIP)
TOP VIEW



HA4-5151/883 (CERAMIC LCC)
TOP VIEW



HA2-5151/883 (METAL CAN)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage 7V
Voltage at Either Input Terminal .... V+ to V-
Output Current .... Full Short Circuit Protection
Output Current Duration .... Indefinite, One Amplifier Shorted to Ground
Junction Temperature (T_J) .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... <2000V
Lead Temperature (Soldering 10 sec) .... +275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	83°C/W	28°C/W
Ceramic LCC Package	74°C/W	30°C/W
Metal Can Package	149°C/W	45°C/W

Package Power Dissipation Limit at +75°C For $T_J \leq$ +175°C
- Ceramic DIP Package 1.21W
- Ceramic LCC Package 1.34W
- Metal Can Package 670mW

Package Power Dissipation Derating Factor Above +75°C
- Ceramic DIP Package .... 12.1mW/°C
- Ceramic LCC Package .... 13.4mW/°C
- Metal Can Package .... 6.7mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±1.5V to ±15V or 3V to 30V

$V_{INcm} \leq 1/2$ (V+ - V-)
$R_L \geq$ 10kΩ

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.
Subscript 1 Refers to Supply Voltages (±V_S) = ±15V, Subscript 2 Refers to +V_S = 5.0V, -V_S = 0.0V.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO1}	V_{CM} = 0V	1	+25°C	-3	3	mV
			2, 3	+125°C, -55°C	-4	4	mV
	V_{IO2}	V_{CM} = 0V V_{OUT} = 1.4V	1	+25°C	-3	3	mV
			2, 3	+125°C, -55°C	-4	4	mV
Input Bias Current	$+I_{B1}$	V_{CM} = 0V $+R_S$ = 10kΩ $-R_S$ = 100Ω	1	+25°C	-250	250	nA
			2, 3	+125°C, -55°C	-400	400	nA
	$-I_{B1}$	V_{CM} = 0V $+R_S$ = 100Ω $-R_S$ = 10kΩ	1	+25°C	-250	250	nA
			2, 3	+125°C, -55°C	-400	400	nA
	$+I_{B2}$	V_{CM} = 0V, V_{OUT} = 1.4V $+R_S$ = 10kΩ $-R_S$ = 100Ω	1	+25°C	-250	250	nA
			2, 3	+125°C, -55°C	-400	400	nA
	$-I_{B2}$	V_{CM} = 0V, V_{OUT} = 1.4V $+R_S$ = 100Ω $-R_S$ = 10kΩ	1	+25°C	-250	250	nA
			2, 3	+125°C, -55°C	-400	400	nA
Input Offset Current	I_{IO1}	V_{CM} = 0V $+R_S$ = 10kΩ $-R_S$ = 10kΩ	1	+25°C	-50	50	nA
			2, 3	+125°C, -55°C	-80	80	nA
	I_{IO2}	V_{CM} = 0V, V_{OUT} = 1.4V $+R_S$ = 10kΩ $-R_S$ = 10kΩ	1	+25°C	-50	50	nA
			2, 3	+125°C, -55°C	-80	80	nA
Common Mode Range	$+CMR_1$	V+ = 5V V- = -25V	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	$-CMR_1$	V+ = 25V V- = -5V	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
	$+CMR_2$	V+ = 5V to 2V V- = 0V to -3V V_{OUT} = 1.4V to -1.6V	1	+25°C	0 to 3	-	V
			2, 3	+125°C, -55°C	0 to 3	-	V

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: $R_{SOURCE} = 100\Omega$, $R_{LOAD} = 500k\Omega$, $V_{OUT} = 0V$, Unless Otherwise Specified.
Subscript 1 Refers to Supply Voltages $(\pm V_S) = \pm 15V$; Subscript 2 Refers to $+V_S = 5.0V$, $-V_S = 0.0V$.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Large Signal Voltae Gain	$+A_{VOL1}$	V_{OUT} = 0V and 10V $R_L = 10k\Omega$	4	+25°C	50	-	kV/V
			5, 6	+125°C, -55°C	25	-	kV/V
	$-A_{VOL1}$	V_{OUT} = 0V and -10V $R_L = 10k\Omega$	4	+25°C	50	-	kV/V
			5, 6	+125°C, -55°C	25	-	kV/V
	$+A_{VOL2}$	V_{OUT} = 1.4V and 2.5V $R_L = 10k\Omega$	4	+25°C	50	-	kV/V
			5, 6	+125°C, -55°C	25	-	kV/V
Common Mode Rejection Ratio	$+CMRR_1$	ΔV_{CM} = 10V +V = 5V -V = -25V V_{OUT} = -10V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	$-CMRR_1$	ΔV_{CM} = 10V +V = 25V -V = -5V V_{OUT} = 10V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	$+CMRR_2$	ΔV_{CM} = 0V to 3V +V = 2V -V = -3V V_{OUT} = -3V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
Output Voltage Swing	$+V_{OUT1}$	$R_L = 10k\Omega$	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	$-V_{OUT1}$	$R_L = 10k\Omega$	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
	$+V_{OUT2}$	$R_L = 10k\Omega$ Terminated at 2.5V	1	+25°C	3.2	-	V
			2, 3	+125°C, -55°C	2.9	-	V
	$-V_{OUT2}$	$R_L = 10k\Omega$ Terminated at 2.5V	1	+25°C	-	1	V
			2, 3	+125°C, -55°C	-	1.2	V
Quiescent Power Supply Current	$+I_{CC1}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-	250	µA
			2, 3	+125°C, -55°C	-	275	µA
	$-I_{CC1}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-250	-	µA
			2, 3	+125°C, -55°C	-275	-	µA
	$+I_{CC2}$	V_{OUT} = 1.4V I_{OUT} = 0mA	1	+25°C	-	250	µA
			2, 3	+125°C, -55°C	-	275	µA
Power Supply Rejection Ratio	$+PSRR_1$	ΔV_{SUP} = 10V +V = 10V, -V = -15V +V = 20V, -V = -15V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	$-PSRR_1$	ΔV_{SUP} = 10V +V = 15V, -V = -10V +V = 15V, -V = -20V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	$+PSRR_2$	ΔV_{SUP} = 10V +V = 5V, -V = 0V +V = 15V, -V = 0V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $R_{SOURCE} = 50\Omega$, $R_{LOAD} = 10k\Omega$, $C_{LOAD} = 100pF$, $V_{OUT} = 0V$, Unless Otherwise Specified.
Subscript 1 Refers to Supply Voltages ($\pm V_S$) = ±15V; Subscript 2 Refers to $+V_S = 5.0V$, $-V_S = 0.0V$.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Slew Rate	$+SR_1$	V_{OUT} = -3V to 3V V_{IN} S.R. $\leq$ 25V/µs	4	+25°C	4	-	V/µs
	$-SR_1$	V_{OUT} = 3V to -3V V_{IN} S.R. $\leq$ 25V/µs	4	+25°C	4	-	V/µs
	$+SR_2$	V_{OUT} = 0V to 3V V_{IN} S.R. $\leq$ 25V/µs	4	+25°C	2	-	V/µs
	$-SR_2$	V_{OUT} = 3V to 0V V_{IN} S.R. $\leq$ 25V/µs	4	+25°C	2	-	V/µs

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $R_{SOURCE} = 50\Omega$, $R_{LOAD} = 10k\Omega$, $C_{LOAD} = 100pF$, $A_V = 1V/V$, Unless Otherwise Specified.
Subscript 1 Refers to Supply Voltages ($\pm V_S$) = ±15V; Subscript 2 Refers to $+V_S = 5.0V$, $-V_S = 0.0V$.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Gain Bandwidth Product	GBWP	V_O = 200mV, f_o = 10kHz	1	+25°C	0.7	-	MHz
Full Power Bandwidth	$FPBW_1$	V_{PEAK} = 10V	1, 2	+25°C	64	-	kHz
	$FPBW_2$	V_{PEAK} = 1.1V V_{Ref} = 2.5V	1, 2	+25°C	290	-	kHz
Minimum Closed Loop Stable Gain	CLSG	$R_L = 10k\Omega$, C_L = 100pF	1	-55°C to +125°C	1	-	V/V
Quiecent Power Consumption	PC_1	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	8.25	mW
	PC_2	V_{OUT} = 1.4V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	1.4	mW

NOTES: 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).

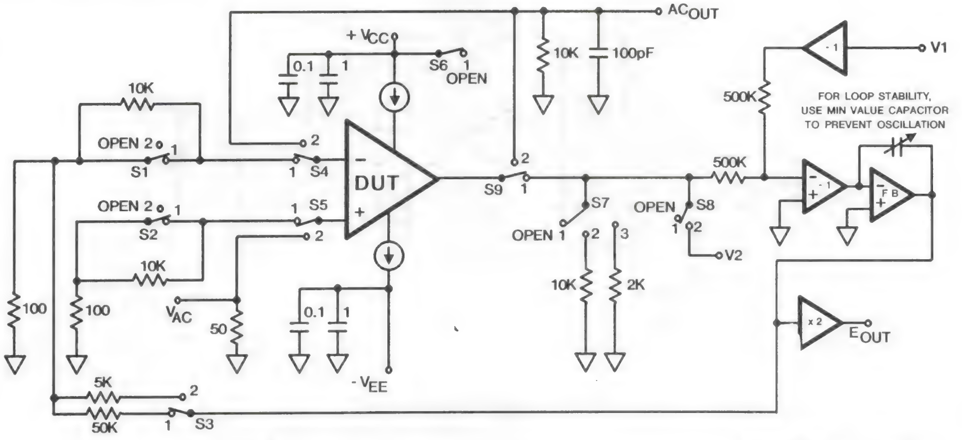
3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6
Group A Test Requirements	1, 2, 3, 4, 5, 6
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

Test Circuit (Applies to Tables 1 and 2)

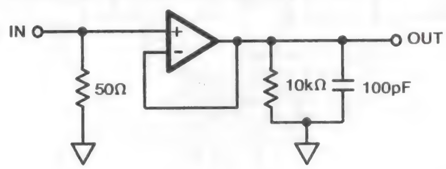


ALL RESISTORS = ± 1% (Ω)
ALL CAPACITORS = ± 10% (μF)

For Detailed Information, Refer to HA-5151/883 Test Tech Brief

Test Waveforms

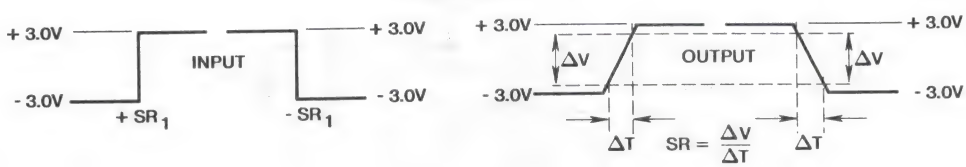
SIMPLIFIED TEST CIRCUIT (Applies to Table 2)



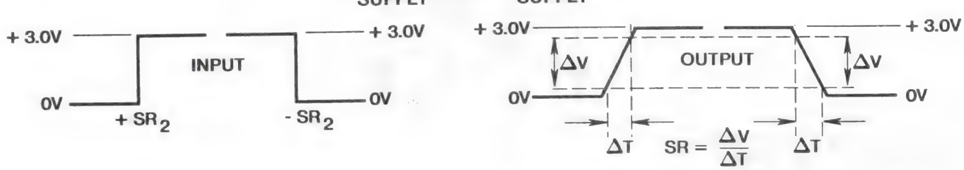
NOTE: $\pm V_{SUPPLY}$ ($\pm V_S$) Tested with ±15V and 0V, +5V. V_{IN} Slew Rate Maintained with Less Than 10V/μs Input for Voltage Follower Configuration.

SLEW RATE WAVEFORMS, A_V = 1V/V

$\pm V_{SUPPLY} = \pm 15V$

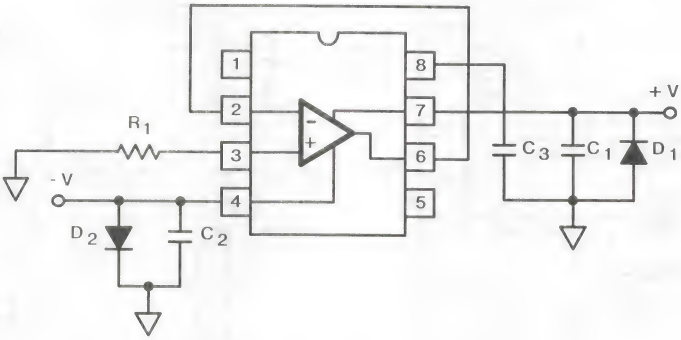


$+V_{SUPPLY} = 5V$, $-V_{SUPPLY} = 0V$

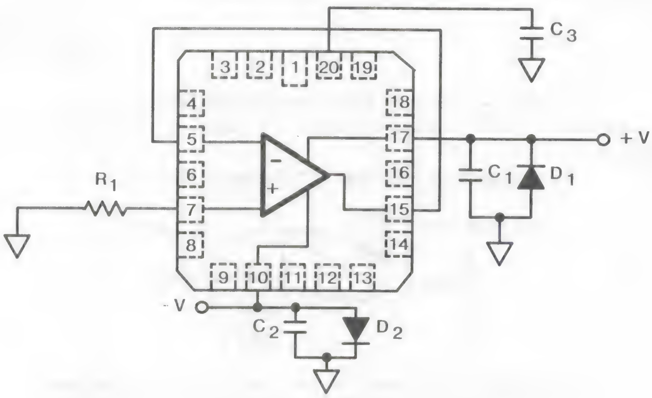


Burn-In Circuits

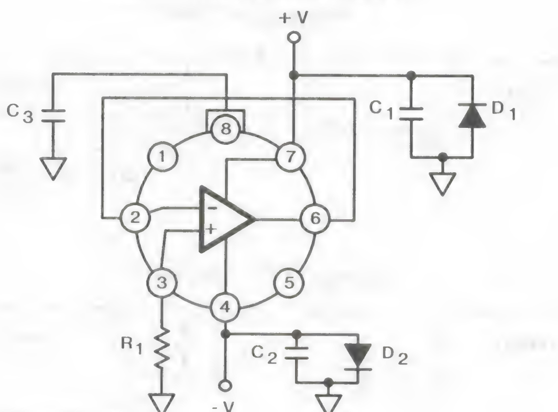
HA7-5151/883 CERAMIC DIP



HA4-5151/883 CERAMIC LCC



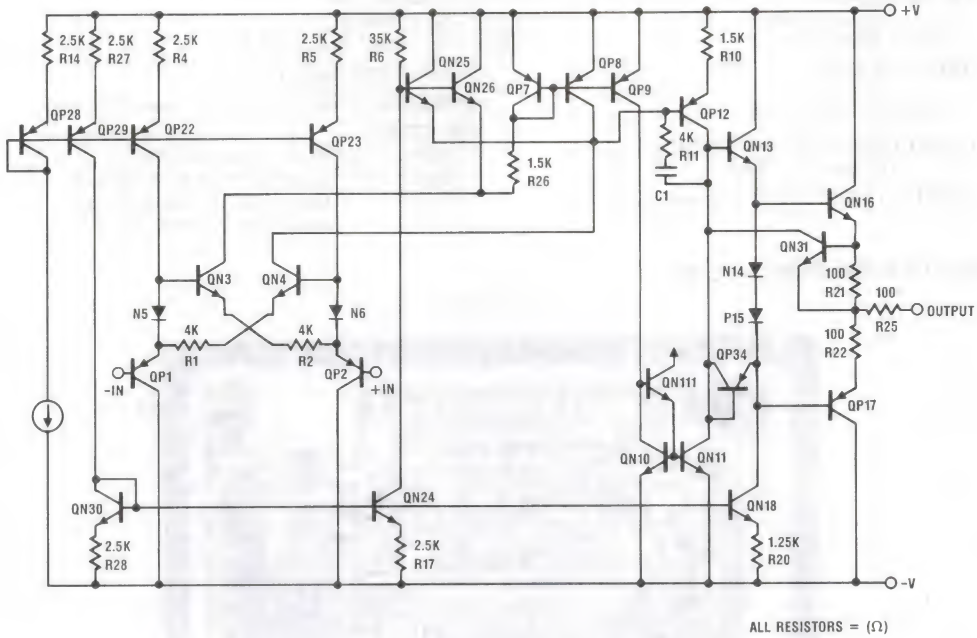
HA2-5151/883 TO-99 METAL CAN



NOTES:

R_1 = 1MΩ, ±5%, 1/4W (Min)
$C_1 = C_2$ = 0.01µF/Socket (Min) or 0.1µF/Row, (Min)
C_3 = 0.01µF/Socket, 10% (Not Required)
$D_1 = D_2$ = IN4002 or Equivalent/Board
$|(V+) - (V-)| = 30V$

Schematic Diagram



Die Characteristics

DIE DIMENSIONS:
58.7 x 53.1 x 19 mils
(1490 x 1350 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$0.6 \times 10^5 A/cm^2$ @ 2.5mA

SUBSTRATE POTENTIAL (Powered Up): V-

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

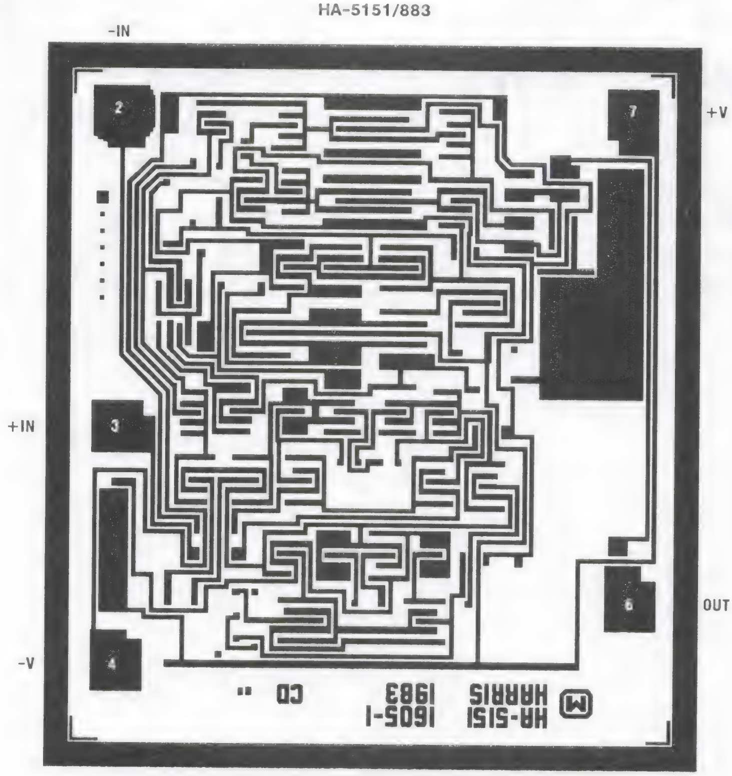
TRANSISTOR COUNT: 36

PROCESS: HFSB Bipolar/JFET Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)
Metal Can — 420°C (Max)

Metallization Mask Layout

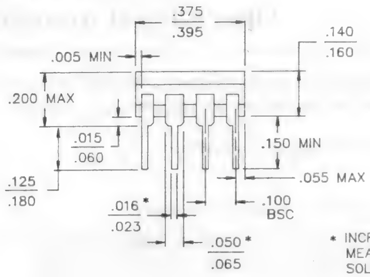
HA-5151/883

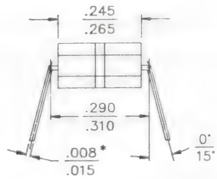


NOTE: Pad Numbers Refer to 8 Pin Ceramic Mini-DIP or Metal Can Package Pinouts Only.

Packaging †

8 PIN CERAMIC DIP

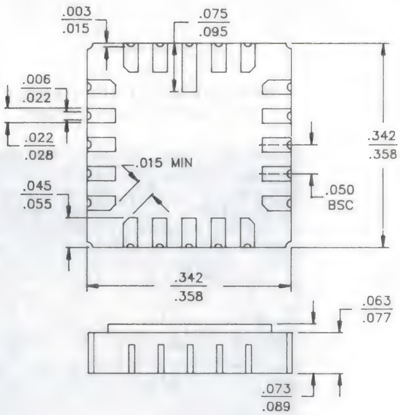




* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

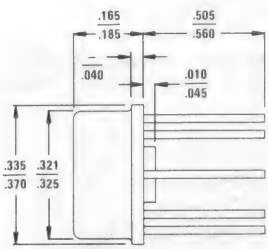
LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-4

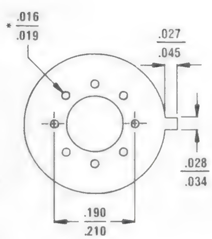
20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Ceramic, 90% Al_2O_3
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

8 PIN TO-99 METAL CAN





LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
Material: No Seal Material
Temperature: Room Temperature
Method: Resistance Weld
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonjc Bonded
COMPLIANT OUTLINE: 38510 A-1

*Dimension Maximum Limits Are Increased by 0.003 inches for Solder Dip Finish

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

3 OP AMPs & COMPARATORS

HARRIS

HA-5151

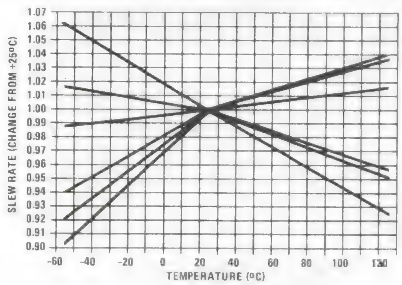
DESIGN INFORMATION

Single, Low Power Operational Amplifier

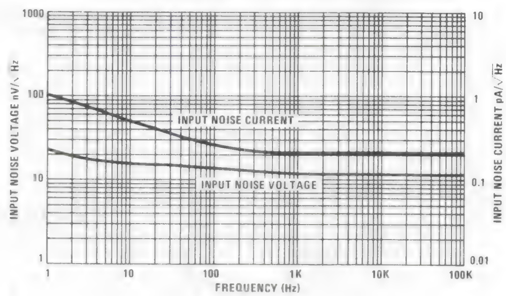
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

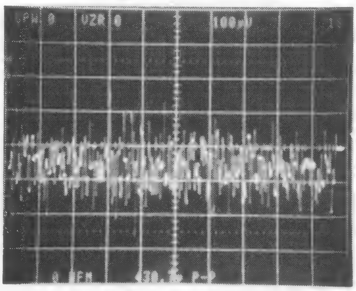
SLEW RATE vs. TEMPERATURE
Normalized to Unity at +25°C, 6 Representative Units



NOISE SPECTRAL DENSITY

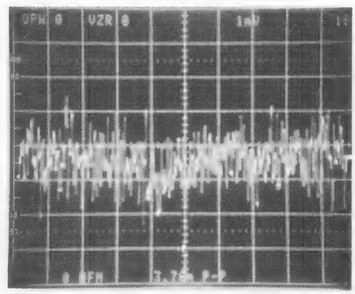


PEAK-TO-PEAK NOISE 0.1Hz TO 10Hz
$T_A = +25^oC$, $A_V = 1000V/V$



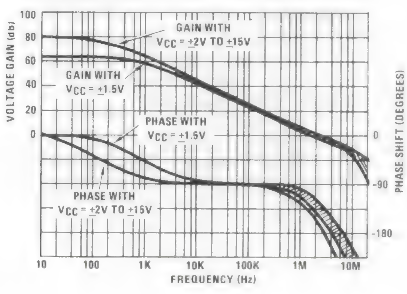
Vertical Scale: (Volts: 100µs/Div.)
Horizontal Scale: (Time: 1sec/Div.)
$430nV_{p-p}$ RTI

PEAK-TO-PEAK 0.1Hz TO 1MHz
$T_A = +25^oC$, $A_V = 1000V/V$

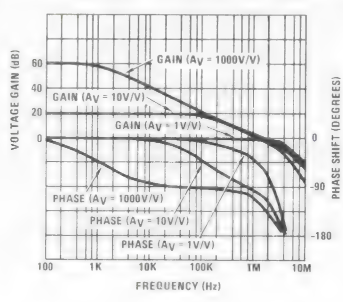


Vertical Scale: (Volts: 1mV/Div.)
Horizontal Scale: (Time: 1sec/Div.)
$3.70\mu V_{p-p}$ RTI

FREQUENCY RESPONSE vs. SUPPLY VOLTAGE
$T_A = +25^oC$, $R_L = 10K$, $C_L = 100pF$



FREQUENCY RESPONSE AT VARIOUS GAINS
$T_A = +25^oC$, $V_{CC} = \pm 15V$, $R_L = 10K$, $C_L = 100pF$

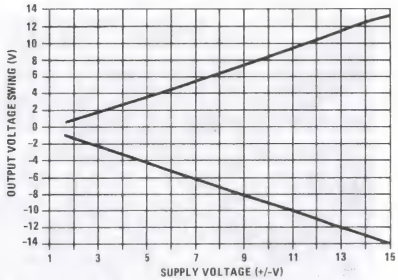


DESIGN INFORMATION (Continued)

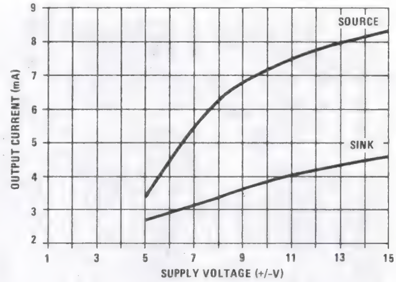
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

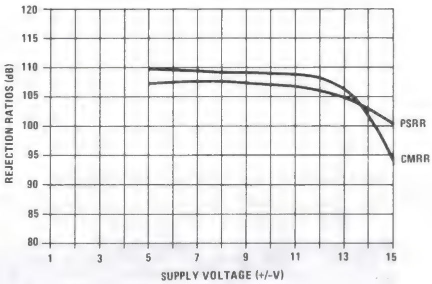
OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE
(+25°C)



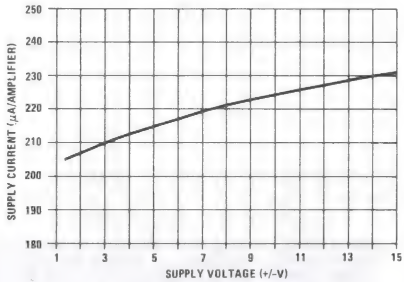
OUTPUT CURRENT vs. SUPPLY VOLTAGE
(+25°C)



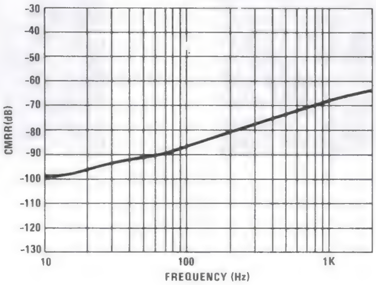
CMRR AND PSRR vs. SUPPLY VOLTAGE
(+25°C)



SUPPLY CURRENT vs. SUPPLY VOLTAGE
Per Amplifier (+25°C)



CMRR vs. FREQUENCY
$T_A = +25^oC$, $V_{CC} = \pm15V$

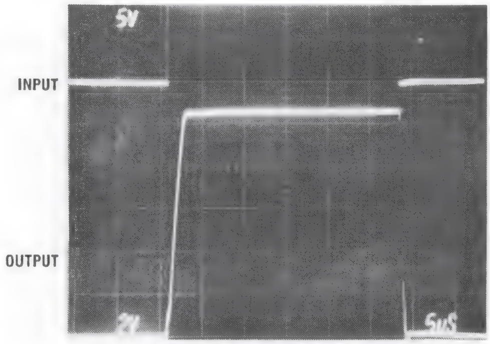


DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

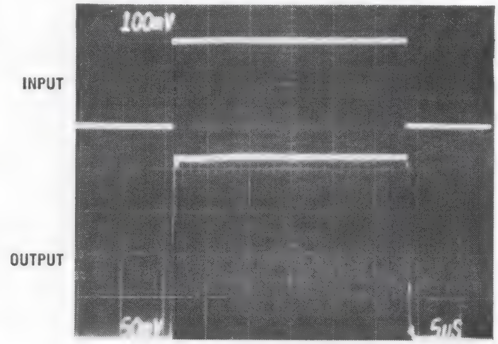
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

MEASURED LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 5V/Div.; Output = 2V/Div.)
Horizontal Scale: (Time: 5μs/Div.)



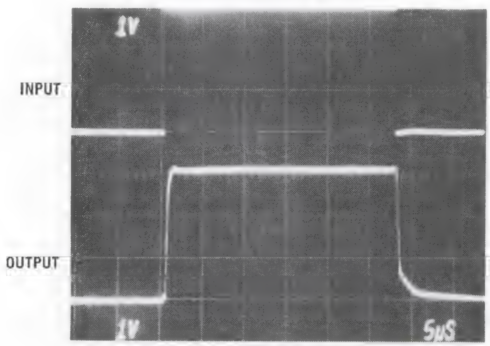
$+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$

MEASURED SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 100mV/Div.; Output = 50mV/Div.)
Horizontal Scale: (Time: 5μs/Div.)



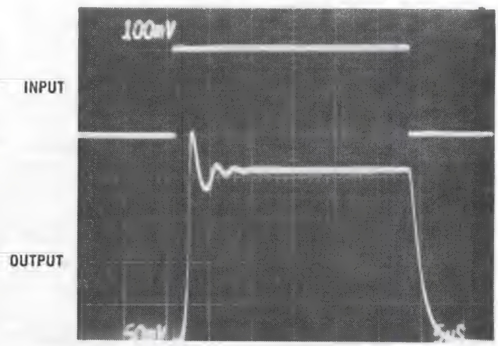
$+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$

MEASURED LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 1V/Div.; Output = 1V/Div.)
Horizontal Scale: (Time: 5μs/Div.)



$+V_{SUPPLY} = +5V$, $-V_{SUPPLY} = 0V$

MEASURED SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 100mV/Div.; Output = 50mV/Div.)
Horizontal Scale: (Time: 5μs/Div.)



$+V_{SUPPLY} = +5V$, $-V_{SUPPLY} = 0V$

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Applications Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

Loading

Although the standard load is 10kΩ, the HA-5151 is capable of driving resistive loads down to 2kΩ and capacitive loads beyond 300pF.

Input Stage

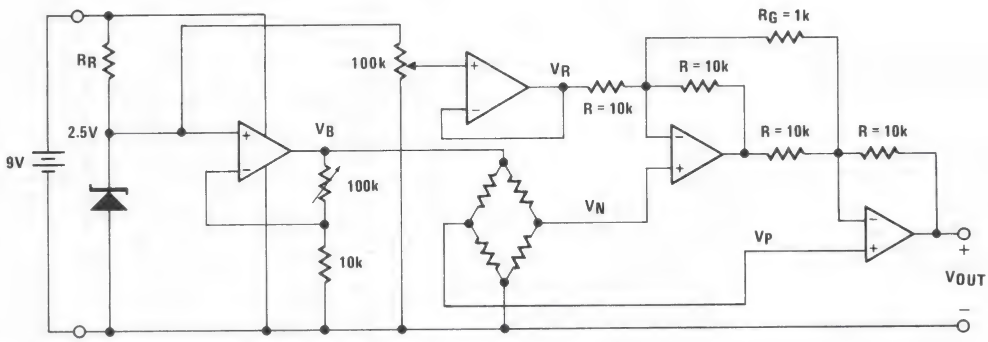
This amplifier uses a current amplifying input stage (see Application Note 544) and is not recommended for use in applications which involve large differential input voltages such as open-loop comparators. Most op amp applications use feedback and keep the input terminals at approximately the same voltage. The HA-5151 will perform well in these circuits as long as the input terminals see less than 7 volts differential.

Typical Applications

The low power consumption of the HA-5151 makes it ideal for applications like battery-powered instrumentation where the bridge amplifier circuit below would be used.

Choose a low-current zener voltage reference such as LM285Z-2.5 and select R_R accordingly. This circuit was evaluated using the resistor values shown and a laboratory voltage source for the 2.5V reference. With unmatched, off-the-shelf, 1% resistors, a gain accuracy of 1% to 2% can be expected. Temperature testing indicated a voltage offset tempco of less then 100µV/oC referred to output.

$$V_{OUT} = (V_P - V_N)\ [2\ (1 + \frac{R}{R_G}\ )] + V_R$$



DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = 0V, 5 to ±15V, R_L = 10kΩ, C_L = 100pF, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage	V_{CM} = 0V	Full	0.5	Table 1	mV
Offset Voltage Drift	Versus Temperature	Full	3	6	µV/°C
Bias Current	V_{CM} = 0V	+25°C, +125°C	130	Table 1	nA
		-55°C	150	Table 1	nA
Offset Current	V_{CM} = 0V	Full	5	Table 1	nA
Differential Input Resistance		+25°C	1.5	1	MΩ
Input Noise Voltage	f_O = 10Hz	+25°C	18	25	nV/$\sqrt{Hz}$
	f_O = 100Hz	+25°C	15	20	nV/$\sqrt{Hz}$
	f_O = 1kHz	+25°C	14.8	18	nV/$\sqrt{Hz}$
Input Noise Current	f_O = 10Hz	+25°C	0.5	0.7	pA/$\sqrt{Hz}$
	f_O = 100Hz	+25°C	0.3	0.6	pA/$\sqrt{Hz}$
	f_O = 1kHz	+25°C	0.25	0.4	pA/$\sqrt{Hz}$
Large Signal Voltage Gain	R_L = 10kΩ	+25°C, +125°C	150K	Table 1	V/V
		-55°C	100K	Table 1	V/V
CMRR		Full	105	Table 1	dB
PSRR		Full	105	Table 1	dB
Unity Gain Bandwidth	f @ -3dB	+25°C	1.3	0.7	MHz
+ Slew Rate	V_S = 0V, 5V	-55°C	4	2	V/µs
	V_S = 0V, 5V to ±15V	+25°C, +125°C	6.5	4	V/µs
- Slew Rate	V_S = 0V, 5V	Full	12	2	V/µs
	V_S = ±15V	Full	25	4	V/µs
+ I_{OUT}		+25°C, +125°C	3	1.5	mA
		-55°C	0.8	0.4	mA
- I_{OUT}		-55°C, +25°C	-7.5	-6	mA
		+125°C	-4.5	-3.5	mA
Rise Time	V_S = ±15V, V_O = 200mV	Full	250	500	ns
Fall Time	V_S = ±15V, V_O = -200mV	-55°C, +25°C	110	300	ns
		+125°C	200	400	ns
Overshoot	V_S = ±15V, V_O = ±200mV	Full	2	10	%
Supply Current	V_S = 0V, 5V	+25°C	180	Table 1	µA
	V_S = ±15V	+25°C	200	Table 1	µA

HARRIS

HA-5152/883

Dual, Low Power Operational Amplifier

January 1989

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- Low Supply Current (Both Amplifiers) ..... 500μA (Max)
- Wide Supply Voltage Range .... Single 3V to 30V or Dual ±1.5 to ±15V
- High Slew Rate .... +S.R. 4V/μs (Min) 6V/μs (Typ)
- Low V_{OS} Drift (Over Full Temp) .... 3μV/°C (Typ)
- Low Noise (1kHz).................. 15nV/$\sqrt{Hz}$ (Typ)
- 100% Tested at ±15V and +5V Power Supplies
- Dielectric Isolation

Applications

- Portable Instruments
- Meter Amplifiers
- Telephone Headsets
- Microphone Amplifiers
- Remote Sensor/Transmitter
- Battery Powered Equipment
- For Further Design Ideas See App. Note 544

Description

The HA-5152/883 dual operational amplifier is part of a family of dielectrically isolated bipolar amplifiers designed to provide excelllent AC performance while drawing less than 250μA of supply current per amplifier at +25°C. This series consists of single (5151), dual (5152) or quad (5154), unity gain stable amplifiers which are especially well suited for portable and lightweight equipment where available power is limited.

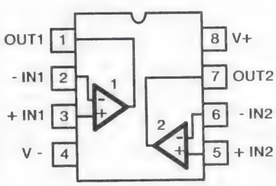
The HA-5152/883 combines superior low power AC performance with DC precision not usually found in general purpose amplifiers. The DC performance is centered around low input offset voltage (3mV), low offset voltage drift (3μV/°C), and low input bias current (250nA). This is combined with a very low input noise voltage of 15nV/$\sqrt{Hz}$ at 1kHz.

The AC performance of the HA-5152/883 surpasses that of typical low power amplifiers with 4V/μs slew rate and a full power bandwidth of 64kHz. This makes the HA-5152/883 an excellent choice for virtually all audio processing applications as well as remote sensor/transmitter designs requiring both low power and high speed. The suitability of the HA-5152/883 for remote and low power operation is further enhanced by the wide range of supply voltages (±1.5V to ±15V) as well as single supply operation (3V to 30V).

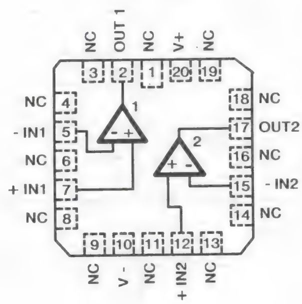
The HA-5152/883 is available in 8 pin Ceramic Mini-DIP, 20 pad Ceramic LCC or 8 pin (TO-99) Metal Can, and is interchangeable with most other operational amplifiers in their class.

Pinouts

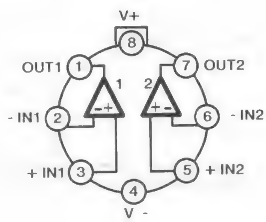
HA7-5152/883 (CERAMIC MINI-DIP)
TOP VIEW



HA4-5152/883 (CERAMIC LCC)
TOP VIEW



HA2-5152/883 (METAL CAN)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage 7V
Voltage at Either Input Terminal .... V+ to V-
Output Current .... Full Short Circuit Protection
Output Current Duration .... Indefinite, One Amplifier Shorted to Ground
Junction Temperature (T_J) .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... <2000V
Lead Temperature (Soldering 10 sec) .... +275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	82°C/W	26°C/W
Ceramic LCC Package	74°C/W	20°C/W
Metal Can Package	111°C/W	35°C/W

Package Power Dissipation Limit at +75°C For $T_J \le$ +175°C
Ceramic DIP Package 1.22W
Ceramic LCC Package 1.35W
Metal Can Package 900mW
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 12.2mW/°C
Ceramic LCC Package .... 13.5mW/°C
Metal Can Package .... 9mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±1.5V to ±15V or 3V to 30V

$V_{INcm} \le 1/2$ (V+ - V-)
$R_L \ge 10k\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $R_{SOURCE} = 100\Omega$, $R_{LOAD} = 500k\Omega$, V_{OUT} = 0V, Unless Otherwise Specified.
Subscript 1 Refers to Supply Voltages ($\pm V_S$) = ±15V, Subscript 2 Refers to $+V_S$ = 5.0V, $-V_S$ = 0.0V.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO1}	V_{CM} = 0V	1	+25°C	-3	3	mV
			2, 3	+125°C, -55°C	-4	4	mV
	V_{IO2}	V_{CM} = 0V V_{OUT} = 1.4V	1	+25°C	-3	3	mV
			2, 3	+125°C, -55°C	-4	4	mV
Input Bias Current	$+I_{B1}$	V_{CM} = 0V $+R_S = 10k\Omega$ $-R_S = 100\Omega$	1	+25°C	-250	250	nA
			2, 3	+125°C, -55°C	-400	400	nA
	$-I_{B1}$	V_{CM} = 0V $+R_S = 100\Omega$ $-R_S = 10k\Omega$	1	+25°C	-250	250	nA
			2, 3	+125°C, -55°C	-400	400	nA
	$+I_{B2}$	V_{CM} = 0V, V_{OUT} = 1.4V $+R_S = 10k\Omega$ $-R_S = 100\Omega$	1	+25°C	-250	250	nA
			2, 3	+125°C, -55°C	-400	400	nA
	$-I_{B2}$	V_{CM} = 0V, V_{OUT} = 1.4V $+R_S = 100\Omega$ $-R_S = 10k\Omega$	1	+25°C	-250	250	nA
			2, 3	+125°C, -55°C	-400	400	nA
Input Offset Current	I_{IO1}	V_{CM} = 0V $+R_S = 10k\Omega$ $-R_S = 10k\Omega$	1	+25°C	-50	50	nA
			2, 3	+125°C, -55°C	-80	80	nA
	I_{IO2}	V_{CM} = 0V, V_{OUT} = 1.4V $+R_S = 10k\Omega$ $-R_S = 10k\Omega$	1	+25°C	-50	50	nA
			2, 3	+125°C, -55°C	-80	80	nA
Common Mode Range	$+CMR_1$	V+ = 5V V- = -25V	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	$-CMR_1$	V+ = 25V V- = -5V	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
	$+CMR_2$	V+ = 5V to 2V V- = 0V to -3V V_{OUT} = 1.4V to -1.6V	1	+25°C	0 to 3	-	V
			2, 3	+125°C, -55°C	0 to 3	-	V

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: $R_{SOURCE} = 100\Omega$, $R_{LOAD} = 500k\Omega$, $V_{OUT} = 0V$, Unless Otherwise Specified.
Subscript 1 Refers to Supply Voltages ($\pm V_S$) = ±15V; Subscript 2 Refers to $+V_S = 5.0V$, $-V_S = 0.0V$.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Large Signal Voltae Gain	$+A_{VOL1}$	V_{OUT} = 0V and 10V $R_L = 10k\Omega$	4	+25°C	50	-	kV/V
			5, 6	+125°C, -55°C	25	-	kV/V
	$-A_{VOL1}$	V_{OUT} = 0V and -10V $R_L = 10k\Omega$	4	+25°C	50	-	kV/V
			5, 6	+125°C, -55°C	25	-	kV/V
	$+A_{VOL2}$	V_{OUT} = 1.4V and 2.5V $R_L = 10k\Omega$	4	+25°C	50	-	kV/V
			5, 6	+125°C, -55°C	25	-	kV/V
Common Mode Rejection Ratio	$+CMRR_1$	ΔV_{CM} = 10V +V = 5V -V = -25V V_{OUT} = -10V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	$-CMRR_1$	ΔV_{CM} = 10V +V = 25V -V = -5V V_{OUT} = 10V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	$+CMRR_2$	ΔV_{CM} = 0V to 3V +V = 2V -V = -3V V_{OUT} = -3V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
Output Voltage Swing	$+V_{OUT1}$	$R_L = 10k\Omega$	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	$-V_{OUT1}$	$R_L = 10k\Omega$	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
	$+V_{OUT2}$	$R_L = 10k\Omega$ Terminated at 2.5V	1	+25°C	3.2	-	V
			2, 3	+125°C, -55°C	2.9	-	V
	$-V_{OUT2}$	$R_L = 10k\Omega$ Terminated at 2.5V	1	+25°C	-	1	V
			2, 3	+125°C, -55°C	-	1.2	V
Quiescent Power Supply Current (Both Amplifiers)	$+I_{CC1}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-	500	μA
			2, 3	+125°C, -55°C	-	650	μA
	$-I_{CC1}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-500	-	μA
			2, 3	+125°C, -55°C	-650	-	μA
	$+I_{CC2}$	V_{OUT} = 1.4V I_{OUT} = 0mA	1	+25°C	-	500	μA
			2, 3	+125°C, -55°C	-	650	μA
Power Supply Rejection Ratio	$+PSRR_1$	ΔV_{SUP} = 10V +V = 10V, -V = -15V +V = 20V, -V = -15V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	$-PSRR_1$	ΔV_{SUP} = 10V +V = 15V, -V = -10V +V = 15V, -V = -20V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	$+PSRR_2$	ΔV_{SUP} = 10V +V = 5V, -V = 0V +V = 15V, -V = 0V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
Channel Separation	±CS	$R_L = 10k\Omega$	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $R_{SOURCE} = 50\Omega$, $R_{LOAD} = 10k\Omega$, $C_{LOAD} = 100pF$, $V_{OUT} = 0V$, Unless Otherwise Specified.
Subscript 1 Refers to Supply Voltages ($\pm V_S$) = ±15V; Subscript 2 Refers to $+V_S = 5.0V$, $-V_S = 0.0V$.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Slew Rate	$+SR_1$	$V_{OUT} = -3V$ to 3V V_{IN} S.R. $\leq 25V/\mu s$	4	+25°C	4	-	V/µs
	$-SR_1$	$V_{OUT} = 3V$ to -3V V_{IN} S.R. $\leq 25V/\mu s$	4	+25°C	4	-	V/µs
	$+SR_2$	$V_{OUT} = 0V$ to 3V V_{IN} S.R. $\leq 25V/\mu s$	4	+25°C	2	-	V/µs
	$-SR_2$	$V_{OUT} = 3V$ to 0V V_{IN} S.R. $\leq 25V/\mu s$	4	+25°C	2	-	V/µs

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $R_{SOURCE} = 50\Omega$, $R_{LOAD} = 10k\Omega$, $C_{LOAD} = 100pF$, $A_V = 1V/V$, Unless Otherwise Specified.
Subscript 1 Refers to Supply Voltages ($\pm V_S$) = ±15V; Subscript 2 Refers to $+V_S = 5.0V$, $-V_S = 0.0V$.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Gain Bandwidth Product	GBWP	$V_O = 200mV$, $f_o = 10kHz$	1	+25°C	0.7	-	MHz
Full Power Bandwidth	$FPBW_1$	$V_{PEAK} = 10V$	1, 2	+25°C	64	-	kHz
	$FPBW_2$	$V_{PEAK} = 1.1V$ $V_{Ref} = 2.5V$	1, 2	+25°C	290	-	kHz
Minimum Closed Loop Stable Gain	CLSG	$R_L = 10k\Omega$, $C_L = 100pF$	1	-55°C to +125°C	1	-	V/V
Quiecent Power Consumption	PC_1	$V_{OUT} = 0V$, $I_{OUT} = 0mA$	1, 3	-55°C to +125°C	-	16.5	mW
	PC_2	$V_{OUT} = 1.4V$, $I_{OUT} = 0mA$	1, 3	-55°C to +125°C	-	2.75	mW

NOTES: 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).

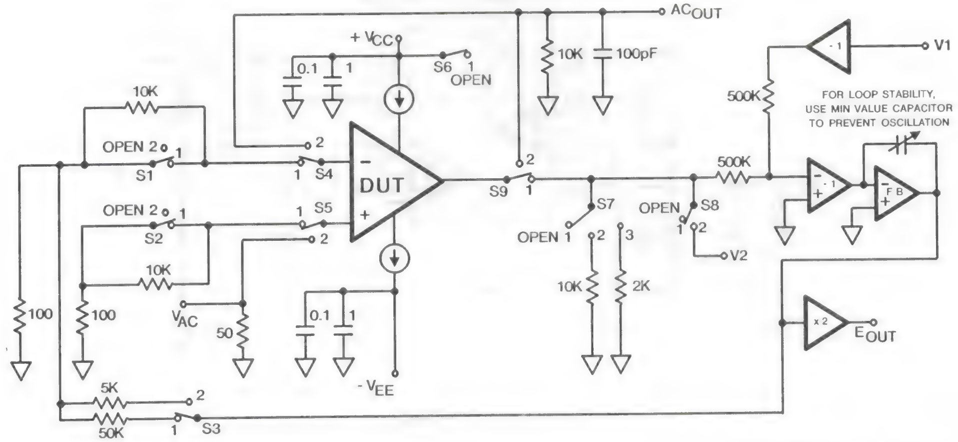
3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6
Group A Test Requirements	1, 2, 3, 4, 5, 6
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

Test Circuit (Applies to Tables 1 and 2)



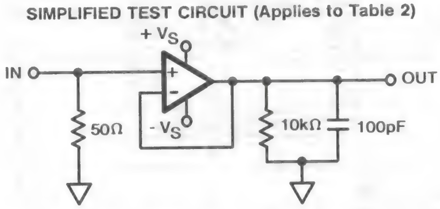
ONE OF TWO TEST LOOPS FOR THE HA - 5152/ 883

ALL RESISTORS = ± 1% (Ω)
ALL CAPACITORS = ± 10% (μF)

For Detailed Information, Refer to HA-5152/883 Test Tech Brief

Test Waveforms

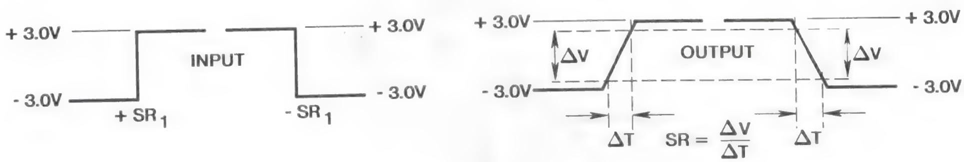
SIMPLIFIED TEST CIRCUIT (Applies to Table 2)



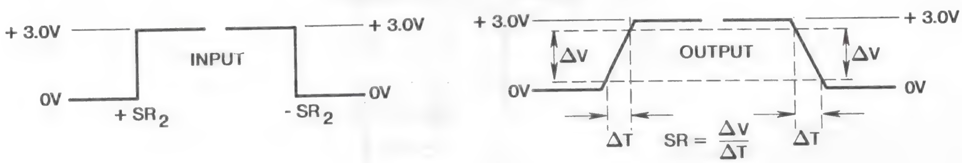
NOTE: $\pm V_{SUPPLY}$ ($\pm V_S$) Tested with ±15V and 0V, +5V. V_{IN} Slew Rate Maintained with Less Than 10V/µs Input for Voltage Follower Configuration.

SLEW RATE WAVEFORMS, A_V = 1V/V

$\pm V_{SUPPLY} = \pm 15V$

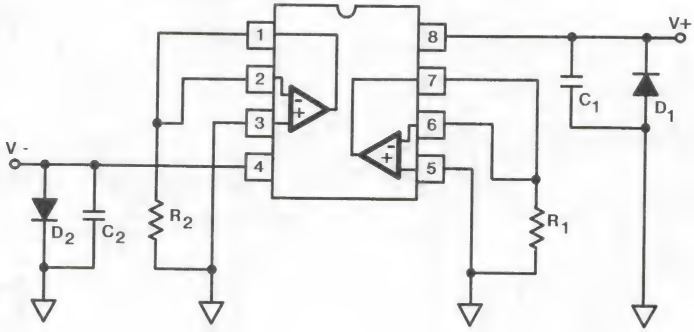


$+V_{SUPPLY} = 5V, -V_{SUPPLY} = 0V$

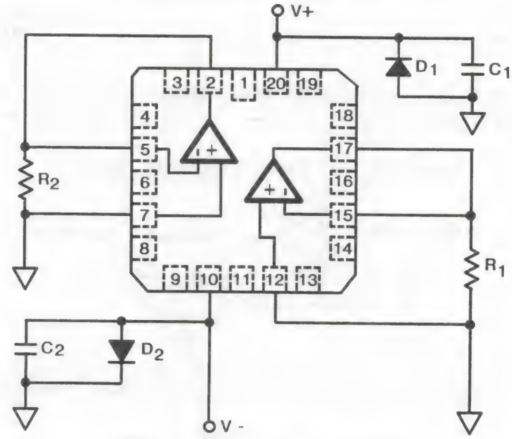


Burn-In Circuits

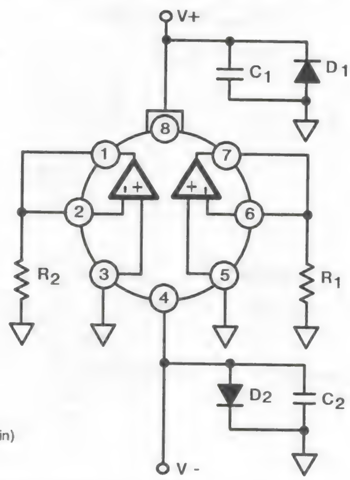
HA7-5152/883 CERAMIC DIP



HA4-5152/883 CERAMIC LCC



HA2-5152/883 TO-99 METAL CAN



NOTES:

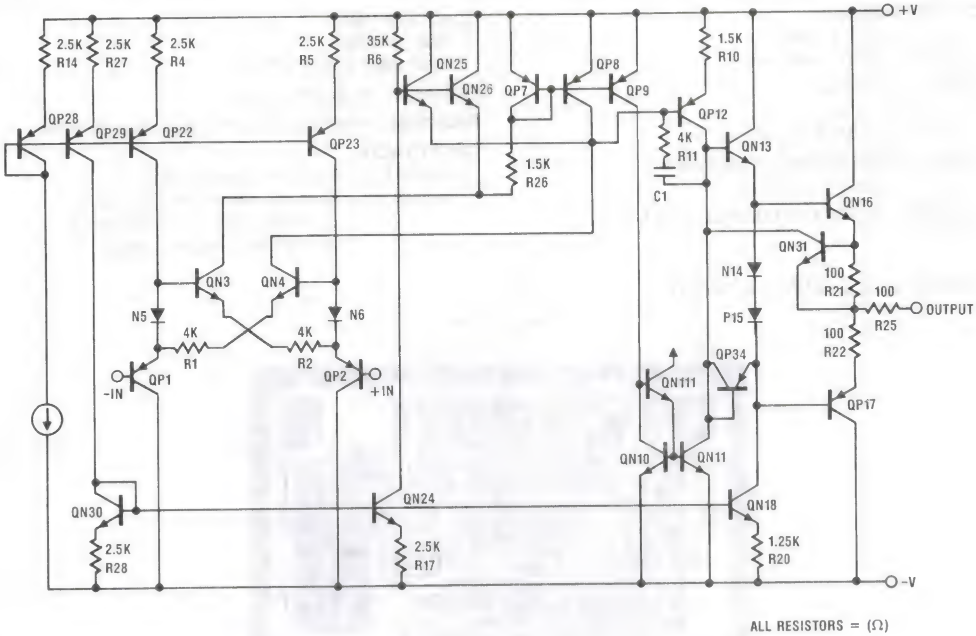
$R_1 = R_2 = 2k\Omega$, ±5%, 1/4W (Min)

$C_1 = C_2 = 0.01\mu F$/Socket (Min) or $0.1\mu F$/Row, (Min)

$D_1 = D_2$ = IN4002 or Equivalent/Board

$|(V+) - (V-)| = 30V$

Schematic Diagram (1/2 Of HA-5152/883)



3

OP AMPs & COMPARATORS

Die Characteristics

DIE DIMENSIONS:
53.9 x 103.1 x 19 mils
(1370 x 2620 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$0.6 \times 10^5 A/cm^2$ @ 2.5mA

SUBSTRATE POTENTIAL (Powered Up): V-

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

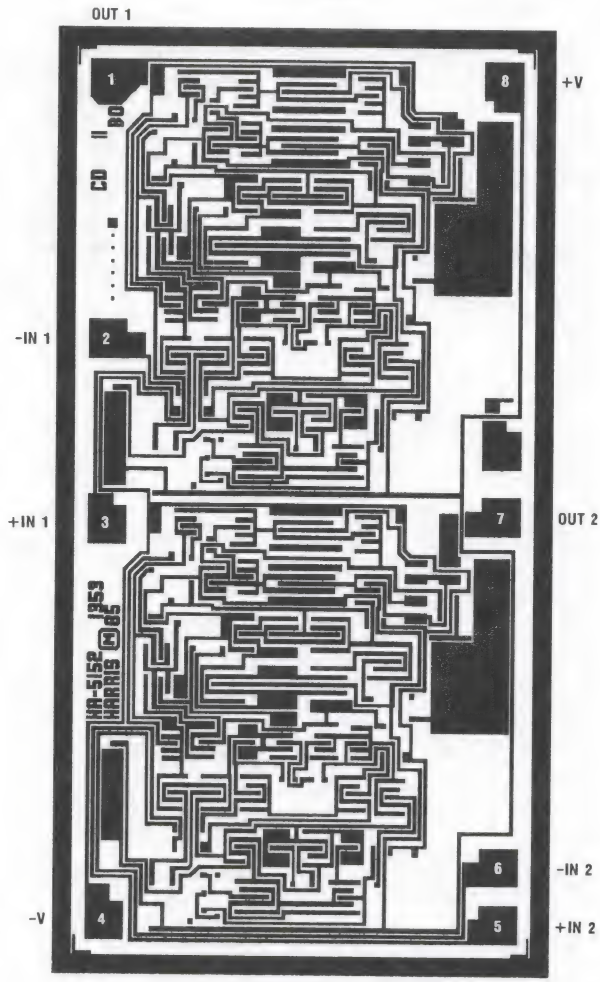
TRANSISTOR COUNT: 72

PROCESS: HFSB Bipolar/JFET Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)
Metal Can — 420°C (Max)

Metallization Mask Layout

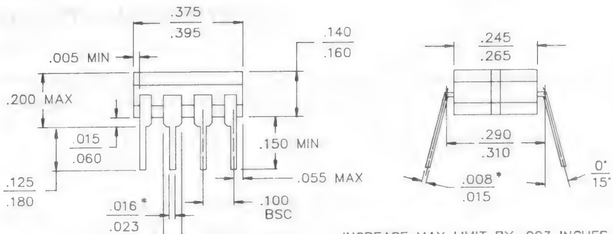
HA-5152/883



NOTE: Pad Numbers Refer to 8 Pin Ceramic Mini-DIP or Metal Can Package Pinouts Only.

Packaging †

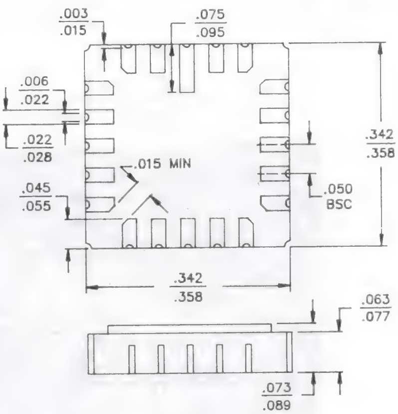
8 PIN CERAMIC DIP



* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

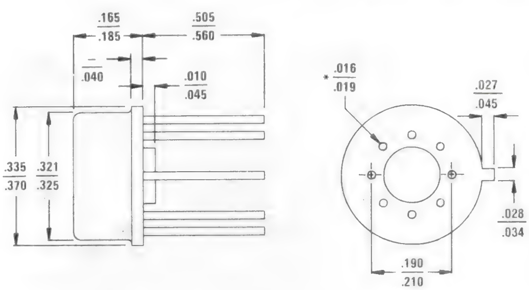
LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-4

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Ceramic, 90% Al_2O_3
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

8 PIN TO-99 METAL CAN



LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
Material: No Seal Material
Temperature: Room Temperature
Method: Resistance Weld
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic Bonded
COMPLIANT OUTLINE: 38510 A-1

*Dimension Maximum Limits Are Increased by 0.003 inches for Solder Dip Finish

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions

HA-5152

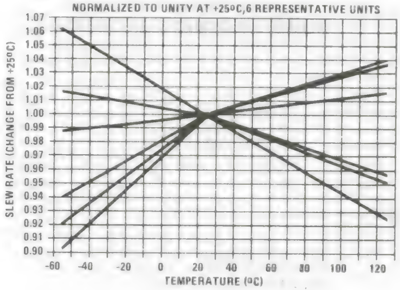
DESIGN INFORMATION

Dual, Low Power Operational Amplifier

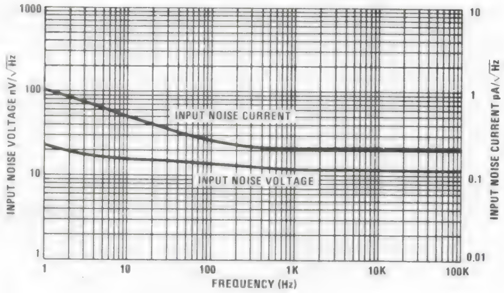
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

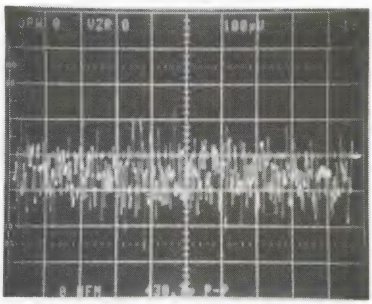
SLEW RATE vs. TEMPERATURE
Normalized to Unity at +25°C, 6 Representative Units



NOISE SPECTRAL DENSITY

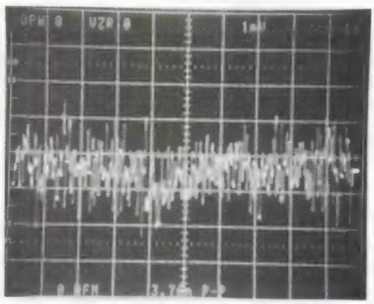


PEAK-TO-PEAK NOISE 0.1Hz TO 10Hz
$T_A = +25^oC$, $A_V = 1000V/V$



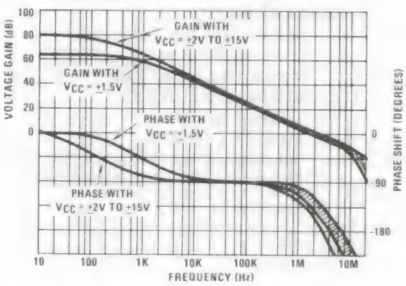
Vertical Scale: (Volts: 100µs/Div.)
Horizontal Scale: (Time: 1sec/Div.)
430nV$_{p-p}$ RTI

PEAK-TO-PEAK 0.1Hz TO 1MHz
$T_A = +25^oC$, $A_V = 1000V/V$

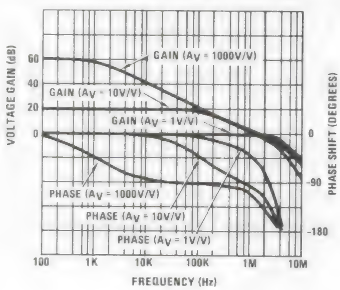


Vertical Scale: (Volts: 1mV/Div.)
Horizontal Scale: (Time: 1sec/Div.)
3.70µV$_{p-p}$ RTI

FREQUENCY RESPONSE vs. SUPPLY VOLTAGE
$T_A = +25^oC$, $R_L = 10K$, $C_L = 100pF$



FREQUENCY RESPONSE AT VARIOUS GAINS
$T_A = +25^oC$, $V_{CC} = \pm15V$, $R_L = 10K$, $C_L = 100pF$



DESIGN INFORMATION (Continued)

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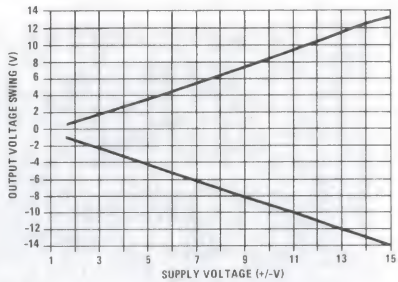
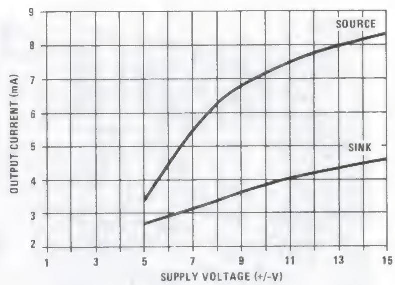
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

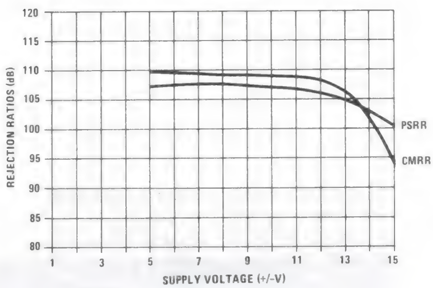
OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE
(+25°C)



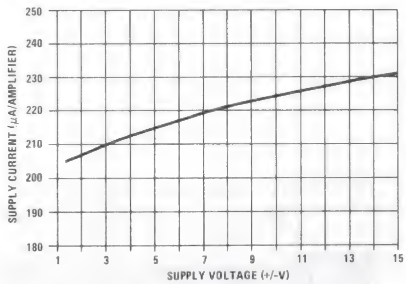
OUTPUT CURRENT vs. SUPPLY VOLTAGE
(+25°C)



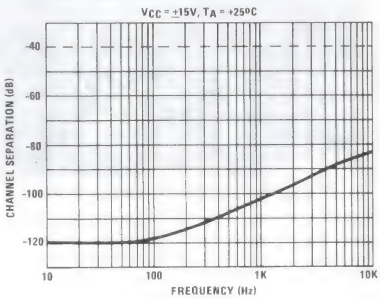
CMRR AND PSRR vs. SUPPLY VOLTAGE
(+25°C)



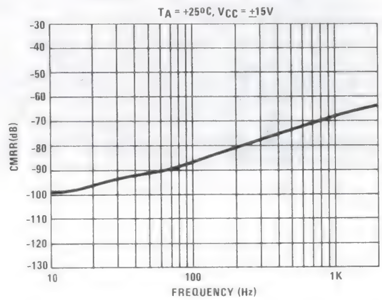
SUPPLY CURRENT vs. SUPPLY VOLTAGE
Per Amplifier (+25°C)



CHANNEL SEPARATION vs. FREQUENCY
$V_{CC} = \pm 15V$, $T_A = +25^oC$



CMRR vs. FREQUENCY
$T_A = +25^oC$, $V_{CC} = \pm 15V$



DESIGN INFORMATION (Continued)

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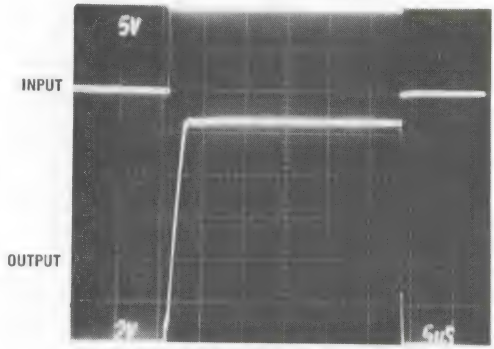
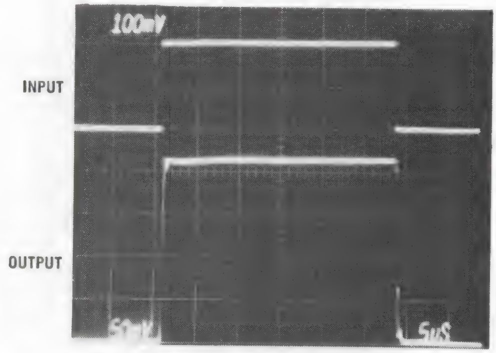
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

MEASURED LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 5V/Div.; Output = 2V/Div.)
Horizontal Scale: (Time: 5μs/Div.)



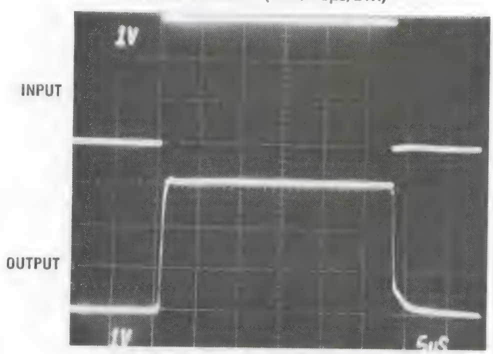
$+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$

MEASURED SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 100mV/Div.; Output = 50mV/Div.)
Horizontal Scale: (Time: 5μs/Div.)



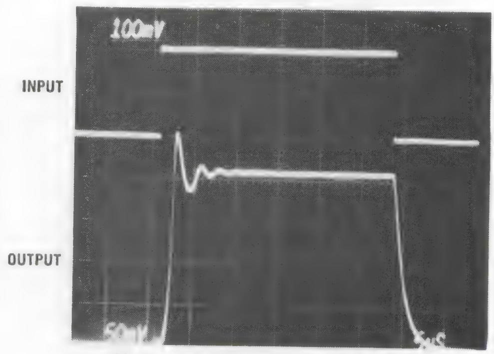
$+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$

MEASURED LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 1V/Div.; Output = 1V/Div.)
Horizontal Scale: (Time: 5μs/Div.)



$+V_{SUPPLY} = +5V$, $-V_{SUPPLY} = 0V$

MEASURED SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 100mV/Div.; Output = 50mV/Div.)
Horizontal Scale: (Time: 5μs/Div.)



$+V_{SUPPLY} = +5V$, $-V_{SUPPLY} = 0V$

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Applications Unless Otherwise Specified: T_A = +25°C, V_{SUPPLY} = ±15V

Independent Amplifier

The HA-5152 dual op amp consist of completely separate amplifier circuits. Unlike most duals, this device does not share a common bias network. Thus, one amplifier passing large, or noisy signals will have minimal effect on another channel carrying small, sensitive signals.

Loading

Although the standard load is 10kΩ, the HA-5152 is capable of driving resistive loads down to 2kΩ and capacitive loads beyond 300pF.

Input Stage

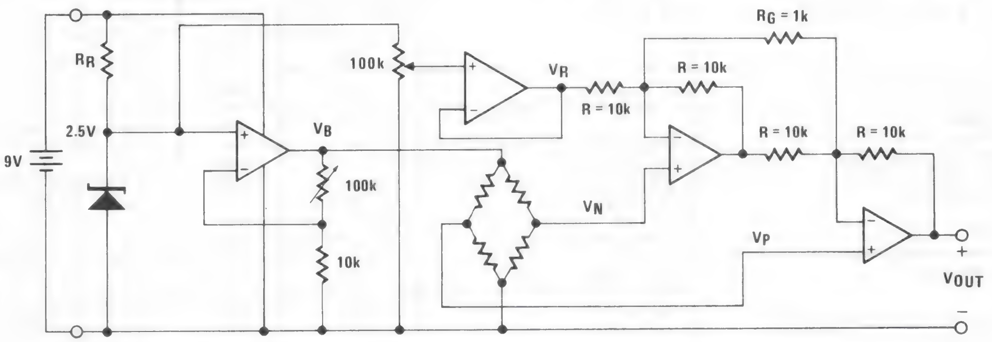
This amplifier uses a current amplifying input stage (see Application Note 544) and is not recommended for use in applications which involve large differential input voltages such as open-loop comparators. Most op amp applications use feedback and keep the input terminals at approximately the same voltage. The HA-5152 will perform well in these circuits as long as the input terminals see less than 7 volts differential.

Typical Applications

The low power consumption of the HA-5152 makes it ideal for applications like battery-powered instrumentation where the bridge amplifier circuit below would be used.

Choose a low-current zener voltage reference such as LM285Z-2.5 and select R_R accordingly. This circuit was evaluated using the resistor values shown and a laboratory voltage source for the 2.5V reference. With unmatched, off-the-shelf, 1% resistors, a gain accuracy of 1% to 2% can be expected. Temperature testing indicated a voltage offset tempco of less then 100μV/oC referred to output.

$$V_{OUT} = (V_P - V_N)\left[2\left(1 + \frac{R}{R_G}\right)\right] + V_R$$



DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = 0V, 5 to ±15V, R_L = 10kΩ, C_L = 100pF, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage	V_{CM} = 0V	Full	0.5	Table 1	mV
Offset Voltage Drift	Versus Temperature	Full	3	6	μV/°C
Bias Current	V_{CM} = 0V	+25°C, +125°C	130	Table 1	nA
		-55°C	150	Table 1	nA
Offset Current	V_{CM} = 0V	Full	5	Table 1	nA
Differential Input Resistance		+25°C	1.5	1	MΩ
Input Noise Voltage	f_O = 10Hz	+25°C	18	25	$nV/\sqrt{Hz}$
	f_O = 100Hz	+25°C	15	20	$nV/\sqrt{Hz}$
	f_O = 1kHz	+25°C	14.8	18	$nV/\sqrt{Hz}$
Input Noise Current	f_O = 10Hz	+25°C	0.5	0.7	$pA/\sqrt{Hz}$
	f_O = 100Hz	+25°C	0.3	0.6	$pA/\sqrt{Hz}$
	f_O = 1kHz	+25°C	0.25	0.4	$pA/\sqrt{Hz}$
Large Signal Voltage Gain	R_L = 10kΩ	+25°C, +125°C	150K	Table 1	V/V
		-55°C	100K	Table 1	V/V
CMRR		Full	105	Table 1	dB
PSRR		Full	105	Table 1	dB
Unity Gain Bandwidth	f @ -3dB	+25°C	1.3	0.7	MHz
+ Slew Rate	V_S = 0V, 5V	-55°C	4	2	V/μs
	V_S = 0V, 5V to ±15V	+25°C, +125°C	6.5	4	V/μs
- Slew Rate	V_S = 0V, 5V	Full	12	2	V/μs
	V_S = ±15V	Full	25	4	V/μs
+ I_{OUT}		+25°C, +125°C	3	1.5	mA
		-55°C	0.8	0.4	mA
- I_{OUT}		-55°C, +25°C	-7.5	-6	mA
		+125°C	-4.5	-3.5	mA
Rise Time	V_S = ±15V, V_O = 200mV	Full	250	500	ns
Fall Time	V_S = ±15V, V_O = -200mV	-55°C, +25°C	110	300	ns
		+125°C	200	400	ns
Overshoot	V_S = ±15V, V_O = ±200mV	Full	2	10	%
Supply Current (All Four Amplifiers)	V_S = 0V, 5V	+25°C	350	Table 1	μA
	V_S = ±15V	+25°C	470	Table 1	μA

HARRIS

HA-5154/883

Quad, Low Power Operational Amplifier

January 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low Supply Current (All 4 Amplifiers) .... 1mA (Max)
- Wide Supply Voltage Range .... Single 3V to 30V or Dual ±1.5 to ±15V
- High Slew Rate .... +S.R. 4V/μs (Min) 6V/μs (Typ)
- Low V_{OS} Drift (Over Full Temp) .... 3μV/^{o}C (Typ)
- Low Noise (1kHz) .... 15nV/$\sqrt{Hz}$ (Typ)
- 100% Tested at ±15V and +5V Power Supplies
- Dielectric Isolation

Applications

- Portable Instruments
- Meter Amplifiers
- Telephone Headsets
- Microphone Amplifiers
- Remote Sensor/Transmitter
- Battery Powered Equipment
- For Further Design Ideas See App. Note 544

Description

The HA-5154/883 quad operational amplifier completes the family of dielectrically isolated bipolar amplifiers designed to provide excelllent AC performance while drawing less than 250μA of supply current per amplifier at +25^{o}C. This series consists of single (5151), dual (5152) or quad (5154), unity gain stable amplifiers which are especially well suited for portable and lightweight equipment where available power is limited.

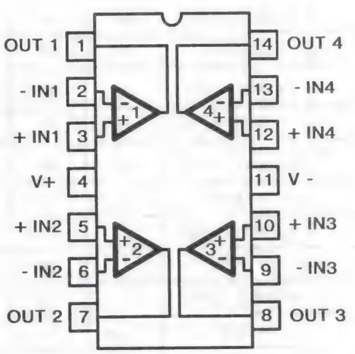
The HA-5154/883 combines superior low power AC performance with DC precision not usually found in general purpose amplifiers. The DC performance is centered around low input offset voltage (3mV), low offset voltage drift (3μV/^{o}C), and low input bias current (250nA). This is combined with a very low input noise voltage of 15nV/$\sqrt{Hz}$ at 1kHz.

The AC performance of the HA-5154/883 surpasses that of typical low power amplifiers with 4V/μs slew rate and a full power bandwidth of 64kHz. This makes the HA-5154/883 an excellent choice for virtually all audio processing applications as well as remote sensor/transmitter designs requiring both low power and high speed. The suitability of the HA-5154/883 for remote and low power operation is further enhanced by the wide range of supply voltages (±1.5V to ±15V) as well as single supply operation (3V to 30V).

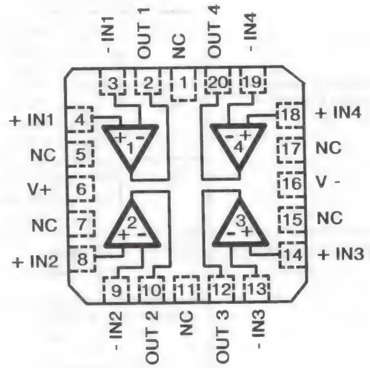
The HA-5154/883 is available in 14 pin Ceramic DIP or 20 pad Ceramic LCC, and is interchangeable with most other operational amplifiers in their class.

Pinouts

HA1-5154/883 (CERAMIC DIP)
TOP VIEW



HA4-5154/883 (CERAMIC LCC)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage 7V
Voltage at Either Input Terminal .... V+ to V-
Output Current .... Full Short Circuit Protection
Output Current Duration .... Indefinite, One Amplifier Shorted to Ground
Junction Temperature (T_J) .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... <2000V
Lead Temperature (Soldering 10 sec) .... +275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	75°C/W	17°C/W
Ceramic LCC Package	76°C/W	19°C/W

Package Power Dissipation Limit at +75°C For $T_J \leq$ +175°C
Ceramic DIP Package 1.33mW
Ceramic LCC Package 1.32W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 13.3mW/°C
Ceramic LCC Package .... 13.2mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±1.5V to ±15V or 3V to 30V
$V_{INcm} \leq 1/2\ (V+ - V-)$
$R_L \geq 10k\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $R_{SOURCE} = 100\Omega$, $R_{LOAD} = 500k\Omega$, $V_{OUT} = 0V$, Unless Otherwise Specified.
Subscript 1 Refers to Supply Voltages ($\pm V_S$) = ±15V, Subscript 2 Refers to $+V_S = 5.0V$, $-V_S = 0.0V$.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO1}	$V_{CM} = 0V$	1	+25°C	-3	3	mV
			2, 3	+125°C, -55°C	-4	4	mV
	V_{IO2}	$V_{CM} = 0V$, $V_{OUT} = 1.4V$	1	+25°C	-3	3	mV
			2, 3	+125°C, -55°C	-4	4	mV
Input Bias Current	$+I_{B1}$	$V_{CM} = 0V$, $+R_S = 10k\Omega$, $-R_S = 100\Omega$	1	+25°C	-250	250	nA
			2, 3	+125°C, -55°C	-400	400	nA
	$-I_{B1}$	$V_{CM} = 0V$, $+R_S = 100\Omega$, $-R_S = 10k\Omega$	1	+25°C	-250	250	nA
			2, 3	+125°C, -55°C	-400	400	nA
	$+I_{B2}$	$V_{CM} = 0V$, $V_{OUT} = 1.4V$, $+R_S = 10k\Omega$, $-R_S = 100\Omega$	1	+25°C	-250	250	nA
			2, 3	+125°C, -55°C	-400	400	nA
	$-I_{B2}$	$V_{CM} = 0V$, $V_{OUT} = 1.4V$, $+R_S = 100\Omega$, $-R_S = 10k\Omega$	1	+25°C	-250	250	nA
			2, 3	+125°C, -55°C	-400	400	nA
Input Offset Current	I_{IO1}	$V_{CM} = 0V$, $+R_S = 10k\Omega$, $-R_S = 10k\Omega$	1	+25°C	-50	50	nA
			2, 3	+125°C, -55°C	-80	80	nA
	I_{IO2}	$V_{CM} = 0V$, $V_{OUT} = 1.4V$, $+R_S = 10k\Omega$, $-R_S = 10k\Omega$	1	+25°C	-50	50	nA
			2, 3	+125°C, -55°C	-80	80	nA
Common Mode Range	$+CMR_1$	$V+ = 5V$, $V- = -25V$	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	$-CMR_1$	$V+ = 25V$, $V- = -5V$	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
	$+CMR_2$	$V+ = 5V$ to $2V$, $V- = 0V$ to $-3V$, $V_{OUT} = 1.4V$ to $-1.6V$	1	+25°C	0 to 3	-	V
			2, 3	+125°C, -55°C	0 to 3	-	V

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: $R_{SOURCE} = 100\Omega$, $R_{LOAD} = 500k\Omega$, $V_{OUT} = 0V$, Unless Otherwise Specified.
Subscript 1 Refers to Supply Voltages ($\pm V_S$) = ±15V; Subscript 2 Refers to $+V_S = 5.0V$, $-V_S = 0.0V$.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Large Signal Voltae Gain	$+A_{VOL1}$	V_{OUT} = 0V and 10V $R_L = 10k\Omega$	4	+25°C	50	-	kV/V
			5, 6	+125°C, -55°C	25	-	kV/V
	$-A_{VOL1}$	V_{OUT} = 0V and -10V $R_L = 10k\Omega$	4	+25°C	50	-	kV/V
			5, 6	+125°C, -55°C	25	-	kV/V
	$+A_{VOL2}$	V_{OUT} = 1.4V and 2.5V $R_L = 10k\Omega$	4	+25°C	50	-	kV/V
			5, 6	+125°C, -55°C	25	-	kV/V
Common Mode Rejection Ratio	$+CMRR_1$	ΔV_{CM} = 10V +V = 5V -V = -25V V_{OUT} = -10V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	$-CMRR_1$	ΔV_{CM} = 10V +V = 25V -V = -5V V_{OUT} = 10V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	$+CMRR_2$	ΔV_{CM} = 0V to 3V +V = 2V -V = -3V V_{OUT} = -3V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
Output Voltage Swing	$+V_{OUT1}$	$R_L = 10k\Omega$	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	$-V_{OUT1}$	$R_L = 10k\Omega$	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
	$+V_{OUT2}$	$R_L = 10k\Omega$ Terminated at 2.5V	1	+25°C	3.2	-	V
			2, 3	+125°C, -55°C	2.9	-	V
	$-V_{OUT2}$	$R_L = 10k\Omega$ Terminated at 2.5V	1	+25°C	-	1	V
			2, 3	+125°C, -55°C	-	1.2	V
Quiescent Power Supply Current (All Four Amplifiers)	$+I_{CC1}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-	1	mA
			2, 3	+125°C, -55°C	-	1.1	mA
	$-I_{CC1}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-1	-	mA
			2, 3	+125°C, -55°C	-1.1	-	mA
	$+I_{CC2}$	V_{OUT} = 1.4V I_{OUT} = 0mA	1	+25°C	-	1	mA
			2, 3	+125°C, -55°C	-	1.1	mA
Power Supply Rejection Ratio	$+PSRR_1$	ΔV_{SUP} = 10V +V = 10V, -V = -15V +V = 20V, -V = -15V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	$-PSRR_1$	ΔV_{SUP} = 10V +V = 15V, -V = -10V +V = 15V, -V = -20V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	$+PSRR_2$	ΔV_{SUP} = 10V +V = 5V, -V = 0V +V = 15V, -V = 0V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
Channel Separation	±CS	$R_L = 10k\Omega$	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $R_{SOURCE} = 50\Omega$, $R_{LOAD} = 10k\Omega$, $C_{LOAD} = 100pF$, $V_{OUT} = 0V$, Unless Otherwise Specified.
Subscript 1 Refers to Supply Voltages ($\pm V_S$) = ±15V; Subscript 2 Refers to $+V_S = 5.0V$, $-V_S = 0.0V$.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Slew Rate	$+SR_1$	$V_{OUT} = -3V$ to $3V$ V_{IN} S.R. $\leq 25V/\mu s$	4	+25°C	4	-	V/µs
	$-SR_1$	$V_{OUT} = 3V$ to $-3V$ V_{IN} S.R. $\leq 25V/\mu s$	4	+25°C	4	-	V/µs
	$+SR_2$	$V_{OUT} = 0V$ to $3V$ V_{IN} S.R. $\leq 25V/\mu s$	4	+25°C	2	-	V/µs
	$-SR_2$	$V_{OUT} = 3V$ to $0V$ V_{IN} S.R. $\leq 25V/\mu s$	4	+25°C	2	-	V/µs

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $R_{SOURCE} = 50\Omega$, $R_{LOAD} = 10k\Omega$, $C_{LOAD} = 100pF$, $A_V = 1V/V$, Unless Otherwise Specified.
Subscript 1 Refers to Supply Voltages ($\pm V_S$) = ±15V; Subscript 2 Refers to $+V_S = 5.0V$, $-V_S = 0.0V$.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Gain Bandwidth Product	GBWP	$V_O = 200mV$, $f_O = 10kHz$	1	+25°C	0.7	-	MHz
Full Power Bandwidth	$FPBW_1$	$V_{PEAK} = 10V$	1, 2	+25°C	64	-	kHz
	$FPBW_2$	$V_{PEAK} = 1.1V$ $V_{Ref} = 2.5V$	1, 2	+25°C	290	-	kHz
Minimum Closed Loop Stable Gain	CLSG	$R_L = 10k\Omega$, $C_L = 100pF$	1	-55°C to +125°C	1	-	V/V
Quiecent Power Consumption	PC_1	$V_{OUT} = 0V$, $I_{OUT} = 0mA$	1, 3	-55°C to +125°C	-	33	mW
	PC_2	$V_{OUT} = 1.4V$, $I_{OUT} = 0mA$	1, 3	-55°C to +125°C	-	5.5	mW

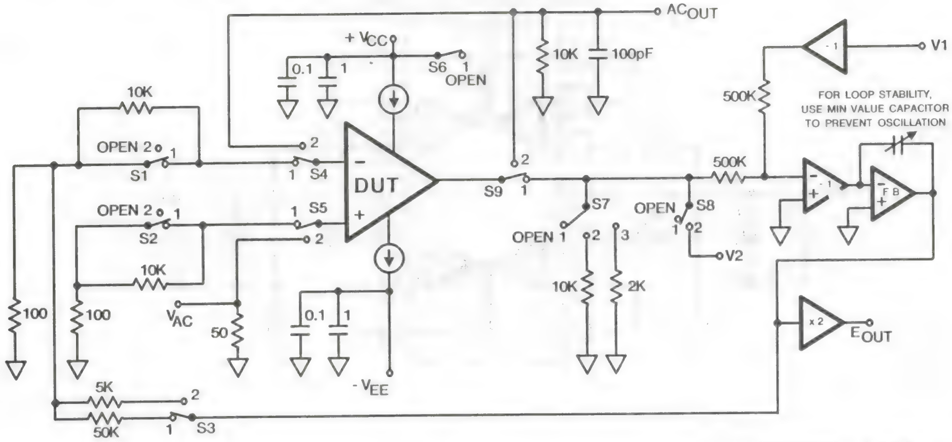
NOTES:
1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).
3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6
Group A Test Requirements	1, 2, 3, 4, 5, 6
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

Test Circuit (Applies to Tables 1 and 2)



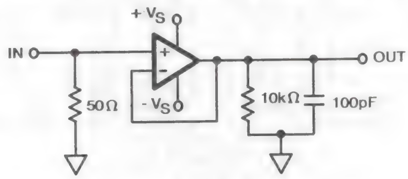
ONE OF FOUR TEST LOOPS FOR THE HA - 5154/ 883

ALL RESISTORS = ± 1% (Ω)
ALL CAPACITORS = ± 10% (μF)

For Detailed Information, Refer to HA-5154/883 Test Tech Brief

Test Waveforms

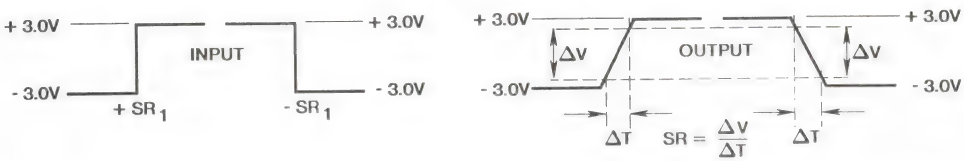
SIMPLIFIED TEST CIRCUIT (Applies to Table 2)



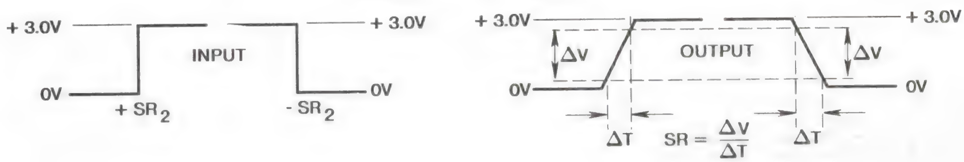
NOTE: $\pm V_{SUPPLY}$ ($\pm V_S$) Tested with ±15V and 0V, +5V. V_{IN} Slew Rate Maintained with Less Than 10V/μs Input for Voltage Follower Configuration.

SLEW RATE WAVEFORMS, A_V = 1V/V

$\pm V_{SUPPLY} = \pm 15V$



$+V_{SUPPLY} = 5V$, $-V_{SUPPLY} = 0V$

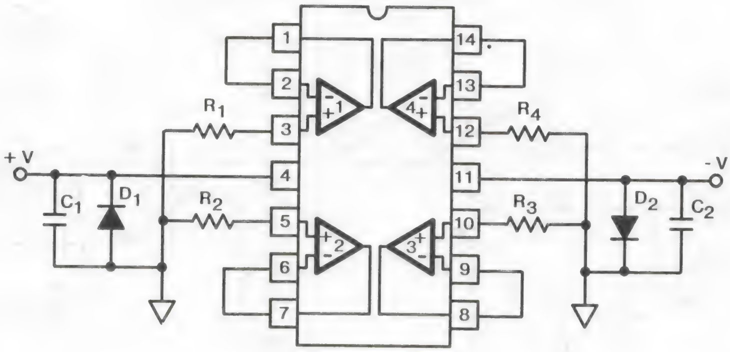


3

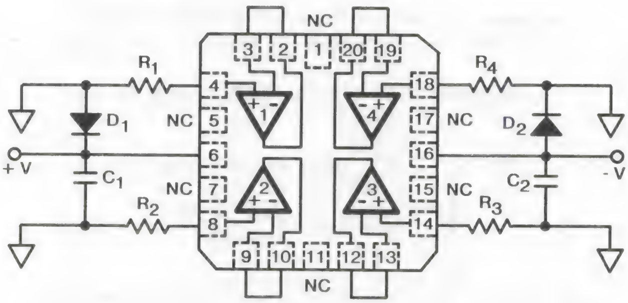
OP AMPs & COMPARATORS

Burn-In Circuits

HA1-5154/883 CERAMIC DIP



HA4-5154/883 CERAMIC LCC



NOTES:

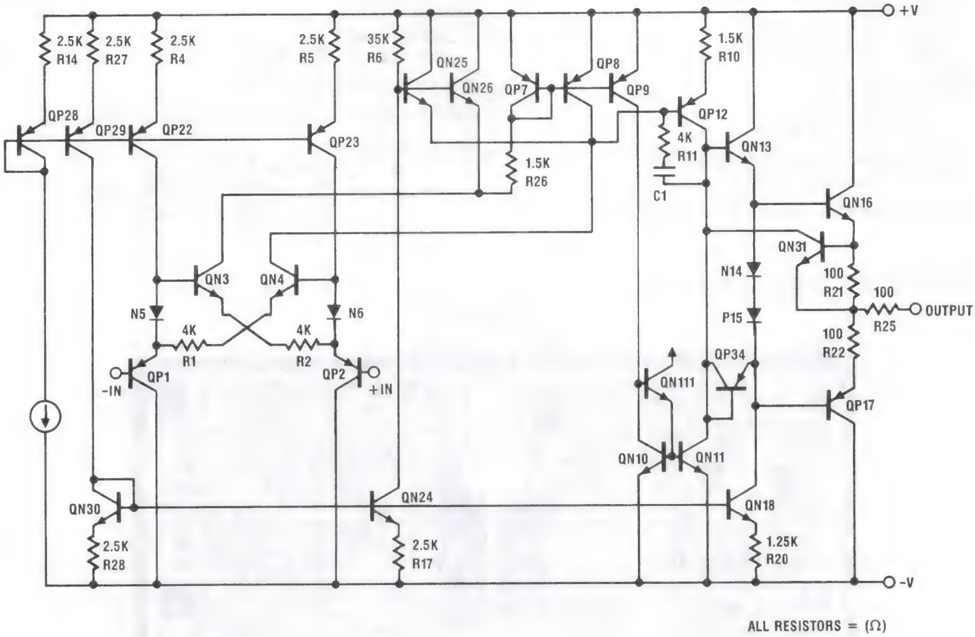
$R_1 = R_2 = R_3 = R_4 = 1M\Omega$, ±5%, 1/4W (Min)

$C_1 = C_2 = 0.01\mu F$/Socket (Min) or $0.1\mu F$/Row, (Min)

$D_1 = D_2$ = IN4002 or Equivalent/Board

$|(V+) - (V-)| = 30V$

Schematic Diagram (1/4 Of HA-5154/883)



3

OP AMPs & COMPARATORS

Die Characteristics

DIE DIMENSIONS:
95.7 x 101.6 x 19 mils
(2430 x 2580 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
0.45 x 10^5A/cm^2 @ 2.5mA

SUBSTRATE POTENTIAL (Powered Up): V-

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

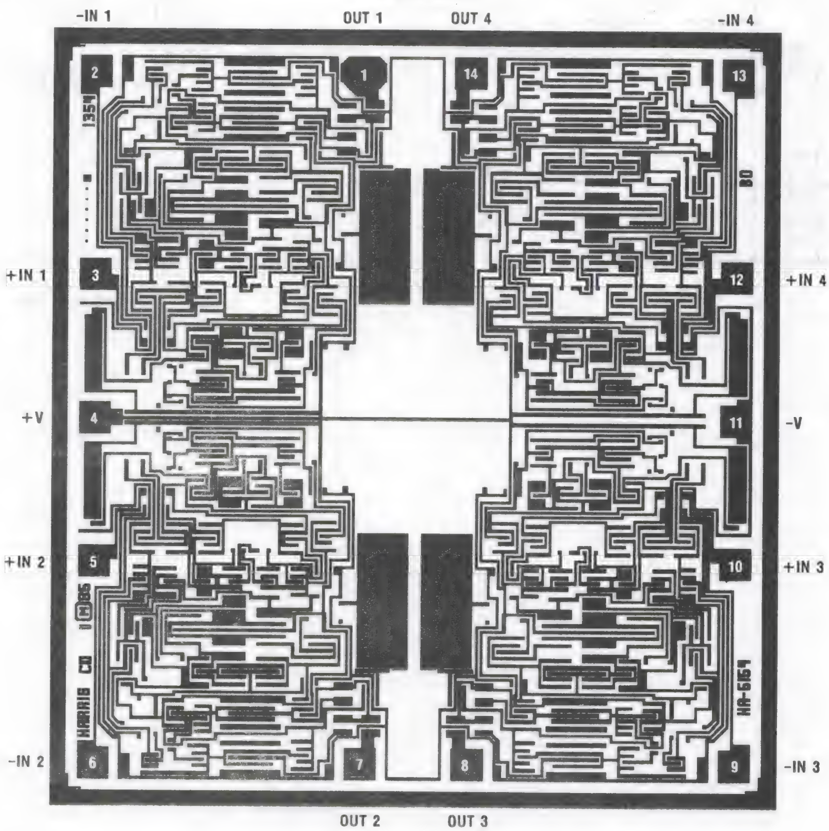
TRANSISTOR COUNT: 144

PROCESS: HFSB Bipolar/JFET Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

Metallization Mask Layout

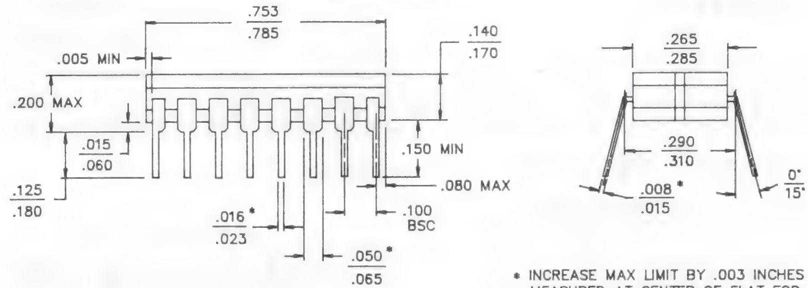
HA-5154/883



NOTE: Pad Numbers Refer to 14 Pin Ceramic DIP Package Pinout Only.

Packaging†

14 PIN CERAMIC DIP



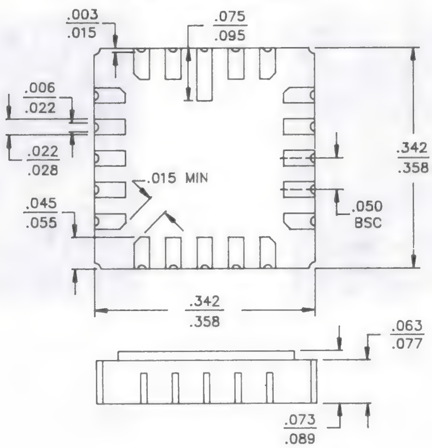
* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
- Material: Glass Frit
- Temperature: 450°C ± 10°C
- Method: Furnace Seal

INTERNAL LEAD WIRE:
- Material: Aluminum
- Diameter: 1.25 Mil
- Bonding Method: Ultrasonic

COMPLIANT OUTLINE: 38510 D-1

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
- Material: Gold/Tin (80/20)
- Temperature: 320°C ± 10°C
- Method: Furnace Braze

INTERNAL LEAD WIRE:
- Material: Aluminum
- Diameter: 1.25 Mil
- Bonding Method: Ultrasonic

COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

DESIGN INFORMATION

Quad, Low Power Operational Amplifier

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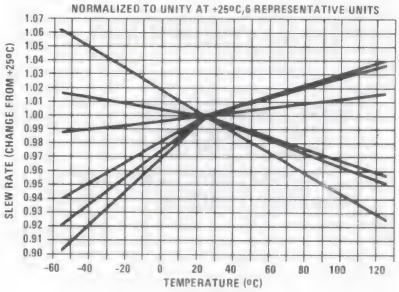
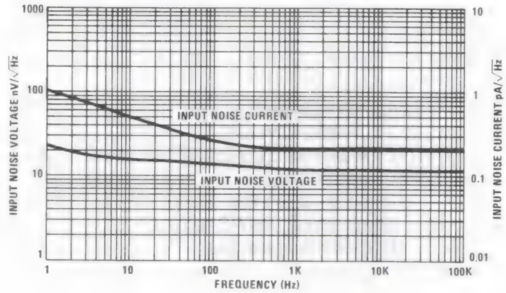
Typical Performance Curves

Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

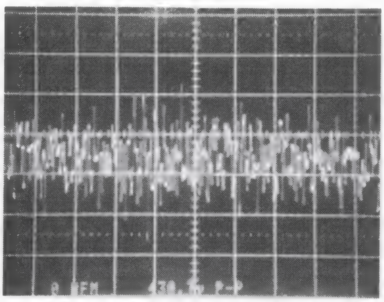
SLEW RATE vs. TEMPERATURE
Normalized to Unity at +25°C, 6 Representative Units



NOISE SPECTRAL DENSITY

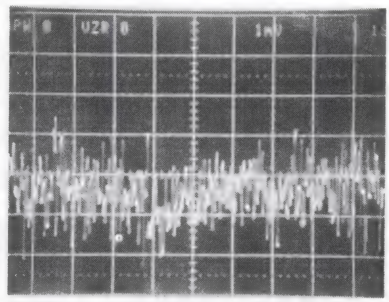


PEAK-TO-PEAK NOISE 0.1Hz TO 10Hz
$T_A = +25^oC$, $A_V = 1000V/V$



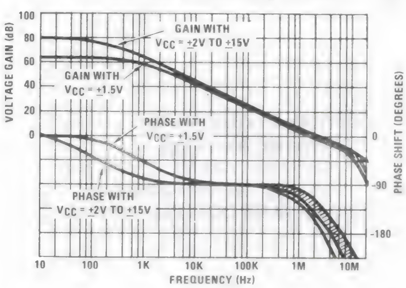
Vertical Scale: (Volts: 100µs/Div.)
Horizontal Scale: (Time: 1sec/Div.)
$430nV_{p-p}$ RTI

PEAK-TO-PEAK 0.1Hz TO 1MHz
$T_A = +25^oC$, $A_V = 1000V/V$

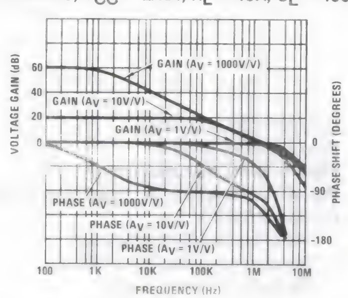


Vertical Scale: (Volts: 1mV/Div.)
Horizontal Scale: (Time: 1sec/Div.)
$3.70\mu V_{p-p}$ RTI

FREQUENCY RESPONSE vs. SUPPLY VOLTAGE
$T_A = +25^oC$, $R_L = 10K$, $C_L = 100pF$



FREQUENCY RESPONSE AT VARIOUS GAINS
$T_A = +25^oC$, $V_{CC} = \pm 15V$, $R_L = 10K$, $C_L = 100pF$



DESIGN INFORMATION (Continued)

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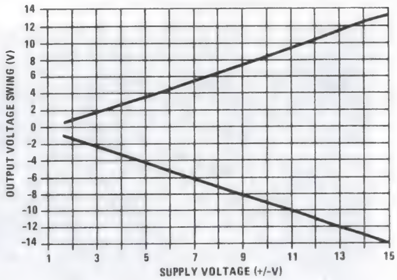
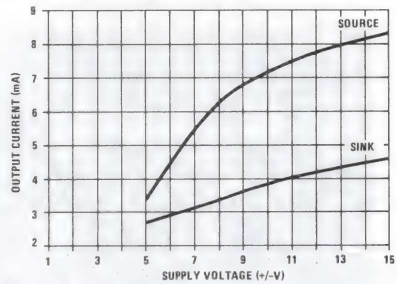
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

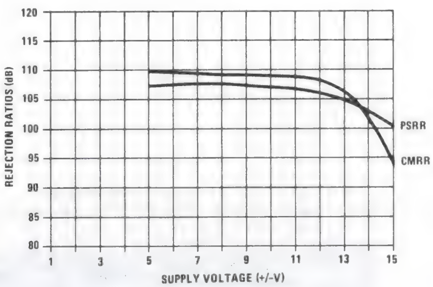
OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE (+25°C)



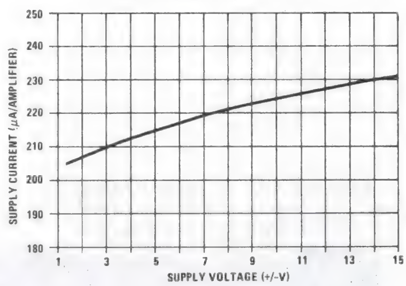
OUTPUT CURRENT vs. SUPPLY VOLTAGE (+25°C)



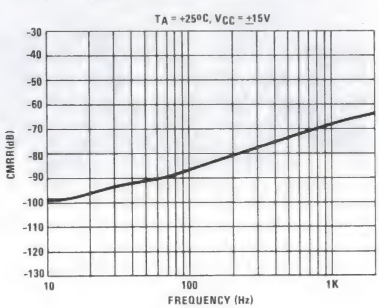
CMRR AND PSRR vs. SUPPLY VOLTAGE (+25°C)



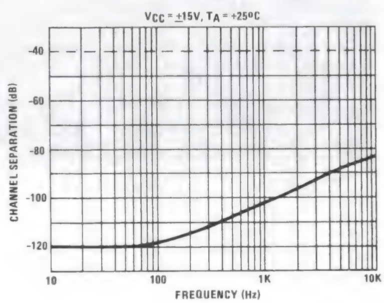
SUPPLY CURRENT vs. SUPPLY VOLTAGE Per Amplifier (+25°C)



CHANNEL SEPARATION vs. FREQUENCY $V_{CC} = \pm15V$, $T_A = +25^oC$



CMRR vs. FREQUENCY $T_A = +25^oC$, $V_{CC} = \pm15V$

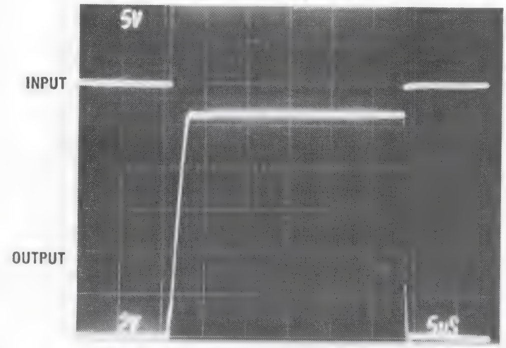


DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

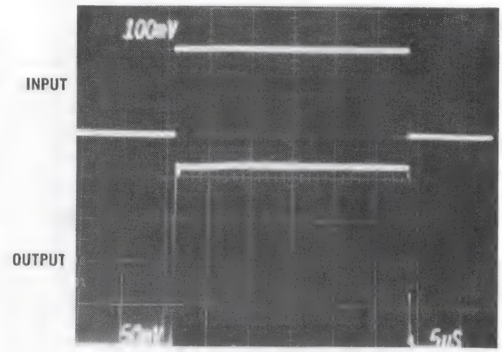
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

MEASURED LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 5V/Div.; Output = 2V/Div.)
Horizontal Scale: (Time: 5µs/Div.)



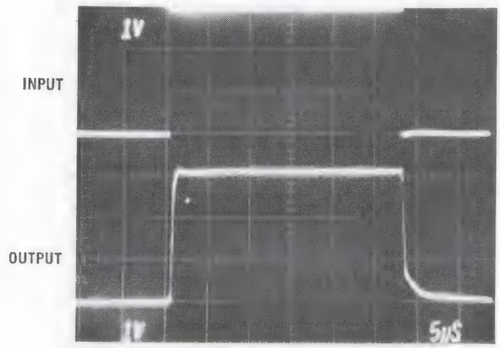
$+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$

MEASURED SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 100mV/Div.; Output = 50mV/Div.)
Horizontal Scale: (Time: 5µs/Div.)



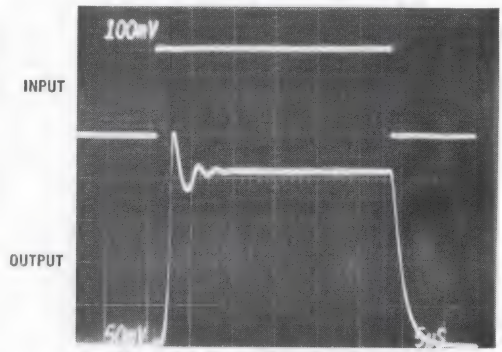
$+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$

MEASURED LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 1V/Div.; Output = 1V/Div.)
Horizontal Scale: (Time: 5µs/Div.)



$+V_{SUPPLY} = +5V$, $-V_{SUPPLY} = 0V$

MEASURED SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 100mV/Div.; Output = 50mV/Div.)
Horizontal Scale: (Time: 5µs/Div.)



$+V_{SUPPLY} = +5V$, $-V_{SUPPLY} = 0V$

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Applications Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

Independent Amplifier

The HA-5154 quad op amp consist of completely separate amplifier circuits. Unlike most quads, this device does not share a common bias network. Thus, one amplifier passing large, or noisy signals will have minimal effect on another channel carrying small, sensitive signals.

Loading

Although the standard load is 10kΩ, the HA-5154 is capable of driving resistive loads down to 2kΩ and capacitive loads beyond 300pF.

Input Stage

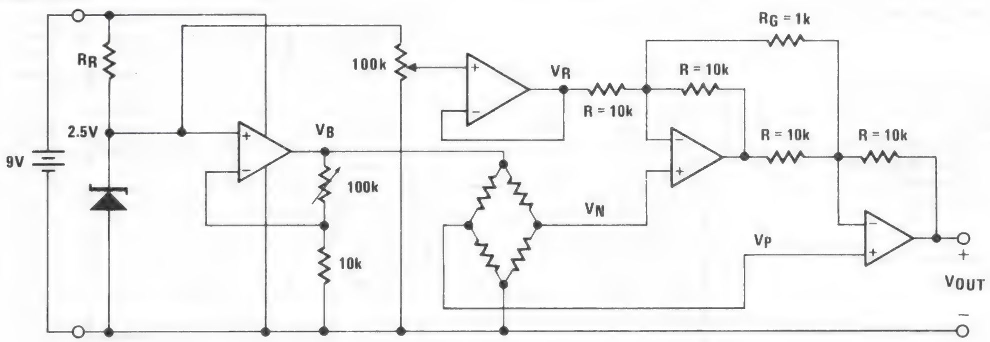
This amplifier uses a current amplifying input stage (see Application Note 544) and is not recommended for use in applications which involve large differential input voltages such as open-loop comparators. Most op amp applications use feedback and keep the input terminals at approximately the same voltage. The HA-5154 will perform well in these circuits as long as the input terminals see less than 7 volts differential.

Typical Applications

The low power consumption of the HA-5154 makes it ideal for applications like battery-powered instrumentation where the bridge amplifier circuit below would be used.

Choose a low-current zener voltage reference such as LM285Z-2.5 and select R_R accordingly. This circuit was evaluated using the resistor values shown and a laboratory voltage source for the 2.5V reference. With unmatched, off-the-shelf, 1% resistors, a gain accuracy of 1% to 2% can be expected. Temperature testing indicated a voltage offset tempco of less then 100µV/oC referred to output.

$$V_{OUT} = (V_P - V_N)\left[2\left(1 + \frac{R}{R_G}\right)\right] + V_R$$



DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = 0V, 5 to ±15V, R_L = 10kΩ, C_L = 100pF, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage	V_{CM} = 0V	Full	0.5	Table 1	mV
Offset Voltage Drift	Versus Temperature	Full	3	6	μV/°C
Bias Current	V_{CM} = 0V	+25°C, +125°C	130	Table 1	nA
		-55°C	150	Table 1	nA
Offset Current	V_{CM} = 0V	Full	5	Table 1	nA
Differential Input Resistance		+25°C	1.5	1	MΩ
Input Noise Voltage	f_O = 10Hz	+25°C	18	25	nV/$\sqrt{Hz}$
	f_O = 100Hz	+25°C	15	20	nV/$\sqrt{Hz}$
	f_O = 1kHz	+25°C	14.8	18	nV/$\sqrt{Hz}$
Input Noise Current	f_O = 10Hz	+25°C	0.5	0.7	pA/$\sqrt{Hz}$
	f_O = 100Hz	+25°C	0.3	0.6	pA/$\sqrt{Hz}$
	f_O = 1kHz	+25°C	0.25	0.4	pA/$\sqrt{Hz}$
Large Signal Voltage Gain	R_L = 10kΩ	+25°C, +125°C	150K	Table 1	V/V
		-55°C	100K	Table 1	V/V
CMRR		Full	105	Table 1	dB
PSRR		Full	105	Table 1	dB
Unity Gain Bandwidth	f @ -3dB	+25°C	1.3	0.7	MHz
+ Slew Rate	V_S = 0V, 5V	-55°C	4	2	V/μs
	V_S = 0V, 5V to ±15V	+25°C, +125°C	6.5	4	V/μs
- Slew Rate	V_S = 0V, 5V	Full	12	2	V/μs
	V_S = ±15V	Full	25	4	V/μs
+ I_{OUT}		+25°C, +125°C	3	1.5	mA
		-55°C	0.8	0.4	mA
- I_{OUT}		-55°C, +25°C	-7.5	-6	mA
		+125°C	-4.5	-3.5	mA
Rise Time	V_S = ±15V, V_O = 200mV	Full	250	500	ns
Fall Time	V_S = ±15V, V_O = -200mV	-55°C, +25°C	110	300	ns
		+125°C	200	400	ns
Overshoot	V_S = ±15V, V_O = ±200mV	Full	2	10	%
Supply Current (All Four Amplifiers)	V_S = 0V, 5V	+25°C	700	Table 1	μA
	V_S = ±15V	+25°C	880	Table 1	μA

HA-5177/883

Ultra-Low Offset Voltage Operational Amplifier

January 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low Offset Voltage .... 60μV (Max) 10μV (Typ)
- Low Offset Voltage Drift .... 0.6μV/°C (Max) 0.1μV/°C (Typ)
- High Voltage Gain .... 126dB (Min) 150dB (Typ)
- High CMRR.............................. 110dB (Min) 140dB (Typ)
- High PSRR .... 110dB (Min) 135dB (Typ)
- Low Noise .... $11nV/\sqrt{Hz}$ (Max) $9nV/\sqrt{Hz}$ (Typ)
- Low Power Consumption .... 51mW (Max)
- Wide Gain Bandwidth Product .... 2MHz (Min)
- Unity Gain Stable

Applications

- High Gain Instrumentation Amplifiers
- Precision Control Systems
- Precision Integrators
- High Resolution Data Converters
- Precision Threshold Detectors
- Low Level Transducer Amplifiers

Description

The HA-5177/883 is a monolithic, all bipolar, precision operational amplifier, utilizing Harris Dielectric Isolation and advance processing techniques. This design features a combination of precision input characteristics, wide gain bandwidth (2MHz) and high speed (0.5V/μs min) and is an improved version of the HA-5135/883.

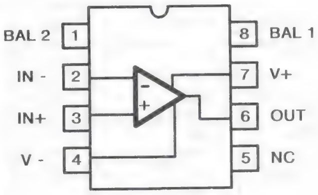
The HA-5177/883 uses advanced matching techniques and laser trimming to produce low offset voltage (10μV typ, 60μV max) and low offset voltage drift (0.1μV/°C typ, 0.6μV/°C max). This design also features low voltage noise ($9nV/\sqrt{Hz}$ typ), Low current noise ($0.32pA/\sqrt{Hz}$ typ), nanoamp input currents, and 126dB minimum gain.

These outstanding features along with high CMRR (140dB typ, 110dB min) and high PSRR (135dB typ, 110dB min) make this unity gain stable amplifier ideal for high resolution data acquisition systems, precision integrators, and low level transducer amplifiers.

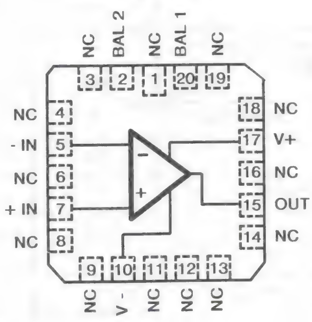
The HA-5177/883 can be used as a direct replacement for the OP05, OP07, and OP77 while offering higher bandwidth and slew rate. The HA-5177/883 is packaged in an 8 pin (TO-99) Metal Can and 8 pin Ceramic Mini-DIP and is pin compatible with many exisiting op amps. The 20 pad Ceramic Leadless Chip Carrier (LCC) is also available for surface mount applications. All packages are specified for -55°C to +125°C operation.

Pinouts

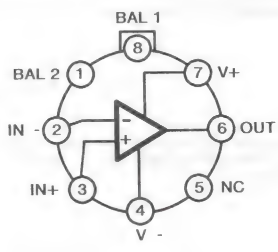
HA7-5177/883 (CERAMIC MINI-DIP)
TOP VIEW



HA4-5177/883 (CERAMIC LCC)
TOP VIEW



HA2-5177/883 (METAL CAN)
TOP VIEW



OP AMPs & COMPARATORS 3

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 44V
Differential Input Voltage (Note 6) 15V
Voltage at Either Input Terminal .... V+ to V-
Input Current 25mA
Output Current .... Full Short Circuit Protected
Junction Temperature .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... <2000V
Lead Temperature (Soldering 10 sec) .... +275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	82°C/W	25°C/W
Ceramic LCC Package	74°C/W	20°C/W
Metal Can Package	98°C/W	30°C/W

Package Power Dissipation Limit at +75°C for $T_J \leq$ +175°C
Ceramic DIP Package 1.22mW
Ceramic LCC Package 1.36W
Metal Can Package 1.02W

Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 12.2mW/°C
Ceramic LCC Package .... 13.6mW/°C
Metal Can Package .... 10.2mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±15V
$V_{INcm} \leq 1/2\ (V+ - V-)$
$R_L \geq 600\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, $R_{SOURCE} = 50\Omega$, $R_{LOAD} = 100k\Omega$, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	V_{CM} = 0V	1	+25°C	-60	60	µV
			2, 3	+125°C, -55°C	-100	100	µV
Input Bias Current	I_B	V_{CM} =0V $+R_S = 10k\Omega, 50\Omega$ $\left(\frac{\lvert +I_B \rvert + \lvert -I_B \rvert}{2}\right)$	1	+25°C	-6	6	nA
			2, 3	+125°C, -55°C	-8	8	nA
Input Offset Current	I_{IO}	V_{CM} = 0V $+R_S = 10k\Omega$ $-R_S = 10k\Omega$	1	+25°C	-6	6	nA
			2, 3	+125°C, -55°C	-8	8	nA
Common Mode Range	+CMR	V+ = 3V V- = -27V	1	+25°C	12	-	V
			2, 3	+125°C, -55°C	12	-	V
	-CMR	V+ = 27V V- = -3V	1	+25°C	-	-12	V
			2, 3	+125°C, -55°C	-	-12	V
Large Signal Voltage Gain	$+A_{VOL}$	V_{OUT} = 0V and +10V $R_L = 2k\Omega$	4	+25°C	126	-	dB
			5, 6	+125°C, -55°C	120	-	dB
	$-A_{VOL}$	V_{OUT} = 0V and -10V $R_L = 2k\Omega$	4	+25°C	126	-	dB
			5, 6	+125°C, -55°C	120	-	dB
Common Mode Rejection Ratio	+CMRR	ΔV_{CM} = 10V +V = +5V -V = -25V V_{OUT} = -10V	1	+25°C	116	-	dB
			2, 3	+125°C, -55°C	110	-	dB
	-CMRR	ΔV_{CM} = 10V +V = +25V -V = -5V V_{OUT} = +10V	1	+25°C	116	-	dB
			2, 3	+125°C, -55°C	110	-	dB

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 100kΩ, C_{LOAD} = 120pF, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Voltage Swing	$+V_{OUT1}$	R_L = 2kΩ	4	+25°C	12	-	V
			5, 6	+125°C, -55°C	12	-	V
	$-V_{OUT1}$	R_L = 2kΩ	4	+25°C	-	-12	V
			5, 6	+125°C, -55°C	-	-12	V
	$+V_{OUT2}$	R_L = 600Ω	4	+25°C	10	-	V
	$-V_{OUT2}$	R_L = 600Ω	4	+25°C	-	-10	V
Output Current	$+I_{OUT}$	V_{OUT} = -10V	4	+25°C	15	-	mA
			5, 6	+125°C, -55°C	15	-	mA
	$-I_{OUT}$	V_{OUT} = +10V	4	+25°C	-	-15	mA
			5, 6	+125°C, -55°C	-	-15	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-	1.7	mA
			2, 3	+125°C, -55°C	-	1.7	mA
	$-I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-1.7	-	mA
			2, 3	+125°C, -55°C	-1.7	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = 15V +V = +5V, -V = -15V +V = +20V, -V = -15V	1	+25°C	110	-	dB
			2, 3	+125°C, -55°C	110	-	dB
	-PSRR	ΔV_{SUP} = 15V +V = +15V, -V = -5V +V = +15V, -V = -20V	1	+25°C	110	-	dB
			2, 3	+125°C, -55°C	110	-	dB
Offset Voltage Adjustment	$+V_{IO}Adj$	Note 5	1	+25°C	0.3	-	mV
			2, 3	+125°C, -55°C	0.3	-	mV
	$-V_{IO}Adj$	Note 5	1	+25°C	-	-0.3	mV
			2, 3	+125°C, -55°C	-	-0.3	mV

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_{VCL} = +1V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Slew Rate	+SR	V_{OUT} = -3V to +3V V_{IN} S.R. ≤ 25V/µs	7	+25°C	0.5	-	V/µs
	-SR	V_{OUT} = +3V to -3V V_{IN} S.R. ≤ 25V/µs	7	+25°C	0.5	-	V/µs
Rise & Fall Time	T_R	V_{OUT} = 0 to +200mV 10% ≤ T_R ≤ 90%	7	+25°C	-	420	ns
	T_F	V_{OUT} = 0 to -200mV 10% ≤ T_F ≤ 90%	7	+25°C	-	420	ns
Overshoot	+OS	V_{OUT} = 0 to +200mV	7	+25°C	-	40	%
	-OS	V_{OUT} = 0 to -200mV	7	+25°C	-	40	%

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_V = +1V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Average Offset Voltage Drift	$V_{IO}TC$	V_{CM} = 0V	1	-55°C to +125°C	-	0.6	μV/°C
Average Offset Current Drift	$I_{IO}TC$	Versus Temperature	1	-55°c to +125°C	-	40	pA/°C
Average Bias Current Drift	I_BTC	Versus Temperature	1	-55°C to +125°C	-	40	pA/°C
Differential Input Resistance	R_{IN}	V_{CM} = 0V	1	+25°C	20	-	MΩ
Low Frequency Peak-to-Peak Noise Voltage	E_{np-p}	0.1Hz to 10Hz	1	+25°C	-	0.6	μV_{p-p}
Low Frequency Peak-to-Peak Noise Current	I_{np-p}	0.1Hz to 10Hz	1	+25°C	-	45	pA_{p-p}
Input Noise Voltage Density	E_n	R_S = 20Ω, f_O = 10Hz	1, 4	+25°C	-	18	$nV/\sqrt{Hz}$
		R_S = 20Ω, f_O = 100Hz	1, 4	+25°C	-	13	$nV/\sqrt{Hz}$
		R_S = 20Ω, f_O = 1kHz	1, 4	+25°C	-	11	$nV/\sqrt{Hz}$
Input Noise Current Density	I_n	R_S = 2MΩ, f_O = 10Hz	1, 4	+25°C	-	4	$pA/\sqrt{Hz}$
		R_S = 2MΩ, f_O = 100Hz	1, 4	+25°C	-	2.3	$pA/\sqrt{Hz}$
		R_S = 2MΩ, f_O = 1kHz	1, 4	+25°C	-	1	$pA/\sqrt{Hz}$
Gain Bandwidth Product	GBWP	V_O = 100mV, 1Hz ≤ f_O ≤ 100kHz	1	+25°C	2	-	MHz
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	+25°C	8	-	kHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 2kΩ, C_L = 50pF	1	-55°C to +125°C	+1	-	V/V
Settling Time	T_S	To 0.1% for a 10V Step	1	+25°C	-	15	μs
Output Resistance	R_{OUT}	Open Loop	1	+25°C	-	70	Ω
Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	51	mW

NOTES:
1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).
3. Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)
4. Input Noise Voltage Density and Input Noise Current Density is sample tested on every lot.
5. This test is for functionality only to assure adjustment through 0V.
6. The input stage has series 500Ω resistors along with back to back diodes. This allows large differential input voltages protection at a slight increase towards noise voltage.

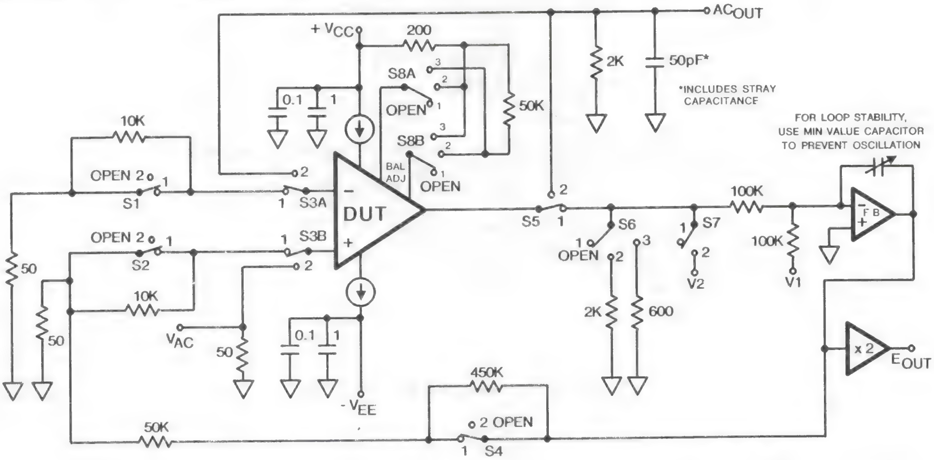
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6, 7
Group A Test Requirements	1, 2, 3, 4, 5, 6, 7
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

The Subgroup assignments of the parameters in these tables were patterned after Mil-M-38510/135, except for V_{IO} which is Subgroup 1, 2, and 3.

Test Circuit (Applies to Tables 1 and 2)

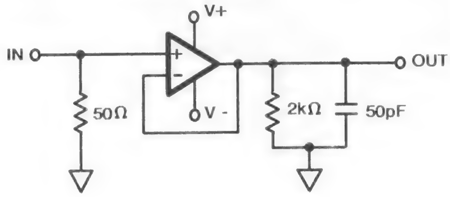


ALL RESISTORS = ± 1% (Ω)
ALL CAPACITORS = ± 10% (μF)

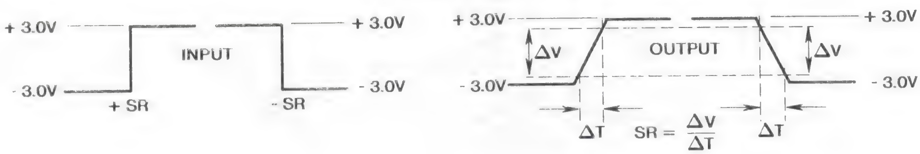
For Op-Amp Test Circuits and Conditions, Refer to the Harris Tech Brief "HA-5177/883 Test Methods".

Test Waveforms (Applies to Tables 2 and 3)

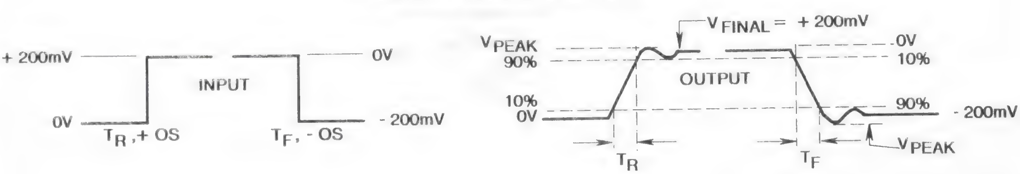
SIMPLIFIED TEST CIRCUIT



LARGE SIGNAL WAVEFORM



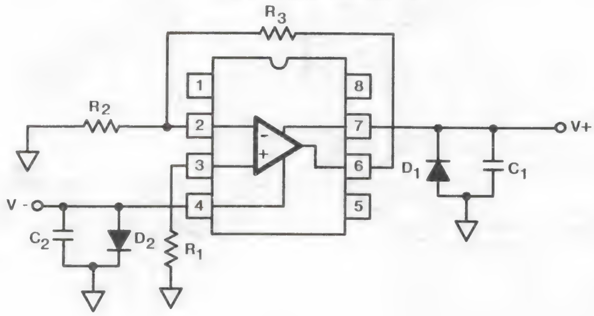
TRANSIENT RESPONSE WAVEFORM



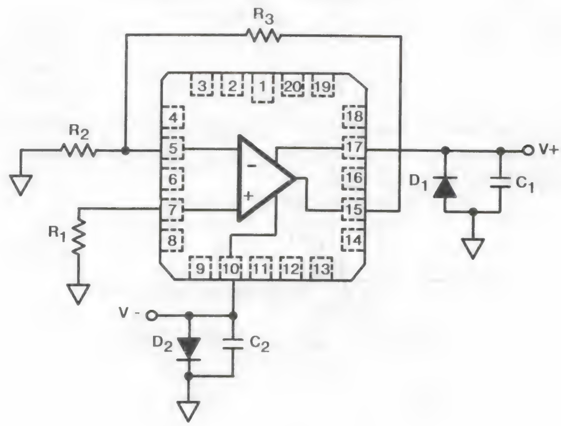
NOTE: Measured on Both positive and negative transitions.

Burn-In Circuits

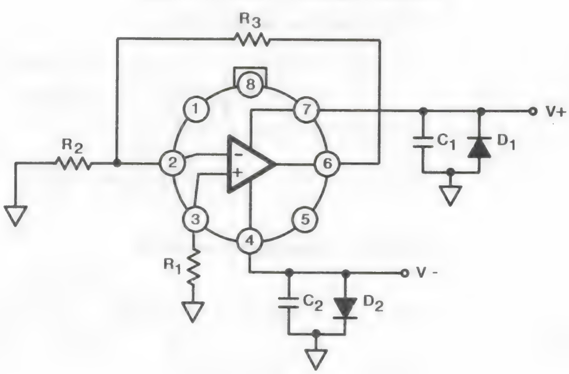
HA7-5177/883 CERAMIC Mini-DIP



HA4-5177/883 CERAMIC LCC



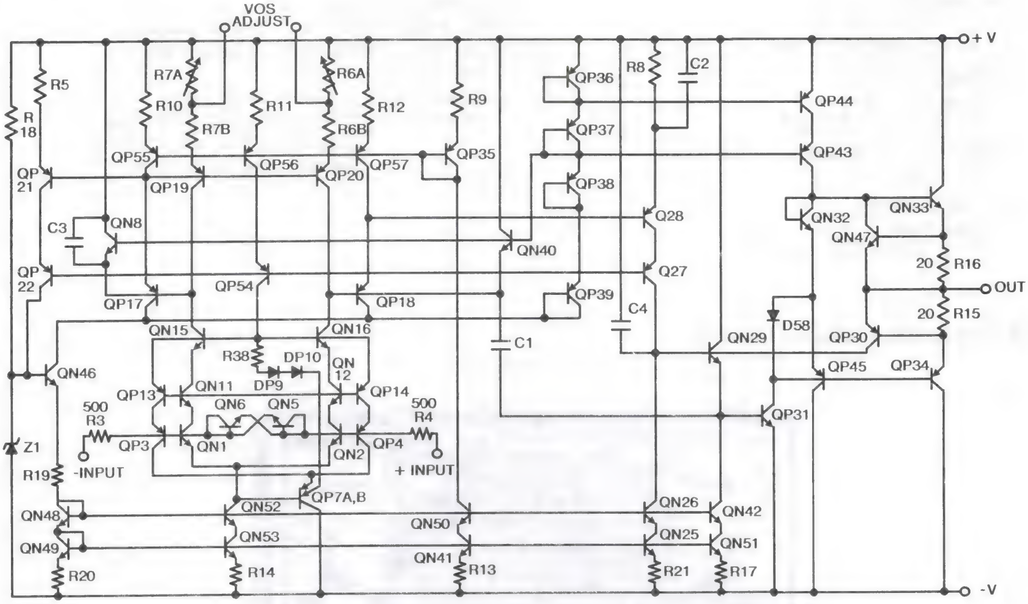
HA2-5177/883 (TO-99) METAL CAN



NOTES:

$R_1 = R_2 = 1k\Omega$, ±5%, 1/4W (Min)
$R_3 = 10k\Omega$ ±5%, 1/4W (Min)
$C_1 = C_2 = 0.01\mu F$/Socket (Min) or $0.1\mu F$/Row (Min)
$D_1 = D_2$ = IN4002 or Equivalent/Board
$|(V+) - (V-)| = 30V$

Schematic Diagram



Die Characteristics

DIE DIMENSIONS:
71.7 x 102 x 19 mils
(1820 x 2590 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$0.7 \times 10^5 A/cm^2$

GLASSIVATION:
Type: Silox
Thickness: 9.5kÅ ± 2.5kÅ

TRANSISTOR COUNT: 71

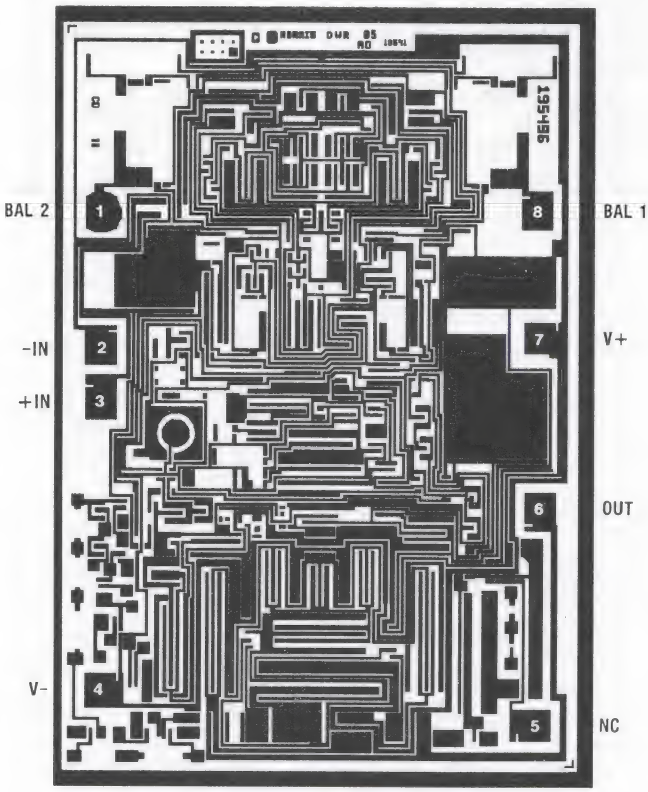
PROCESS: HFHB Bipolar Dielectric Isolation

SUBSTRATE POTENTIAL (Powered Up): V-

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)
Metal Can — 420°C (Max)

Metallization Mask Layout

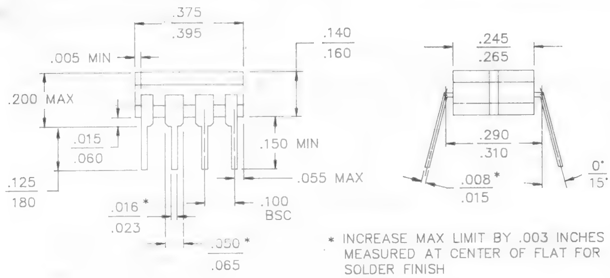
HA-5177/883



NOTE: Pin Numbers Correspond to 8 Pin Metal Can and Mini-DIP Packages Only.

Packaging †

8 PIN CERAMIC MINI-DIP

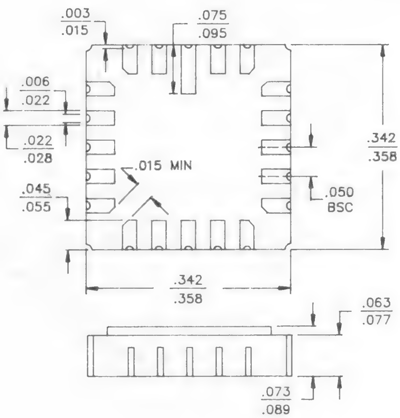


LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
- Material: Glass Frit
- Temperature: 450°C ± 10°C
- Method: Furnace Seal

INTERNAL LEAD WIRE:
- Material: Aluminum
- Diameter: 1.25 Mil
- Bonding Method: Ultrasonic

COMPLIANT OUTLINE: 38510 D-4

20 PAD CERAMIC LCC

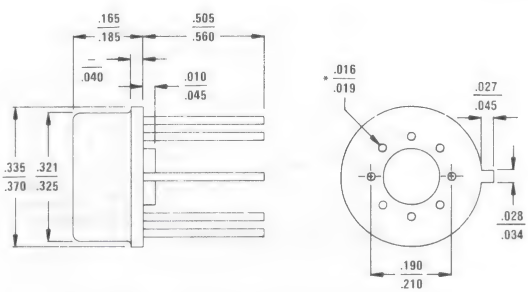


PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Ceramic, 90% Al_2O_3
PACKAGE SEAL:
- Material: Gold/Tin (80/20)
- Temperature: 320°C ± 10°C
- Method: Furnace Braze

INTERNAL LEAD WIRE:
- Material: Aluminum
- Diameter: 1.25 Mil
- Bonding Method: Ultrasonic

COMPLIANT OUTLINE: 38510 C-2

8 PIN TO-99 METAL CAN



*Dimension Maximum Limits Are Increased by 0.003 inches for Solder Dip Finish

LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
- Material: No Seal Material
- Temperature: Room Temperature
- Method: Resistance Weld

INTERNAL LEAD WIRE:
- Material: Aluminum
- Diameter: 1.25 Mil
- Bonding Method: Ultrasonic Bonded

COMPLIANT OUTLINE: 38510 A-1

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

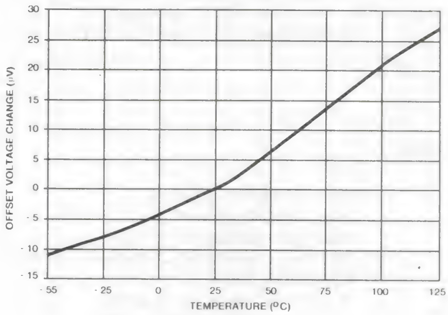
DESIGN INFORMATION

Ultra-Low Offset Voltage Operational Amplifier

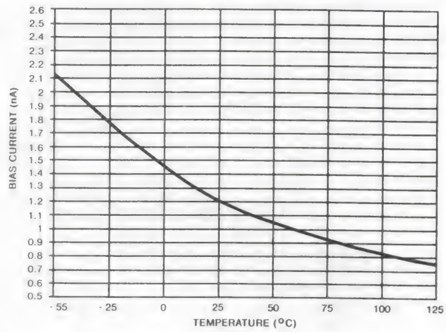
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

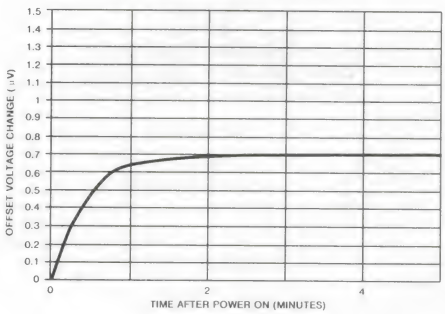
OFFSET VOLTAGE vs. TEMPERATURE



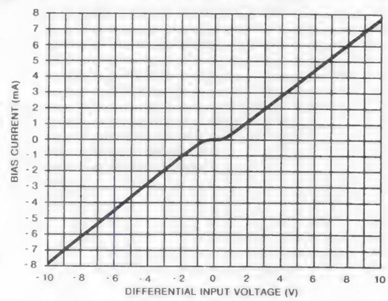
BIAS CURRENT vs. TEMPERATURE



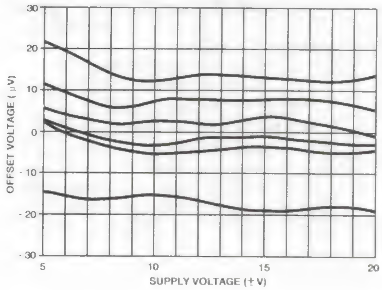
OFFSET VOLTAGE WARM-UP DRIFT



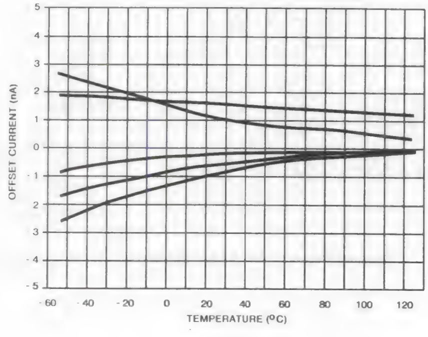
BIAS CURRENT vs. DIFFERENTIAL INPUT VOLTAGE



OFFSET VOLTAGE vs. SUPPLY VOLTAGE
Six Representative Units



OFFSET CURRENT vs. TEMPERATURE
Five Representative Units

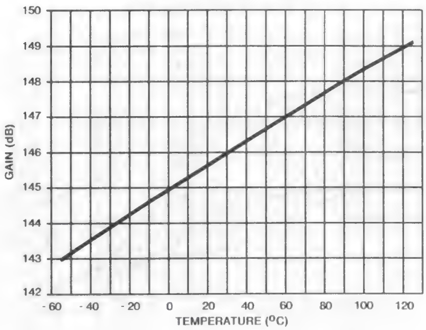


DESIGN INFORMATION (Continued)

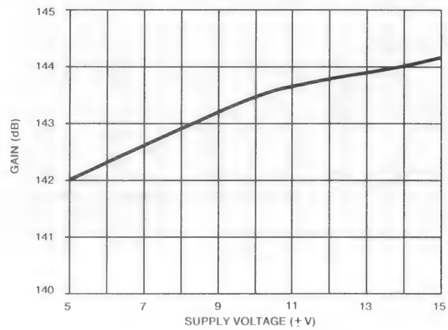
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

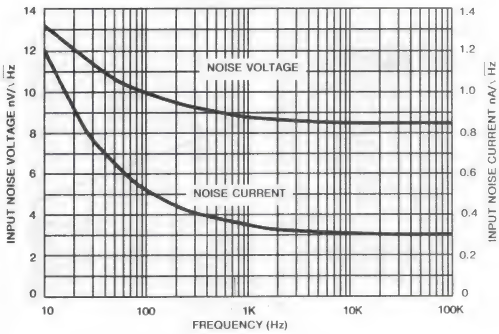
OPEN LOOP GAIN vs. TEMPERATURE



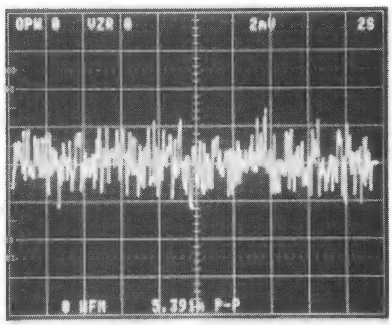
OPEN LOOP GAIN vs. SUPPLY VOLTAGE



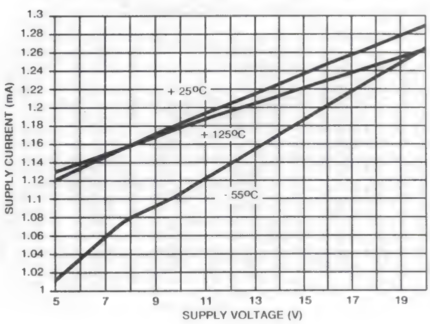
INPUT NOISE vs. FREQUENCY



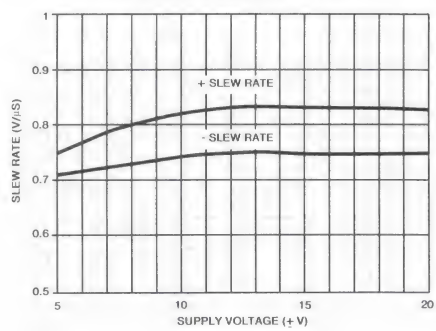
PEAK-TO-PEAK NOISE 0.1Hz TO 10Hz
$A_V = 25{,}000$, $0.22\mu V_{p-p}$ RTI



SUPPLY CURRENT vs. SUPPLY VOLTAGE



SLEW RATE vs. SUPPLY VOLTAGE
$A_V = 1$, $R_L = 2K$, $C_L = 50pF$



DESIGN INFORMATION (Continued)

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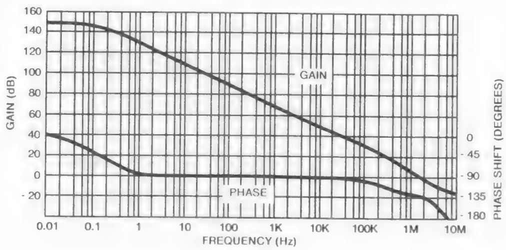
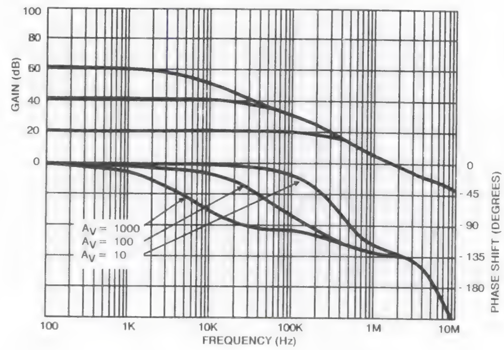
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

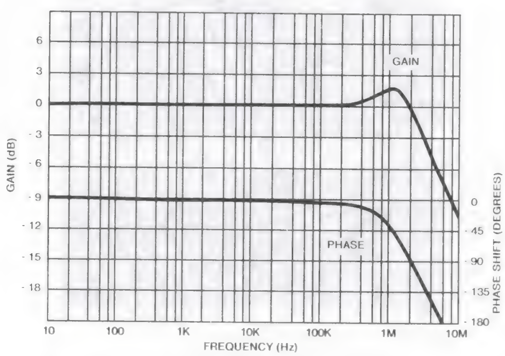
OPEN LOOP GAIN AND PHASE vs. FREQUENCY



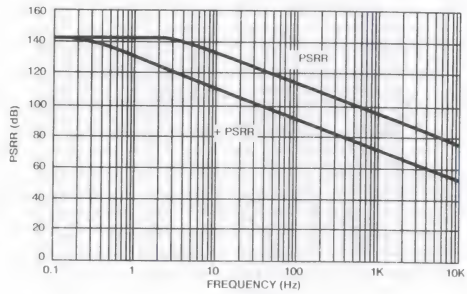
VARIOUS CLOSED LOOP GAINS vs. FREQUENCY
R_L = 2K, C_L = 50pF



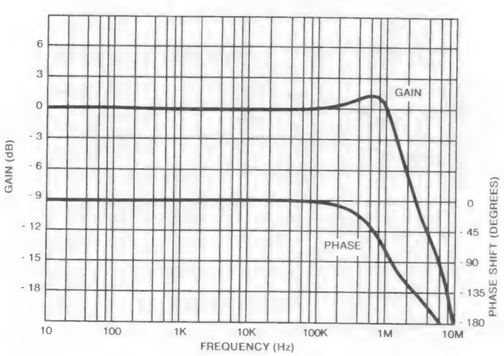
CLOSED LOOP GAIN AND PHASE vs. FREQUENCY
A_V = +1, R_L = 2K, C_L = 50pF



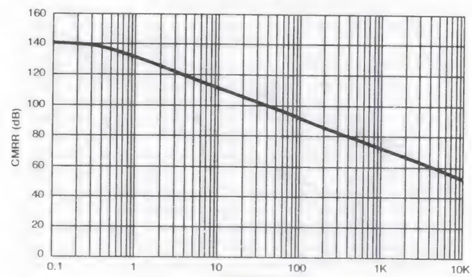
PSRR vs. FREQUENCY



CLOSED LOOP GAIN AND PHASE vs. FREQUENCY
A_V = −1, R_L = 2K, C_L = 50pF



CMRR vs. FREQUENCY

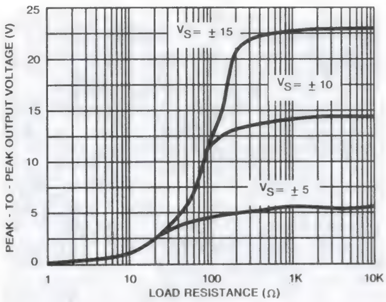


DESIGN INFORMATION (Continued)

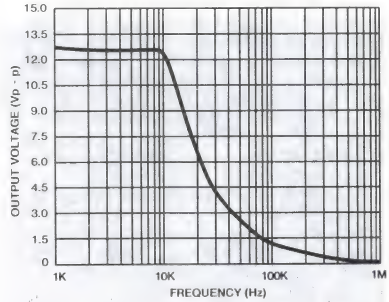
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

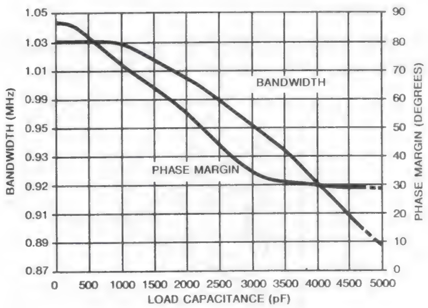
OUTPUT VOLTAGE vs. LOAD RESISTANCE
$A_V = -1$, $V_{IN} = 100Hz$, $C_L = 50pF$



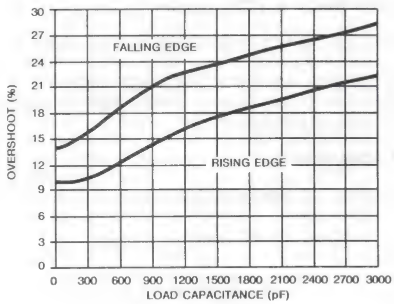
OUTPUT VOLTAGE vs. FREQUENCY
$A_V = -1$, $R_L = 2K$, $C_L = 50pF$



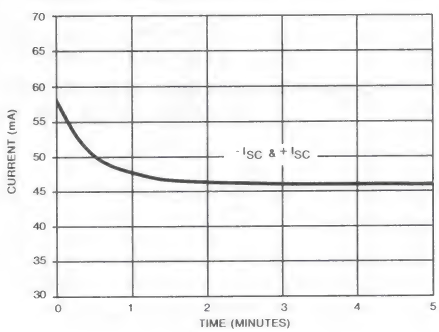
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN vs. LOAD CAPACITANCE
$A_V = +1$



OVERSHOOT vs. LOAD CAPACITANCE
$V_S = \pm15V$, $A_V = +1$, $V_{OUT} = \pm200mV$



OUTPUT SHORT CIRCUIT CURRENT vs. TIME
$V_{IN} = \pm10V$, $A_V = -1$

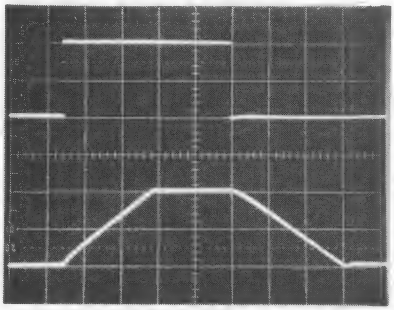


DESIGN INFORMATION (Continued)

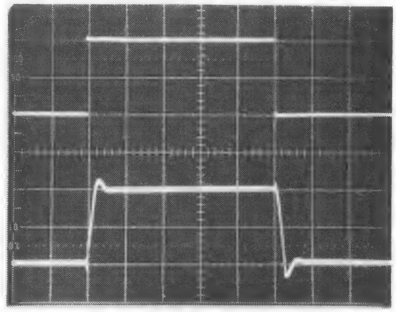
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

MEASURED LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: 5V/Div.)
Horizontal Scale: (Time: 5μs/Div.)



MEASURED SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: 100mV/Div.)
Horizontal Scale: (Time: 2μs/Div.)



Applications Information

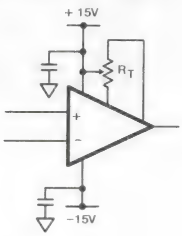
Operation Below ±15V Supply

The HA-5177 performs well down to ±5V supplies.

At ±5V supplies there is a slight degradation of slew rate and open loop gain. There is very little change in bias currents and offset voltage.

Offset Adjustment

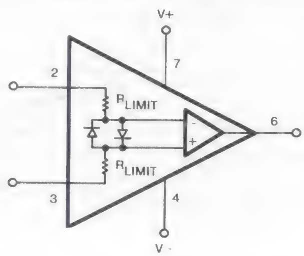
The following is the recommended V_{IO} adjust configuration:



Setting $R_T = 20k\Omega$ will give an adjustment range of at least ±2.6mV.

Input Protection

The HA-5177 input stage has built in back-to-back protection diodes with series current limiting resistors.



The Bias currents will increase when a differential voltage of 0.7 volts is exceeded.

The internal current limiting resistors (500Ω) sufficiently limit current, therefore, no external resistors are required.

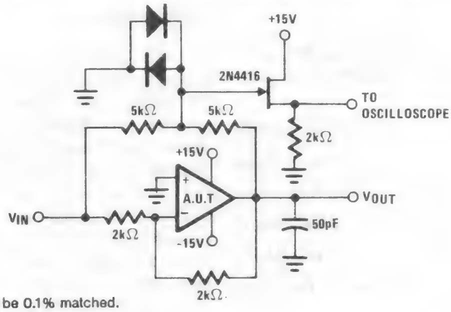
Refer to the "Bias Current vs. Differential Input Voltage" curve in the Typical Performance Curves section.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Application Information (Continued)

SETTLING TIME CIRCUIT (Applies to Table 3 only)



- $A_V = -1$
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional. HP5082-2810 recommended.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_L = 2KΩ, C_L = 50pF, A_V = +1V/V, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage	V_{CM} = 0V	+25°C	10	Table 1	µV
		Full	40	Table 1	µV
Offset Voltage Drift	Versus Temperature	Full	0.1	Table 3	µV/°C
Bias Current	V_{CM} = 0V	+25°C	1.2	Table 1	nA
		Full	2.4	Table 1	nA
Bias Current Drift	Versus Temperature	Full	15	35	pA/°C
Offset Current Drift	Versus Temperature	Full	1.5	50	pA/°C
Differential Input Resistance		+25°C	47	Table 3	MΩ
Input Noise Voltage Density	f_O = 1Hz	+25°C	15	30	nV/$\sqrt{Hz}$
	f_O = 10Hz	+25°C	13	Table 3	nV/$\sqrt{Hz}$
	f_O = 100Hz	+25°C	10	Table 3	nV/$\sqrt{Hz}$
	f_O = 1kHz	+25°C	9	Table 3	nV/$\sqrt{Hz}$
Input Noise Current Density	f_O = 1Hz	+25°C	1.5	4	pA/$\sqrt{Hz}$
	f_O = 10Hz	+25°C	0.4	Table 3	pA/$\sqrt{Hz}$
	f_O = 100Hz	+25°C	0.2	Table 3	pA/$\sqrt{Hz}$
	f_O = 1kHz	+25°C	0.14	Table 3	pA/$\sqrt{Hz}$
Low Frequency P-P Noise Voltage	0.1Hz to 10Hz	+25°C	0.35	0.6	μV_{p-p}
Voltage Gain	V_{OUT} = ±10V R_L = 2kΩ	+25°C	150	Table 1	dB
		Full	140	Table 1	dB
CMRR	ΔV = ±10V	Full	140	Table 1	dB
PSRR	ΔV_S = ±10 to ±20V	Full	135	Table 1	dB
Slew Rate	V_{OUT} = ±5V	+25°C	1.0	Table 2	V/µs
Settling Time	10V Step to 0.1%	+25°C	12	15	µs
Rise/Fall Time	V_{OUT} = ±200mV	+25°C	310	Table 2	ns
Overshoot	V_{OUT} = ±200mV	+25°C	10	Table 2	%
Supply Current	No Load	Full	1.2	Table 1	mA
Minimum Supply Voltage	Functional Operation Only. Other Parameters Will Vary.	+25°C	±5	±6	V

HARRIS

HA-5190/883

Wideband, Fast Settling Operational Amplifier

January 1989

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Very High Slew Rate .... 160V/μs (Min)**
- **Fast Settling Time .... 100ns (Typ)**
- **Wide Gain Bandwidth .... 150MHz (Min)**
- **Power Bandwidth .... 5MHz (Min)**
- **Low Offset Voltage .... 5mV (Max)**
- **Input Voltage Noise @ 1kHz .... 6nV/$\sqrt{Hz}$ (Typ)**
- **Monolithic Bipolar Construction**

Applications

- **Fast, Precise D/A Converters**
- **High Speed Sample and Hold Circuits**
- **Pulse and Video Amplifiers**
- **WideBand Amplifiers**
- **Replace Costly Hybrids**

Description

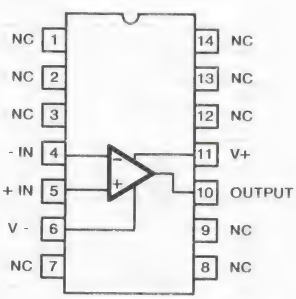
The HA-5190/883 is a monolithic operational amplifier featuring an ultimate combination of speed, precision, and bandwidth. Employing monolithic bipolar construction coupled with Dielectric Isolation, this device is capable of delivering an unparalleled 160V/μs slew rate (min) with a settling time of 100ns (typ). This truly differential amplifier is designed to operate at a gain of 5 without the need for external compensation. Other oustanding HA-5190/883 features are 150MHz (min) gain-bandwidth-product and 5MHz full power bandwidth. In addition to these dynamic characteristics, this amplifier also has excellent input characteristics such as 5mV offset voltage (max) and 6.0nV (typ) input voltage noise density at 1kHz.

With such dynamic A.C. performance, the HA-5190/883 makes an ideal output amplifier for accurate, high speed D/A converters or the main component in high speed sample and hold circuits. The HA-5190/883 is also ideally suited for a variety of pulse and wideband video amplifier applications.

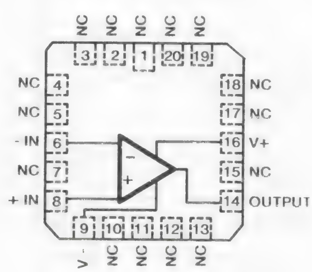
The HA-5190/883 is available in Metal Can (TO-8), 20 pin Ceramic LCC, and 14 pin Ceramic DIP packages and is specified over the -55°C to +125°C temperature range.

Pinouts

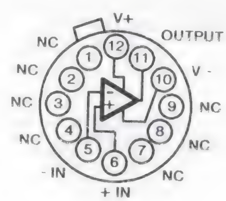
HA1-5190/883 (CERAMIC DIP)
TOP VIEW



HA4-5190/883 (CERAMIC LCC)
TOP VIEW



HA2-5190/883 (TO-8 METAL CAN)
TOP VIEW



Case Tied To V-

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage (Note 8) 6V
Voltage at Either Input Terminal .... V+ to V-
Peak Output Current (< 10% Duty Cycle) 50mA
Junction Temperature (T_J) .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... < 2000V
Lead Temperature (Soldering 10 sec) .... +275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	98°C/W	30°C/W
Ceramic LCC Package	95°C/W	35°C/W
Metal Can Package	69°C/W	31°C/W

Package Power Dissipation Limit at +75°C For $T_J \leq$ 175°C
Ceramic DIP Package 1.02mW
Ceramic LCC Package 1.06W
Metal Can Package 1.45W

Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 10.2mW/°C
Ceramic LCC Package .... 10.6mW/°C
Metal Can Package .... 14.5mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±12V to ±15V
$V_{INcm} \leq$ 1/2 (V+ - V-)
$R_L \geq 200\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, $R_{SOURCE} = 100\Omega$, $R_{LOAD} = 500k\Omega$, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	V_{CM} = 0V	1	+25°C	-5	5	mV
			2, 3	+125°C, -55°C	-10	10	mV
Input Bias Current	$+I_B$	V_{CM} = 0V $+R_S = 1.1k\Omega$ $-R_S = 100\Omega$	1	+25°C	-15	15	µA
			2, 3	+125°C, -55°C	-20	20	µA
	$-I_B$	V_{CM} = 0V $+R_S = 100\Omega$ $-R_S = 1.1k\Omega$	1	+25°C	-15	15	µA
			2, 3	+125°C, -55°C	-20	20	µA
Input Offset Current	I_{IO}	V_{CM} = 0V $+R_S = 1.1k\Omega$ $-R_S = 1.1k\Omega$	1	+25°C	-4	4	µA
			2, 3	+125°C, -55°C	-6	6	µA
Common Mode Range	+CMR	V+ = 10V V- = -20V	1	+25°C	5	-	V
			2, 3	+125°C, -55°C	5	-	V
	-CMR	V+ = 20V V- = -10V	1	+25°C	-	-5	V
			2, 3	+125°C, -55°C	-	-5	V
Large Signal Voltage Gain	$+A_{VOL}$	V_{OUT} = 0V and +5V $R_L = 200\Omega$	4	+25°C	15	-	kV/V
			5, 6	+125°C, -55°C	5	-	kV/V
	$-A_{VOL}$	V_{OUT} = 0V and -5V $R_L = 200\Omega$	4	+25°C	15	-	kV/V
			5, 6	+125°C, -55°C	5	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔV_{CM} = +5V +V = +10V -V = -20V V_{OUT} = -5V	1	+25°C	74	-	dB
			2, 3	+125°C, -55°C	74	-	dB
	-CMRR	ΔV_{CM} = -5V +V = +20V -V = -10V V_{OUT} = +5V	1	+25°C	74	-	dB
			2, 3	+125°C, -55°C	74	-	dB

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 10Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Voltage Swing	$+V_{OUT}$	R_L = 200Ω	1	+25°C	5	-	V
			2, 3	+125°C, -55°C	5	-	V
	$-V_{OUT}$	R_L = 200Ω	1	+25°C	-	-5	V
			2, 3	+125°C, -55°C	-	-5	V
Output Current	$+I_{OUT}$	$V_{OUT} \geq -5V$	1	+25°C	25	-	mA
	$-I_{OUT}$	$V_{OUT} \leq +5V$	1	+25°C	-	-25	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-	24	mA
			2, 3	+125°C, -55°C	-	24	mA
	$-I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-24	-	mA
			2, 3	+125°C, -55°C	-24	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = 10V +V = +10V, -V = -15V +V = +20V, -V = -15V	1	+25°C	70	-	dB
			2, 3	+125°C, -55°C	70	-	dB
	-PSRR	ΔV_{SUP} = 10V +V = +15V, -V = -10V +V = +15V, -V = -20V	1	+25°C	70	-	dB
			2, 3	+125°C, -55°C	70	-	dB

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 200Ω, $C_{LOAD} \leq$ 10pF, A_{VCL} = 5V/V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Slew Rate	+SR	V_{OUT} = -5V to +5V	7	+25°C	160	-	V/µs
	-SR	V_{OUT} = +5V to -5V	7	+25°C	160	-	V/µs
Rise & Fall Time	T_R	V_{OUT} = 0 to +200mV $10\% \leq T_R \leq 90\%$	7	+25°C	-	18	ns
	T_F	V_{OUT} = 0 to -200mV $10\% \leq T_F \leq 90\%$	7	+25°C	-	18	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_{LOAD} = 1kΩ, $C_{LOAD} \leq$ 10pF, A_V = 5V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Gain Bandwidth Product	GBWP	$V_O \leq$ 200mV, f_O = 10kHz	1	+25°C	150	-	MHz
		$V_O \leq$ 200mV, f_O = 1MHz	1	+25°C	150	-	MHz
Full Power Bandwidth	FPBW	V_{PEAK} = 5V	1, 2	+25°C	5	-	MHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 200Ω, $C_L \leq$ 10pF	1	-55°C to +125°C	5	-	V/V
Overshoot	+OS	V_{OUT} = 0V to +200mV	1	+25°C	-	45	%
	-OS	V_{OUT} = 0V to -200mV	1	+25°C	-	45	%
Output Resistance	R_{OUT}	Open Loop	1	+25°C	-	60	Ω
Quiescent Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	720	mW

NOTES: 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).

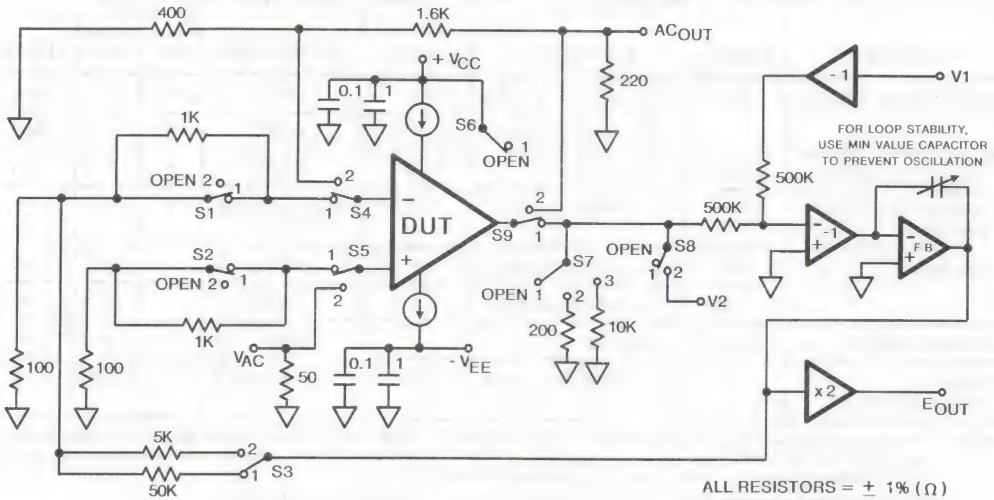
3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6, 7
Group A Test Requirements	1, 2, 3, 4, 5, 6, 7
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

Test Circuit (Applies to Table 1)

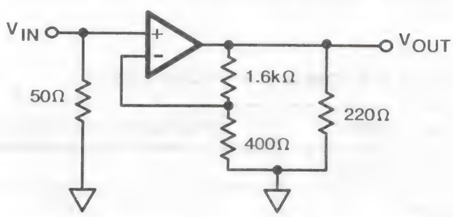


ALL RESISTORS = ± 1% (Ω)
ALL CAPACITORS = ± 10% (μF)

For Detailed Information, Refer to HA-5190/883 Test Tech Brief

Test Waveforms

SIMPLIFIED TEST CIRCUIT FOR LARGE AND SMALL SIGNAL RESPONSE (Applies to Tables 2 and 3)

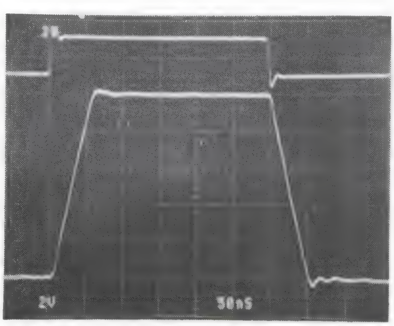


$A_V = +5$
$C_L \leq 10pF$

MEASURED LARGE SIGNAL RESPONSE
Vertical Scale: Input = 2V/Div., Output = 2V/Div.
Horizontal Scale: Time: 50ns/Div.

INPUT

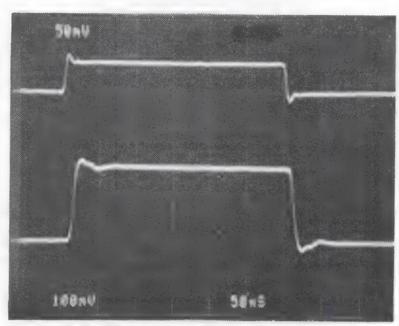
OUTPUT



MEASURED SMALL SIGNAL RESPONSE
Vertical Scale: Input = 50mV/Div., Output = 100mV/Div.
Horizontal Scale: 50ns/Div.

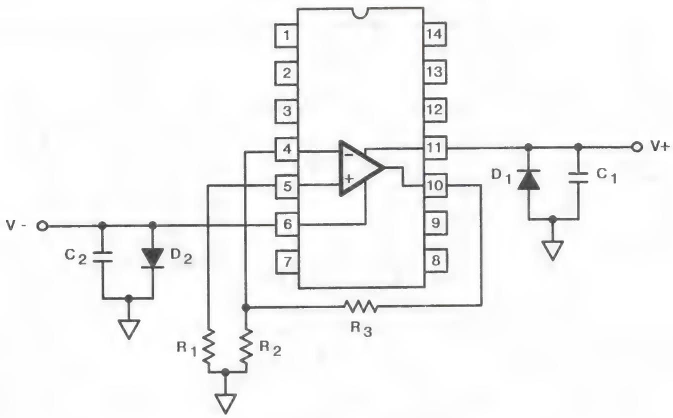
INPUT

OUTPUT

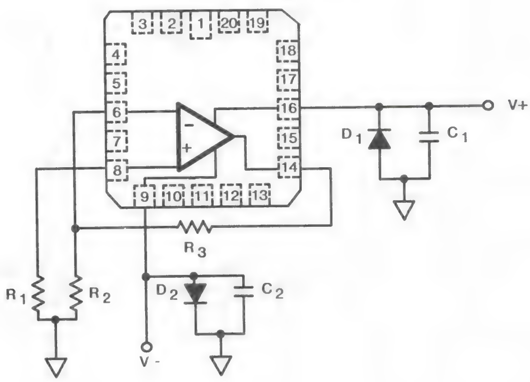


Burn-In Circuits

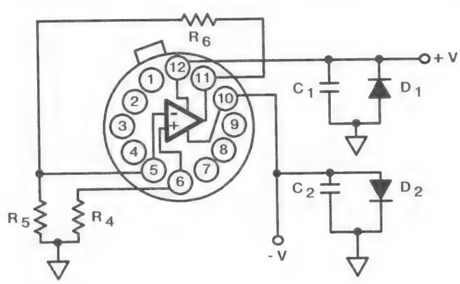
HA1-5190/883 CERAMIC DIP



HA4-5190/883 CERAMIC LCC



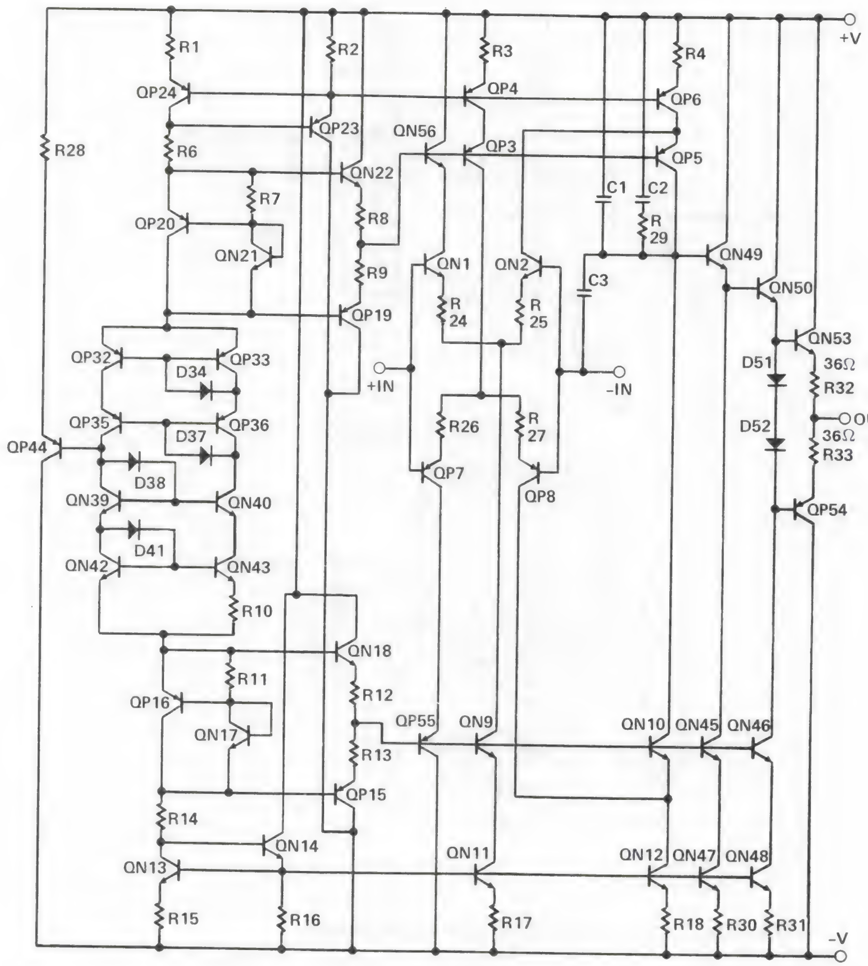
HA2-5190/883 TO-8 METAL CAN



NOTES:

$R_1 = R_2 = 1k\Omega$, ±5%, 1/4W (Min)
$R_3 = 10k\Omega$, ±5%, 1/4W (Min)
$R_4 = R_5 = 100k\Omega$, ±5%, 1/4W (Min)
$R_6 = 1M\Omega$, ±5%, 1/4W (Min)
$C_1 = C2 = 0.01\mu F$/Socket (Min) or $0.1\mu F$/Row, (Min)
$D_1 = D_2$ = IN4002 or Equivalent/Board
$|(V+) - (V-)| = 30V$

Schematic Diagram



Die Characteristics

DIE DIMENSIONS:
87 x 52 x 19 mils
(2210 x 1320 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 20kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$0.7 \times 10^5 A/cm^2$ @ 3.72mA

SUBSTRATE POTENTIAL (POWERED UP): V-

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

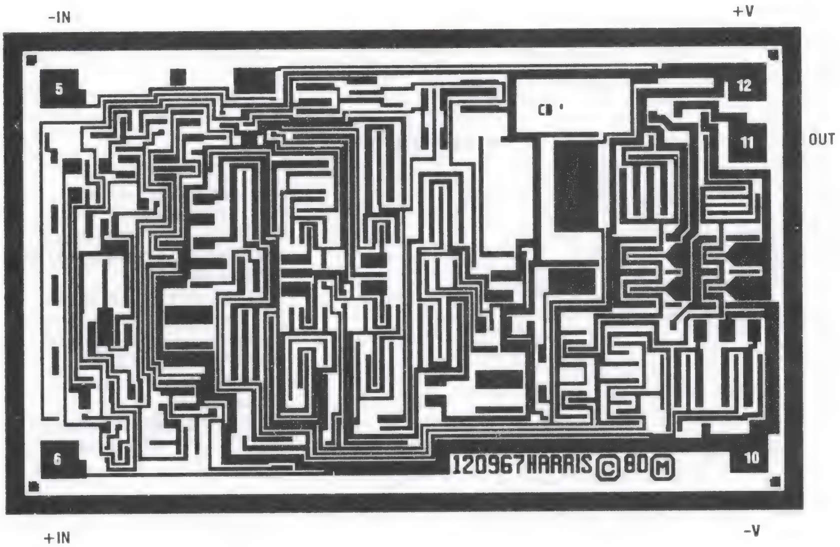
TRANSISTOR COUNT: 49

PROCESS: High Frequency Bipolar Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)
Metal Can — 420°C (Max)

Metallization Mask Layout

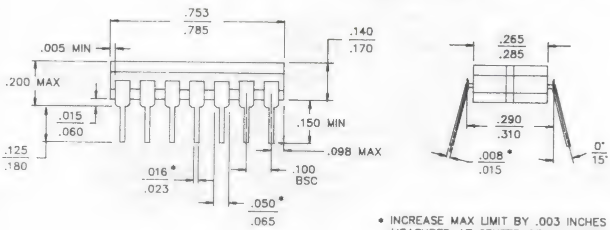
HA-5190/883



NOTE: Pin Numbers Correspond to 12 Pin (TO-8) Metal Can Package Only.

Packaging †

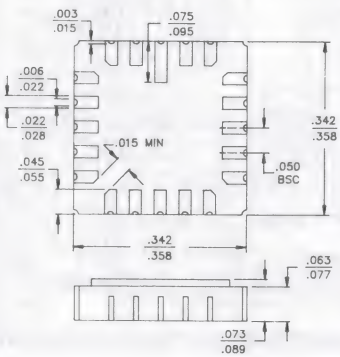
14 PIN CERAMIC DIP



* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

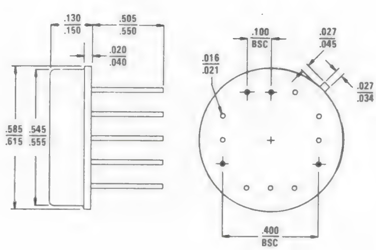
LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
  Material: Glass Frit
  Temperature: 450°C ± 10°C
  Method: Furnace Seal
INTERNAL LEAD WIRE:
  Material: Aluminum
  Diameter: 1.25 Mil
  Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-1

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Ceramic, 90% Al_2O_3
PACKAGE SEAL:
  Material: Gold/Tin (80/20)
  Temperature: 320°C ± 10°C
  Method: Furnace Braze
INTERNAL LEAD WIRE:
  Material: Aluminum
  Diameter: 1.25 Mil
  Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

12 PIN TO-8 METAL CAN



LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
  Material: No Seal Material
  Temperature: Room Temperature
  Method: Resistance Weld
INTERNAL LEAD WIRE:
  Material: Aluminum
  Diameter: 1.25 Mil
  Bonding Method: Ultrasonic Bonded
PACKAGE CASE VOLTAGE POTENTIAL: V-
COMPLIANT PACKAGE: None
PACKAGE USED: JEDEC 'AB'

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

HA-5190

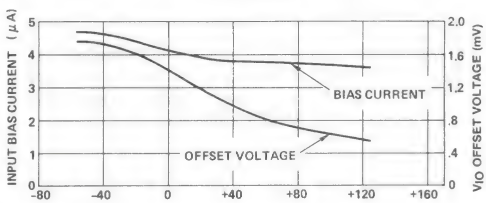
DESIGN INFORMATION

Wideband, Fast Settling Operational Amplifier

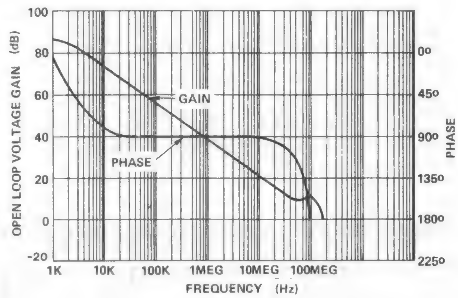
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

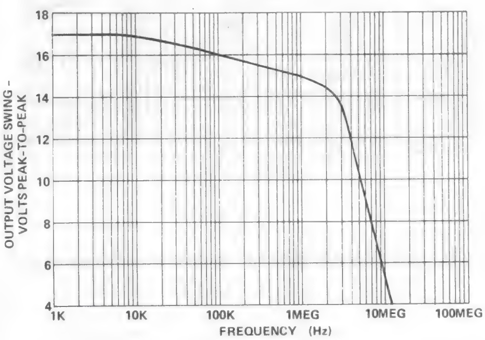
INPUT OFFSET VOLTAGE AND BIAS CURRENT vs. TEMPERATURE



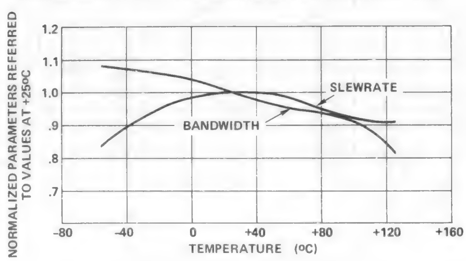
OPEN LOOP FREQUENCY RESPONSE



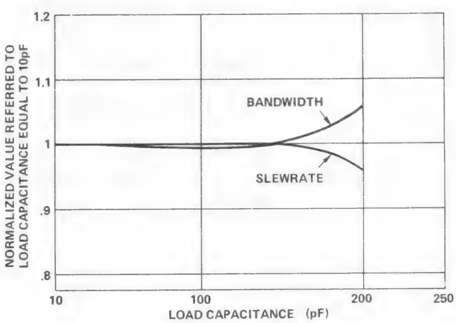
OUTPUT VOLTAGE SWING vs. FREQUENCY



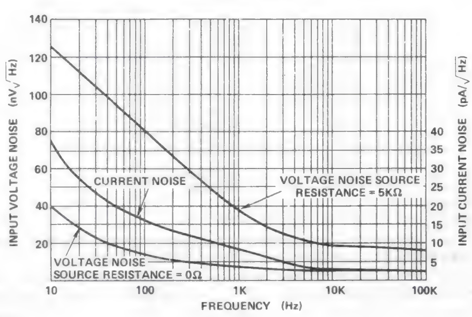
NORMALIZED AC PARAMETERS vs. TEMPERATURE



NORMALIZED AC PARAMETERS vs. LOAD CAPACITANCE



INPUT NOISE VOLTAGE AND NOISE CURRENT vs. FREQUENCY



(Also See Application Notes 525, 526, 556)

DESIGN INFORMATION (Continued)

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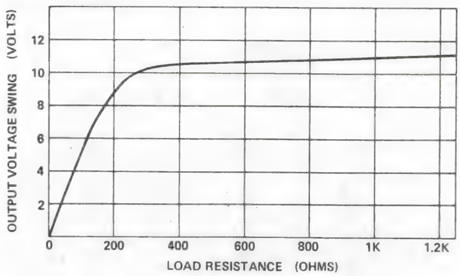
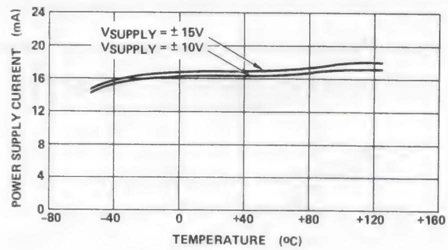
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^{\circ}C$, $V_{SUPPLY} = \pm 15V$

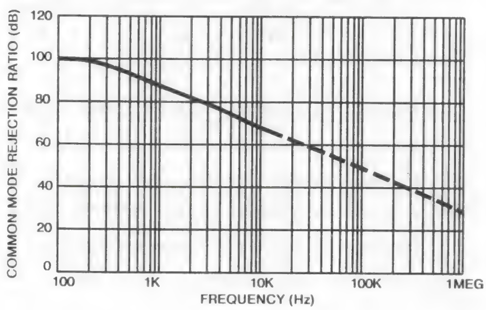
OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



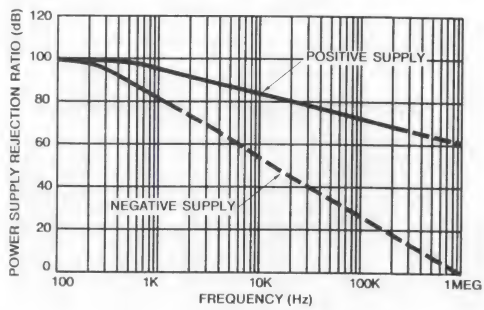
POWER SUPPLY CURRENT vs. TEMPERATURE



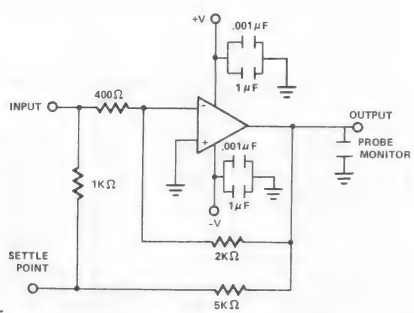
COMMON MODE REJECTION RATIO vs. FREQUENCY



POWER SUPPLY REJECTION RATIO vs. FREQUENCY

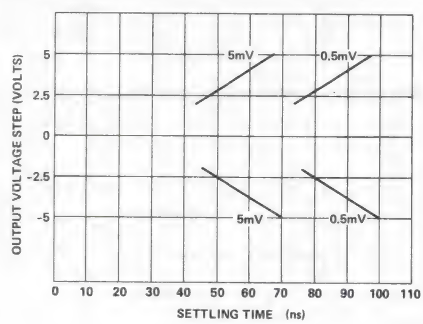


SETTLING TIME TEST CIRCUIT



- $A_V = -5$
- Load Capacitance should be less than 10pF.
- It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched to 0.1%.
- Settle Point (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



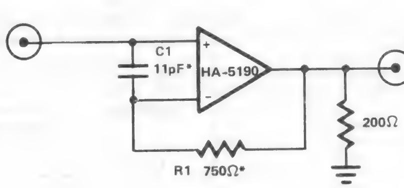
DESIGN INFORMATION (Continued)

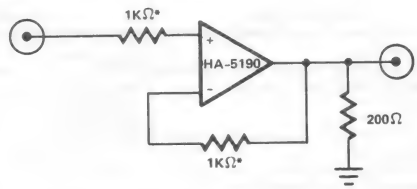
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Applications (Also see Application Notes 525 and 526)

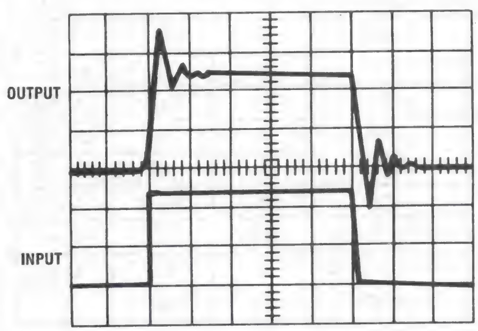
SUGGESTED COMPENSATION FOR UNITY GAIN STABILITY:

NONINVERTING

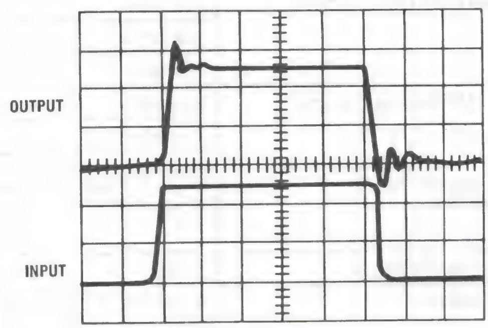




Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (Time: 100ns/Div.)

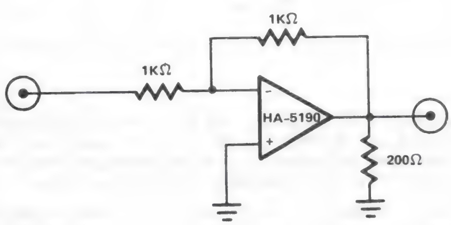


Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (Time: 100ns/Div.)

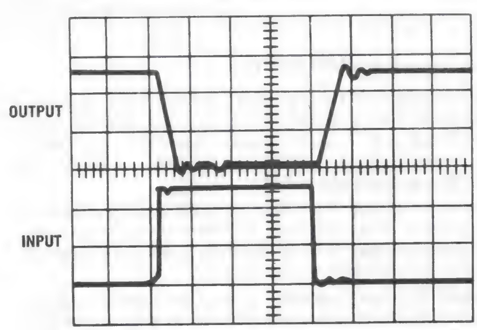


* Values were determined experimentally for optimum speed and settling time. R1 and C1 should be optimized for each particular application to ensure best overall frequency response.

INVERTING



Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (Time: 50ns/Div.)



DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_L = 200Ω, $C_L \le$ 100pF, A_V = 5V/V, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage	V_{CM} = 0V	+25°C	3	Table 1	mV
Average Offset Voltage Drift	Versus Temperature	-55°C to +125°C	20	30	μV/°C
	Versus Time	+40°C	8	15	μV/Month
Bias Current		+25°C	5	Table 1	μA
Differential Input Resistance		+25°C	10	5	kΩ
Input Capacitance		+25°C	1	3	pF
Input Noise Voltage Density	f_O = 10Hz	+25°C	14	30	$nV/\sqrt{Hz}$
	f_O = 100Hz	+25°C	10	20	$nV/\sqrt{Hz}$
	f_O = 1kHz	+25°C	6	10	$nV/\sqrt{Hz}$
Input Noise Current Density	f_O = 10Hz	+25°C	35	60	$pA/\sqrt{Hz}$
	f_O = 100Hz	+25°C	10	30	$pA/\sqrt{Hz}$
	f_O = 1kHz	+25°C	5	15	$pA/\sqrt{Hz}$
Slew Rate	V_{OUT} = ±5V	+25°C	200	Table 2	V/μs
		-55°C to +125°C	125	110	V/μs
Full Power Bandwidth	V_{PEAK} = 10V	-55°C to +125°C	4	3.5	MHz
Settling Time	A_V = -5V/V, 5V Step to 0.1%	+25°C	70	130	ns
	A_V = -5V/V, 5V Step to 0.01%	+25°C	100	200	ns
	A_V = -5V/V, 2.5V Step to 0.1%	+25°C	50	110	ns
	A_V = -5V/V, 2.5V Step to 0.01%	+25°C	80	185	ns
Differential Gain Error	$f_O \le$ 5MHz	+25°C	3	5	%
Differential Phase Error	$f_O \le$ 5MHz	+25°C	1	2	Degree
Output Resistance	Open Loop	+25°C	30	Table 3	Ω
Supply Current	I_{OUT} = 0mA	-55°C to +125°C	19	Table 1	mA
Minimum Supply Voltage	Functional Operation Only. Other Parameters Will Vary.	+25°C	±5	±7	V

Applying the HA-5190

1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with 0.01μF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.
2. STABILITY CONSIDERATIONS: HA-5190 is stable at gains > 5. Gains $\le$ 5 are covered elsewhere in this data sheet. Feedback resistors should be of carbon composition located as near to the input terminals as possible.
3. WIRING CONSIDERATIONS: Video pulse circuits should be built on a ground plane. Minimum point to point connections directly to the amplifier terminals should be used. When ground planes cannot be used, good single point grounding techniques should be applied.
4. OUTPUT SHORT CIRCUIT: HA-5190 does not have output short circuit protection. Short circuits to ground can be tolerated for approximately 10 seconds. Short circuits to either supply will result in immediate destruction of the device.
5. HEAVY CAPACITIVE LOADS: When driving heavy capacitive loads ($\ge$ 100pF) a small resistor (≈ 100Ω) should be connected in series with the output and inside the feedback loop.
6. HEAT SINKING: Although not required for /883 qualification, heat sinking is suggested in high ambient conditions. Recommended heat sinks include thermalloy #2240A or #2268B for TO-8 Metal Can; AAVID #5602B for 14 pin Ceramic DIP. Heat sinking power density may be necessary depending on package used to maintain $T_J \le$ +175°C.

ANALOG

CMOS Analog Switches

4

CMOS ANALOG SWITCH DATA SHEETS

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

HI-200/883

January 1989

Dual SPST CMOS Analog Switch

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low "On" Resistance .... 100Ω Max
- Wide Analog Signal Range .... ±15V
- TTL/CMOS Compatible .... 2.4V (Logic "1")
- Turn-On Time 500ns
- Analog Current Range (Continuous) 25mA
- No Latch-Up
- Replaces DG200

Applications

- High Frequency Analog Switching
- Sample and Hold Circuits
- Digital Filters
- Op Amp Gain Switching Networks

Description

HI-200/883 is a monolithic device comprising two independently selectable SPST switches which feature fast switching speeds (240ns typical) combined with low power dissipation (15mW typical @ +25°C).

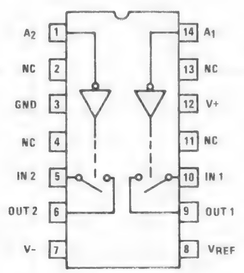
Each switch provides low "ON" resistance operation for input signal voltages up to the supply rails and for signal currents up to 25mA continuous. Rugged DI construction eliminates latch-up and substrate SCR failure modes.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-200/883 is an ideal component for use in high frequency analog switching. Typical applications include signal path switching, sample and hold circuits, digital filters, and op amp gain switching networks.

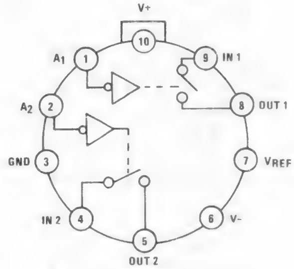
HI-200/883 is available in a 14 pin Ceramic DIP package and a 10 pin Metal Can (TO-100) package.

Pinouts

HI-200/883 (CERAMIC DIP)
TOP VIEW

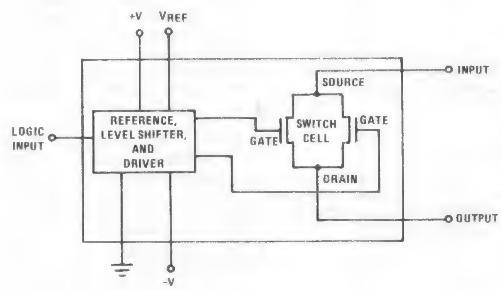


HI-200/883 (METAL CAN)
TOP VIEW



Case Tied to V-

Functional Diagram



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
$\pm V_{SUPPLY}$ to Ground (V+, V-) .... ±20V
Analog Input Voltage $+V_S$ .... $+V_{SUPPLY}$ +2V
$-V_S$ .... $-V_{SUPPLY}$ -2V
Digital Input Voltage $+V_A$ .... $+V_{SUPPLY}$ +4V
$-V_A$ .... $-V_{SUPPLY}$ -4V
Peak Current (S or D)
(Pulse at 1ms, 10% Duty Cycle Max) 40mA
Continuous Current Any Terminal (Except S or D) 25mA
Junction Temperature .... +175°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering 10 sec) .... ≤275°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	100°C/W	31°C/W
Metal Can Package	122°C/W	37°C/W

Package Power Dissipation at +75°C
Ceramic DIP Package 0.76W
Metal Can Package 0.62W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 10.08mW/°C
Metal Can Package .... 8.24mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) .... ±15V
Analog Input Voltage (V_S) .... $\pm V_{SUPPLY}$
Logic Low Level (V_{AL}) .... 0V to 0.8V
Logic High Level (V_{AH}) .... 2.4V to $+V_{SUPPLY}$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{REF} = OPEN, GND = 0V, Unless Otherwise Specified

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	MAX	UNITS
Switch "ON" Resistance	R_{DS}	V_A = 0.8V, V_S = 10V, I_D = -1mA All Unused Channels V_A = 0.8V	1	+25°C	-	70	Ω
			2, 3	-55°C to +125°C	-	100	Ω
		V_A = 0.8V, V_S = -10V, I_D = 1mA All Unused Channels V_A = 0.8V	1	+25°C	-	70	Ω
			2, 3	-55°C to +125°C	-	100	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = +14V, V_D = -14V, V_A = 2.4V All Unused Channels V_A = 2.4V, V_D = +14V, V_S = -14V	1	+25°C	-5	5	nA
			2, 3	-55°C to +125°C	-500	500	nA
		V_S = -14V, V_D = +14V, V_A = 2.4V All Unused Channels V_A = 2.4V, V_D = -14V, V_S = +14V	1	+25°C	-5	5	nA
			2, 3	-55°C to +125°C	-500	500	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_D = -14V, V_S = +14V, V_A = 2.4V All Unused Channels V_A = 2.4V, V_D = +14V, V_S = -14V	1	+25°C	-5	5	nA
			2, 3	-55°C to +125°C	-500	500	nA
		V_D = +14V, V_S = -14V, V_A = 2.4V All Unused Channels V_A = 2.4V, V_D = -14V, V_S = +14V	1	+25°C	-5	5	nA
			2, 3	-55°C to +125°C	-500	500	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = +14V, V_A = 0.8V All Unused Channels V_A = 0.8V, V_D = V_S = -14V	1	+25°C	-5	5	nA
			2, 3	-55°C to +125°C	-500	500	nA
		V_D = V_S = -14V, V_A = 0.8V All Unused Channels V_A = 0.8V, V_D = V_S = +14V	1	+25°C	-5	5	nA
			2, 3	-55°C to +125°C	-500	500	nA
Low Level Input Current	I_{AL}	V_{AL} = 0.8V All Unused Channels V_A = 2.4V	1	+25°C	-1.0	1.0	µA
			2, 3	-55°C to +125°C	-1.0	1.0	µA
High Level Input Current	I_{AH}	V_{AH} = 2.4V All Unused Channels V_A = 2.4V	1	+25°C	-1.0	1.0	µA
			2, 3	-55°C to +125°C	-1.0	1.0	µA
Supply Current	$+I_{CC}$	All Channels V_A = 0V	1, 2	+25°C, +125°C	-	2.0	mA
			3	-55°C	-	2.0	mA
		All Channels V_A = 3V	1, 2	+25°C, +125°C	-	2.0	mA
			3	-55°C	-	2.0	mA
Supply Current	$-I_{CC}$	All Channels V_A = 0V	1, 2	+25°C, +125°C	-2.0	-	mA
			3	-55°C	-2.0	-	mA
		All Channels V_A = 3V	1, 2	+25°C, +125°C	-2.0	-	mA
			3	-55°C	-2.0	-	mA

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$, V_{REF} = OPEN, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Turn "ON" Time	$t_{(ON)}$	$C_L = 35pF$ $R_L = 1k\Omega$	9	$+25^oC$	-	500	ns
			10, 11	$-55^oC, +125^oC$	-	800	ns
Turn "OFF" Time	$t_{(OFF)}$	$C_L = 35pF$ $R_L = 1k\Omega$	9	$+25^oC$	-	500	ns
			10, 11	$-55^oC, +125^oC$	-	650	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Characterized at: $+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$, V_{REF} = OPEN, GND = 0V

PARAMETERS	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address Capacitance	C_A	$f = 1MHz, V_{AL} = 0V$	1	$+25^oC$	-	20	pF
Switch Input Capacitance	$C_{S(OFF)}$	$f = 1MHz, V_{AH} = 5V$ Measure Input to Ground	1	$+25^oC$	-	20	pF
Switch Output Capacitance	$C_{D(OFF)}$	$f = 1MHz, V_{AH} = 5V$ Measure Output to Ground	1	$+25^oC$	-	20	pF
	$C_{D(ON)}$	$f = 1MHz, V_{AL} = 0V$ Measure Output to Ground	1	$+25^oC$	-	30	pF
Drain to Source Capacitance	C_{DS}	$f = 1MHz, V_{AH} = 5V$	1	$+25^oC$	-	2.0	pF
Off Isolation	V_{ISO}	$f = 200kHz, V_A = 2.4, R_L = 1K$ $V_{GEN} = 1V_{p-p}, C_L = 10pF$	1	$+25^oC$	55	-	dB
Crosstalk	V_{CT}	$f = 200kHz, V_A = 2.4, R_L = 1K$ $V_{GEN} = 1V_{p-p}, C_L = 10pF$	1	$+25^oC$	60	-	dB
Charge Transfer Error	V_{CTE}	$f = 200kHz, V_A = 0$ to $4V$ $C_L = 0.01\mu F$	1	$+25^oC$	-10	10	mV

NOTE 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

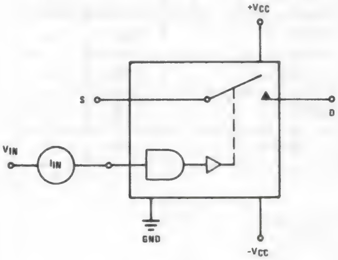
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

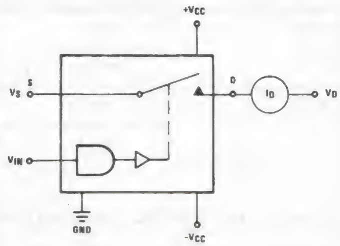
* PDA applies to Subgroup 1 only.

Test Circuits

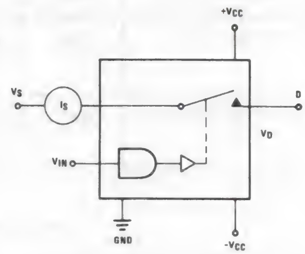
INPUT LEAKAGE CURRENT



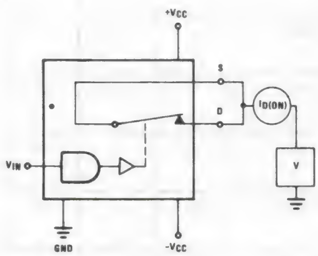
$I_{D(OFF)}$



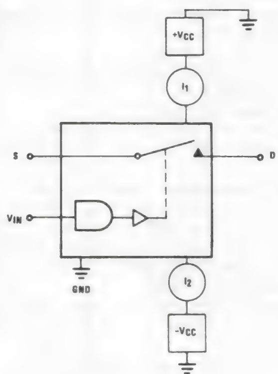
$I_{S(OFF)}$



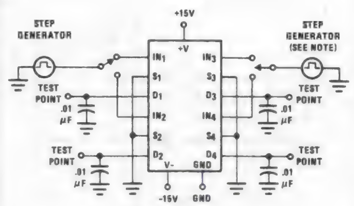
$I_{D(ON)}$



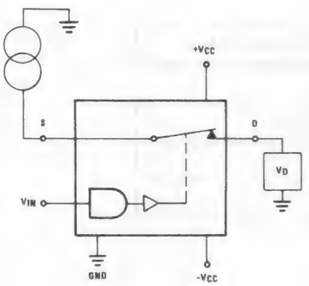
SUPPLY CURRENTS



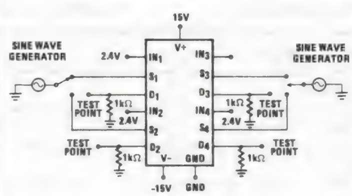
CHARGE TRANSFER ERROR



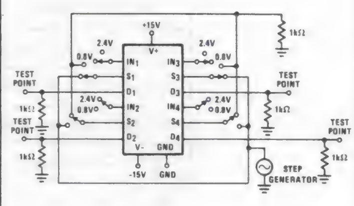
R_{DS}



OFF CHANNEL ISOLATION

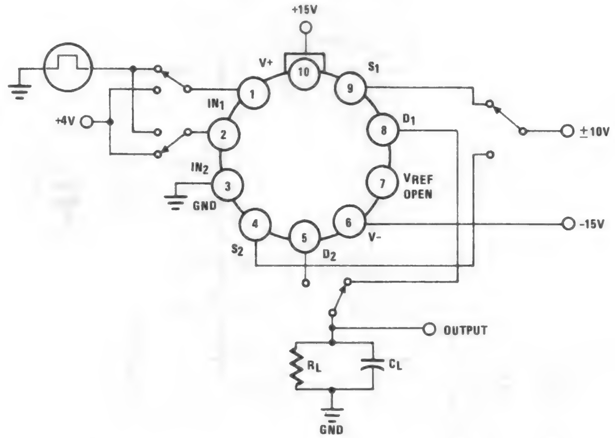


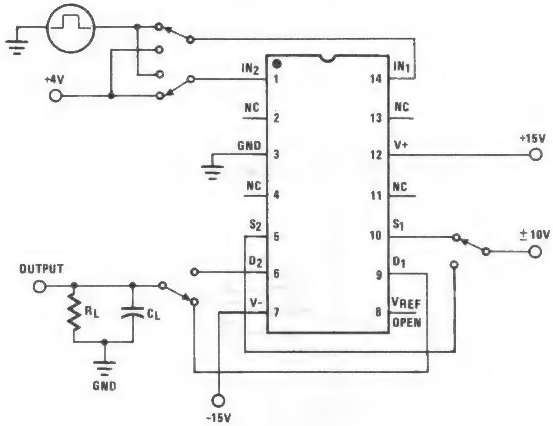
CROSSTALK BETWEEN CHANNELS

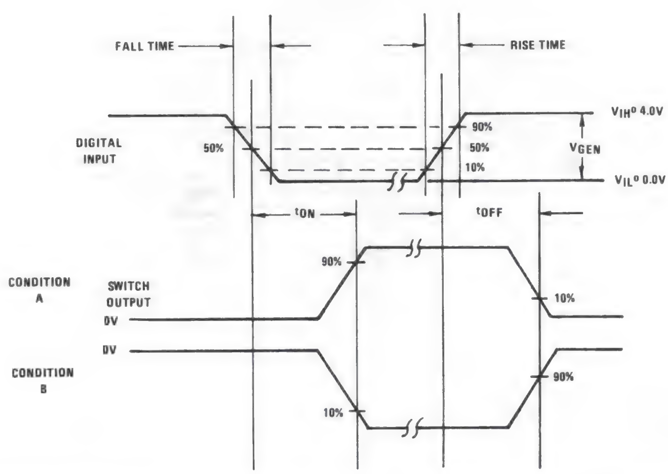


For Detail Information Refer to HI-200/883 Test Tech Brief

Switching Waveforms

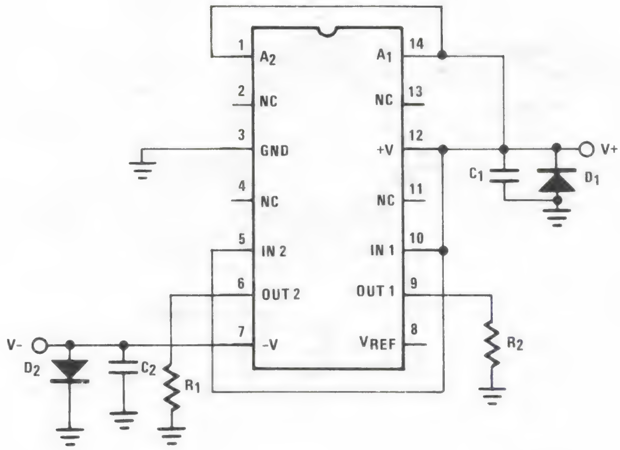




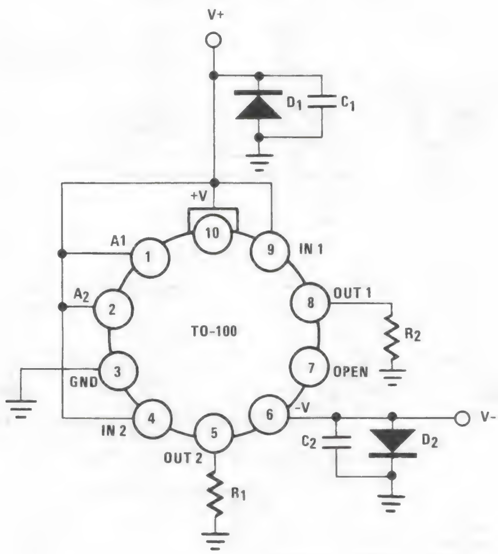


Burn-In Circuits

HI-200/883 CERAMIC DIP



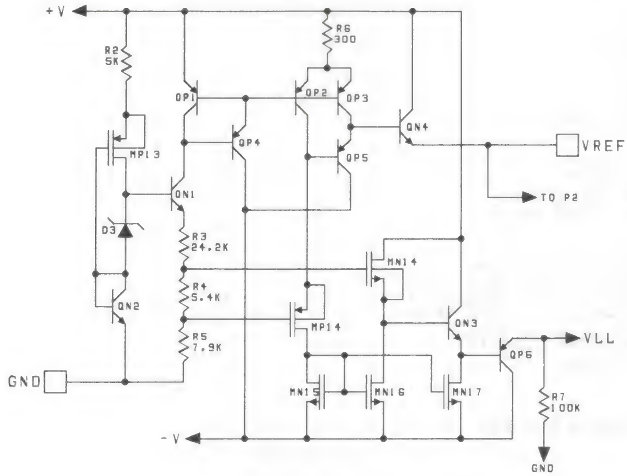
HI-200/883 METAL CAN (TO-99)



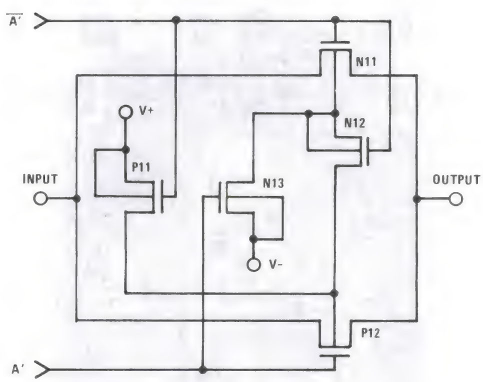
NOTES:
$R_1 = R_2 = 10k\Omega$
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2 =$ IN4002 or Equivalent
$|(V+) - (V-)| = 30V$

Schematic Diagrams

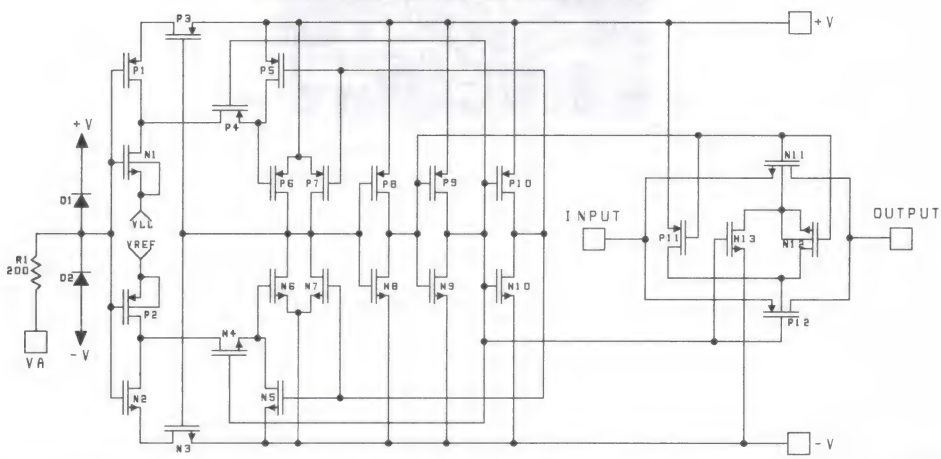
TTL/CMOS REFERENCE CIRCUIT



SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



Die Characteristics

DIE DIMENSIONS:
54 x 79 x 19 mils

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

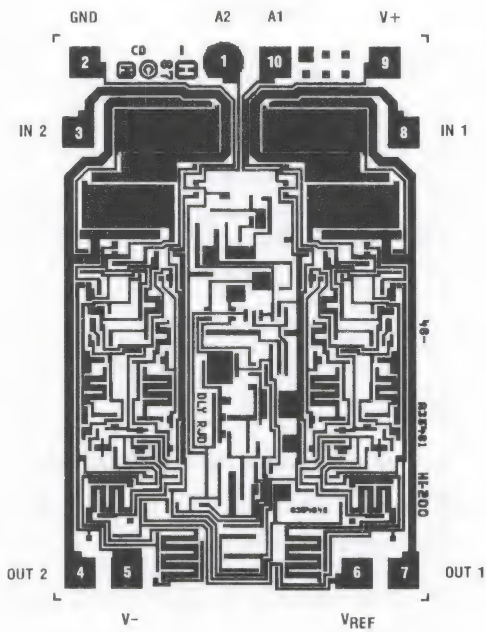
GLASSIVATION:
Type: Nitride over Silox
Silox Thickness: 12kÅ ± 2kÅ
Nitride Thickness: 3.5kÅ ± 1kÅ

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Metal Can — 420°C (Max)

WORST CASE CURRENT DENSITY:
$2 \times 10^5 A/cm^2$ at 25mA

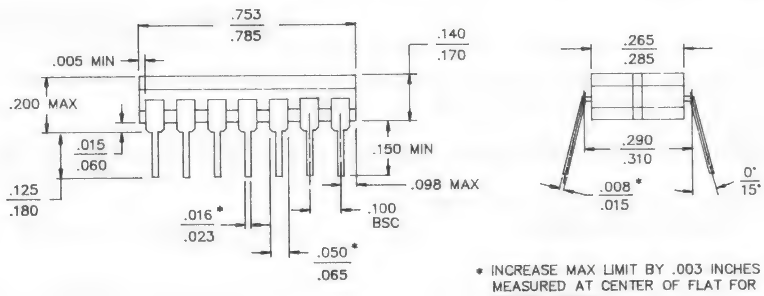
Metallization Mask Layout

H1-200/883



Packaging†

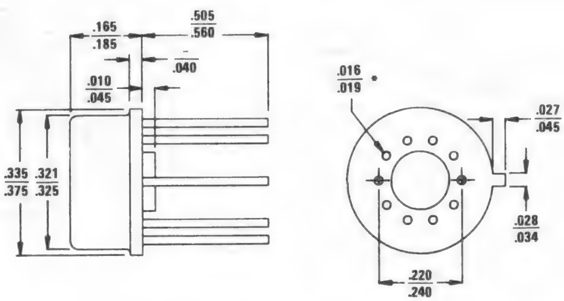
14 PIN CERAMIC DIP



LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-1

10 PIN METAL CAN



* Maximum Limits are Increased by 0.003 inches for Solder Dip Finish.

LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
Material: No Seal Material
Temperature: Room Temperature
Method: Resistance Weld

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 A-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

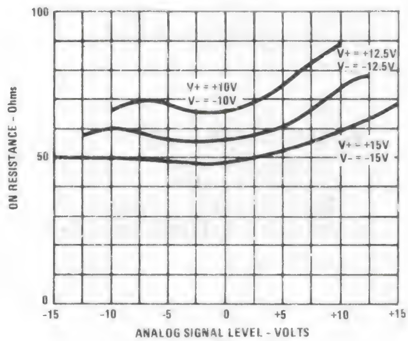
† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

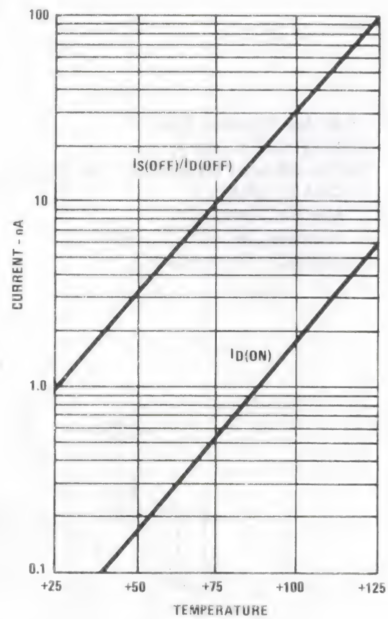
Typical Performance Characteristics

Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH}=2.4V$, $V_{AL}=0.8V$, V_{REF}=Open

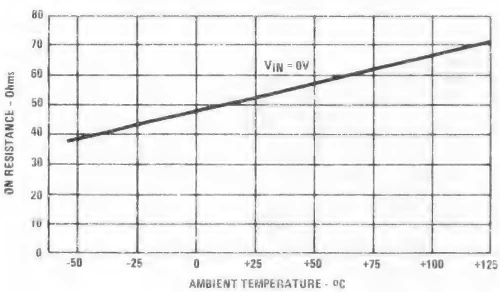
ON RESISTANCE vs. ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE



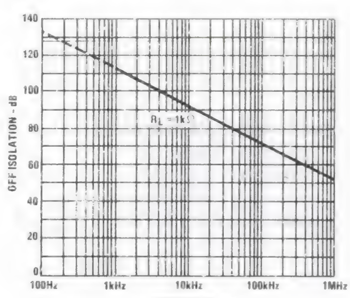
LEAKAGE CURRENT vs. TEMPERATURE



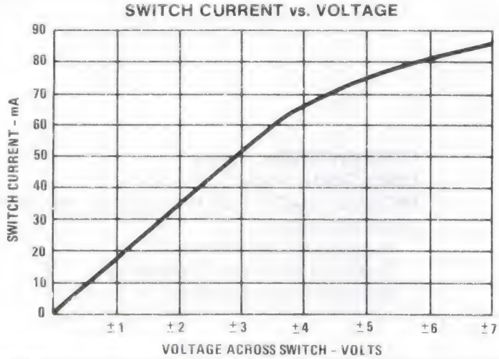
ON RESISTANCE vs. TEMPERATURE



OFF ISOLATION vs. FREQUENCY



SWITCH CURRENT vs. VOLTAGE



HARRIS

HI-201/883

January 1989

Quad SPST CMOS Analog Switch

Features

- **This Circuit Is Processed In Accordance to Mil-Std-883 and Is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Low "On" Resistance .... 100Ω Max**
- **Wide Analog Signal Range .... ±15V**
- **TTL/CMOS Compatible .... 2.4V (Logic "1")**
- **Turn-On Time 500ns**
- **Analog Current Range (Continuous) 25mA**
- **No Latch-Up**
- **Replaces DG201**

Applications

- **High Frequency Analog Switching**
- **Sample and Hold Circuits**
- **Digital Filters**
- **Op Amp Gain Switching Networks**

Description

HI-201/883 is a monolithic device comprising four independently selectable SPST switches which feature fast switching speeds (185ns typical) combined with low power dissipation (15mW typical @ +25°C).

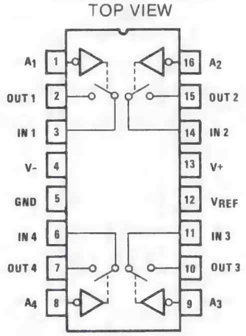
Each switch provides low "ON" resistance operation for input signal voltages up to the supply rails and for signal currents up to 25mA continuous. Rugged DI construction eliminates latch-up and substrate SCR failure modes.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-201/883 is an ideal component for use in high frequency analog switching. Typical applications include signal path switching, sample and hold circuits, digital filters, and op amp gain switching networks.

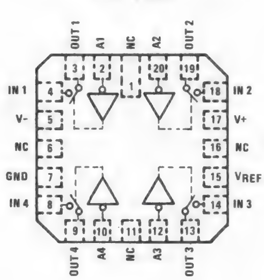
HI-201/883 is available in a 16 pin Ceramic DIP package and a 20 pin LCC package.

Pinouts

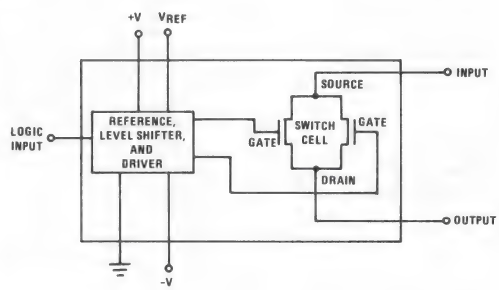
HI-201/883 (CERAMIC DIP)
TOP VIEW



HI-201/883 (CERAMIC LCC)
TOP VIEW



Functional Diagram



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
$\pm V_{SUPPLY}$ to Ground (V+, V-) .... ±20V
Analog Input Voltage $+V_S$ .... $+V_{SUPPLY}$ +2V
$-V_S$ .... $-V_{SUPPLY}$ -2V
Digital Input Voltage $+V_A$ .... $+V_{SUPPLY}$ +4V
$-V_A$ .... $-V_{SUPPLY}$ -4V
Peak Current (S or D)
(Pulse at 1ms, 10% Duty Cycle Max) 40mA
Continuous Current Any Terminal (Except S or D) 25mA
Junction Temperature .... +175°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering 10 sec) .... ≤275°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	86°C/W	22°C/W
Ceramic LCC Package	84°C/W	24°C/W

Package Power Dissipation at +75°C
Ceramic DIP Package 0.88W
Ceramic LCC Package 0.9W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 11.76mW/°C
Ceramic LCC Package .... 12.0mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) .... ±15V
Analog Input Voltage (V_S) .... $\pm V_{SUPPLY}$
Logic Low Level (V_{AL}) .... 0V to 0.8V
Logic High Level (V_{AH}) .... 2.4V to $+V_{SUPPLY}$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{REF} = OPEN, GND = 0V, Unless Otherwise Specified

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch "ON" Resistance	R_{DS}	V_A = 0.8V, V_S = 10V, I_D = -1mA All Unused Channels V_A = 2.4V	1	+25°C	-	70	Ω
			2, 3	-55°C to +125°C	-	100	Ω
		V_A = 0.8V, V_S = -10V, I_D = 1mA All Unused Channels V_A = 2.4V	1	+25°C	-	70	Ω
			2, 3	-55°C to +125°C	-	100	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = +14V, V_D = -14V, V_A = 2.4V All Unused Channels V_A = 2.4V, V_D = +14V, V_S = -14V	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = -14V, V_D = +14V, V_A = 2.4V All Unused Channels V_A = 2.4V, V_D = -14V, V_S = +14V	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-100	100	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_D = -14V, V_S = +14V, V_A = 2.4V All Unused Channels V_A = 2.4V, V_D = +14V, V_S = -14V	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_D = +14V, V_S = -14V, V_A = 2.4V All Unused Channels V_A = 2.4V, V_D = -14V, V_S = +14V	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-100	100	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = +14V, V_A = 0.8V All Unused Channels V_A = 0.8V, V_D = V_S = -14V	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_D = V_S = -14V, V_A = 0.8V All Unused Channels V_A = 0.8V, V_D = V_S = +14V	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-200	200	nA
Low Level Input Current	I_{AL}	V_{AL} = 0.8V All Unused Channels V_A = 2.4V	1	+25°C	-0.5	0.5	µA
			2, 3	-55°C to +125°C	-1.0	1.0	µA
High Level Input Current	I_{AH}	V_{AH} = 2.4V and 15V All Unused Channels V_A = 2.4V	1	+25°C	-0.5	0.5	µA
			2, 3	-55°C to +125°C	-1.0	1.0	µA
Supply Current	$+I_{CC}$	All Channels V_A = 0.8V	1, 2	+25°C, +125°C	-	1.5	mA
			3	-55°C	-	2.0	mA
		All Channels V_A = 2.4V	1, 2	+25°C, +125°C	-	1.5	mA
			3	-55°C	-	2.0	mA
Supply Current	$-I_{CC}$	All Channels V_A = 0.8V	1, 2	+25°C, +125°C	-1.5	-	mA
			3	-55°C	-2.0	-	mA
		All Channels V_A = 2.4V	1, 2	+25°C, +125°C	-1.5	-	mA
			3	-55°C	-2.0	-	mA

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{REF} = OPEN, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Turn "ON" Time	$t_{(ON)}$	C_L = 100pF R_L = 1kΩ	9	+25°C	-	600	ns
			10, 11	-55°C, +125°C	-	800	ns
Turn "OFF" Time	$t_{(OFF)}$	C_L = 100pF R_L = 1kΩ	9	+25°C	-	500	ns
			10, 11	-55°C, +125°C	-	650	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Characterized at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{REF} = OPEN, GND = 0V

PARAMETERS	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address Capacitance	C_A	f= 1MHz, V_{AL} = 0V	1	+25°C	-	15	pF
Switch Input Capacitance	$C_{S(OFF)}$	f = 1MHz, V_{AH} = 5V Measure Input to Ground	1	+25°C	-	15	pF
Switch Output Capacitance	$C_{D(OFF)}$	f = 1MHz, V_{AH} = 5V Measure Output to Ground	1	+25°C	-	20	pF
	$C_{D(ON)}$	f = 1MHz, V_{AL} = 0V Measure Output to Ground	1	+25°C	-	30	pF
Drain to Source Capacitance	C_{DS}	f = 1MHz, V_{AH} = 5V	1	+25°C	-	2.0	pF
Off Isolation	V_{ISO}	f = 200kHz, V_A = 2.4, R_L = 1K V_{GEN} = $1V_{p-p}$, C_L = 10pF	1	+25°C	55	-	dB
Crosstalk	V_{CT}	f = 200kHz, V_A = 2.4, R_L = 1K V_{GEN} = $1V_{p-p}$, C_L = 10pF	1	+25°C	60	-	dB
Charge Transfer Error	V_{CTE}	f = 200kHz, V_A = 0 to 4V C_L = 0.01µF	1	+25°C	-10	10	mV

NOTE 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

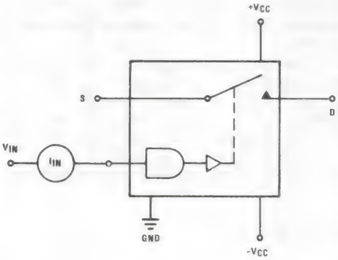
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

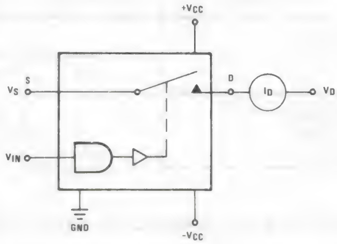
* PDA applies to Subgroup 1 only.

Test Circuits

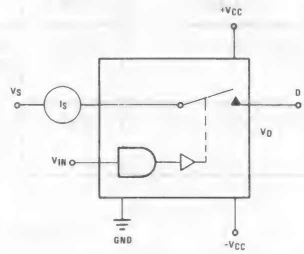
INPUT LEAKAGE CURRENT



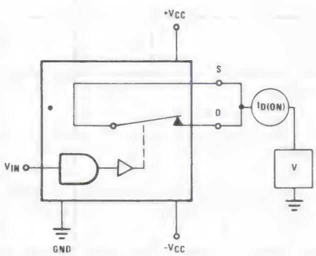
ID(OFF)



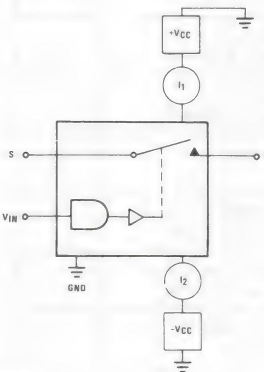
IS(OFF)



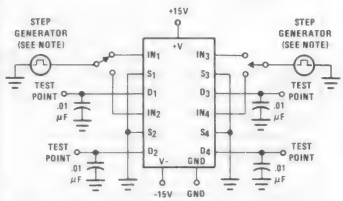
ID(ON)



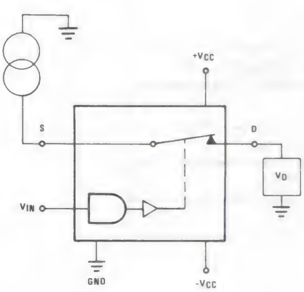
SUPPLY CURRENTS



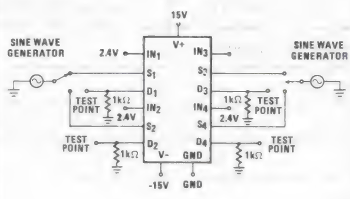
CHARGE TRANSFER ERROR



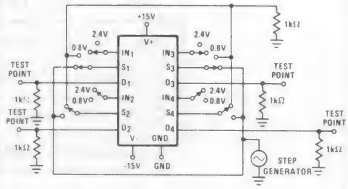
RDS



OFF CHANNEL ISOLATION

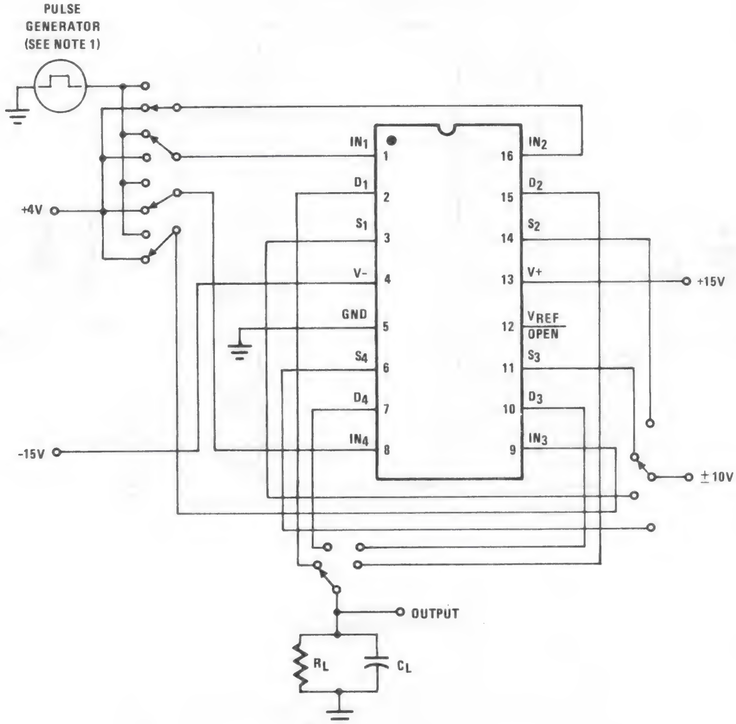


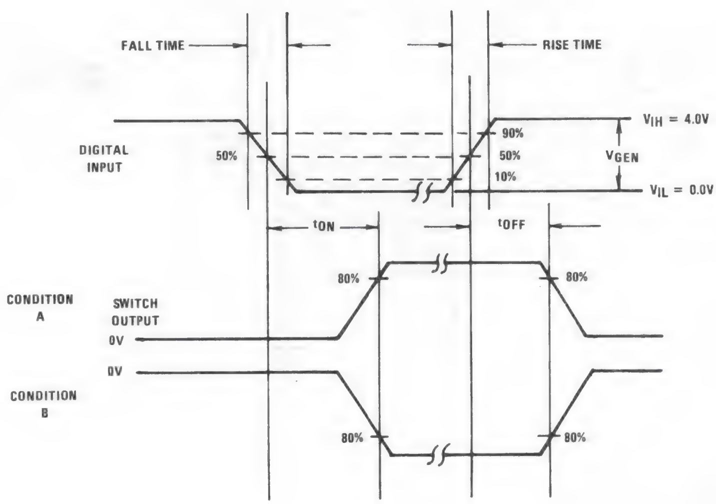
CROSSTALK BETWEEN CHANNELS



For Detail Information Refer to HI-201/883 Test Tech Brief

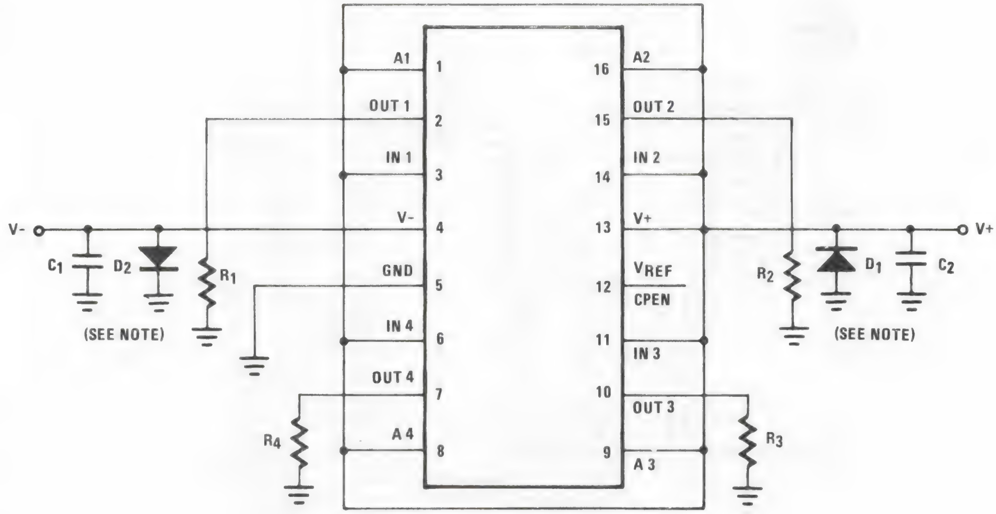
Switching Waveforms



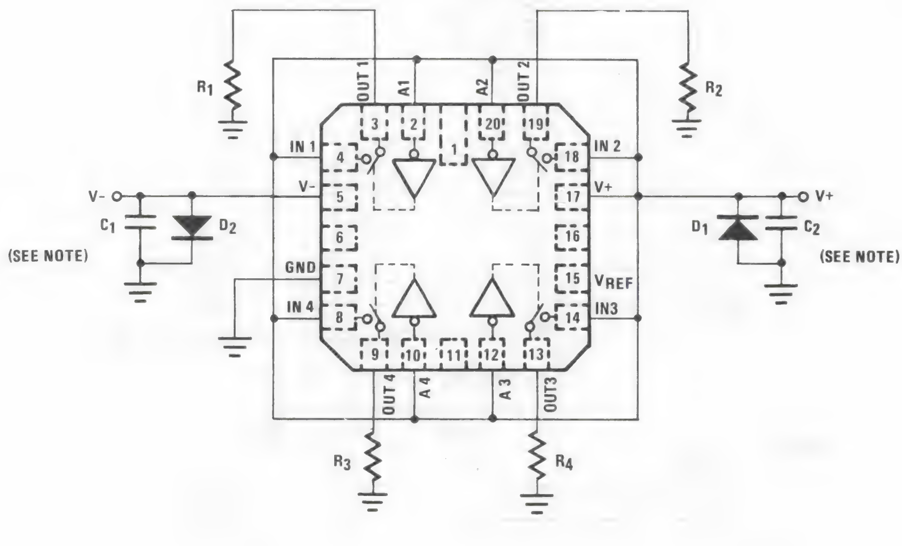


Burn-In Circuits

HI-201/883 CERAMIC DIP



HI-201/883 CERAMIC LCC



NOTES:

$R_1 = R_2 = R_3 = R_4 = 10k\Omega$

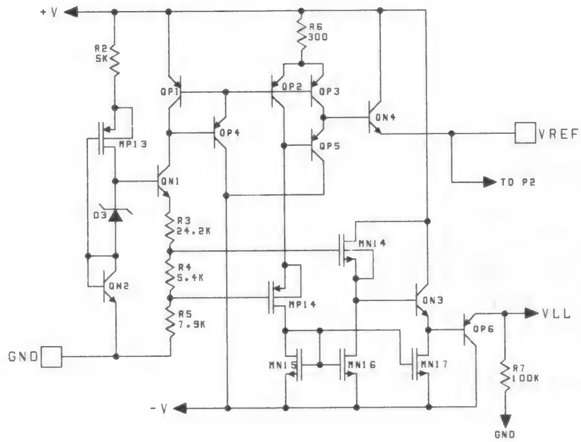
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)

$D_1 = D_2 =$ IN4002 or Equivalent/Board

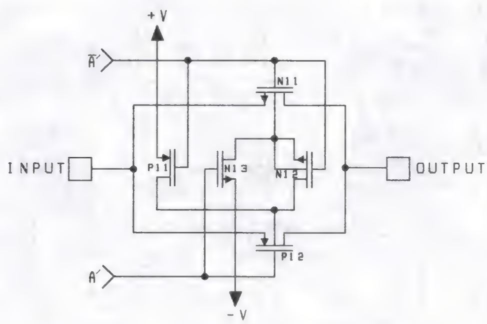
$|(V+) + (V-)| = 30V$

Schematic Diagrams

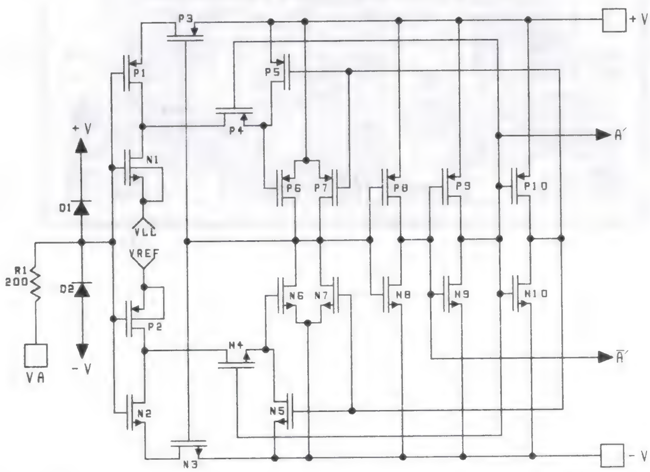
TTL/CMOS REFERENCE CIRCUIT



SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



Die Characteristics

DIE DIMENSIONS:
81 x 85 x 19 mils

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

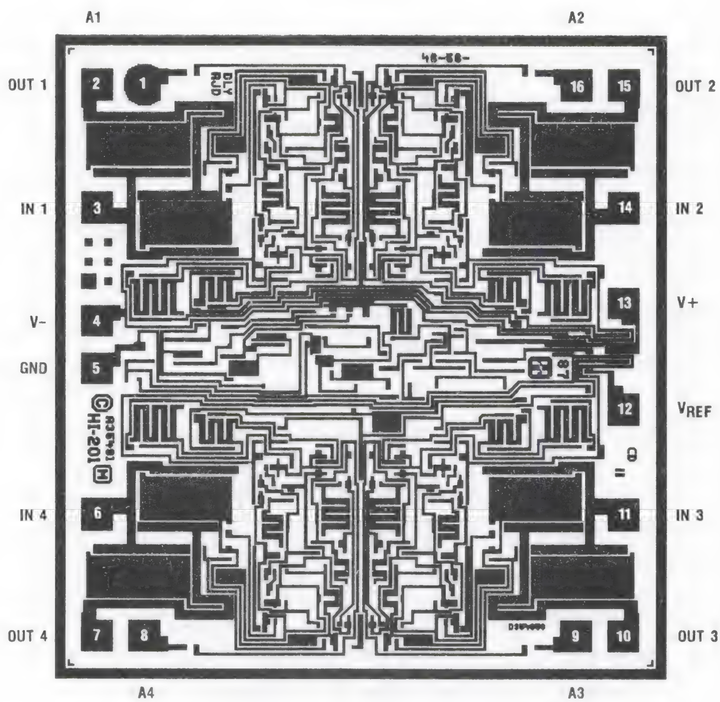
GLASSIVATION:
Type: Nitride over Silox
Silox Thickness: 12kÅ ± 2kÅ
Nitride Thickness: 3.5kÅ ± 1kÅ

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:
$2 \times 10^5 A/cm^2$ at 25mA

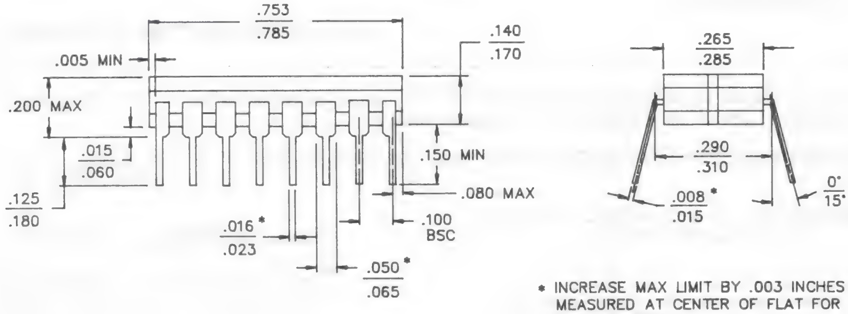
Metallization Mask Layout

H1-201/883



Packaging†

16 PIN CERAMIC DIP

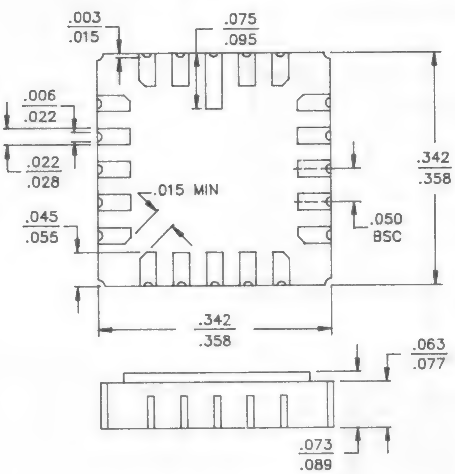


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-2

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

4 CMOS ANALOG SWITCHES

DESIGN INFORMATION

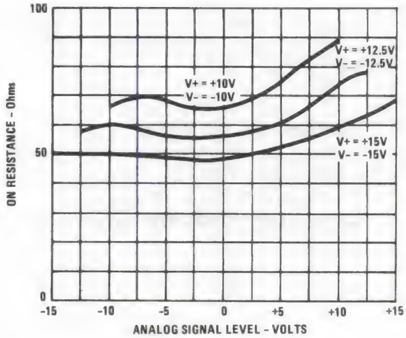
Quad SPST CMOS Analog Switch

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. No guarantee is implied.

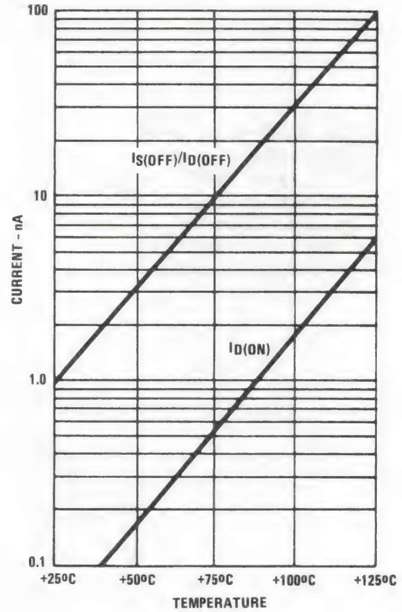
Typical Performance Characteristics

Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$
$V_{AH} = 2.4V$, $V_{AL} = 0.8V$, V_{REF} = Open

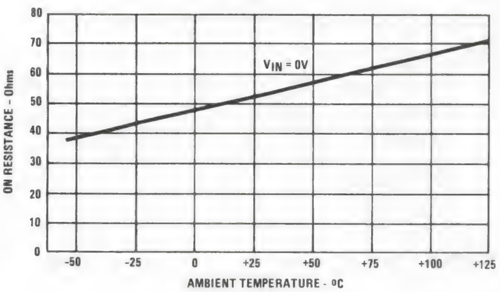
ON RESISTANCE vs. ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE



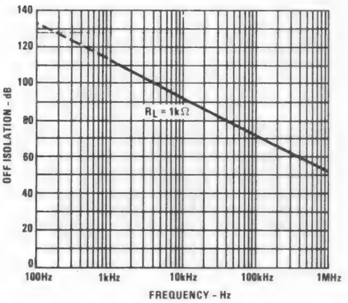
LEAKAGE CURRENT vs. TEMPERATURE



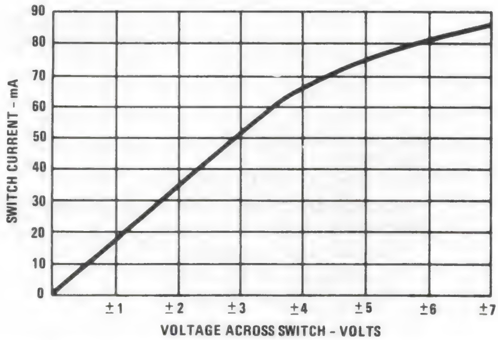
ON RESISTANCE vs. TEMPERATURE



OFF ISOLATION vs. FREQUENCY



SWITCH CURRENT vs. VOLAGE



HARRIS HI-201HS/883

High Speed Quad SPST CMOS Analog Switch

January 1989

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Low "ON" Resistance .... 50Ω Max**
- **Wide Analog Signal Range .... ±15V**
- **Turn-On Time 50ns**
- **Analog Current Range (Continuous) 25mA**
- **TTL/CMOS Compatible**
- **No Latch-Up**
- **Pin Compatible with Standard HI-201**

Applications

- **High Speed Multiplexing**
- **High Frequency Analog Switching**
- **Sample and Hold Circuits**
- **Digital Filters**
- **Op Amp Gain Switching Networks**
- **Integrator Reset Circuits**

Description

HI-201HS/883 is a monolithic CMOS Analog Switch featuring very fast switching speeds and low ON resistance. This integrated circuit consists of four independently selectable SPST switches and is pin compatible with the industry standard HI-201 switch.

Fabricated using silicon-gate technology and the Harris dielectric isolation process, this TTL compatible device offers improved performance over previously available CMOS analog switches while eliminating the problem of latch-up associated with other fabricated processes. Featuring maximum switching times of 50ns, low ON resistance of 50Ω maximum, and a wide analog signal range, the HI-201HS/883 is designed for any military application where improved switching performance, particularly switching speed, is required. (A more detailed discussion on the design and application of the HI-201HS/883 can be found in Application Note 543).

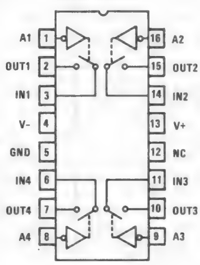
The HI-201HS/883 is available in a 16 pin Ceramic DIP package and a 20 pin LCC package. The HI-201HS/883 is specified over the temperature range of -55°C to +125°C.

4

CMOS ANALOG SWITCHES

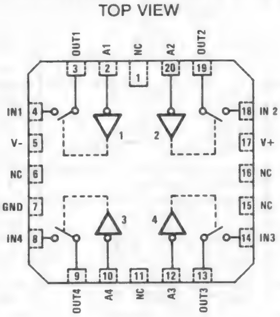
Pinouts

HI1-201HS/883 (CERAMIC DIP)
TOP VIEW

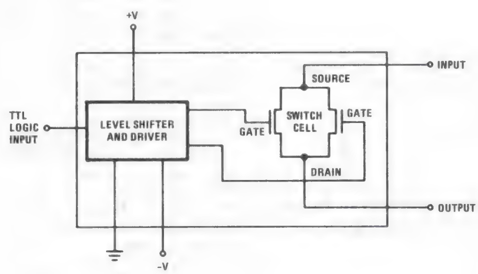


LOGIC	SWITCH
0	ON
1	OFF

HI4-201HS/883 (CERAMIC LCC)
TOP VIEW



Functional Diagram



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 36V
$\pm V_{SUPPLY}$ to Ground (V+, V-) .... ±18V
Analog Input Voltage $+V_S$ .... $+V_{SUPPLY}$ +2V
$-V_S$ .... $-V_{SUPPLY}$ -2V
Digital Input Voltage $+V_A$ .... $+V_{SUPPLY}$ +4V
$-V_A$ .... $-V_{SUPPLY}$ -4V
Peak Current (S or D)
(Pulse at 1ms, 10% Duty Cycle Max) 50mA
Continuous Current Any Terminal (Except S or D) 25mA
Junction Temperature .... +175°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering 10 sec) .... ≤275°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	75°C/W	16°C/W
Ceramic LCC Package	76°C/W	19°C/W

Package Power Dissipation at +75°C
Ceramic DIP Package 1.0W
Ceramic LCC Package 0.99W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 13.36mW/°C
Ceramic LCC Package .... 13.12mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) .... ±15V
Analog Input Voltage (V_S) .... $\pm V_{SUPPLY}$
Logic Low Level (V_{AL}) .... 0V to 0.8V
Logic High Level (V_{AH}) .... 3.0V to $+V_{SUPPLY}$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = −15V, GND = 0V, Unless Otherwise Specified

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	MAX	UNITS
Switch "ON" Resistance	R_{DS}	V_{AL} = 0.8V, V_S = 10V, I_D = −1mA All Unused Channels V_{AL} = 0.8V	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
		V_{AL} = 0.8V, V_S = −10V, I_D = 1mA All Unused Channels V_{AL} = 0.8V	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = +14V, V_D = −14V, V_{AH} = 3.0V All Unused Channels V_{AH} = 3.0V, V_D = +14V, V_S = −14V	1	+25°C	-10	10	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = −14V, V_D = +14V, V_{AH} = 3.0V All Unused Channels V_{AH} = 3.0V, V_D = −14V, V_S = +14V	1	+25°C	-10	10	nA
			2, 3	-55°C to +125°C	-100	100	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_D = −14V, V_S = +14V, V_{AH} = 3.0V All Unused Channels V_{AH} = 3.0V, V_D = +14V, V_S = −14V	1	+25°C	-10	10	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_D = +14V, V_S = −14V, V_{AH} = 3.0V All Unused Channels V_{AH} = 3.0V, V_D = −14V, V_S = +14V	1	+25°C	-10	10	nA
			2, 3	-55°C to +125°C	-100	100	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = +14V, V_{AL} = 0.8V All Unused Channels V_{AL} = 0.8V, V_D = V_S = −14V	1	+25°C	-10	10	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_D = V_S = −14V, V_{AL} = 0.8V All Unused Channels V_{AL} = 0.8V, V_D = V_S = +14V	1	+25°C	-10	10	nA
			2, 3	-55°C to +125°C	-100	100	nA
Low Level Input Current	I_{AL}	V_{AL} = 0.8V All Unused Channels V_{AH} = 4.0V	1	+25°C	-	500	μA
			2, 3	-55°C to +125°C	-	500	μA
High Level Input Current	I_{AH}	V_{AH} = 4.0V All Unused Channels V_{AL} = 0.8V	1	+25°C	-	40	μA
			2, 3	-55°C to +125°C	-	40	μA
Supply Current	$+I_{CC}$	All Channels V_{AL} = 0.8V	1, 2	+25°C, +125°C	-	10	mA
			3	-55°C	-	10	mA
		All Channels V_{AH} = 3.0V	1, 2	+25°C, +125°C	-	10	mA
			3	-55°C	-	10	mA
Supply Current	$-I_{CC}$	All Channels V_{AL} = 0.8V	1, 2	+25°C, +125°C	-	6	mA
			3	-55°C	-	6	mA
		All Channels V_{AH} = 3.0V	1, 2	+25°C, +125°C	-	6	mA
			3	-55°C	-	6	mA

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Turn "ON" Time	$t_{(ON)}$	$C_L = 35pF$, $R_L = 1k\Omega$ $V_{AH} = 3.0V$, $V_{AL} = 0.8V$	9	+25°C	-	50	ns
			10, 11	-55°C, +125°C	-	100	ns
Turn "OFF" Time	$t_{(OFF)}$	$C_L = 35pF$, $R_L = 1k\Omega$ $V_{AH} = 3.0V$, $V_{AL} = 0.8V$	9	+25°C	-	50	ns
			10, 11	-55°C, +125°C	-	100	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Characterized at: $+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$, GND = 0V

PARAMETERS	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Address Capacitance	C_A	f= 1MHz, $V_{AL} = 0V$	1	+25°C	-	35	pF
Switch Input Capacitance	$C_{S(OFF)}$	f = 1MHz, $V_{AH} = 5V$ Measure Input to Ground	1	+25°C	-	20	pF
Switch Output Capacitance	$C_{D(OFF)}$	f = 1MHz, $V_{AH} = 5V$ Measure Output to Ground	1	+25°C	-	20	pF
	$C_{D(ON)}$	f = 1MHz, $V_{AL} = 0V$ Measure Output to Ground	1	+25°C	-	50	pF
Drain to Source Capacitance	C_{DS}	f = 1MHz, $V_{AH} = 5V$	1	+25°C	-	2.0	pF
Off Isolation	V_{ISO}	f = 100kHz, $V_A = 3.0$, $R_L = 1K$ $V_{GEN} = 1V_{p-p}$, $C_L = 10pF$	1	+25°C	50	-	dB
Crosstalk	V_{CT}	f = 100kHz, $V_A = 3.0$, $R_L = 1K$ $V_{GEN} = 1V_{p-p}$, $C_L = 10pF$	1	+25°C	50	-	dB
Charge Transfer Error	V_{CTE}	$R_L = 1K$, $C_L = 0.01\mu F$	1	+25°C	-	10	mV

NOTE 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

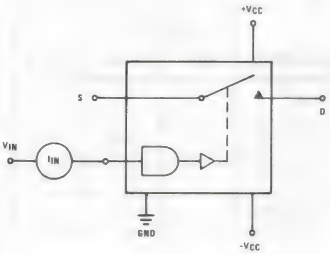
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

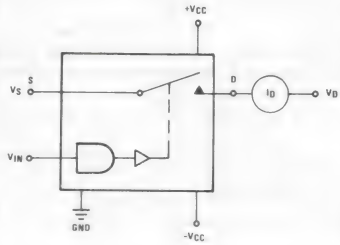
* PDA applies to Subgroup 1 only.

Test Circuits

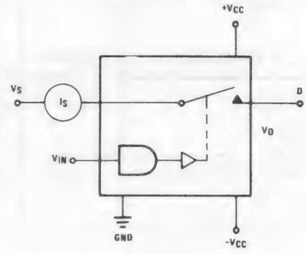
INPUT LEAKAGE CURRENT



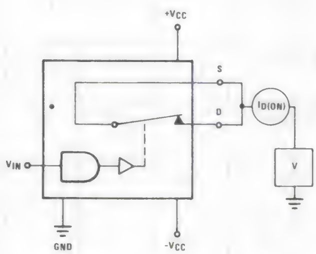
ID(OFF)



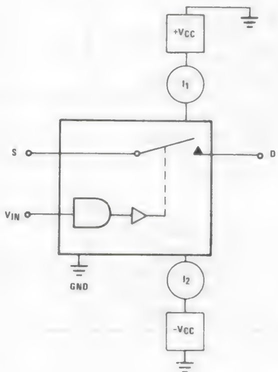
IS(OFF)



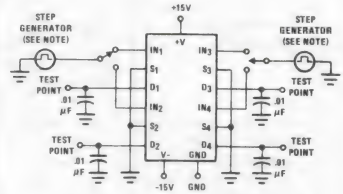
ID(ON)



SUPPLY CURRENTS

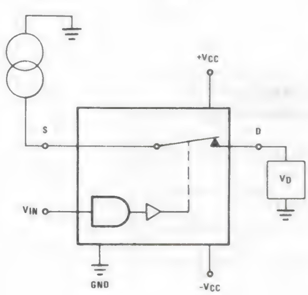


CHARGE TRANSFER ERROR

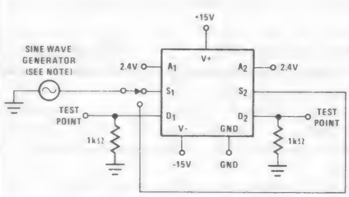


NOTE:
The pulse generator has the following characteristics: V_{GEN} = 0 to 3V, rise time ≤ 20ns, fall time ≤ 20ns, PRR = 100kHz.

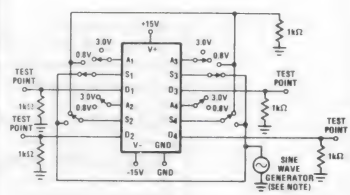
RDS



OFF CHANNEL ISOLATION



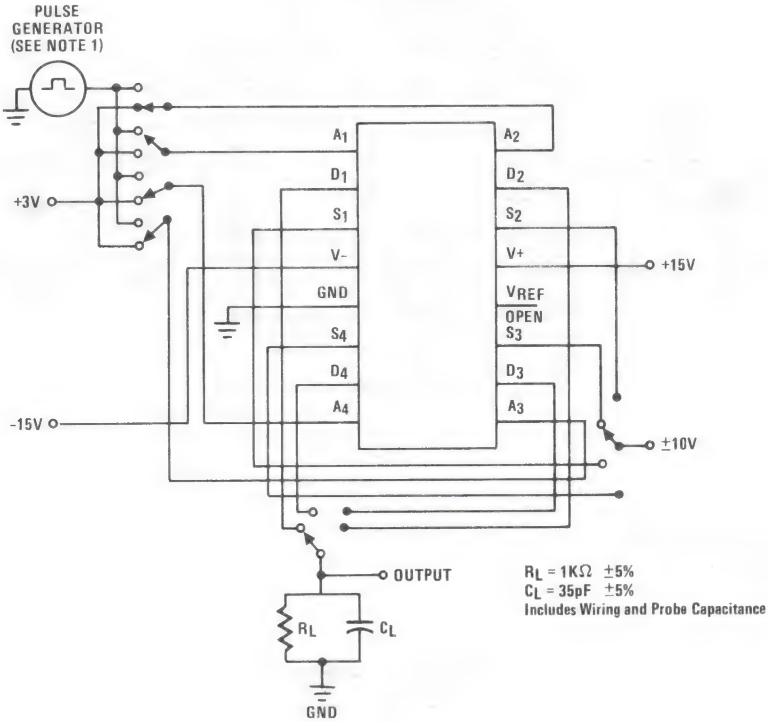
CROSSTALK BETWEEN CHANNELS



NOTE:
The pulse generator has the following characteristics: V_{GEN} = $1V_{p-p}$, frequency = 100kHz.

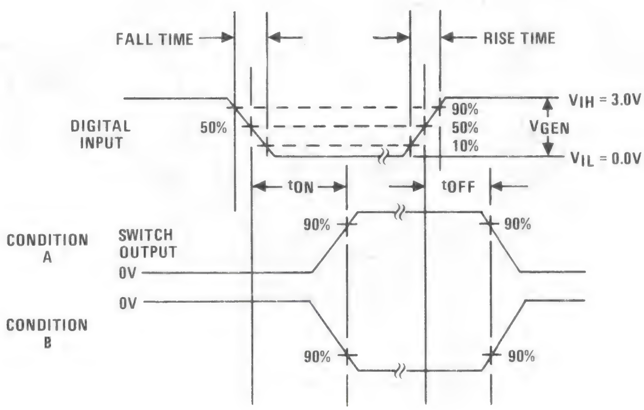
See Test Tech Brief For Additional Information

Switching Waveforms



NOTES: 1. The pulse generator has the following characteristics: V_{GEN} = 3.0V, $t_{THL} \leq$ 20ns.

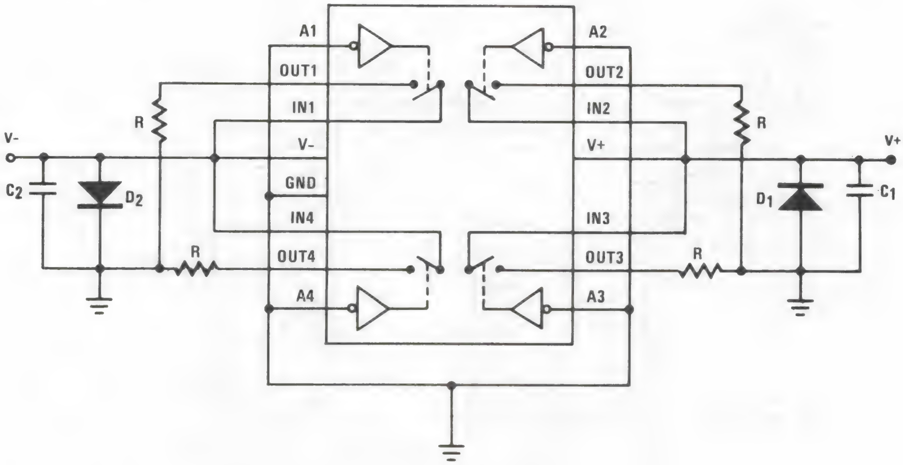
2. See Table 2 for complete terminal conditions.



NOTE: Rise time and fall time ≤ 20ns

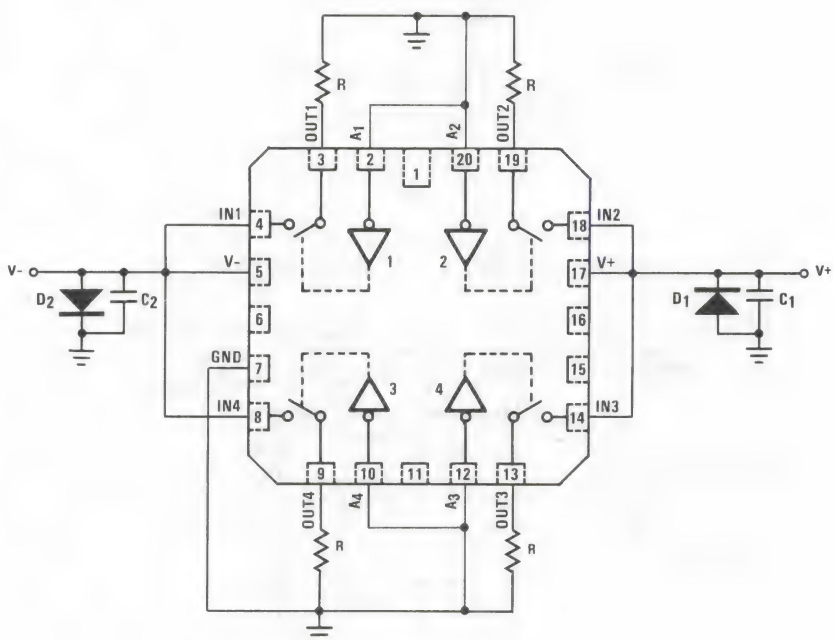
Burn-In Circuits

HI-201HS/883 CERAMIC DIP



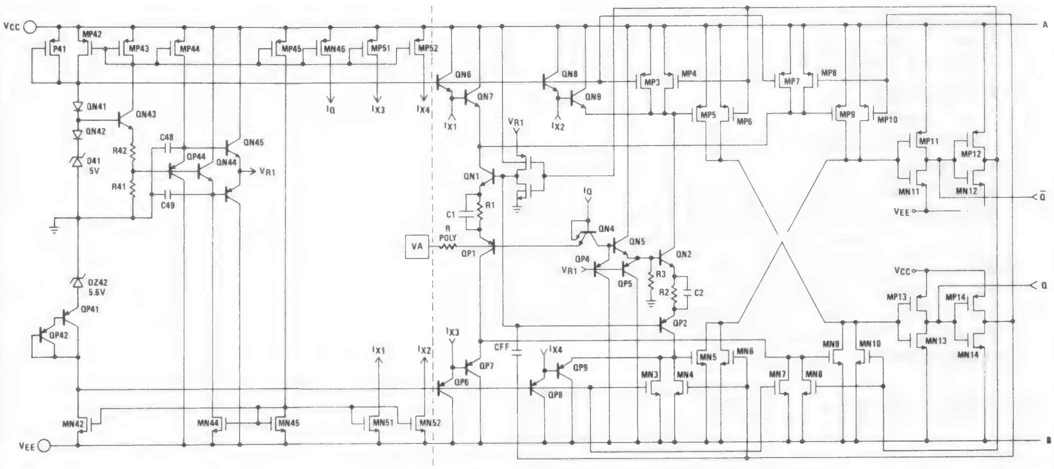
NOTES:
R = 10KΩ, 5%, 1/4 or 1/2W
$C_1 = C_2 = 0.1\mu F$ (one per row) or $.01\mu F$ (one per socket)
$D_1 = D_2$ = IN4002 or equivalent (one per board)
$|(V+) - (V-)| = 30V$

HI-201HS/883 CERAMIC LCC

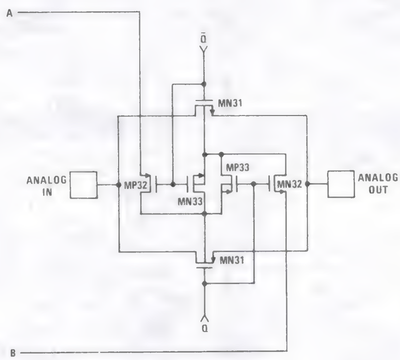


Schematic Diagrams

REFERENCE/LEVEL SHIFTER



SWITCH CELL



Die Characteristics

DIE DIMENSIONS:
92 x 111 x 19 mils

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

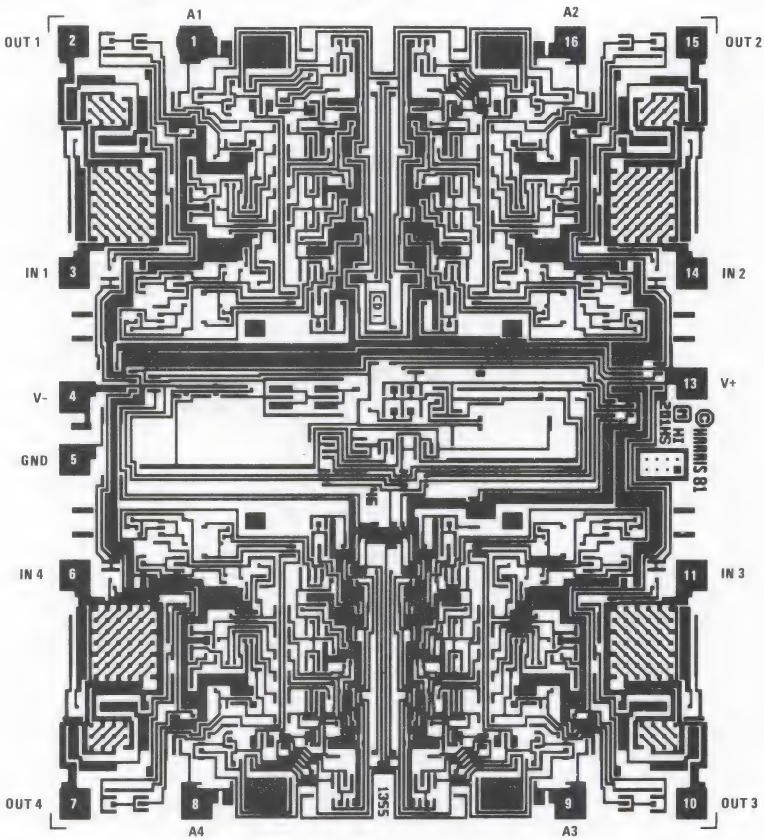
GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:
$4.5 \times 10^5 A/cm^2$ at 25mA
This device meets Glassivation Integrity Test requirement per Mil-Std-883 Method 2021 and Mil-M-38510 paragraph 3.5.5.4.

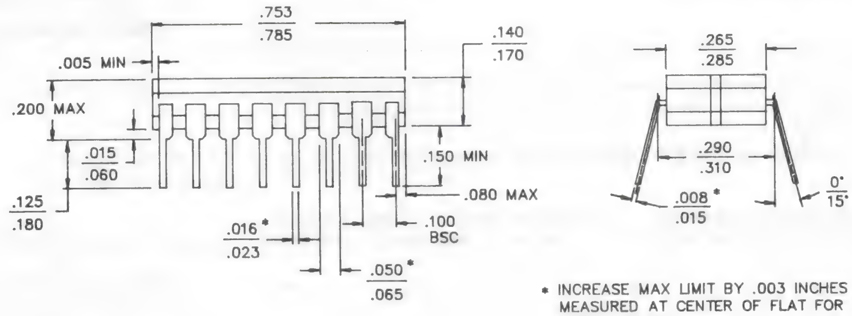
Metallization Mask Layout

HI-201HS/883



Packaging†

16 PIN CERAMIC DIP

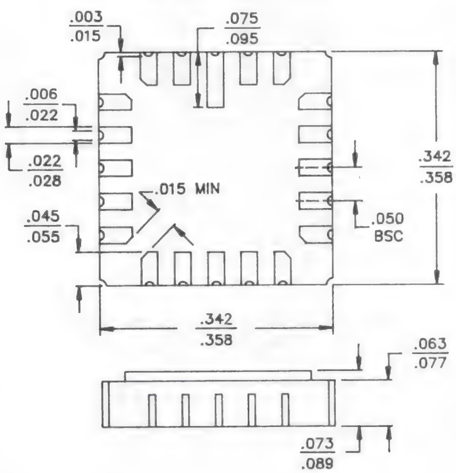


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-2

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

HI-201HS

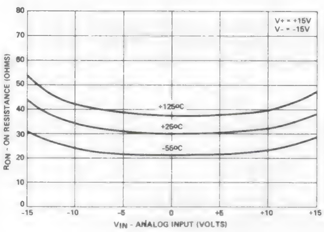
DESIGN INFORMATION

High Speed Quad SPST CMOS Analog Switch

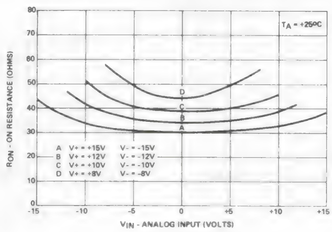
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$, $V_{AH} = 3.0V$, $V_{AL} = 0.8V$

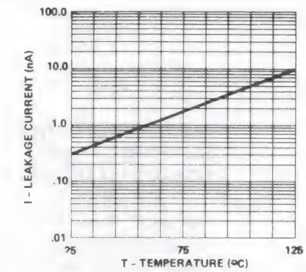
ON RESISTANCE vs. ANALOG SIGNAL LEVEL AND TEMPERATURE



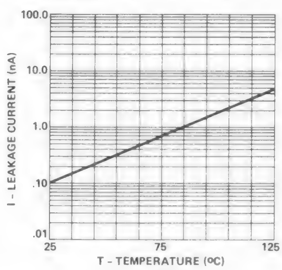
ON RESISTANCE vs. ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE



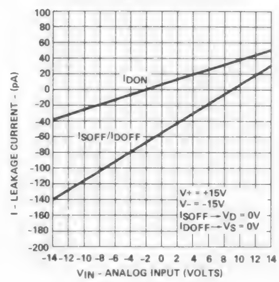
$I_{S(OFF)}$ or $I_{D(OFF)}$ vs. TEMPERATURE



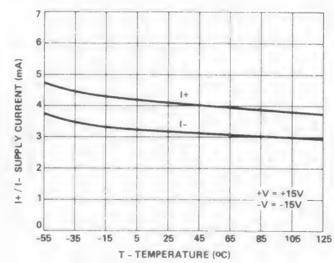
$I_{D(ON)}$ vs. TEMPERATURE



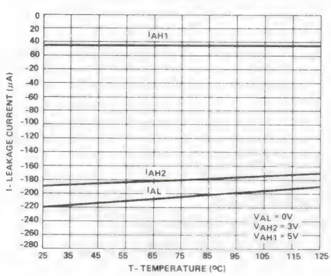
LEAKAGE CURRENT vs. ANALOG INPUT VOLTAGE



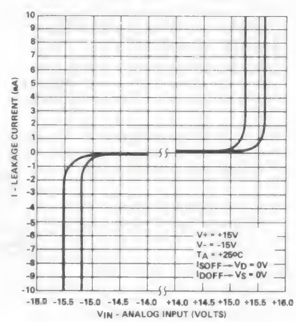
SUPPLY CURRENT vs. TEMPERATURE



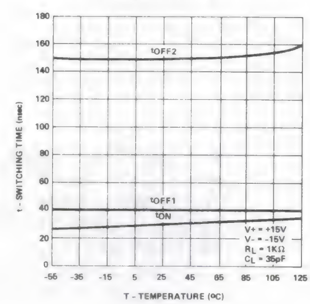
DIGITAL INPUT LEAKAGE CURRENT vs. TEMPERATURE



LEAKAGE CURRENT vs. ANALOG INPUT VOLTAGE ($V_{IN} \geq +14V$, $V_{IN} \geq -14V$)



SWITCHING TIME vs. TEMPERATURE

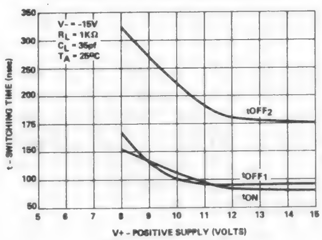


DESIGN INFORMATION (Continued)

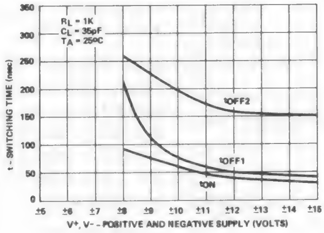
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics Unless Otherwise Specified: T_A = +25°C, V_{SUPPLY} = ±15V, V_{AH} = 3.0V, V_{AL} = 0.8V

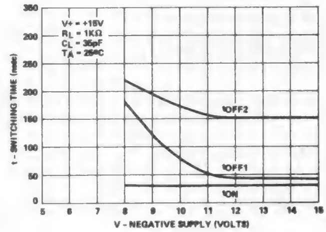
SWITCHING TIME vs. POSITIVE SUPPLY VOLTAGE



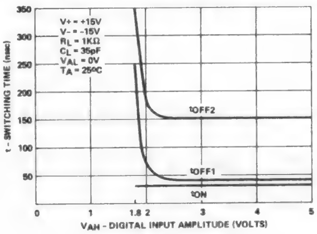
SWITCHING TIME vs. POSITIVE AND NEGATIVE SUPPLY VOLTAGE



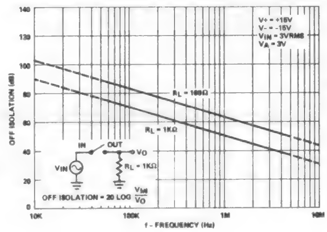
SWITCHING TIME vs. NEGATIVE SUPPLY VOLTAGE



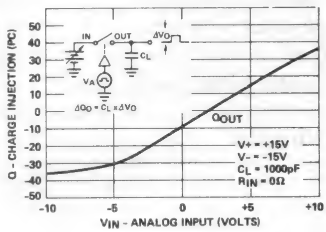
SWITCHING TIME vs. INPUT LOGIC AMPLITUDE



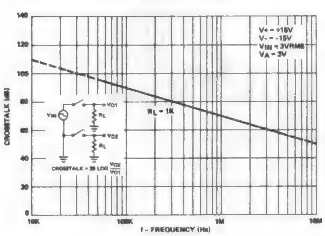
OFF ISOLATION vs. FREQUENCY



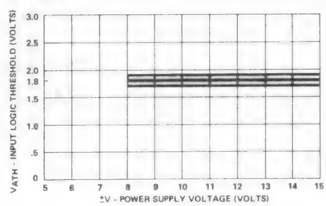
CHARGE INJECTION vs. ANALOG INPUT



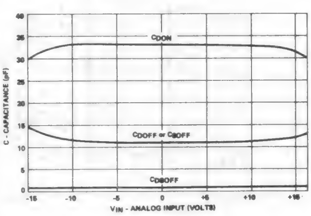
CROSSTALK vs. FREQUENCY



INPUT SWITCHING THRESHOLD vs. POSITIVE AND NEGATIVE SUPPLY VOLTAGES



CAPACITANCE vs. ANALOG INPUT



4

CMOS ANALOG SWITCHES

HARRIS

HI-222/883

January 1989

High Frequency/Video Switch

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Wideband Operation .... 150 MHz
- Differential Gain .... 0.03% (Typ) 0.1% (Max)
- Differential Phase .... 0.003 Degrees (Typ) 0.01 Degrees (Max)
- Switching Speed .... 100ns (Typ) 200ns (Max)
- R_{ON} .... 35Ω (Typ) 75Ω (Max)
- Off Isolation @ 10 MHz .... -65dB (Typ) -60dB (Max)
- Crosstalk @ 10 MHz .... -80dB (Typ) -75dB (Max)

Applications

- Routing Switchers
- Production Mixers
- High Definition TV
- Radar Signal Conditioning
- Medical Imaging
- Heads-Up Displays
- Simulators
- Sonar

Description

The HI-222/883 is a high frequency analog switch that complements the Harris family of high speed op amps and buffers. Fabricated with our Dielectric Isolation process and using silicon gate technology, many key parameters have been enhanced.

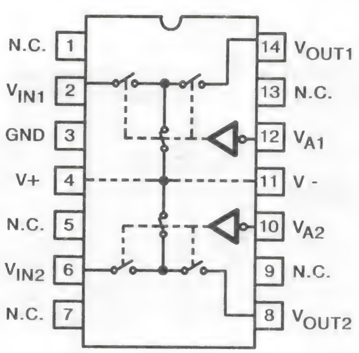
Crosstalk and off isolation are optimized with a T-switch configuration and the use of nonconnected pins for extended shielding. Other features of the HI-222/883 include wideband operation, low R_{ON}, fast switching speeds and low differential gain and phase. The characteristics of this TTL compatible device make it ideal for designs where improved switching performance is required.

The primary application of this dual SPST switch is the routing of high frequency signals in equipment ranging from video production mixers to military RF circuits.

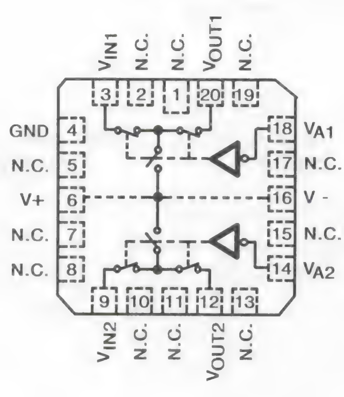
The HI-222/883 is available in a 14 pin Ceramic DIP or a 20 pin Ceramic LCC and is specified over the -55°C to +125°C temperature range.

Pinouts

HI1-222/883 (CERAMIC DIP)
LOGIC "1" INPUT
TOP VIEW



HI4-222/883 (CERAMIC LCC)
LOGIC "0" INPUT
TOP VIEW



NOTE: Source and Drain are arbitrarily depicted as Analog Input and Output, respectively. They may be interchanged without affecting performance. All nonconnected pins should be tied to ground.

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 36V
$\pm V_{SUPPLY}$ to Ground (V+, V-) ..... ±18V
Digital and Analog Input Voltage (V_A, V_S, V_D) ..... $+V_{SUPPLY}$ +2V
$-V_{SUPPLY}$ -2V
Peak Current (Source to Drain)
(Pulse at 0.8ms, 10% Duty Cycle Max) 100mA
Peak Current (Any Pin, 50% Duty Cycle) 28mA
Continuous Current (Any Pin) 15mA
Junction Temperature ..... +175°C
Storage Temperature Range ..... -65°C to +150°C
ESD Rating ..... < 2000V
Lead Temperature (Soldering 10 sec) ..... 300°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	75°C/W	17°C/W
Ceramic LCC Package	76°C/W	19°C/W

Package Power Dissipation Limit at +75°C
Ceramic DIP Package 1.0W
Ceramic LCC Package 1.0W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package ..... 13.4mW/°C
Ceramic LCC Package ..... 13.2mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage ..... ±15V
Analog Input Voltage (V_S) ..... $\pm V_{SUPPLY}$
Address Low Level (V_{AL}) ..... 0V to 0.8V
Address High Level (V_{AH}) ..... 2.0V to +5.0V
Ground All Nonconnected Pins.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, V_{AH} = 2.0V, V_{AL} = +0.8V, Unused Pins are Grounded.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch "ON" Resistance	R_{DS}	V_D = 5V, I_S = 7.5mA S1/S2	1	+25°C	-	60	Ω
			2, 3	-55°C to +125°C	-	75	Ω
		V_D = -5V, I_S = -7.5mA S1/S2	1	+25°C	-	60	Ω
			2, 3	-55°C to +125°C	-	75	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = 5V, V_D = -5V S1/S2	1	+25°C	-2.5	2.5	nA
			2, 3	-55°C to +125°C	-200	200	nA
		V_S = -5V, V_D = 5V S1/S2	1	+25°C	-2.5	2.5	nA
			2, 3	-55°C to +125°C	-200	200	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_D = 5V, V_S = -5V S1/S2	1	+25°C	-2.5	2.5	nA
			2, 3	-55°C to +125°C	-200	200	nA
		V_D = -5V, V_S = 5V S1/S2	1	+25°C	-2.5	2.5	nA
			2, 3	-55°C to +125°C	-200	200	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = 5V S1/S2	1	+25°C	-2.5	2.5	nA
			2, 3	-55°C to +125°C	-200	200	nA
		V_D = V_S = -5V S1/S2	1	+25°C	-2.5	2.5	nA
			2, 3	-55°C to +125°C	-200	200	nA
Low Level Address Current	I_{AL}	V_A = 0.8V A_1, A_2	1	+25°C	-	1.0	µA
			2, 3	-55°C to +125°C	-	1.0	µA
High Level Address Current	I_{AH}	V_A = 2.0V A_1, A_2	1	+25°C	-	1.0	µA
			2, 3	-55°C to +125°C	-	1.0	µA
Positive Supply Current	$+I_{CC}$	V_A = 0.8V, 2.0V A_1, A_2	1	+25°C	-	4.0	mA
			2, 3	-55°C to +125°C	-	6.0	mA
Negative Supply Current	$-I_{CC}$	V_A = 0.8V, 2.0V A_1, A_2	1	+25°C	-4.0	-	mA
			2, 3	-55°C to +125°C	-6.0	-	mA

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, V_{AH} = 2.0V, V_{AL} = 0.8V, Ground All Nonconnected Pins.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Turn "ON" Time	t_{ON}	V_S = 5V, C_L = 35pF, R_L = 2kΩ	9	+25°C	-	150	ns
			10, 11	-55°C, +125°C	-	200	ns
Turn "OFF" Time	t_{OFF}	V_S = 5V, C_L = 35pF, R_L = 2kΩ	9	+25°C	-	150	ns
			10, 11	-55°C, +125°C	-	200	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Characterized at: Supply Voltage = ±15V, V_{AH} = 2.0V, V_{AL} = 0.8V, Ground All Nonconnected Pins.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
"On" Resistance Match (Channel to Channel)	R_{ON} Match	V_D = ±5V, I_D = 7.5mA	1	+25°C	-	5	Ω
Address Capacitance	C_A	V_A = 2.0V, 0.8V	1	+25°C	-	10	pF
Switch Input Capacitance	$C_{S(OFF)}$	Switch Off: V_A = 2.0V	1	+25°C	-	25	pF
Switch Output Capacitance	$C_{D(OFF)}$	Switch Off: V_A = 2.0V	1	+25°C	-	60	pF
	$C_{D(ON)}$	Switch On: V_A = 0.8V	1	+25°C	-	150	pF
Drain to Source Capacitance	$C_{DS(OFF)}$	Switch Off: V_A = 2.0V	1	+25°C	-	2.0	pF
Off Isolation	V_{ISO}	V_S = 300mV_{p-p} @ f = 10MHz, R_L = 50Ω	1	+25°C	-	-60	dB
Crosstalk	V_{CT}	V_S = 300mV_{p-p} @ f = 10MHz, R_L = 50Ω	1	+25°C	-	-75	dB
Gain Tolerance	A_V±	V_S = 300mV_{p-p} R_L = 50Ω @ 1MHz	1	+25°C	-	-0.1	dB
		V_S = 300mV_{p-p} R_L = 50Ω @ 8MHz	1	+25°C	-	-0.5	dB
Differential Gain	A_{DIFF}	V_S = 300mV_{p-p}, R_L = 2kΩ, V_{OFFSET} = 0V to 1V, f = 3.58MHz and 4.43MHz	1	+25°C	-	0.1	%
Differential Phase	Δ_{DIFF}		1	+25°C	-	0.01	Degrees

NOTE 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

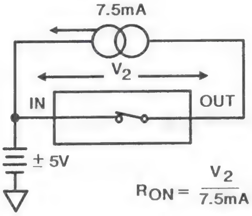
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

Test Circuits

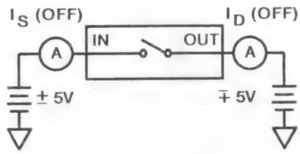
R_{DS}



$R_{ON} = \frac{V_2}{7.5mA}$

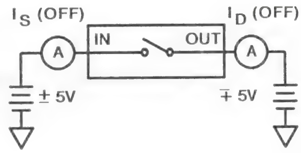
$V_{IN} = \pm5V$, $I = 7.5mA$, $V_A = 0.8V$

$I_{S(OFF)}$



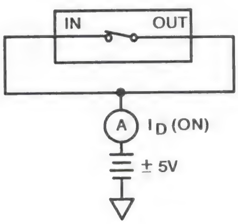
$V_{IN} = \pm5V$, $V_{OUT} = \mp5V$, $V_A = 2.0V$

$I_{D(OFF)}$



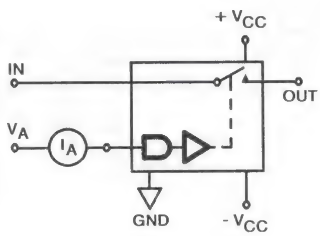
$V_{IN} = \pm5V$, V_{OUT} $\mp5V$, $V_A = 2.0V$

$I_{D(ON)}$



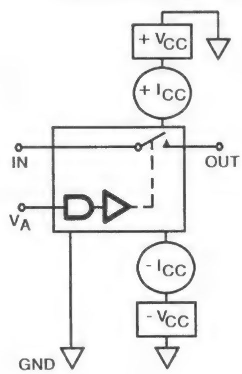
$V_{IN} = \pm5V$, $V_{OUT} = \pm5V$, $V_A = 0.8V$

ADDRESS CURRENT



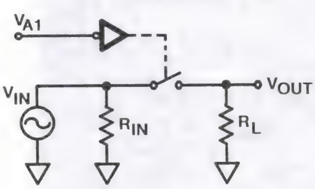
$V_{AH} = 2.0V$, $V_{AL} = 0.8V$

SUPPLY CURRENTS



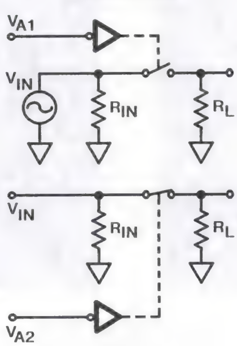
$V_A = 0.8V, 2.0V$

OFF ISOLATION



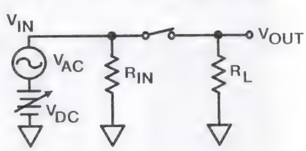
$V_{IN} = 300mV_{p-p}$, $f = 10MHz$, $R_{IN} = R_L = 50\Omega$, $V_{A1} = 2.0V$

CROSSTALK



$V_{IN} = 300mV_{p-p}$, $f = 10MHz$, $R_{IN} = R_L = 50\Omega$, $V_{A1} = 2.0V$, $V_{A2} = 0.8V$

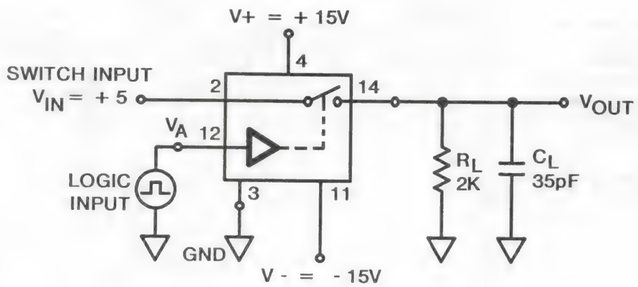
DIFFERENTIAL GAIN, PHASE



$V_{AC} = 300mV_{p-p}$, $f = 3.58MHz$ and $4.43MHz$, $V_{DC} = 0.0V$ to $1.0V$, $R_L = 2k\Omega$, $R_{IN} = 50\Omega$

Test Circuit

SWITCHING TEST CIRCUIT (t_{ON}, t_{OFF1})

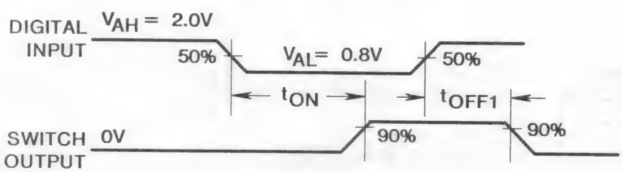


$V_O = V_{IN} \dfrac{R_L}{R_L + R_{ON}}$

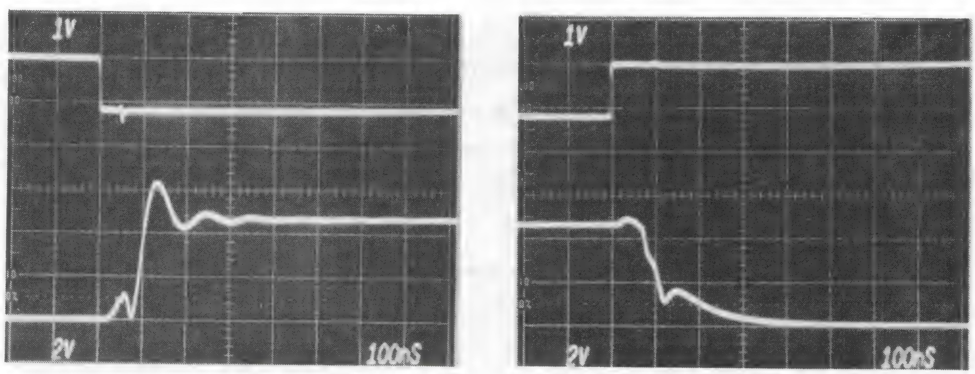
C_L Includes $C_{FIXTURE}$ + C_{PROBE}

Switching Waveforms

LOGIC "0" = SWITCH ON



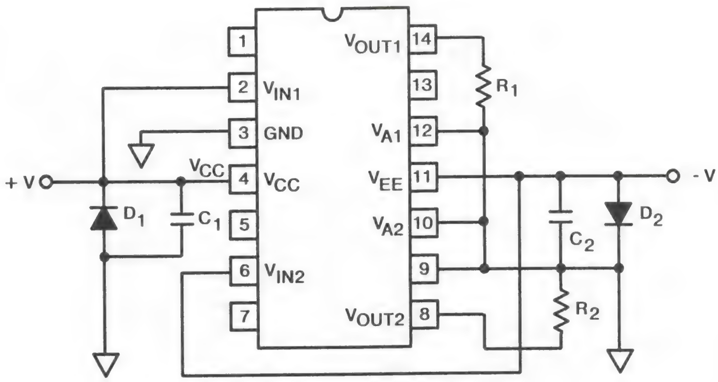
t_{ON}, t_{OFF} (TTL INPUT), V_{AL} = 0.8V, V_{AH} = 2.0V



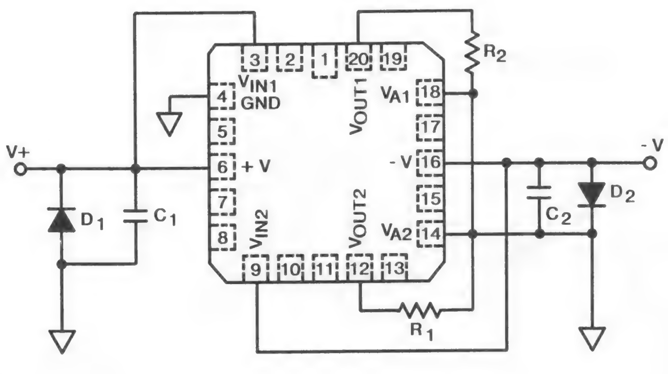
Top: TTL Input (1V/Div.)
Bottom: Output (2V/Div.)
Horizontal: 100ns/Div.

Burn-In Circuits

HI-222/883 CERAMIC DIP



HI-222/883 CERAMIC LCC



NOTES:

Both Switches Are On, One Sourcing 1.5mA and the Other Sinking 1.5mA.

$R_1 = R_2 = 10k\Omega$, ±5%, per Socket, 1/4W (Min)

C_1, C_2 = 0.01μF/Socket (Min) or 0.1μF/Row, (Min)

D_1, D_2 = IN4002 or Equivalent/Board

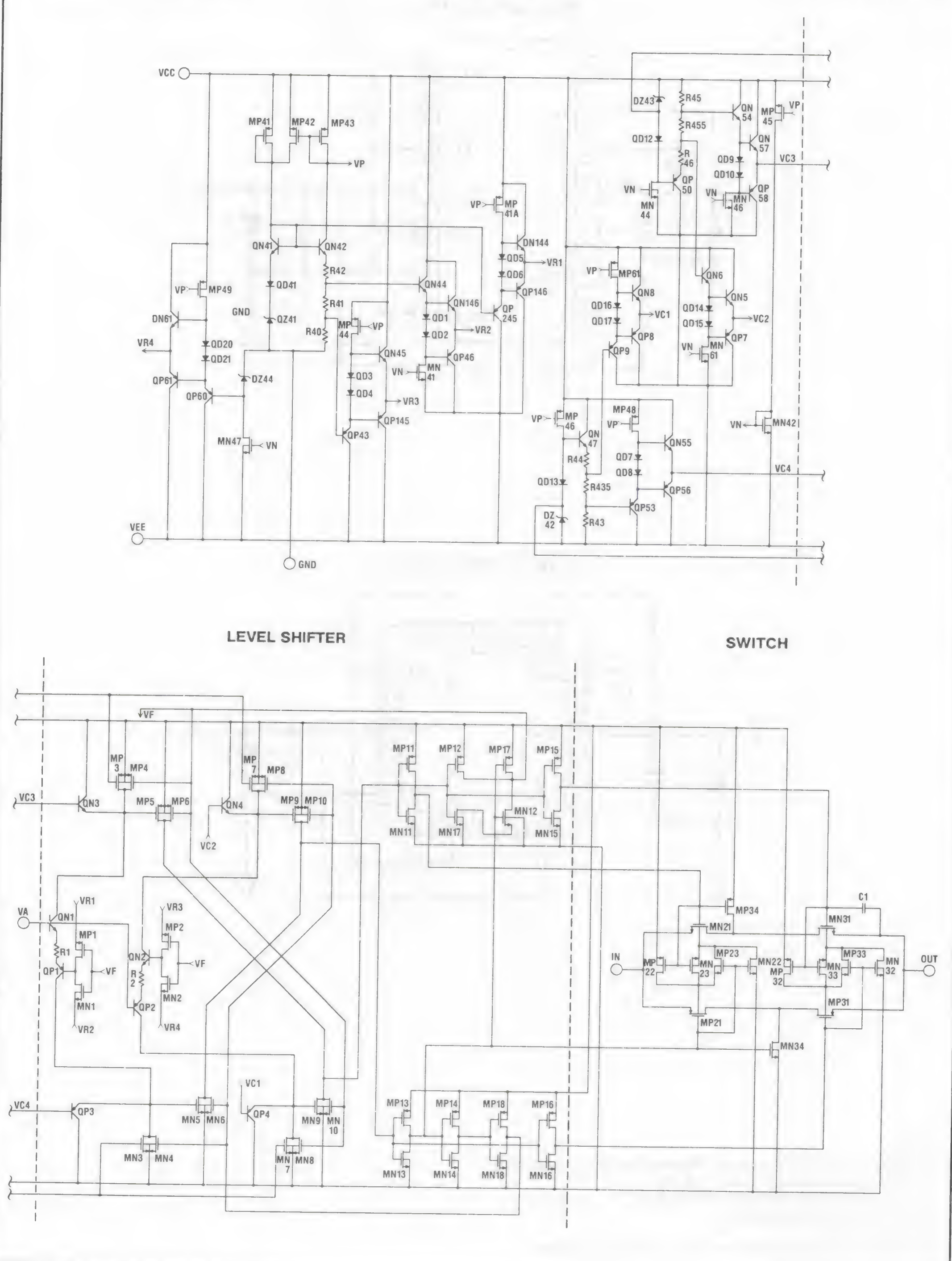
$|(V+) - (V-)| = 30V$

Pin 9 May Be Tied to Ground or Left Open on Ceramic DIP Circuit.

4

CMOS ANALOG SWITCHES

Schematic Diagram



Die Characteristics

DIE DIMENSIONS:
124 x 79 x 19 mils
(3120 x 1440 x 480 μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$0.93 \times 10^5 A/cm^2$ at 15mA (Continuous)

GLASSIVATION:
Type: Nitride
Thickness: 7.0kÅ ± 0.75kÅ

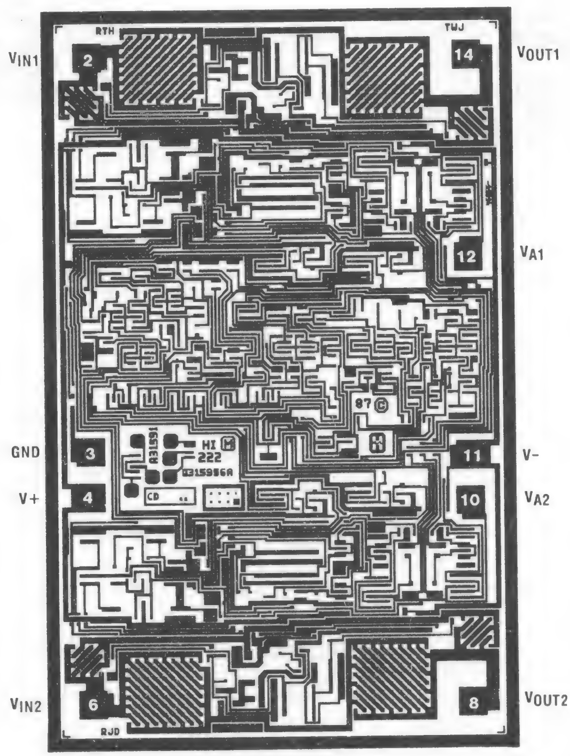
DEVICE COUNT: 183

PROCESS: Silicon Gate/DI

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

Metallization Mask Layout

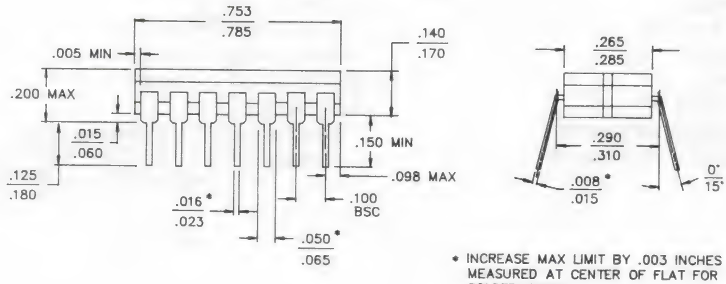
HI-222/883



NOTE: Pin Numbers Correspond to Ceramic DIP Package Only.

Packaging†

14 PIN CERAMIC DIP

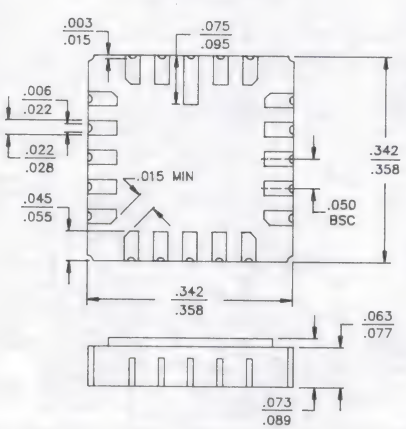


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-1

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

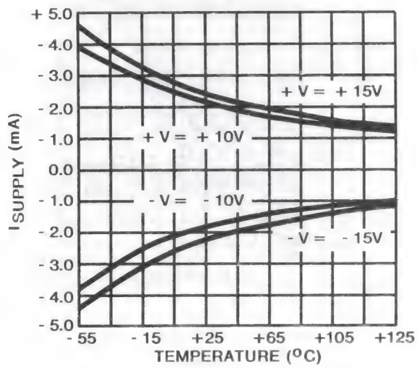
DESIGN INFORMATION

High Frequency/Video Switch

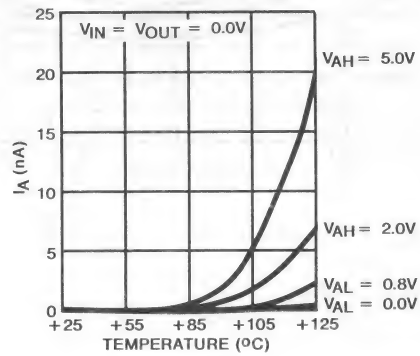
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

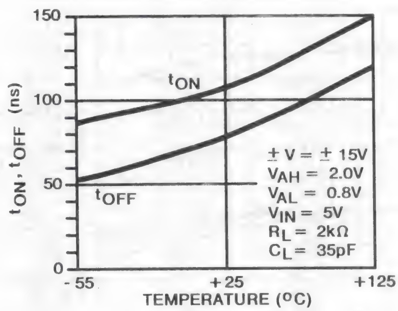
SUPPLY CURRENT vs. TEMPERATURE vs. SUPPLY VOLTAGE



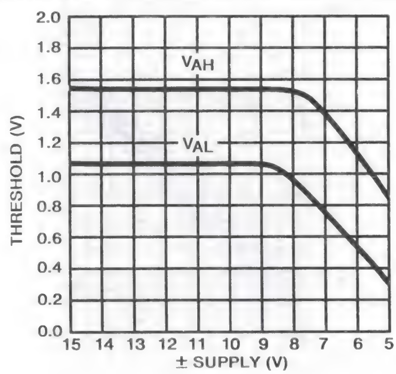
STEADY STATE ADDRESS INPUT CURRENT vs. TEMPERATURE



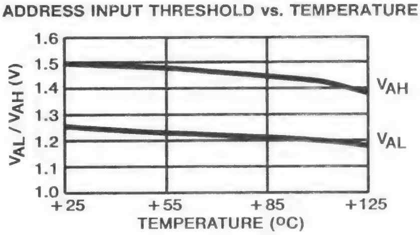
SWITCHING TIME vs. TEMPERATURE



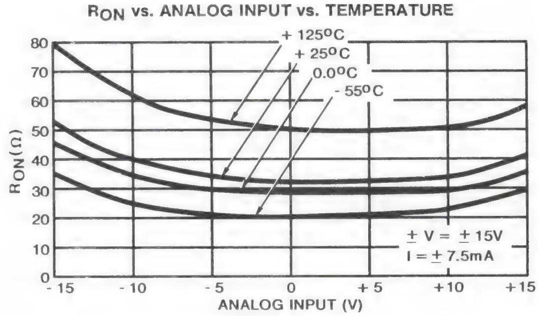
SWITCHING THRESHOLD vs. ± SUPPLY VOLTAGE



ADDRESS INPUT THRESHOLD vs. TEMPERATURE



R_{ON} vs. ANALOG INPUT vs. TEMPERATURE

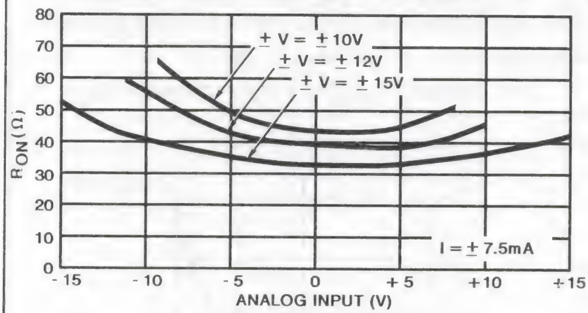


DESIGN INFORMATION (Continued)

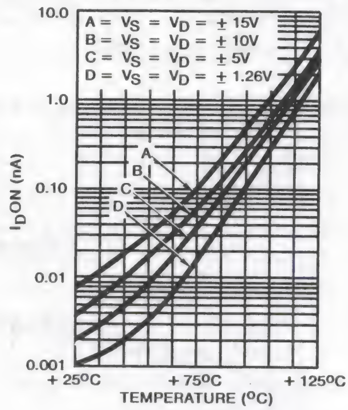
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

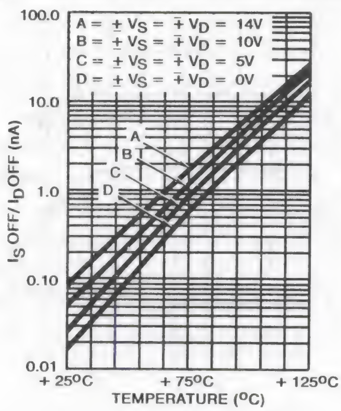
R_{ON} vs. ANALOG INPUT vs. SUPPLY VOLTAGE



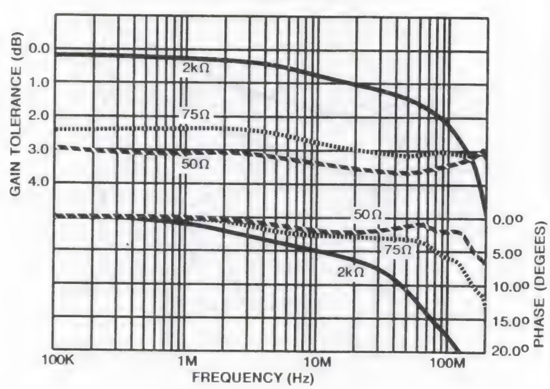
I_{SOFF}/I_{DOFF} vs. TEMPERATURE vs. ANALOG INPUT



I_DON vs. TEMPERATURE vs. ANALOG INPUT



BANDWIDTH

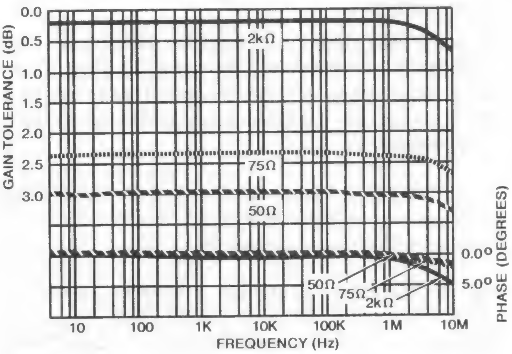


DESIGN INFORMATION (Continued)

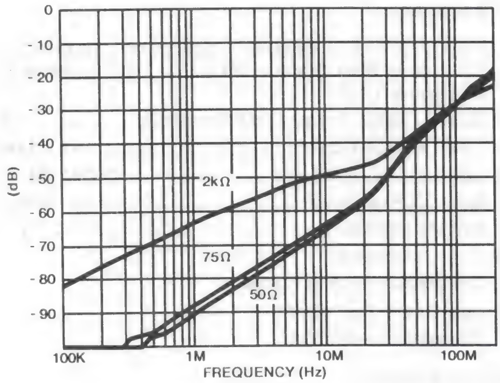
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unles Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

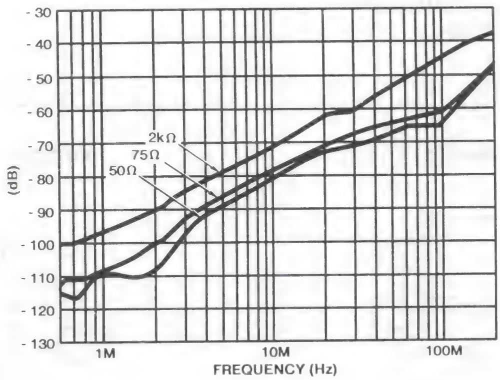
GAIN TOLERANCE



OFF ISOLATION



CROSSTALK



TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, $R_L = 50\Omega$, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	UNITS
Differential Gain	$V_S = 300mV_{p-p}$, $V_{Offset} = 0.0V$ to 1.0V f = 3.58MHz, 4.43MHz @ $R_L = 2k\Omega$	+25°C	0.03	%
	$V_S = 300mV_{p-p}$, $V_{Offset} = 0.0V$ to 1.0V f = 3.58MHz, 4.43MHz @ $R_L = 50\Omega$	+25°C	0.3	%
Differential Phase	$V_S = 300mV_{p-p}$, $V_{Offset} = 0.0V$ to 1.0V f = 3.58MHz, 4.43MHz @ $R_L = 2k\Omega$	+25°C	0.003	Degrees
	$V_S = 300mV_{p-p}$, $V_{Offset} = 0.0V$ to 1.0V f = 3.58MHz, 4.43MHz @ $R_L = 50\Omega$	+25°C	0.2	Degrees

4
CMOS ANALOG SWITCHES

HARRIS

HI-300/883

January 1989

Dual SPST CMOS Analog Switch

Features

- **This Circuit Is Processed in Accordance to Mil-Std-883 and Is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Analog Signal Range (±15V Supplies) .... ±15V**
- **Low Leakage (+25°C) .... 1nA (Max)**
- **Low Leakage (+125°C) .... 100nA (Max)**
- **Low ON Resistance .... 50Ω (Max)**
- **Charge Injection .... 30pC (Typ)**
- **TTL Compatible**
- **Symmetrical Switch Elements**
- **Low Operating Power**
- **Compatible with DG300**

Applications

- **Sample and Hold, i.e. Low Leakage Switching**
- **Op Amp Gain Switching, i.e. Low ON Resistance**
- **Portable, Battery Operated Circuits**
- **Low Level Switching Circuits**
- **Dual or Single Supply Systems**

Description

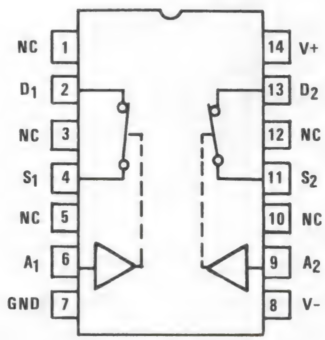
The HI-300/883 switch is a monolithic device fabricated using CMOS technology and the Harris Dielectric Isolation process. This switch features low and nearly constant ON resistance over the full analog signal range, and low power dissipation.

The HI-300/883 is TTL compatible and has a logic "0" condition with an input less than 0.8V and a logic "1" condition with an input greater than 4.0V.

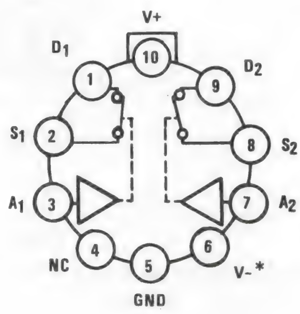
The HI-300/883 is pin-for-pin compatible with the industry standard Siliconix DG300. The device is available in a 14 pin Ceramic DIP and in a 10 pin Metal Can. The HI-300/883 operates over the -55°C to +125°C temperature range.

Pinouts

HI1-300/883 (CERAMIC DIP)
TOP VIEW



HI2-300/883 (METAL CAN)
TOP VIEW



LOGIC	SWITCH
0	OFF
1	ON

*The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 44V
$\pm V_{SUPPLY}$ to Ground (V+, V-) .... ±22V
Analog Input Voltage $+V_S$ .... $+V_{SUPPLY}$ +1.5V
$-V_S$ .... $-V_{SUPPLY}$ -1.5V
Digital Input Voltage $+V_A$ .... $+V_{SUPPLY}$ +4V
$-V_A$ .... $-V_{SUPPLY}$ -4V
Peak Current (S or D)
(Pulse at 1ms, 10% Duty Cycle Max) 40mA
Continuous Current 30mA
Junction Temperature .... +175°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering 10 sec) .... ≤275°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	98°C/W	30°C/W
Metal Can Package	117°C/W	35°C/W

Package Power Dissipation at +75°C
Ceramic DIP Package 0.77W
Metal Can Package 0.64W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 10.32mW/°C
Metal Can Package .... 8.56mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) .... ±15V
Analog Input Voltage (V_S) .... $\pm V_{SUPPLY}$
Logic Low Level (V_{AL}) .... 0V to 0.8V
Logic High Level (V_{AH}) .... 4.0V to $+V_{SUPPLY}$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, GND = 0V, Unless Otherwise Specified

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch "ON" Resistance	R_{DS}	V_A = 4.0V, V_D = 10V, I_S = -10mA S1/S2	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
		V_A = 4.0V, V_D = -10V, I_S = 10mA S1/S2	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = +14V, V_D = -14V, V_A = 0.8V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = -14V, V_D = +14V, V_A = 0.8V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_S = +14V, V_D = -14V, V_A = 0.8V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = -14V, V_D = +14V, V_A = 0.8V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = +14V, V_A = 4.0V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_D = V_S = -14V, V_A = 4.0V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Low Level Input Current	I_{AL}	All Channels V_A = 0.8V	1	+25°C	-1.0	1.0	μA
			2, 3	-55°C to +125°C	-1.0	1.0	μA
High Level Input Current	I_{AH}	All Channels V_A = 4.0V	1	+25°C	-1.0	1.0	μA
			2, 3	-55°C to +125°C	-1.0	1.0	μA
Supply Current	$+I_{CC}$	All Channels V_A = 0.8V	1	+25°C	-	10	μA
			2, 3	-55°C to +125°C	-	100	μA
		V_{A1} = 4.0V, V_{A2} = 0V and V_{A1} = 0V, V_{A2} = 4.0V	1	+25°C	-	0.5	mA
			2, 3	-55°C to +125°C	-	1.0	mA
Supply Current	$-I_{CC}$	All Channels V_A = 0.8V	1	+25°C	-10	-	μA
			2, 3	-55°C to +125°C	-100	-	μA
		V_{A1} = 4.0V, V_{A2} = 0V and V_{A1} = 0V, V_{A2} = 4.0V	1	+25°C	-10	-	μA
			2, 3	-55°C to +125°C	-100	-	μA

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Turn "ON" Time	$t_{(ON)}$	$C_L = 33pF$ $R_L = 300\Omega$	9	+25°C	-	300	ns
			10, 11	-55°C, +125°C	-	500	ns
Turn "OFF" Time	$t_{(OFF)}$	$C_L = 33pF$ $R_L = 300\Omega$	9	+25°C	-	250	ns
			10, 11	-55°C, +125°C	-	450	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Characterized at: $+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Switch Input Capacitance	$C_{IS(OFF)}$	Measured Source to GND	1	+25°C	-	28	pF
Driver Input Capacitance	C_{C1}	$V_A = 0V$	1	+25°C	-	10	pF
	C_{C2}	$V_A = 15V$	1	+25°C	-	10	pF
Switch Output Capacitance	C_{OS}	Measured Drain to GND	1	+25°C	-	28	pF
Off Isolation	V_{ISO}	$f = 1MHz$, $V_{GEN} = 1V_{p-p}$	1	+25°C	40	-	dB
Crosstalk	V_{CT}	$f = 1MHz$, $V_{GEN} = 1V_{p-p}$	1	+25°C	40	-	dB
Charge Transfer	V_{CTE}	$V_S = GND$, $C_L = 0.01\mu F$	1	+25°C	-	15	mV

NOTE 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

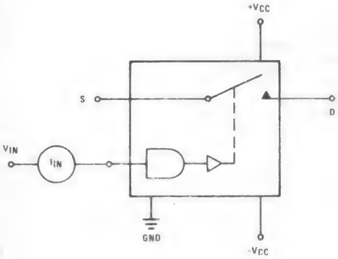
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

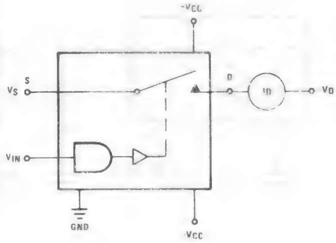
* PDA applies to Subgroup 1 only.

Test Circuits

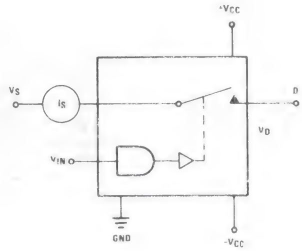
INPUT LEAKAGE CURRENT



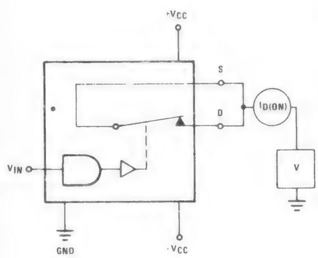
$I_{D(OFF)}$



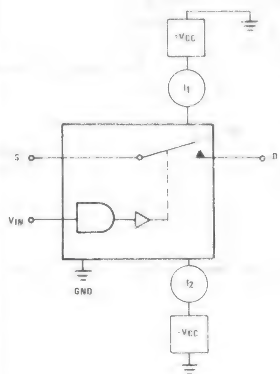
$I_{S(OFF)}$



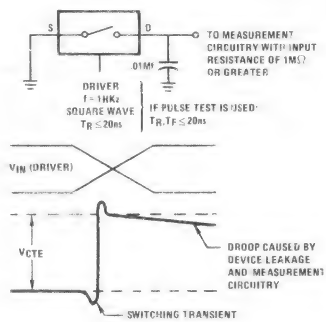
$I_{D(ON)}$



SUPPLY CURRENTS

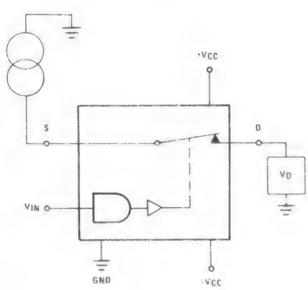


CHARGE TRANSFER ERROR

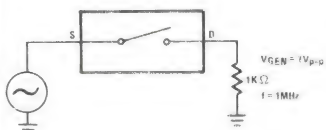


NOTE: V_{CTE} may be a positive or negative value

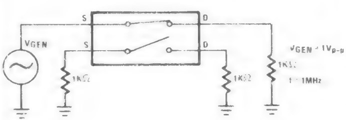
R_{DS}



OFF CHANNEL ISOLATION



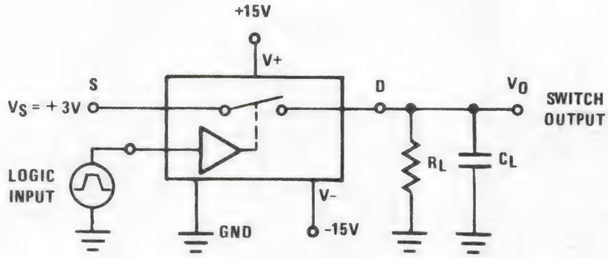
CROSSTALK BETWEEN CHANNELS

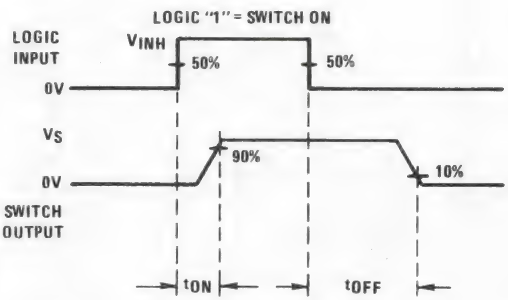


For Detail Information Refer to HI-300/883 Test Tech Brief

4 CMOS ANALOG SWITCHES

Test Waveforms

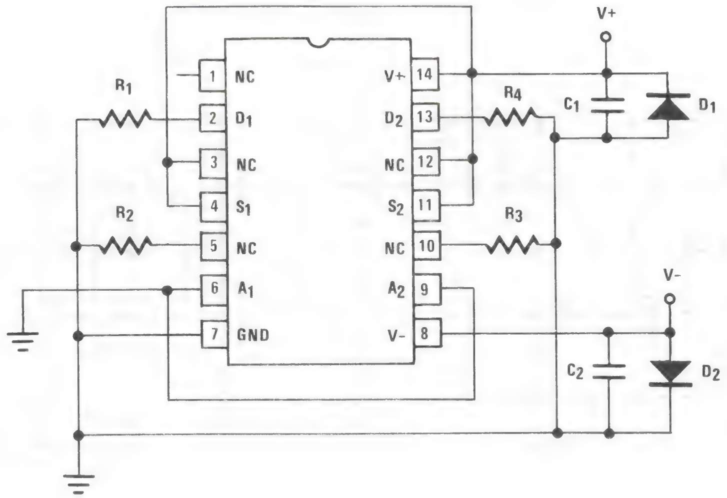




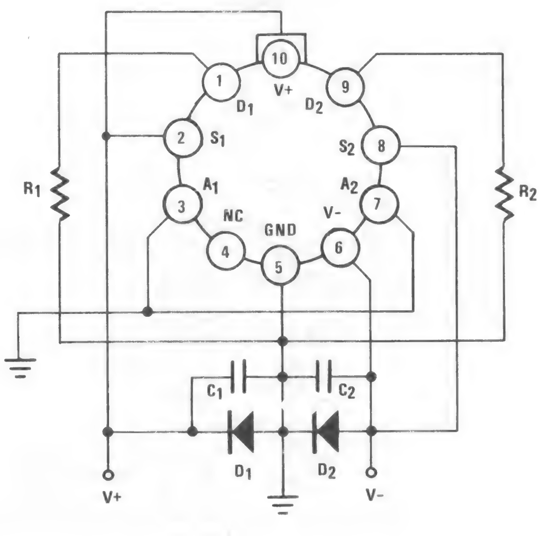
NOTES:
1. $R_L = 300\Omega$; $C_L = 33pF$
2. $V_{INH} = 4V$
   RISETIME (0.4V to 3.6V) $\leq$ 20ns
   FALLTIME (3.6V to 0.4V) $\leq$ 20ns

Burn-In Circuits

HI-300/883 CERAMIC DIP



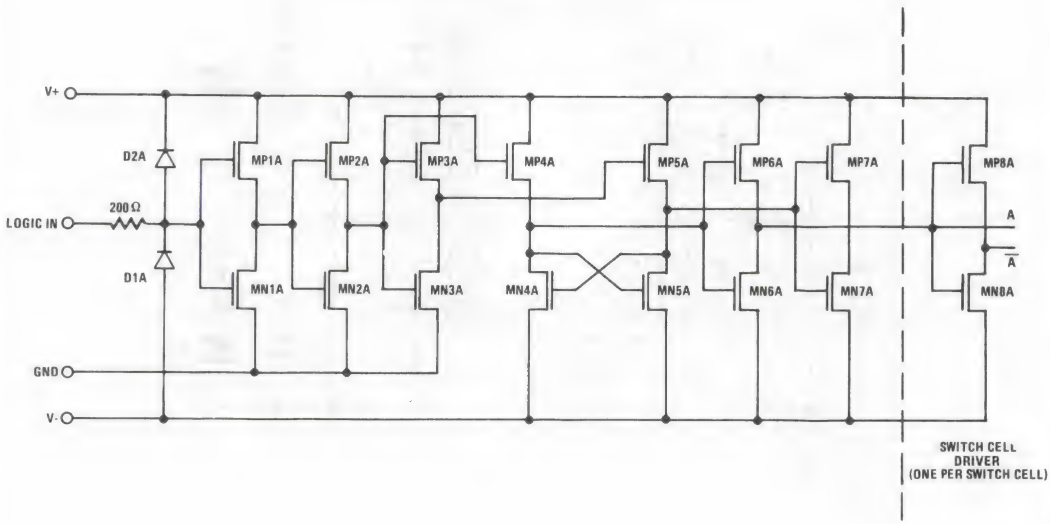
HI-300/883 METAL CAN



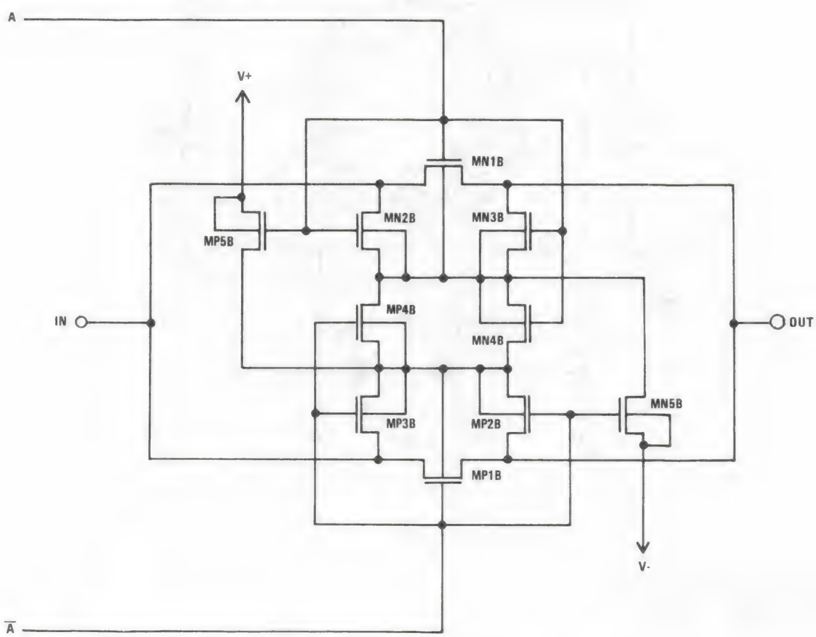
NOTES:
$R_1 = R_2 = R_3 = R_4 = 10K\Omega$, 5%, 1/4 or 1/2 watt.
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2$ = IN4002 (per board)
$|(V+) - (V-)| = 30V$

Schematic Diagram

DIGITAL INPUT BUFFER AND LEVEL SHIFTER



SWITCH CELL



Die Characteristics

DIE DIMENSIONS:
76 x 60.6 x 19 mils

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

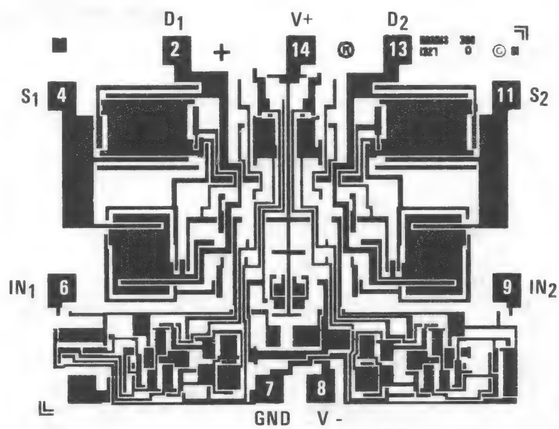
GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Metal Can — 420°C (Max)

WORST CASE CURRENT DENSITY:
$3.9 \times 10^5 A/cm^2$ at 30mA
This device meets Glassivation Integrity Test requirement per Mil-Std-883 Method 2021 and Mil-M-38510 paragraph 3.5.5.4.

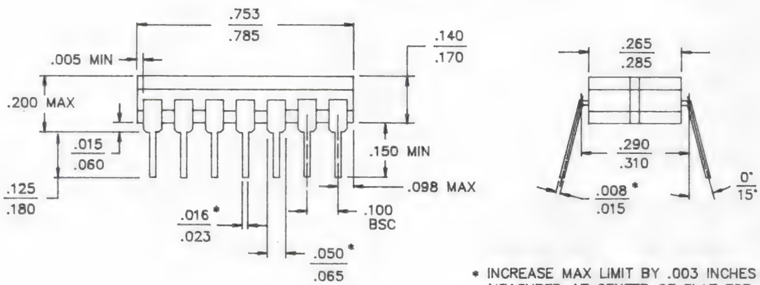
Metallization Mask Layout

HI-300/883



Packaging†

14 PIN CERAMIC DIP

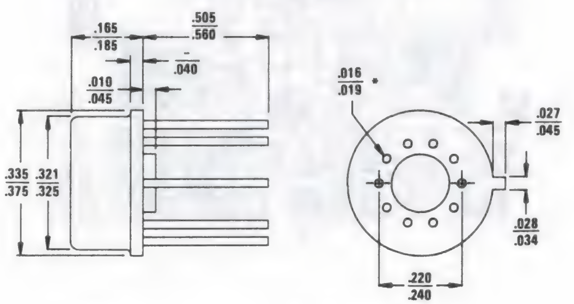


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-1

10 PIN METAL CAN



* Maximum Limits are Increased by 0.003 inches for Solder Dip Finish.

LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
Material: No Seal Material
Temperature: Room Temperature
Method: Resistance Weld

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 A-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

HI-300

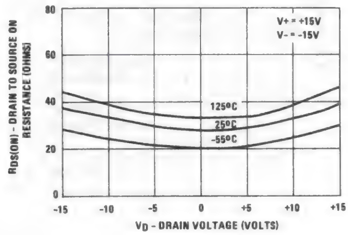
DESIGN INFORMATION

Dual SPST CMOS Analog Switch

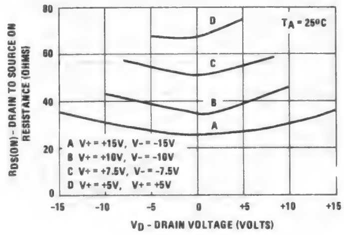
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics Unless Otherwise Specified: V+ = +15V, V- = -15V, T_A = +25°C

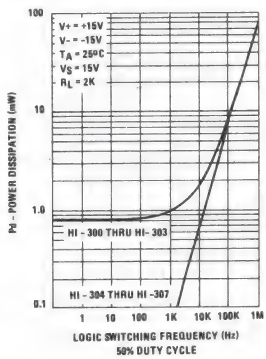
$R_{DS(ON)}$ vs. V_D AND TEMPERATURE



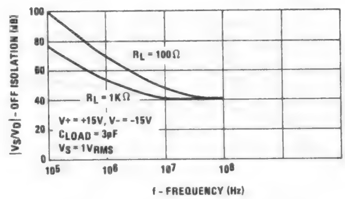
$R_{DS(ON)}$ vs. V_D AND POWER SUPPLY VOLTAGE



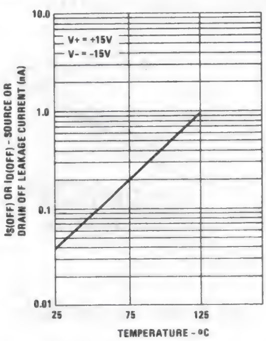
DEVICE POWER DISSIPATION vs. SWITCHING FREQUENCY SIGNAL LOGIC INPUT



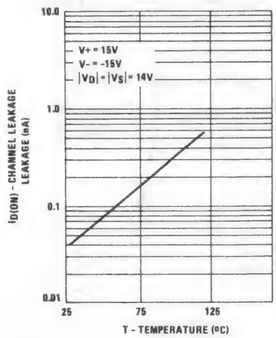
OFF ISOLATION vs. FREQUENCY



$I_{S(OFF)}$ or $I_{D(OFF)}$ vs. TEMPERATURE*



$I_{D(ON)}$ vs. TEMPERATURE*



* The net leakage into the source or drain is the N-channel leakage minus the P-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

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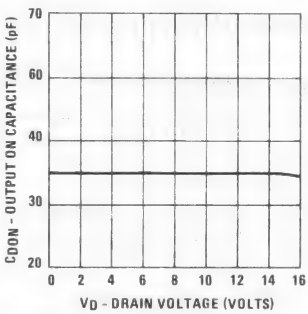
CMOS ANALOG SWITCHES

DESIGN INFORMATION (Continued)

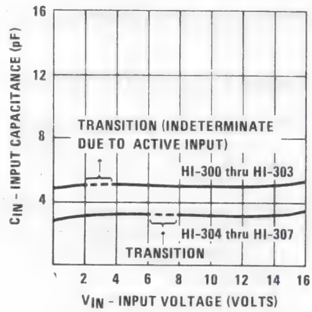
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics Unless Otherwise Specified: V+ = +15V, V- = -15V, T_A = +25°C

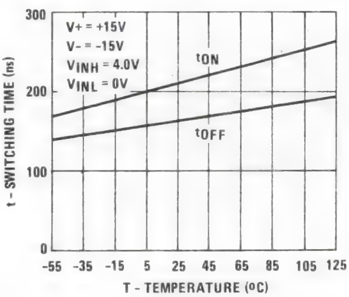
OUTPUT ON CAPACITANCE vs. DRAIN VOLTAGE



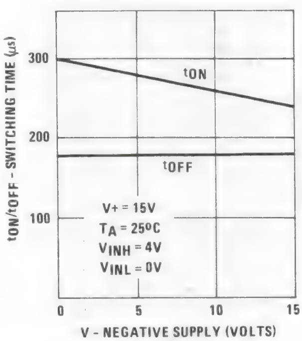
DIGITAL INPUT CAPACITANCE vs. INPUT VOLTAGE



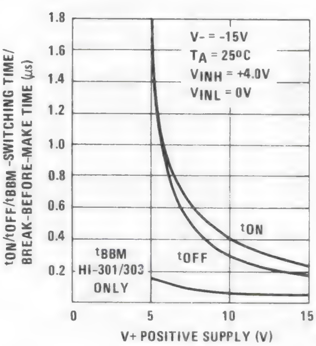
SWITCHING TIME vs. TEMPERATURE



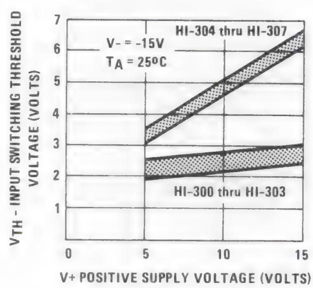
SWITCHING TIME vs. NEGATIVE SUPPLY VOLTAGE



SWITCHING TIME AND BREAK BEFORE MAKE TIME vs. POSITIVE SUPPLY VOLTAGE



INPUT SWITCHING TIME THRESHOLD vs. POSITIVE SUPPLY VOLTAGE



HARRIS HI-301/883

January 1989

SPDT CMOS Analog Switch

Features

- **This Circuit Is Processed in Accordance to Mil-Std-883 and Is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Analog Signal Range (±15V Supplies) .... ±15V**
- **Low Leakage (+25°C)................................... 1nA (Max)**
- **Low Leakage (+125°C)............................... 100nA (Max)**
- **Low ON Resistance.. 50Ω (Max)**
- **Charge Injection .... 30pC (Typ)**
- **TTL Compatible**
- **Symmetrical Switch Elements**
- **Low Operating Power**
- **Compatible with DG301**

Applications

- **Sample and Hold, i.e. Low Leakage Switching**
- **Op Amp Gain Switching, i.e. Low ON Resistance**
- **Portable, Battery Operated Circuits**
- **Low Level Switching Circuits**
- **Dual or Single Supply Systems**

Description

The HI-301/883 switch is monolithic devices fabricated using CMOS technology and the Harris Dielectric Isolation process. This switch features break-before-make switching, low and nearly constant ON resistance over the full analog signal range, and low power dissipation.

The HI-301/883 is TTL compatible and has a logic "0" condition with an input less than 0.8V and a logic "1" condition with an input greater than 4.0V.

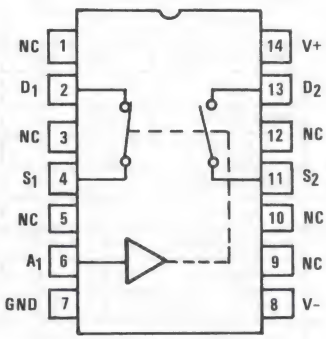
The HI-301/883 is pin-for-pin compatible with the industry standard Siliconix DG301. The device is available in a 14 pin Ceramic DIP and in a 10 pin Metal Can. The HI-301/883 operates over the -55°C to +125°C temperature range.

4

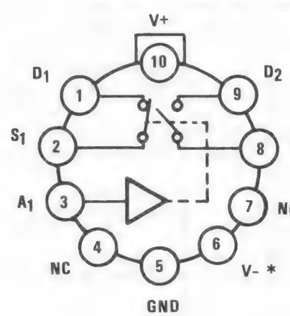
CMOS ANALOG SWITCHES

Pinouts

HI1-301/883 (CERAMIC DIP)
TOP VIEW



HI2-301/883 (METAL CAN)
TOP VIEW



LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

*The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 44V
$\pm V_{SUPPLY}$ to Ground (V+, V-) .... ±22V
Analog Input Voltage $+V_S$ .... $+V_{SUPPLY}$ +1.5V
$-V_S$ .... $-V_{SUPPLY}$ -1.5V
Digital Input Voltage $+V_A$ .... $+V_{SUPPLY}$ +4V
$-V_A$ .... $-V_{SUPPLY}$ -4V
Peak Current (S or D)
(Pulse at 1ms, 10% Duty Cycle Max) 40mA
Continuous Current 30mA
Junction Temperature .... +175°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering 10 sec) .... ≤275°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	98°C/W	30°C/W
Metal Can Package	117°C/W	35°C/W

Package Power Dissipation at +75°C
Ceramic DIP Package 0.77W
Metal Can Package 0.64W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 10.32mW/°C
Metal Can Package .... 8.56mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) .... ±15V
Analog Input Voltage (V_S) .... $\pm V_{SUPPLY}$
Logic Low Level (V_{AL}) .... 0V to 0.8V
Logic High Level (V_{AH}) .... 4.0V to $+V_{SUPPLY}$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, GND = 0V, Unless Otherwise Specified

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch "ON" Resistance	R_{DS}	V_A = 4.0V, V_D = 10V, I_S = -10mA S1/S2	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
		V_A = 4.0V, V_D = -10V, I_S = 10mA S1/S2	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = +14V, V_D = -14V, V_A = 0.8V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = -14V, V_D = +14V, V_A = 0.8V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_S = +14V, V_D = -14V, V_A = 0.8V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = -14V, V_D = +14V, V_A = 0.8V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = +14V, V_A = 4.0V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_D = V_S = -14V, V_A = 4.0V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Low Level Input Current	I_{AL}	All Channels V_A = 0.8V	1	+25°C	-1.0	1.0	μA
			2, 3	-55°C to +125°C	-1.0	1.0	μA
High Level Input Current	I_{AH}	All Channels V_A = 4.0V	1	+25°C	-1.0	1.0	μA
			2, 3	-55°C to +125°C	-1.0	1.0	μA
Supply Current	$+I_{CC}$	All Channels V_A = 0.8V	1	+25°C	-	10	μA
			2, 3	-55°C to +125°C	-	100	μA
		V_A = 4.0V	1	+25°C	-	0.5	mA
			2, 3	-55°C to +125°C	-	1.0	mA
Supply Current	$-I_{CC}$	All Channels V_A = 0.8V	1	+25°C	-10	-	μA
			2, 3	-55°C to +125°C	-100	-	μA
		V_A = 4.0V	1	+25°C	-10	-	μA
			2, 3	-55°C to +125°C	-100	-	μA

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Turn "ON" Time	$t_{(ON)}$	$C_L = 33pF$ $R_L = 300\Omega$	9	$+25^oC$	-	300	ns
			10, 11	$-55^oC, +125^oC$	-	500	ns
Turn "OFF" Time	$t_{(OFF)}$	$C_L = 33pF$ $R_L = 300\Omega$	9	$+25^oC$	-	250	ns
			10, 11	$-55^oC, +125^oC$	-	450	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Characterized at: $+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Switch Input Capacitance	$C_{IS(OFF)}$	Measured Source to GND	1	$+25^oC$	-	28	pF
Driver Input Capacitance	C_{C1}	$V_A = 0V$	1	$+25^oC$	-	10	pF
	C_{C2}	$V_A = 15V$	1	$+25^oC$	-	10	pF
Switch Output Capacitance	C_{OS}	Measured Drain to GND	1	$+25^oC$	-	28	pF
Off Isolation	V_{ISO}	$f = 1MHz, V_{GEN} = 1V_{p-p}$	1	$+25^oC$	40	-	dB
Crosstalk	V_{CT}	$f = 1MHz, V_{GEN} = 1V_{p-p}$	1	$+25^oC$	40	-	dB
Charge Transfer	V_{CTE}	$V_S = GND, C_L = 0.01\mu F$	1	$+25^oC$	-	15	mV

NOTE 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

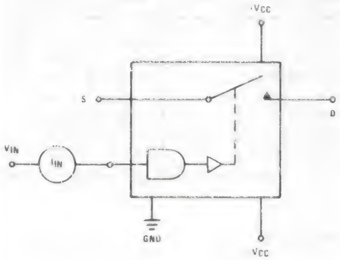
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

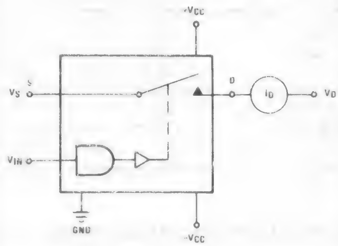
* PDA applies to Subgroup 1 only.

Test Circuits

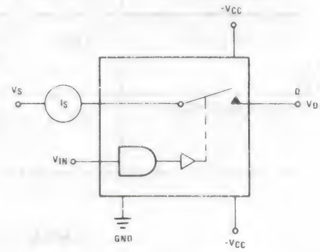
INPUT LEAKAGE CURRENT



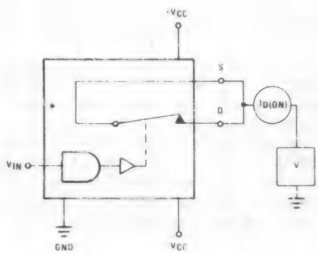
$I_{D(OFF)}$



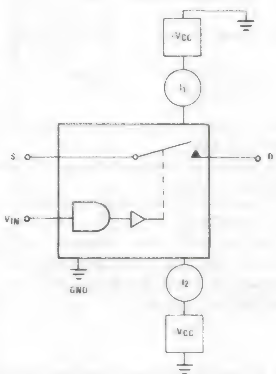
$I_{S(OFF)}$



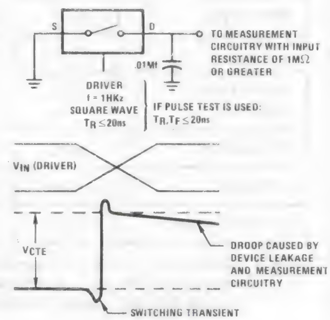
$I_{D(ON)}$



SUPPLY CURRENTS

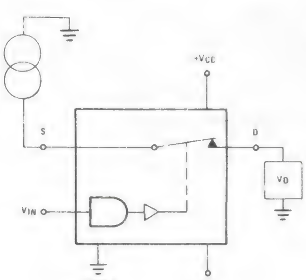


CHARGE TRANSFER ERROR

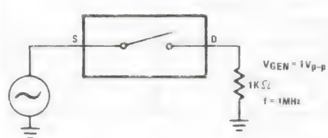


NOTE: V_{CTE} may be a positive or negative value

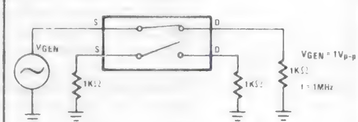
R_{DS}



OFF CHANNEL ISOLATION

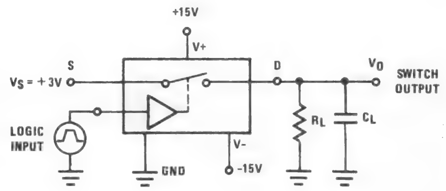


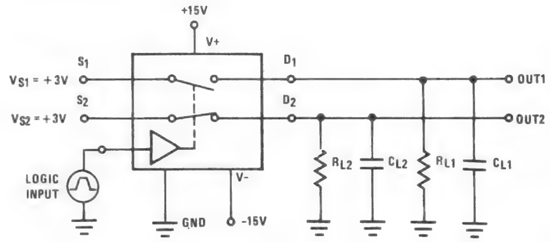
CROSSTALK BETWEEN CHANNELS

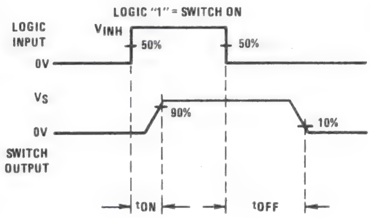


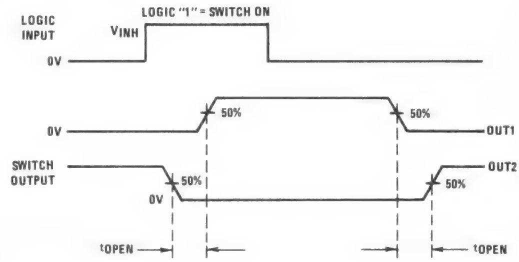
For Detail Information Refer to HI-301/883 Test Tech Brief

Test Waveforms







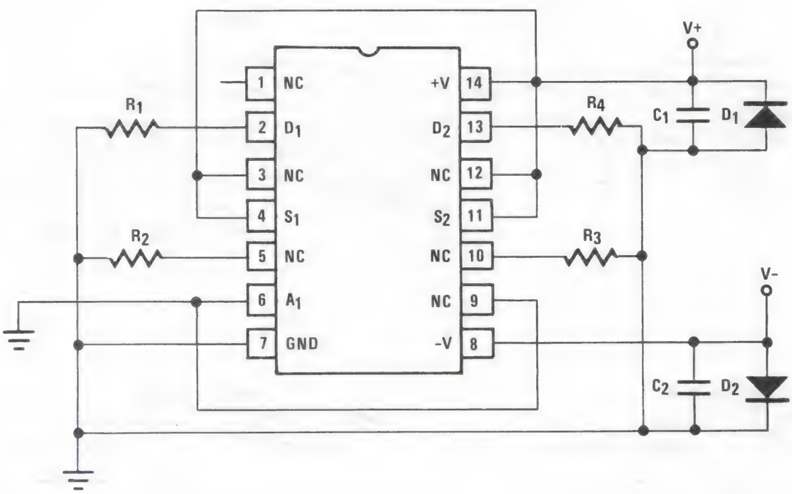


NOTES:

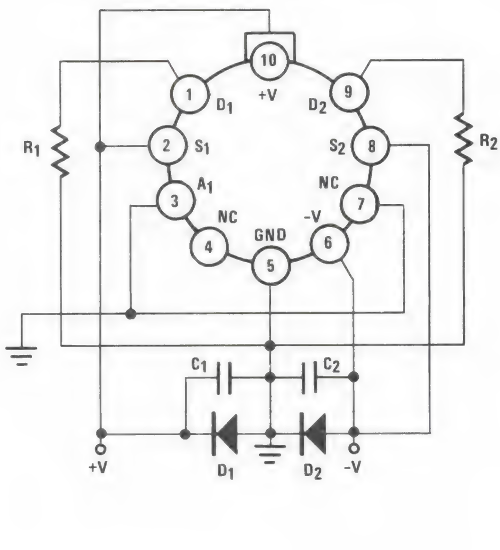
1. $R_L = R_L1 = R_L2 = 300\Omega$; $C_L = C_L1 = C_L2 = 33pF$
2. $V_{INH} = 4V$
   RISETIME (0.4V to 3.6V) $\leq$ 20ns
   FALLTIME (3.6V to 0.4V) $\leq$ 20ns

Burn-In Circuits

HI-301/883 CERAMIC DIP



HI-301/883 METAL CAN



NOTES:

$R_1 = R_2 = R_3 = R_4 = 10K\Omega$, ± 5% (per socket)

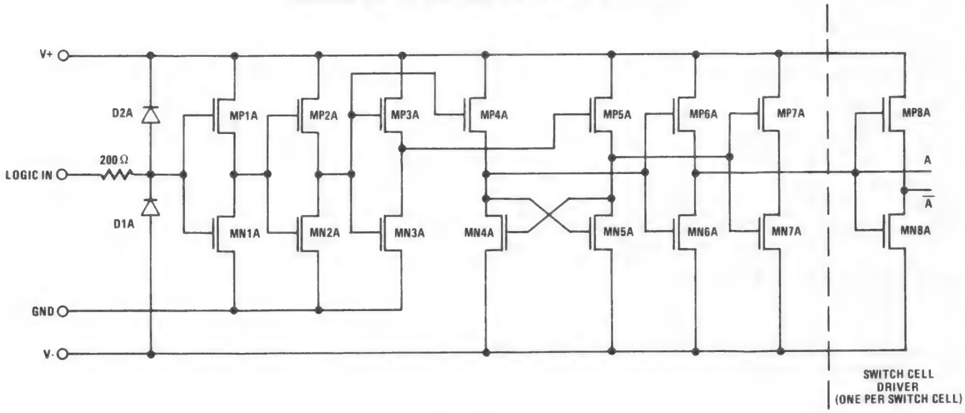
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)

$D_1 = D_2$ = IN4002 or Equivalent/Board

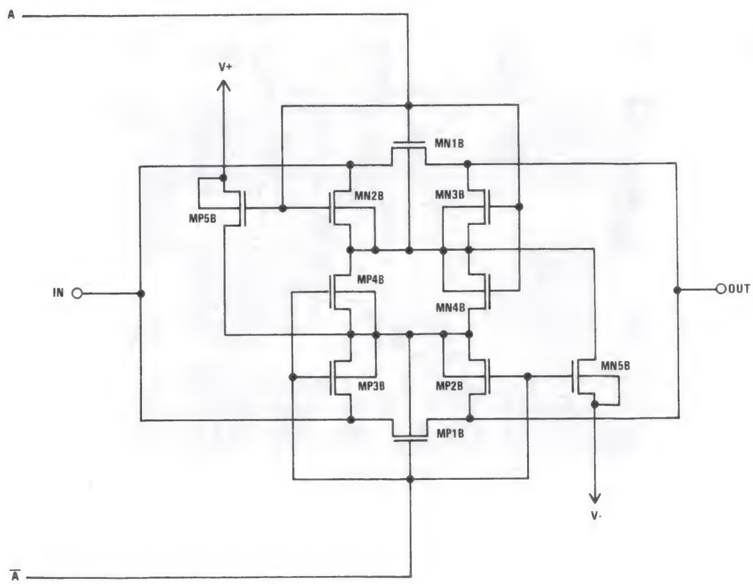
$|(V+) - (V-)| = 30V$

Schematic Diagram

DIGITAL INPUT BUFFER AND LEVEL SHIFTER



SWITCH CELL



Die Characteristics

DIE DIMENSIONS:
76 x 60.6 x 19 mils

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

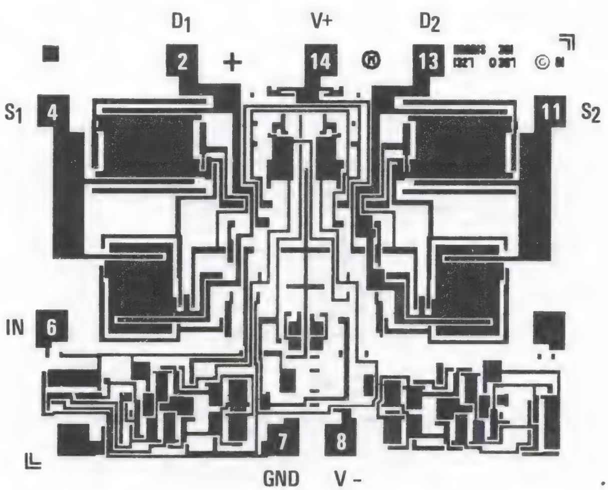
GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Metal Can — 420°C (Max)

WORST CASE CURRENT DENSITY:
$3.9 \times 10^5 A/cm^2$ at 30mA
This device meets Glassivation Integrity Test requirement per Mil-Std-883 Method 2021 and Mil-M-38510 paragraph 3.5.5.4.

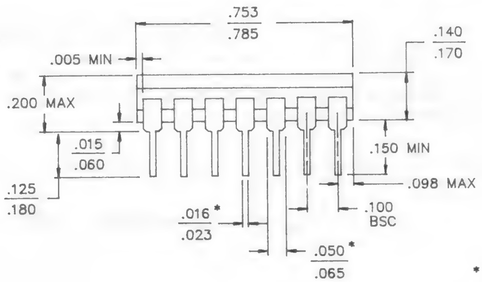
Metallization Mask Layout

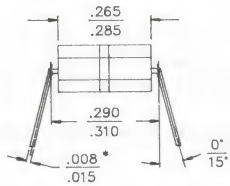
HI-301/883



Packaging†

14 PIN CERAMIC DIP





* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

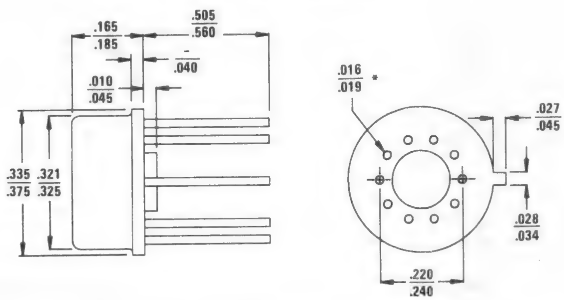
LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-1

4

CMOS ANALOG SWITCHES

10 PIN METAL CAN



* Maximum Limits are Increased by 0.003 inches for Solder Dip Finish.

LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
Material: No Seal Material
Temperature: Room Temperature
Method: Resistance Weld

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 A-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

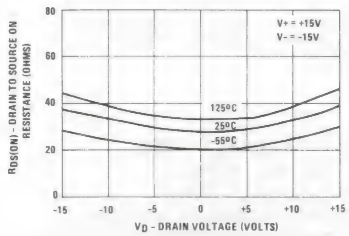
DESIGN INFORMATION

SPDT CMOS Analog Switch

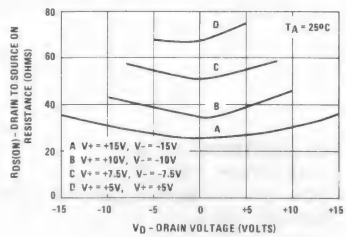
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics Unless Otherwise Specified: V+ = +15V, V- = -15V, T_A = +25°C

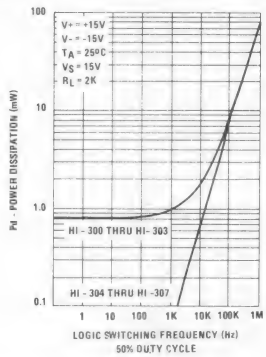
$R_{DS(ON)}$ vs. V_D AND TEMPERATURE



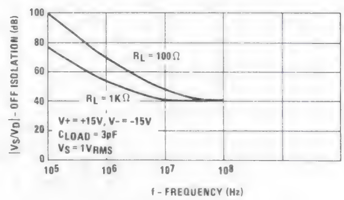
$R_{DS(ON)}$ vs. V_D AND POWER SUPPLY VOLTAGE



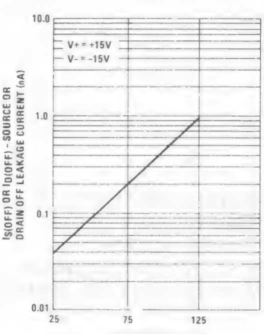
DEVICE POWER DISSIPATION vs. SWITCHING FREQUENCY SIGNAL LOGIC INPUT



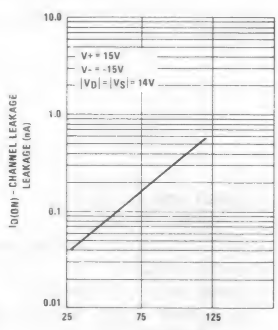
OFF ISOLATION vs. FREQUENCY



$I_{S(OFF)}$ or $I_{D(OFF)}$ vs. TEMPERATURE*



$I_{D(ON)}$ vs. TEMPERATURE*



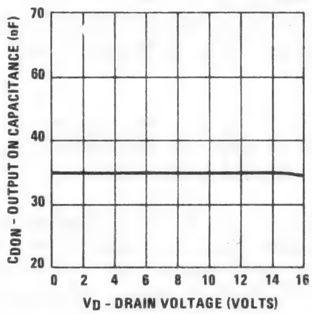
* The net leakage into the source or drain is the N-channel leakage minus the P-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

DESIGN INFORMATION (Continued)

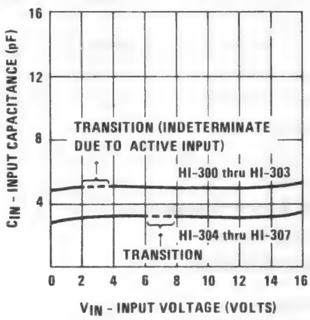
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics Unless Otherwise Specified: V+ = +15V, V- = -15V, T_A = +25°C

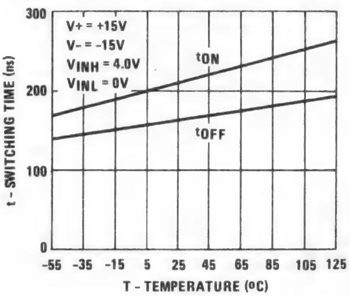
OUTPUT ON CAPACITANCE vs. DRAIN VOLTAGE



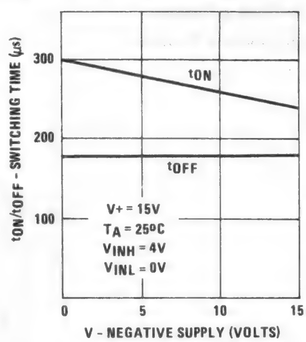
DIGITAL INPUT CAPACITANCE vs. INPUT VOLTAGE



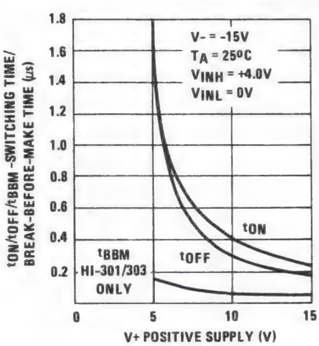
SWITCHING TIME vs. TEMPERATURE



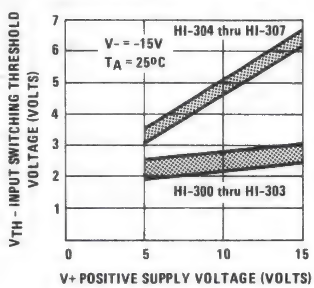
SWITCHING TIME vs. NEGATIVE SUPPLY VOLTAGE



SWITCHING TIME AND BREAK BEFORE MAKE TIME vs. POSITIVE SUPPLY VOLTAGE



INPUT SWITCHING TIME THRESHOLD vs. POSITIVE SUPPLY VOLTAGE



HARRIS

HI-302/883

January 1989

Dual DPST CMOS Analog Switch

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Analog Signal Range (±15V Supplies) .... ±15V
- Low Leakage (+25°C) .... 1nA (Max)
- Low Leakage (+125°C) .... 100nA (Max)
- Low ON Resistance .... 50Ω (Max)
- Charge Injection .... 30pC (Typ)
- TTL Compatible
- Symmetrical Switch Elements
- Low Operating Power
- Compatible with DG302

Applications

- Sample and Hold, i.e. Low Leakage Switching
- Op Amp Gain Switching, i.e. Low ON Resistance
- Portable, Battery Operated Circuits
- Low Level Switching Circuits
- Dual or Single Supply Systems

Description

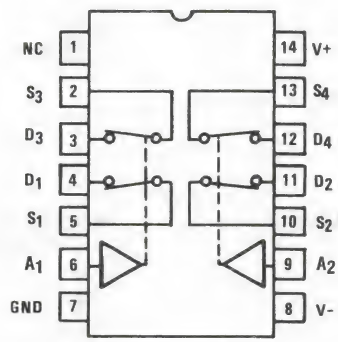
The HI-302/883 switch is a monolithic device fabricated using CMOS technology and the Harris Dielectric Isolation process. This switch features low and nearly constant ON resistance over the full analog signal range, and low power dissipation.

The HI-302/883 is TTL compatible and has a logic "0" condition with an input less than 0.8V and a logic "1" condition with an input greater than 4.0V.

The HI-302/883 is pin-for-pin compatible with the industry standard Siliconix DG302. The device is available in a 14 pin Ceramic DIP. The HI-302/883 operates over the -55°C to +125°C temperature range.

Pinout

HI1-302/883 (CERAMIC DIP)
TOP VIEW



LOGIC	SWITCH
0	OFF
1	ON

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 44V
$\pm V_{SUPPLY}$ to Ground (V+, V-) .... ±22V
Analog Input Voltage $+V_S$ .... $+V_{SUPPLY}$ +1.5V
$-V_S$ .... $-V_{SUPPLY}$ -1.5V
Digital Input Voltage $+V_A$ .... $+V_{SUPPLY}$ +4V
$-V_A$ .... $-V_{SUPPLY}$ -4V
Peak Current (S or D)
(Pulse at 1ms, 10% Duty Cycle Max) 40mA
Continuous Current 30mA
Junction Temperature .... +175°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering 10 sec) .... ≤275°C

Thermal Information

Thermal Resistance — θ_{ja} / θ_{jc}
Ceramic DIP Package .... 88°C/W 24°C/W
Package Power Dissipation at +75°C
Ceramic DIP Package 0.85W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 11.36mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) .... ±15V
Analog Input Voltage (V_S) .... $\pm V_{SUPPLY}$
Logic Low Level (V_{AL}) .... 0V to 0.8V
Logic High Level (V_{AH}) .... 4.0V to $+V_{SUPPLY}$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, GND = 0V, Unless Otherwise Specified

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch "ON" Resistance	R_{DS}	V_A = 4.0V, V_D = 10V, I_S = -10mA S1/S2/S3/S4	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
		V_A = 4.0V, V_D = -10V, I_S = 10mA S1/S2/S3/S4	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = +14V, V_D = -14V, V_A = 0.8V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = -14V, V_D = +14V, V_A = 0.8V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_S = +14V, V_D = -14V, V_A = 0.8V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = -14V, V_D = +14V, V_A = 0.8V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = +14V, V_A = 4.0V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_D = V_S = ±14V, V_A = 4.0V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Low Level Input Current	I_{AL}	All Channels V_A = 0.8V	1	+25°C	-1.0	1.0	µA
			2, 3	-55°C to +125°C	-1.0	1.0	µA
High Level Input Current	I_{AH}	All Channels V_A = 4.0V	1	+25°C	-1.0	1.0	µA
			2, 3	-55°C to +125°C	-1.0	1.0	µA
Supply Current	$+I_{CC}$	All Channels V_A = 0.8V	1	+25°C	-	10	µA
			2, 3	-55°C to +125°C	-	100	µA
		V_{A1} = 0V, V_{A2} = 4.0V and V_{A1} = 4.0V, V_{A2} = 0V	1	+25°C	-	0.5	mA
			2, 3	-55°C to +125°C	-	1.0	mA
Supply Current	$-I_{CC}$	All Channels V_A = 0.8V	1	+25°C	-10	-	µA
			2, 3	-55°C to +125°C	-100	-	µA
		V_{A1} = 0V, V_{A2} = 4.0V and V_{A1} = 4.0V, V_{A2} = 0V	1	+25°C	-10	-	µA
			2, 3	-55°C to +125°C	-100	-	µA

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = −15V, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	MAX	UNITS
Turn "ON" Time	$t_{(ON)}$	C_L = 33pF, R_L = 300Ω	9	+25°C	-	300	ns
			10, 11	-55°C, +125°C	-	500	ns
Turn "OFF" Time	$t_{(OFF)}$	C_L = 33pF, R_L = 300Ω	9	+25°C	-	250	ns
			10, 11	-55°C, +125°C	-	450	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Characterized at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = −15V, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	MAX	UNITS
Switch Input Capacitance	$C_{IS(OFF)}$	Measured Source to GND	1	+25°C	-	28	pF
Driver Input Capacitance	C_{C1}	V_A = 0V	1	+25°C	-	10	pF
	C_{C2}	V_A = 15V	1	+25°C	-	10	pF
Switch Output Capacitance	C_{OS}	Measured Drain to GND	1	+25°C	-	28	pF
Off Isolation	V_{ISO}	f = 1MHz, V_{GEN} = $1V_{p-p}$	1	+25°C	40	-	dB
Crosstalk	V_{CT}	f = 1MHz, V_{GEN} = $1V_{p-p}$	1	+25°C	40	-	dB
Charge Transfer	V_{CTE}	V_S = GND, C_L = 0.01µF	1	+25°C	-	15	mV

NOTE 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

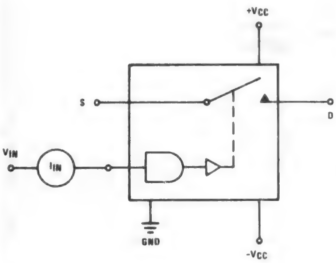
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

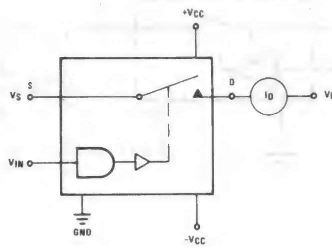
* PDA applies to Subgroup 1 only.

Test Circuits

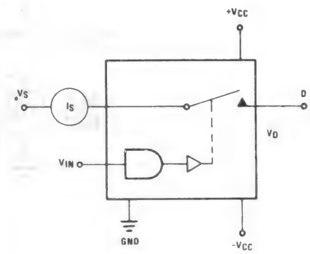
INPUT LEAKAGE CURRENT



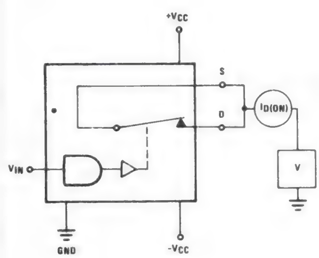
$I_{D(OFF)}$



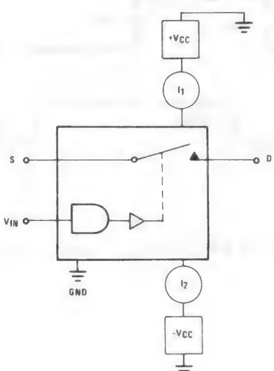
$I_{S(OFF)}$



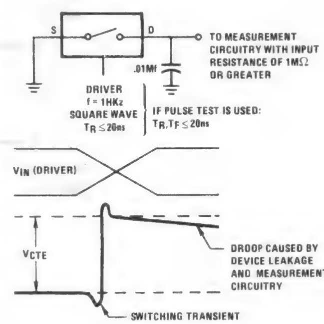
$I_{D(ON)}$



SUPPLY CURRENTS

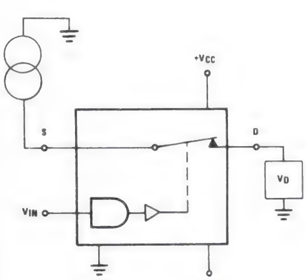


CHARGE TRANSFER ERROR

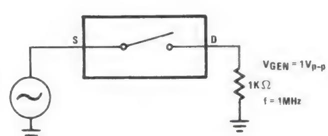


NOTE: V_{CTE} may be a positive or negative value

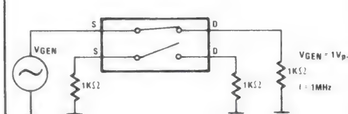
R_{DS}



OFF CHANNEL ISOLATION



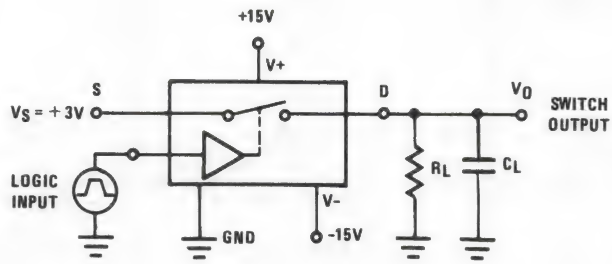
CROSSTALK BETWEEN CHANNELS

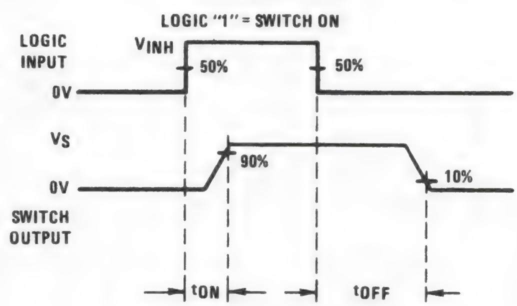


For Detail Information Refer to HI-302/883 Test Tech Brief

4 CMOS ANALOG SWITCHES

Test Waveforms



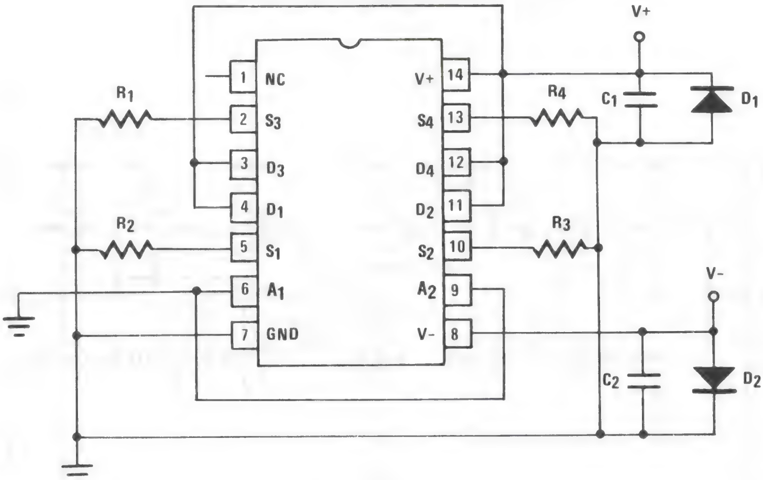


NOTES:

1. $R_L = 300\Omega$: $C_L = 33pF$
2. $V_{INH} = 4V$
   RISETIME (0.4V to 3.6V) $\leq$ 20ns
   FALLTIME (3.6V to 0.4V) $\leq$ 20ns

Burn-In Circuit

HI-302/883 CERAMIC DIP

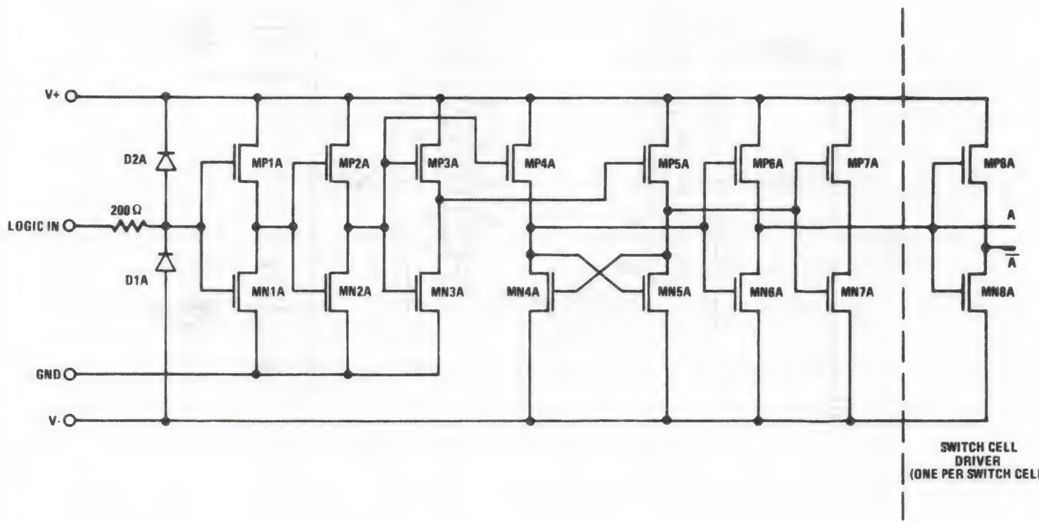


NOTES:
$R_1 = R_2 = R_3 = R_4 = 10K\Omega$, 5%, 1/4 or 1/2 watt
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2$ = IN4002 (per board)
$|(V+) - (V-)| = 30V$

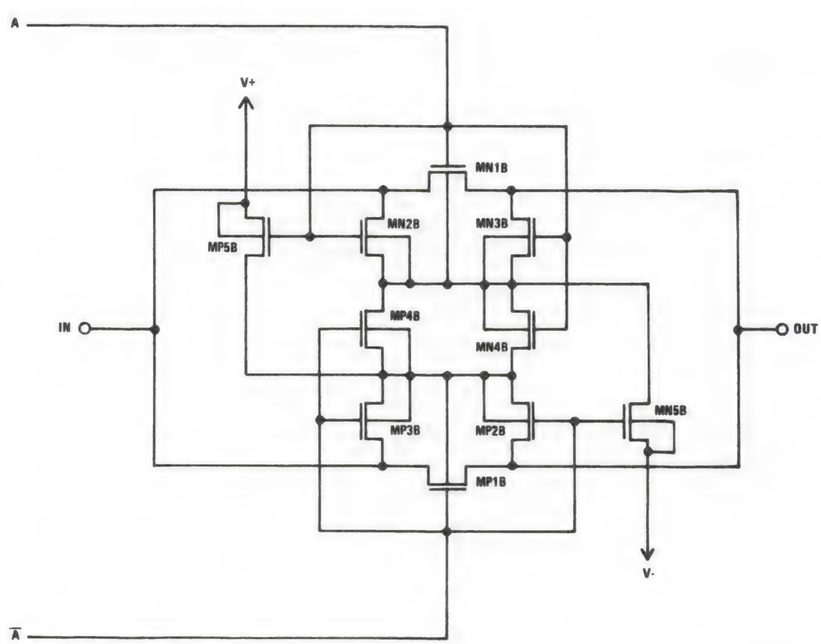
4 CMOS ANALOG SWITCHES

Schematic Diagram

DIGITAL INPUT BUFFER AND LEVEL SHIFTER



SWITCH CELL



Die Characteristics

DIE DIMENSIONS:
76 x 83.9 x 19 mils

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

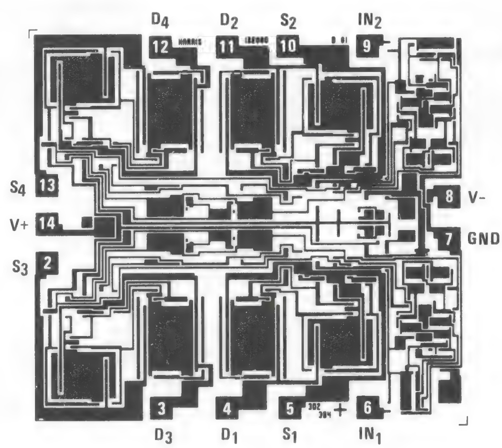
GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)

WORST CASE CURRENT DENSITY:
$3.9 \times 10^5 A/cm^2$ at 30mA
This device meets Glassivation Integrity Test requirement per Mil-Std-883 Method 2021 and Mil-M-38510 paragraph 3.5.5.4.

Metallization Mask Layout

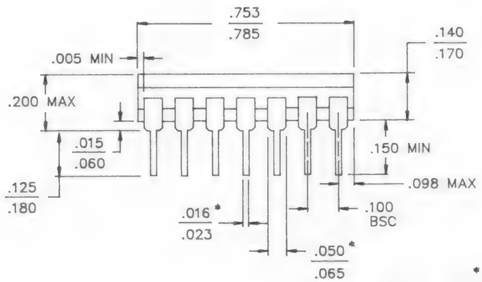
HI-302/883

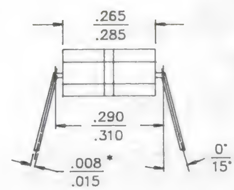


4
CMOS ANALOG SWITCHES

Packaging†

14 PIN CERAMIC DIP





* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-1

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

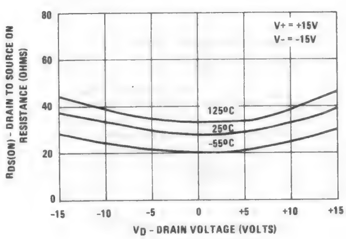
†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

Dual DPST CMOS Analog Switch

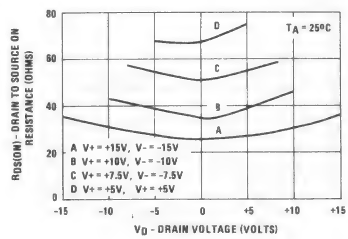
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics Unless Otherwise Specified: V+ = +15V, V- = -15V, T_A = +25°C

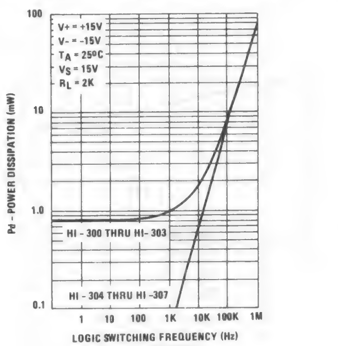
$R_{DS(ON)}$ vs. V_D AND TEMPERATURE



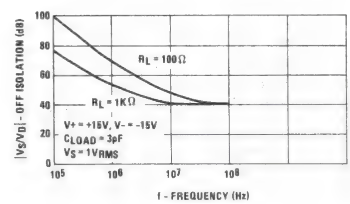
$R_{DS(ON)}$ vs. V_D AND POWER SUPPLY VOLTAGE



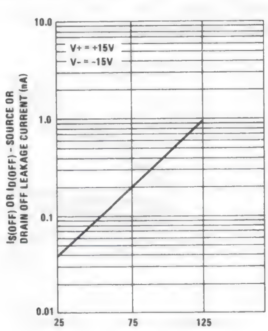
DEVICE POWER DISSIPATION vs. SWITCHING FREQUENCY SIGNAL LOGIC INPUT



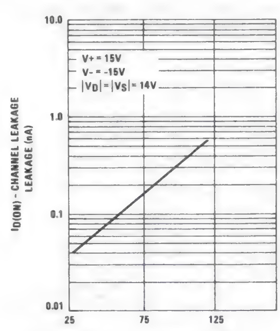
OFF ISOLATION vs. FREQUENCY



$I_{S(OFF)}$ or $I_{D(OFF)}$ vs. TEMPERATURE*



$I_{D(ON)}$ vs. TEMPERATURE*



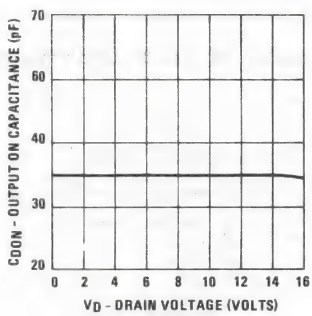
* The net leakage into the source or drain is the N-channel leakage minus the P-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

DESIGN INFORMATION (Continued)

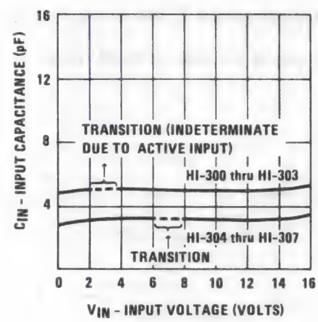
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics Unless Otherwise Specified: V+ = +15V, V- = -15V, T_A = +25°C

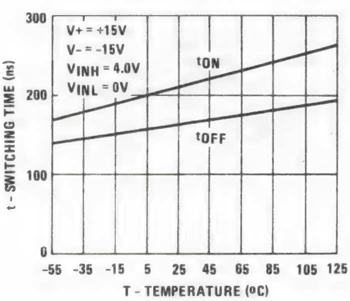
OUTPUT ON CAPACITANCE vs. DRAIN VOLTAGE



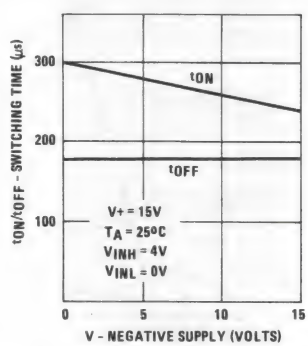
DIGITAL INPUT CAPACITANCE vs. INPUT VOLTAGE



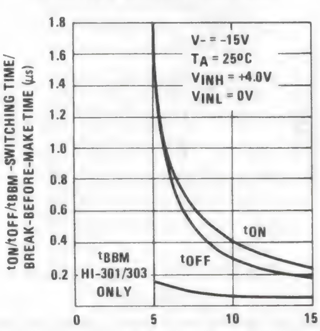
SWITCHING TIME vs. TEMPERATURE



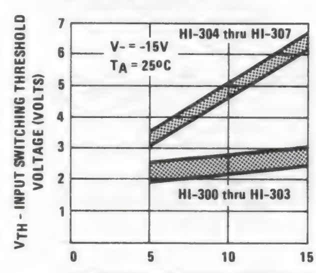
SWITCHING TIME vs. NEGATIVE SUPPLY VOLTAGE



SWITCHING TIME AND BREAK BEFORE MAKE TIME vs. POSITIVE SUPPLY VOLTAGE



INPUT SWITCHING TIME THRESHOLD vs. POSITIVE SUPPLY VOLTAGE



HARRIS

HI-303/883

January 1989

Dual SPDT CMOS Analog Switch

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Analog Signal Range (±15V Supplies) .... ±15V
- Low Leakage (+25°C) .... 1nA (Max)
- Low Leakage (+125°C) .... 100nA (Max)
- Low ON Resistance .... 50Ω (Max)
- Charge Injection .... 30pC (Typ)
- TTL Compatible
- Symmetrical Switch Elements
- Low Operating Power
- Compatible with DG303

Applications

- Sample and Hold, i.e. Low Leakage Switching
- Op Amp Gain Switching, i.e. Low ON Resistance
- Portable, Battery Operated Circuits
- Low Level Switching Circuits
- Dual or Single Supply Systems

Description

The HI-303/883 switch is a monolithic device fabricated using CMOS technology and the Harris Dielectric Isolation process. This switch features break-before-make switching, low and nearly constant ON resistance over the full analog signal range, and low power dissipation.

The HI-303/883 is TTL compatible and has a logic "0" condition with an input less than 0.8V and a logic "1" condition with an input greater than 4.0V.

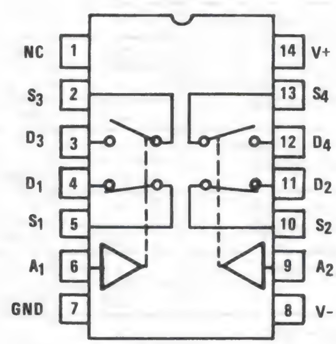
The HI-303/883 is pin-for-pin compatible with the industry standard Siliconix DG303. The device is available in a 14 pin Ceramic DIP. The HI-303/883 operates over the -55°C to +125°C temperature range.

4

CMOS ANALOG SWITCHES

Pinout

HI1-303/883 (CERAMIC DIP)
TOP VIEW



LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 44V
$\pm V_{SUPPLY}$ to Ground (V+, V-) .... ±22V
Analog Input Voltage $+V_S$ .... $+V_{SUPPLY}$ +1.5V
$-V_S$ .... $-V_{SUPPLY}$ -1.5V
Digital Input Voltage $+V_A$ .... $+V_{SUPPLY}$ +4V
$-V_A$ .... $-V_{SUPPLY}$ -4V
Peak Current (S or D)
(Pulse at 1ms, 10% Duty Cycle Max) 40mA
Continuous Current 30mA
Junction Temperature .... +175°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering 10 sec) .... ≤275°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	88°C/W	24°C/W

Package Power Dissipation at +75°C
Ceramic DIP Package 0.85W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 11.36mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) .... ±15V
Analog Input Voltage (V_S) .... $\pm V_{SUPPLY}$
Logic Low Level (V_{AL}) .... 0V to 0.8V
Logic High Level (V_{AH}) .... 4.0V to $+V_{SUPPLY}$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, GND = 0V, Unless Otherwise Specified

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch "ON" Resistance	R_{DS}	V_{A1} = 4.0V, V_D = 10V, I_S = -10mA V_{A2} = 0.8V S1/S2/S3/S4	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
		V_{A1} = 0.8V, V_D = -10V, I_S = 10mA V_{A2} = 4.0V S1/S2/S3/S4	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = +14V, V_D = -14V, V_{A1} = 0.8V V_{A2} = 4.0V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = -14V, V_D = +14V, V_{A1} = 4.0V V_{A2} = 0.8V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_S = +14V, V_D = -14V, V_{A1} = 0.8V V_{A2} = 4.0V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = -14V, V_D = +14V, V_{A1} = 4.0V V_{A2} = 0.8V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = +14V, V_{A1} = 4.0V V_{A2} = 0.8V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_D = V_S = -14V, V_{A1} = 0.8V V_{A2} = 4.0V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Low Level Input Current	I_{AL}	All Channels V_{AL} = 0.8V	1	+25°C	-1.0	1.0	μA
			2, 3	-55°C to +125°C	-1.0	1.0	μA
High Level Input Current	I_{AH}	All Channels V_{AH} = 4.0V	1	+25°C	-1.0	1.0	μA
			2, 3	-55°C to +125°C	-1.0	1.0	μA
Supply Current	$+I_{CC}$	All Channels V_A = 0.8V	1	+25°C	-	10	μA
			2, 3	-55°C to +125°C	-	100	μA
		V_{A1} = 0V, V_{A2} = 4.0V and V_{A1} = 4.0V, V_{A2} = 0V	1	+25°C	-	0.5	mA
			2, 3	-55°C to +125°C	-	1.0	mA
Supply Current	$-I_{CC}$	All Channels V_A = 0.8V	1	+25°C	-10	-	μA
			2, 3	-55°C to +125°C	-100	-	μA
		V_{A1} = 0V, V_{A2} = 4.0V and V_{A1} = 4.0V, V_{A2} = 0V	1	+25°C	-10	-	μA
			2, 3	-55°C to +125°C	-100	-	μA

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Turn "ON" Time	$t_{(ON)}$	$C_L = 33pF$, $R_L = 300\Omega$	9	$+25^oC$	-	300	ns
			10, 11	-55^oC, $+125^oC$	-	500	ns
Turn "OFF" Time	$t_{(OFF)}$	$C_L = 33pF$, $R_L = 300\Omega$	9	$+25^oC$	-	250	ns
			10, 11	-55^oC, $+125^oC$	-	450	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Characterized at: $+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Switch Input Capacitance	$C_{IS(OFF)}$	Measured Source to GND	1	$+25^oC$	-	28	pF
Driver Input Capacitance	C_{C1}	$V_A = 0V$	1	$+25^oC$	-	10	pF
	C_{C2}	$V_A = 15V$	1	$+25^oC$	-	10	pF
Switch Output Capacitance	C_{OS}	Measured Drain to GND	1	$+25^oC$	-	28	pF
Off Isolation	V_{ISO}	$f = 1MHz$, $V_{GEN} = 1V_{p-p}$	1	$+25^oC$	40	-	dB
Crosstalk	V_{CT}	$f = 1MHz$, $V_{GEN} = 1V_{p-p}$	1	$+25^oC$	40	-	dB
Charge Transfer	V_{CTE}	$V_S = GND$, $C_L = 0.01\mu F$	1	$+25^oC$	-	15	mV

NOTE 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

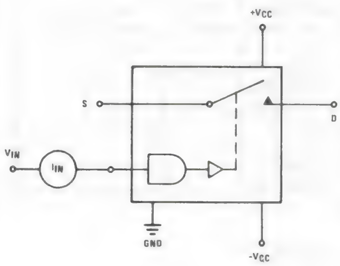
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

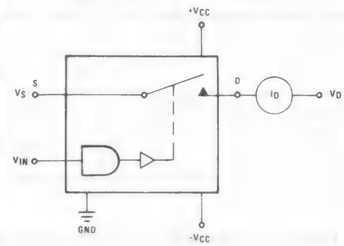
* PDA applies to Subgroup 1 only.

Test Circuits

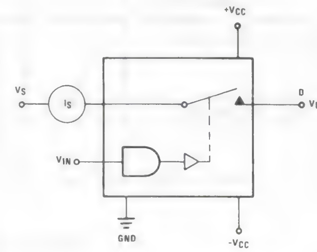
INPUT LEAKAGE CURRENT



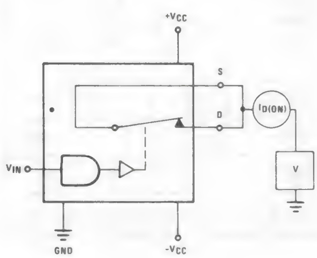
$I_{D(OFF)}$



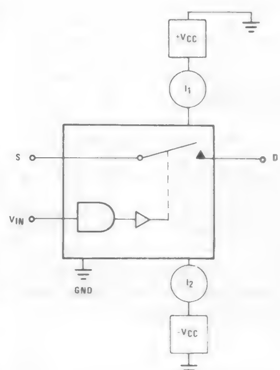
$I_{S(OFF)}$



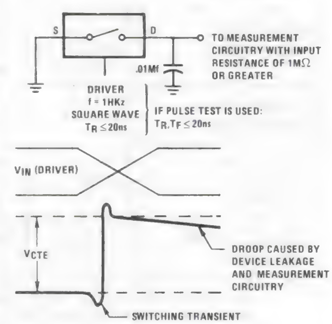
$I_{D(ON)}$



SUPPLY CURRENTS

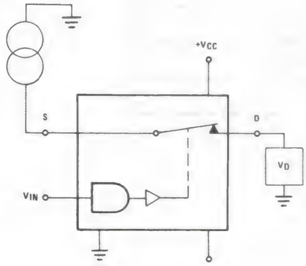


CHARGE TRANSFER ERROR

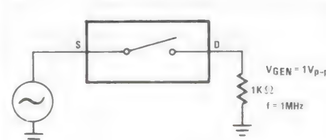


NOTE: V_{CTE} may be a positive or negative value

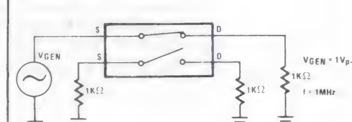
R_{DS}



OFF CHANNEL ISOLATION

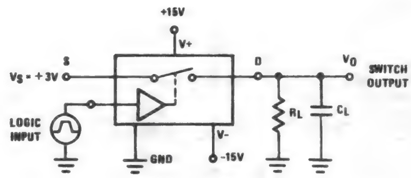


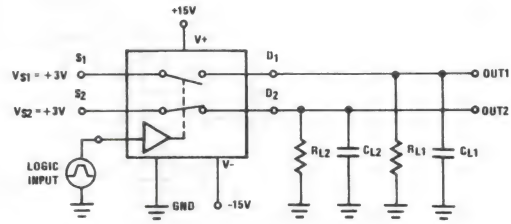
CROSSTALK BETWEEN CHANNELS

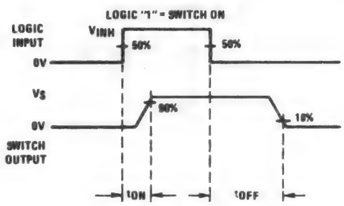


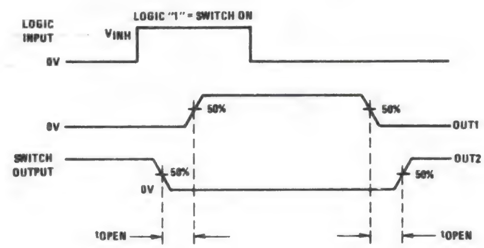
For Detail Information Refer to HI-303/883 Test Tech Brief

Test Waveforms







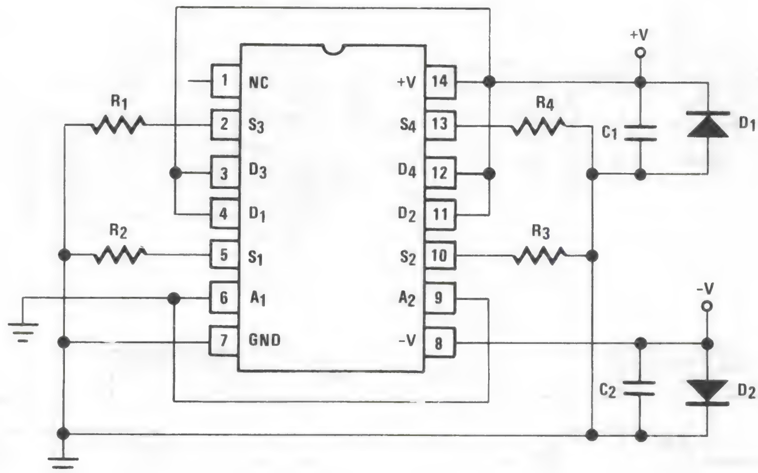


NOTES:

1. $R_L = R_L1 = R_L2 = 300\Omega$; $C_L = C_L1 = C_L2 = 33pF$
2. $V_{INH} = 4V$
   RISETIME (0.4V to 3.6V) $\leq$ 20ns
   FALLTIME (3.6V to 0.4V) $\leq$ 20ns

Burn-In Circuit

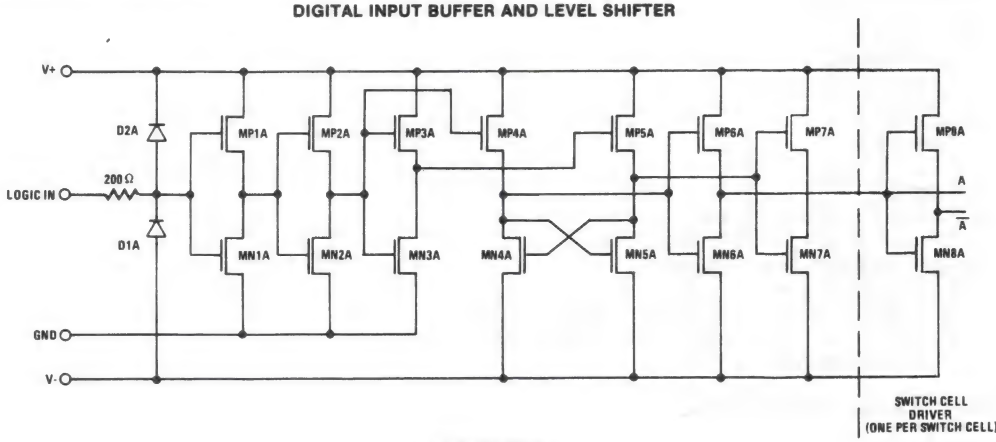
HI-303/883 CERAMIC DIP



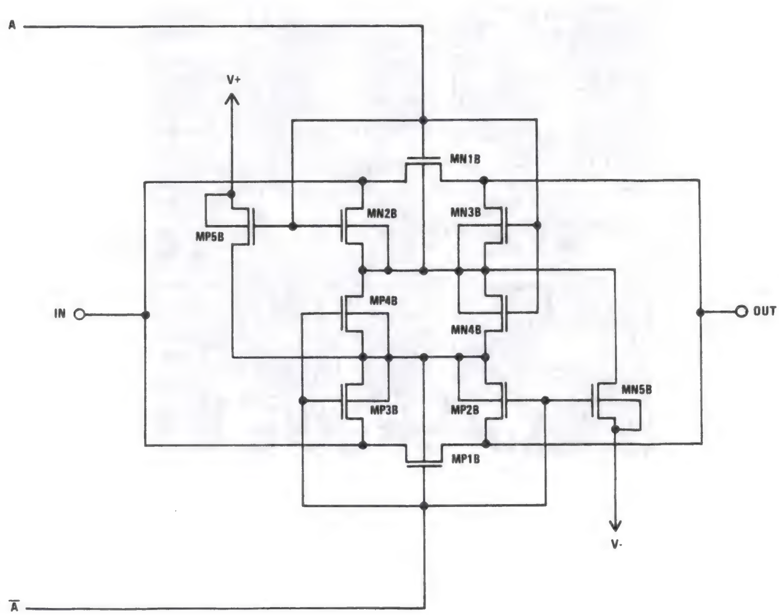
NOTES:
$R_1 = R_2 = R_3 = R_4 = 10K\Omega$, 5%, 1/4 or 1/2 watt
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2$ = IN4002 (per board)
$|(V+) - (V-)| = 30V$

Schematic Diagram

DIGITAL INPUT BUFFER AND LEVEL SHIFTER



SWITCH CELL



Die Characteristics

DIE DIMENSIONS:
76 x 83.9 x 19 mils

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

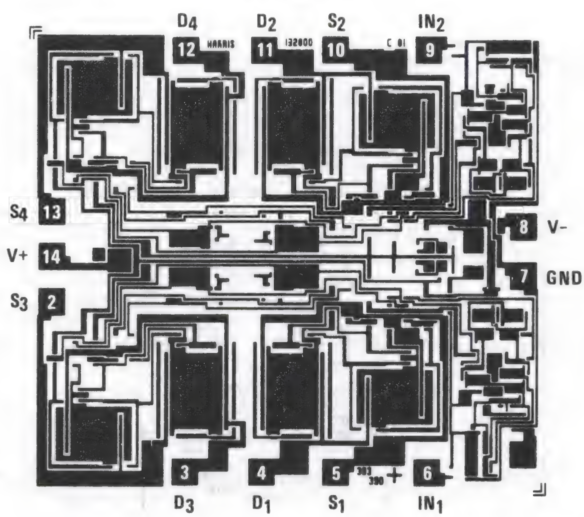
DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)

WORST CASE CURRENT DENSITY:
$3.9 \times 10^5 A/cm^2$ at 30mA

This device meets Glassivation Integrity Test requirement per Mil-Std-883 Method 2021 and Mil-M-38510 paragraph 3.5.5.4.

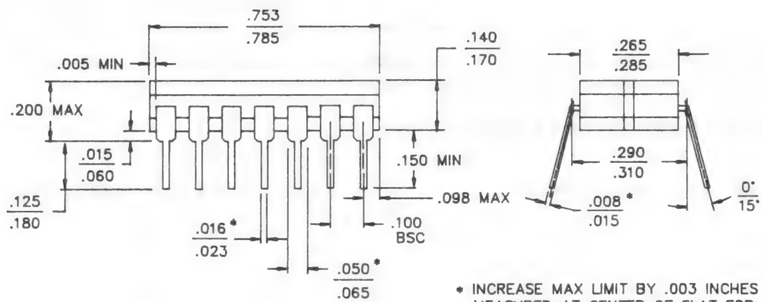
Metallization Mask Layout

HI-303/883



Packaging†

14 PIN CERAMIC DIP



* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-1

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

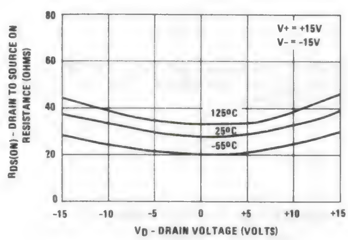
†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

Dual SPDT CMOS Analog Switch

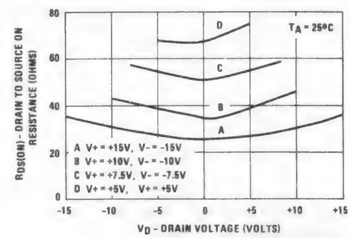
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics Unless Otherwise Specified: V+ = +15V, V- = -15V, T_A = +25°C

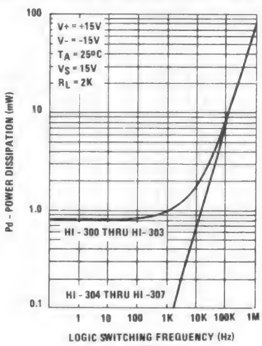
$R_{DS(ON)}$ vs. V_D AND TEMPERATURE



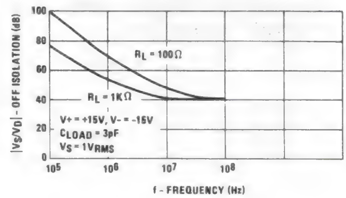
$R_{DS(ON)}$ vs. V_D AND POWER SUPPLY VOLTAGE



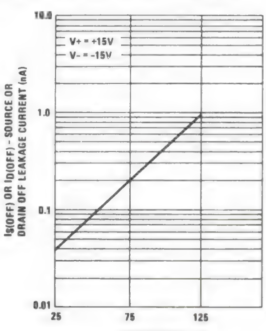
DEVICE POWER DISSIPATION vs. SWITCHING FREQUENCY SIGNAL LOGIC INPUT



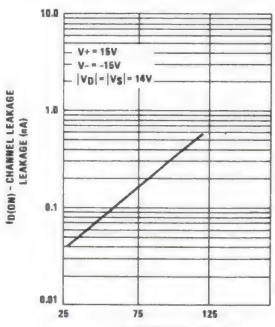
OFF ISOLATION vs. FREQUENCY



$I_{S(OFF)}$ or $I_{D(OFF)}$ vs. TEMPERATURE*



$I_{D(ON)}$ vs. TEMPERATURE*



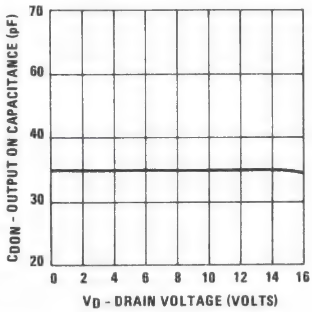
* The net leakage into the source or drain is the N-channel leakage minus the P-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

DESIGN INFORMATION (Continued)

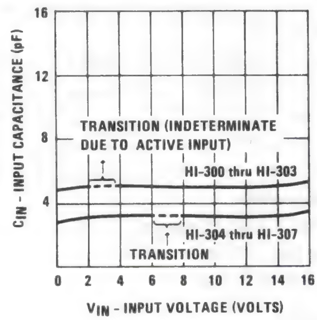
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics Unless Otherwise Specified: V+ = +15V, V- = -15V, T_A = +25°C

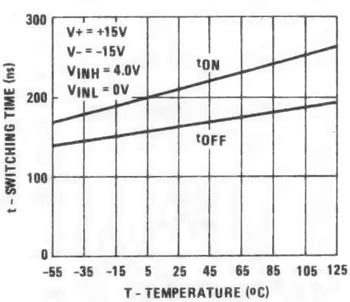
OUTPUT ON CAPACITANCE vs. DRAIN VOLTAGE



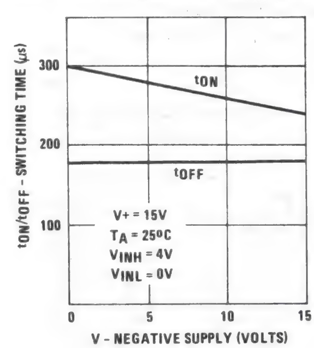
DIGITAL INPUT CAPACITANCE vs. INPUT VOLTAGE



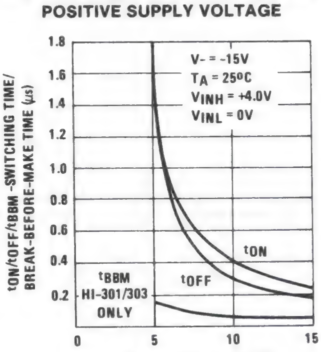
SWITCHING TIME vs. TEMPERATURE



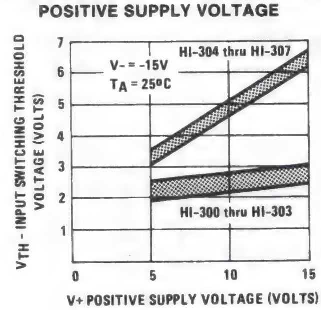
SWITCHING TIME vs. NEGATIVE SUPPLY VOLTAGE



SWITCHING TIME AND BREAK BEFORE MAKE TIME vs. POSITIVE SUPPLY VOLTAGE



INPUT SWITCHING TIME THRESHOLD vs. POSITIVE SUPPLY VOLTAGE



HARRIS

HI-304/883

January 1989

Dual SPST CMOS Analog Switch

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Analog Signal Range (±15V Supplies) .... ±15V
- Low Leakage (+25°C) .... 1nA (Max)
- Low Leakage (+125°C) .... 100nA (Max)
- Low ON Resistance .... 50Ω (Max)
- Charge Injection .... 30pC (Typ)
- CMOS Compatible
- Symmetrical Switch Elements
- Low Operating Power
- Compatible with DG304

Applications

- Sample and Hold, i.e. Low Leakage Switching
- Op Amp Gain Switching, i.e. Low ON Resistance
- Portable, Battery Operated Circuits
- Low Level Switching Circuits
- Dual or Single Supply Systems

Description

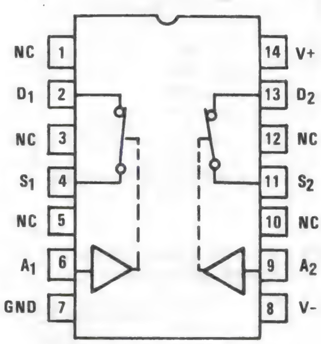
The HI-304/883 switch is a monolithic device fabricated using CMOS technology and the Harris Dielectric Isolation process. This switch features low and nearly constant ON resistance over the full analog signal range, and low power dissipation.

The HI-304/883 is CMOS compatible and has a logic "0" condition with an input less than 3.5V and a logic "1" condition with an input greater than 11V.

The HI-304/883 is pin-for-pin compatible with the industry standard Siliconix DG304. The device is available in a 14 pin Ceramic DIP and in a 10 pin Metal Can. The HI-304/883 operates over the -55°C to +125°C temperature range.

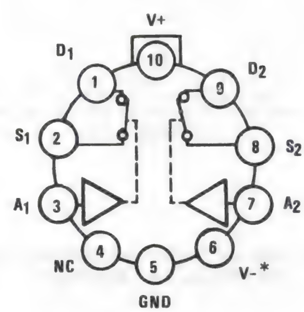
Pinouts

HI1-304/883 (CERAMIC DIP)
TOP VIEW



LOGIC	SWITCH
0	OFF
1	ON

HI2-304/883 (METAL CAN)
TOP VIEW



*The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 44V
$\pm V_{SUPPLY}$ to Ground (V+, V-) ..... ±22V
Analog Input Voltage $+V_S$ ..... $+V_{SUPPLY}$ +1.5V
$-V_S$ ..... $-V_{SUPPLY}$ -1.5V
Digital Input Voltage $+V_A$ ..... $+V_{SUPPLY}$ +4V
$-V_A$ ..... $-V_{SUPPLY}$ -4V
Peak Current (S or D)
(Pulse at 1ms, 10% Duty Cycle Max) 40mA
Continuous Current 30mA
Junction Temperature ..... +175°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... ≤275°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	98°C/W	30°C/W
Metal Can Package	117°C/W	35°C/W

Package Power Dissipation at +75°C
Ceramic DIP Package 0.77W
Metal Can Package 0.64W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package ..... 10.32mW/°C
Metal Can Package ..... 8.56mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) ..... ±15V
Analog Input Voltage (V_S) ..... $\pm V_{SUPPLY}$
Logic Low Level (V_{AL}) ..... 0V to 3.5V
Logic High Level (V_{AH}) ..... 11V to $+V_{SUPPLY}$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, GND = 0V, Unless Otherwise Specified

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch "ON" Resistance	R_{DS}	V_A = 11V, V_D = 10V, I_S = -10mA S1/S2	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
		V_A = 11V, V_D = -10V, I_S = 10mA S1/S2	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = +14V, V_D = -14V, V_A = 3.5V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = -14V, V_D = +14V, V_A = 3.5V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_S = +14V, V_D = -14V, V_A = 3.5V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = -14V, V_D = +14V, V_A = 3.5V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = +14V, V_A = 11V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_D = V_S = -14V, V_A = 11V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Low Level Input Current	I_{AL}	V_A = 3.5V	1	+25°C	-1.0	1.0	µA
			2, 3	-55°C to +125°C	-1.0	1.0	µA
High Level Input Current	I_{AH}	V_A = 11V	1	+25°C	-1.0	1.0	µA
			2, 3	-55°C to +125°C	-1.0	1.0	µA
Supply Current	$+I_{CC}$	V_{A1} = V_{A2} = 0V	1	+25°C	-	10	µA
			2, 3	-55°C to +125°C	-	100	µA
		V_{A1} = V_{A2} = 15V	1	+25°C	-	10	µA
			2, 3	-55°C to +125°C	-	100	µA
Supply Current	$-I_{CC}$	V_{A1} = V_{A2} = 0V	1	+25°C	-10	-	µA
			2, 3	-55°C to +125°C	-100	-	µA
		V_{A1} = V_{A2} = 15V	1	+25°C	-10	-	µA
			2, 3	-55°C to +125°C	-100	-	µA

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = −15V, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Turn "ON" Time	$t_{(ON)}$	$C_L = 33pF$, $R_L = 300\Omega$	9	+25°C	-	250	ns
			10, 11	-55°C, +125°C	-	500	ns
Turn "OFF" Time	$t_{(OFF)}$	$C_L = 33pF$, $R_L = 300\Omega$	9	+25°C	-	150	ns
			10, 11	-55°C, +125°C	-	450	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Characterized at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = −15V, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Switch Input Capacitance	$C_{IS(OFF)}$	Measured Source to GND	1	+25°C	-	28	pF
Driver Input Capacitance	C_{C1}	$V_A = 0V$	1	+25°C	-	10	pF
	C_{C2}	$V_A = 15V$	1	+25°C	-	10	pF
Switch Output Capacitance	C_{OS}	Measured Drain to GND	1	+25°C	-	28	pF
Off Isolation	V_{ISO}	f = 1MHz, $V_{GEN} = 1V_{p-p}$	1	+25°C	40	-	dB
Crosstalk	V_{CT}	f = 1MHz, $V_{GEN} = 1V_{p-p}$	1	+25°C	40	-	dB
Charge Transfer	V_{CTE}	V_S = GND, $C_L = 0.01\mu F$	1	+25°C	-	15	mV

NOTE 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

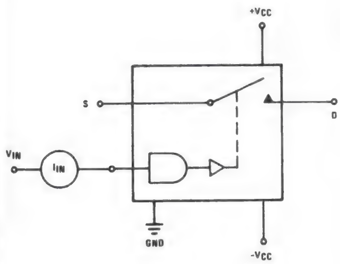
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

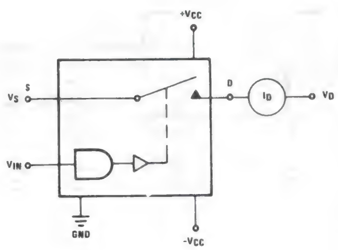
* PDA applies to Subgroup 1 only.

Test Circuits

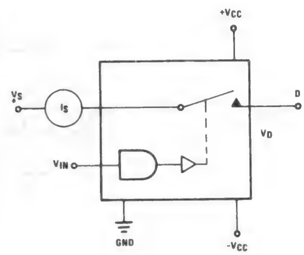
INPUT LEAKAGE CURRENT



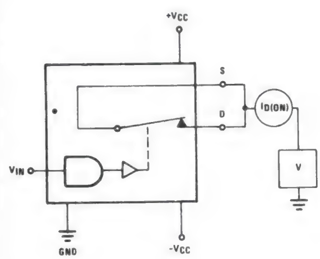
$I_{D(OFF)}$



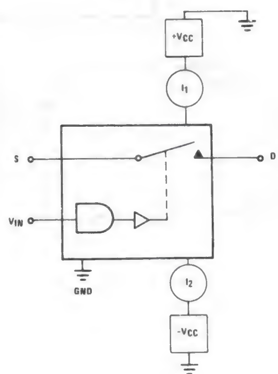
$I_{S(OFF)}$



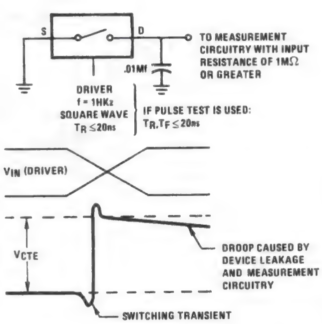
$I_{D(ON)}$



SUPPLY CURRENTS

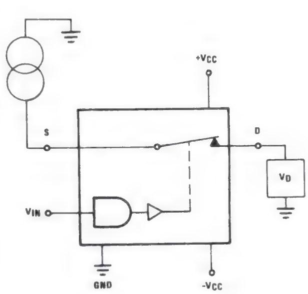


CHARGE TRANSFER ERROR

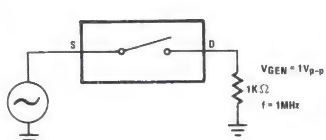


NOTE: V_{CTE} may be a positive or negative value

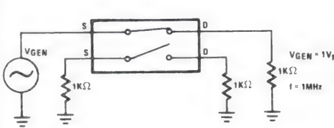
R_{DS}



OFF CHANNEL ISOLATION

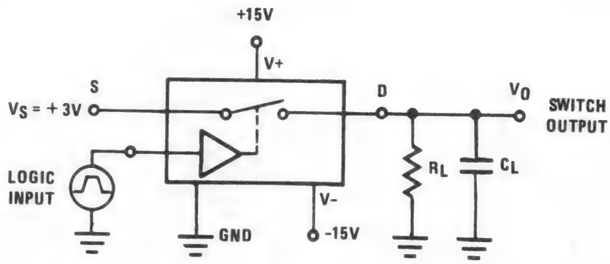


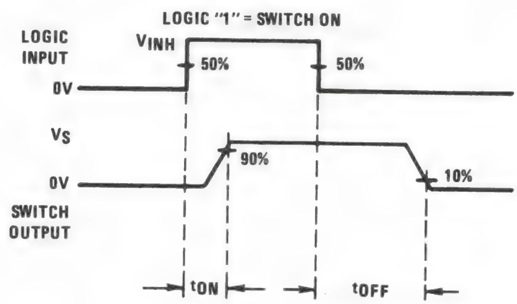
CROSSTALK BETWEEN CHANNELS



For Detail Information Refer to HI-304/883 Test Tech Brief

Test Waveforms



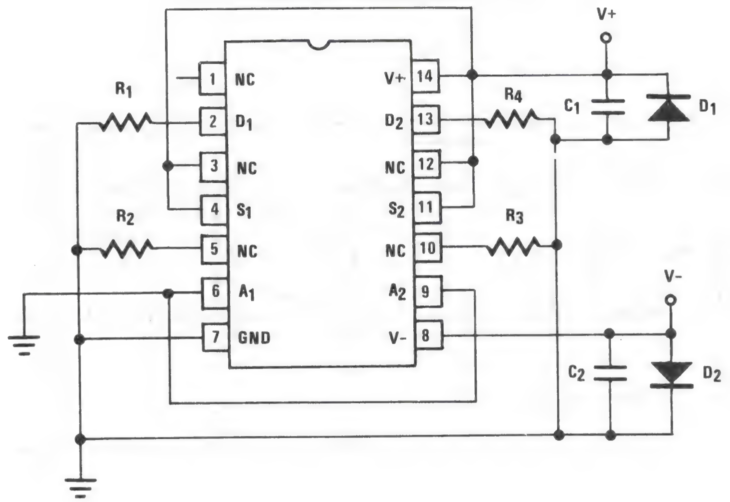


NOTES:

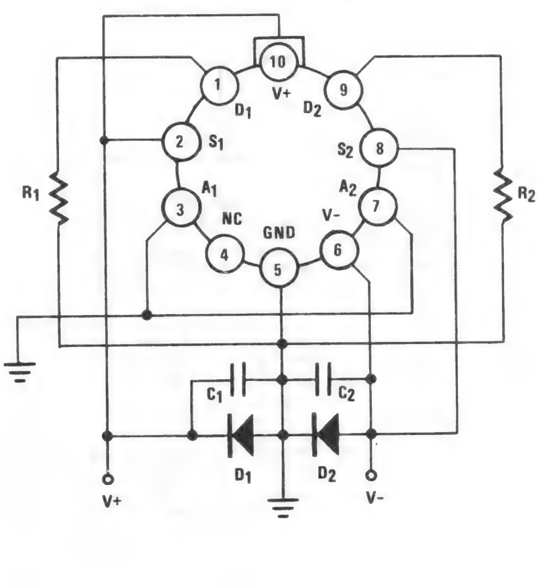
1. R_L = 300Ω: C_L = 33pF
2. V_{INH} = 15V
   RISETIME (1.5V to 13.5V) ≤ 20ns
   FALLTIME (13.5V to 1.5V) ≤ 20ns

Burn-In Circuits

HI-304/883 CERAMIC DIP



HI-304/883 METAL CAN



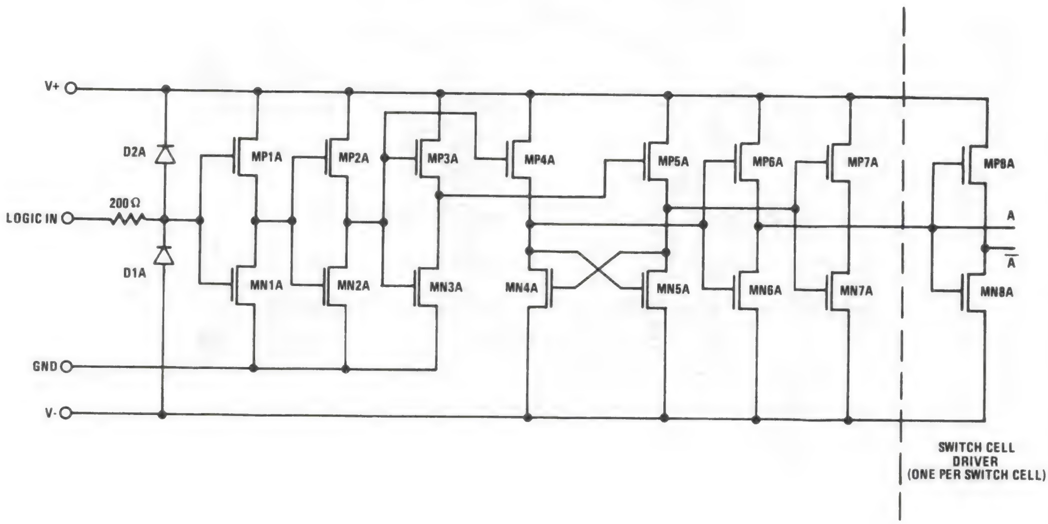
NOTES:

$R_1 = R_2 = R_3 = R_4 = 10K\Omega, \pm 5\%$ (per socket)
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2$ = IN4002 or Equivalent/Board
$|(V+) - (V-)| = 30V$

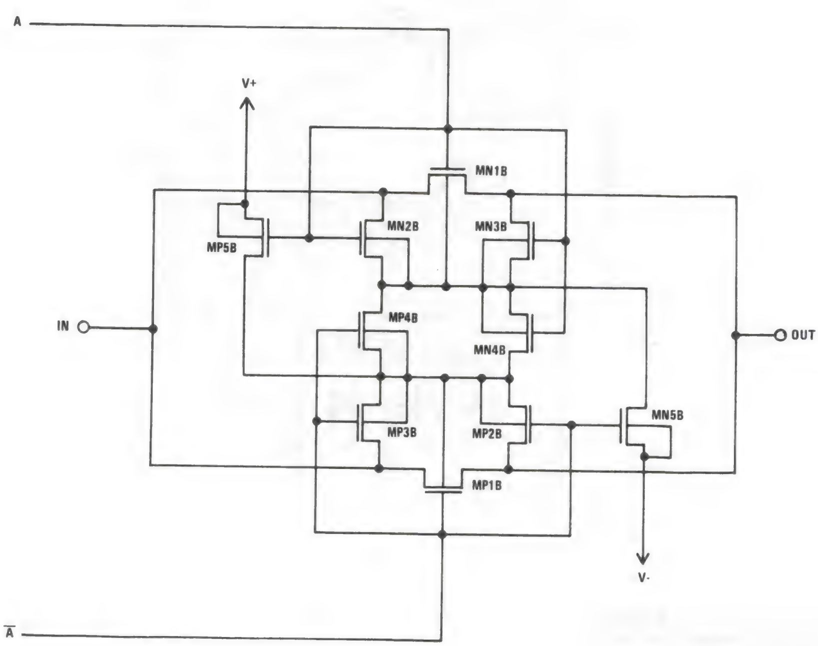
4
CMOS ANALOG SWITCHES

Schematic Diagram

DIGITAL INPUT BUFFER AND LEVEL SHIFTER



SWITCH CELL



Die Characteristics

DIE DIMENSIONS:
76 x 60.6 x 19 mils

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

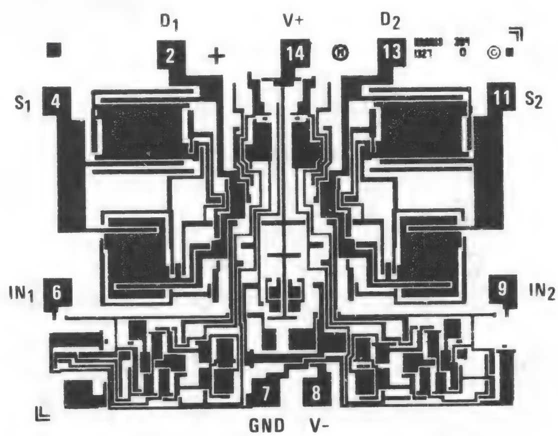
GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Metal Can — 420°C (Max)

WORST CASE CURRENT DENSITY:
$3.9 \times 10^5 A/cm^2$ at 30mA
This device meets Glassivation Integrity Test requirement per Mil-Std-883 Method 2021 and Mil-M-38510 paragraph 3.5.5.4.

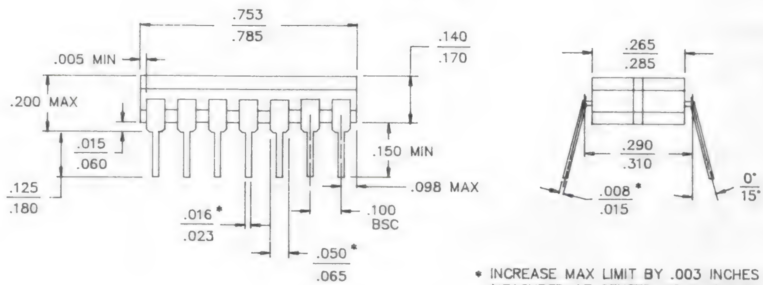
Metallization Mask Layout

HI-304/883



Packaging†

14 PIN CERAMIC DIP

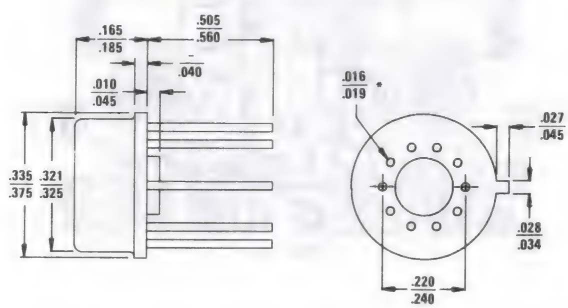


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-1

10 PIN METAL CAN



* Maximum Limits are Increased by 0.003 inches for Solder Dip Finish.

LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
Material: No Seal Material
Temperature: Room Temperature
Method: Resistance Weld

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 A-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

HI-304

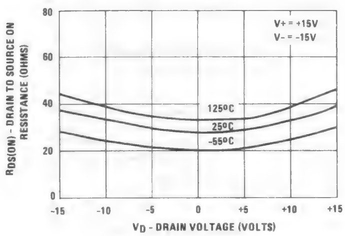
DESIGN INFORMATION

Dual SPST CMOS Analog Switch

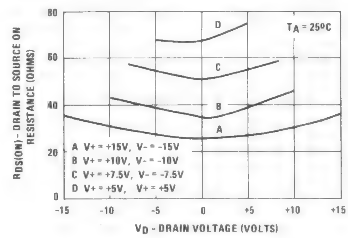
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics Unless Otherwise Specified: V+ = +15V, V- = -15V, T_A = +25°C

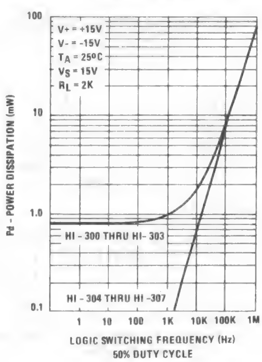
$R_{DS(ON)}$ vs. V_D AND TEMPERATURE



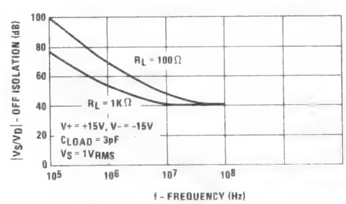
$R_{DS(ON)}$ vs. V_D AND POWER SUPPLY VOLTAGE



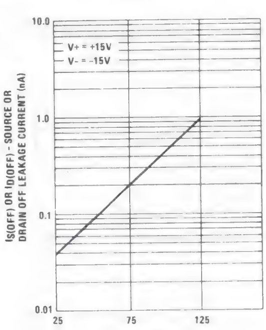
DEVICE POWER DISSIPATION vs. SWITCHING FREQUENCY SIGNAL LOGIC INPUT



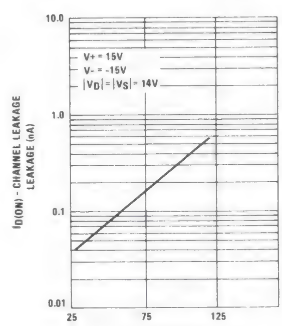
OFF ISOLATION vs. FREQUENCY



$I_{S(OFF)}$ or $I_{D(OFF)}$ vs. TEMPERATURE*



$I_{D(ON)}$ vs. TEMPERATURE*



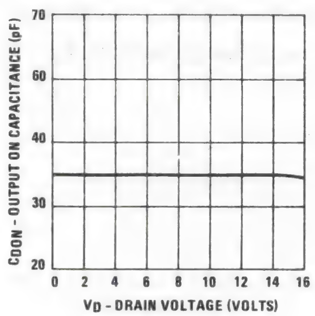
* The net leakage into the source or drain is the N-channel leakage minus the P-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

DESIGN INFORMATION (Continued)

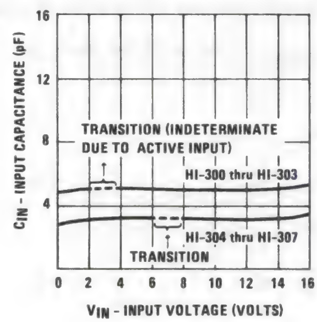
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics Unless Otherwise Specified: V+ = +15V, V- = -15V, T_A = +25°C

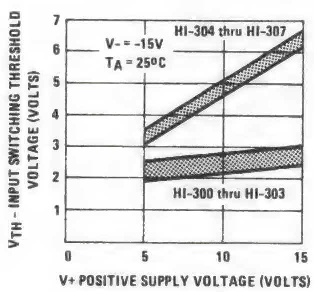
OUTPUT ON CAPACITANCE vs. DRAIN VOLTAGE



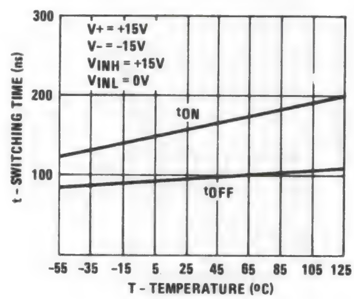
DIGITAL INPUT CAPACITANCE vs. INPUT VOLTAGE



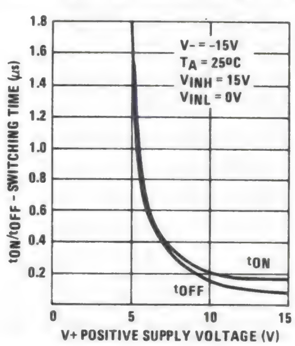
INPUT SWITCHING THRESHOLD vs. POSITIVE SUPPLY VOLTAGE



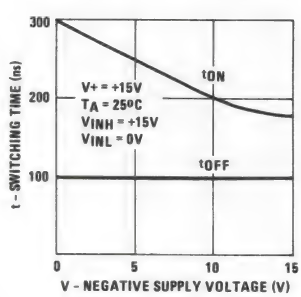
SWITCHING TIME vs. TEMPERATURE



SWITCHING TIME vs. POSITIVE SUPPLY VOLTAGE



SWITCHING TIME vs. NEGATIVE SUPPLY VOLTAGE



HARRIS

HI-305/883

January 1989

SPDT CMOS Analog Switch

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Analog Signal Range (±15V Supplies) .... ±15V
- Low Leakage (+25°C) .... 1nA (Max)
- Low Leakage (+125°C) .... 100nA (Max)
- Low ON Resistance (+25°C) .... 50Ω (Max)
- Charge Injection .... 30pC (Typ)
- CMOS Compatible
- Symmetrical Switch Elements
- Low Operating Power
- Compatible with DG305

Applications

- Sample and Hold, i.e. Low Leakage Switching
- Op Amp Gain Switching, i.e. Low ON Resistance
- Portable, Battery Operated Circuits
- Low Level Switching Circuits
- Dual or Single Supply Systems

Description

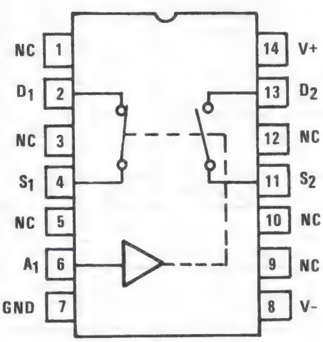
The HI-305/883 switch is a monolithic device fabricated using CMOS technology and the Harris Dielectric Isolation process. This switch features break-before-make switching, low and nearly constant ON resistance over the full analog signal range, and low power dissipation.

The HI-305/883 is CMOS compatible and has a logic "0" condition with an input less than 3.5V and a logic "1" condition with an input greater than 11V.

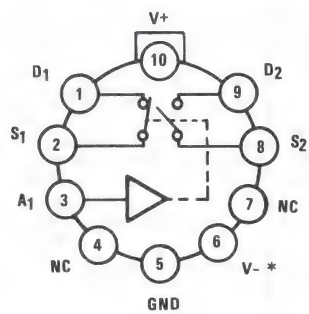
The HI-305/883 is pin-for-pin compatible with the industry standard Siliconix DG305. The device is available in a 14 pin Ceramic DIP and in a 10 pin Metal Can. The HI-305/883 operates over the -55°C to +125°C temperature range.

Pinouts

HI1-305/883 (CERAMIC DIP)
TOP VIEW



HI2-305/883 (METAL CAN)
TOP VIEW



LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

*The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 44V
$\pm V_{SUPPLY}$ to Ground (V+, V-) .... ±22V
Analog Input Voltage $+V_S$ .... $+V_{SUPPLY}$ +1.5V
$-V_S$ .... $-V_{SUPPLY}$ -1.5V
Digital Input Voltage $+V_A$ .... $+V_{SUPPLY}$ +4V
$-V_A$ .... $-V_{SUPPLY}$ -4V
Peak Current (S or D)
(Pulse at 1ms, 10% Duty Cycle Max) 40mA
Continuous Current 30mA
Junction Temperature .... +175°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering 10 sec) .... ≤275°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	98°C/W	30°C/W
Metal Can Package	117°C/W	35°C/W

Package Power Dissipation at +75°C
Ceramic DIP Package 0.77W
Metal Can Package 0.64W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 10.32mW/°C
Metal Can Package .... 8.56mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) .... ±15V
Analog Input Voltage (V_S) .... $\pm V_{SUPPLY}$
Logic Low Level (V_{AL}) .... 0V to 3.5V
Logic High Level (V_{AH}) .... 11V to $+V_{SUPPLY}$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, GND = 0V, Unless Otherwise Specified

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch "ON" Resistance	R_{DS}	V_A = 11V, V_D = 10V, I_S = -10mA S1/S2	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
		V_A = 11V, V_D = -10V, I_S = 10mA S1/S2	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = +14V, V_D = -14V, V_A = 3.5V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = -14V, V_D = +14V, V_A = 3.5V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_S = +14V, V_D = -14V, V_A = 3.5V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = -14V, V_D = +14V, V_A = 3.5V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	$V_D = V_S$ = +14V, V_A = 11V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		$V_D = V_S$ = -14V, V_A = 11V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Low Level Input Current	I_{AL}	V_A = 3.5V	1	+25°C	-1.0	1.0	μA
			2, 3	-55°C to +125°C	-1.0	1.0	μA
High Level Input Current	I_{AH}	V_A = 11V	1	+25°C	-1.0	1.0	μA
			2, 3	-55°C to +125°C	-1.0	1.0	μA
Supply Current	$+I_{CC}$	V_A = 0V	1	+25°C	-	10	μA
			2, 3	-55°C to +125°C	-	100	μA
		V_A = 15V	1	+25°C	-	10	μA
			2, 3	-55°C to +125°C	-	100	μA
Supply Current	$-I_{CC}$	V_A = 0V	1	+25°C	-10	-	μA
			2, 3	-55°C to +125°C	-100	-	μA
		V_A = 15V	1	+25°C	-10	-	μA
			2, 3	-55°C to +125°C	-100	-	μA

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Turn "ON" Time	$t_{(ON)}$	$C_L = 33pF$, $R_L = 300\Omega$	9	$+25^oC$	-	250	ns
			10, 11	-55^oC, $+125^oC$	-	500	ns
Turn "OFF" Time	$t_{(OFF)}$	$C_L = 33pF$, $R_L = 300\Omega$	9	$+25^oC$	-	150	ns
			10, 11	-55^oC, $+125^oC$	-	450	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Characterized at: $+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Switch Input Capacitance	$C_{IS(OFF)}$	Measured Source to GND	1	$+25^oC$	-	28	pF
Driver Input Capacitance	C_{C1}	$V_A = 0V$	1	$+25^oC$	-	10	pF
	C_{C2}	$V_A = 15V$	1	$+25^oC$	-	10	pF
Switch Output Capacitance	C_{OS}	Measured Drain to GND	1	$+25^oC$	-	28	pF
Off Isolation	V_{ISO}	$f = 1MHz$, $V_{GEN} = 1V_{p-p}$	1	$+25^oC$	40	-	dB
Crosstalk	V_{CT}	$f = 1MHz$, $V_{GEN} = 1V_{p-p}$	1	$+25^oC$	40	-	dB
Charge Transfer	V_{CTE}	$V_S = GND$, $C_L = 0.01\mu F$	1	$+25^oC$	-	15	mV

NOTE 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

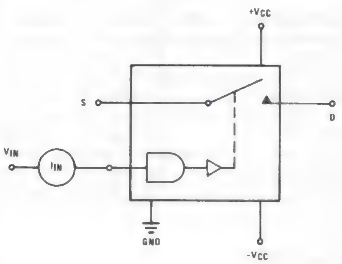
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

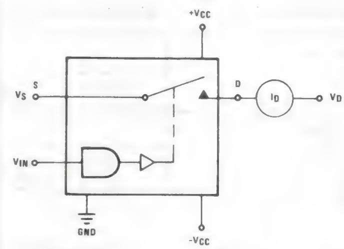
* PDA applies to Subgroup 1 only.

Test Circuits

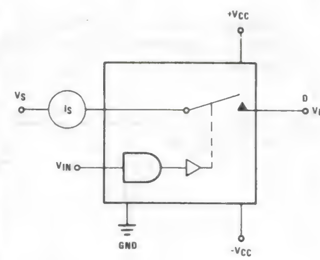
INPUT LEAKAGE CURRENT



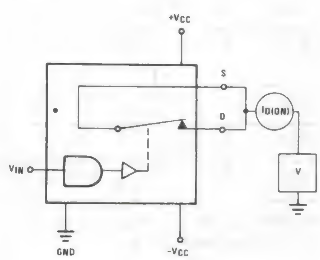
$I_{D(OFF)}$



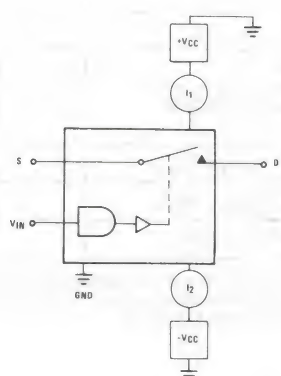
$I_{S(OFF)}$



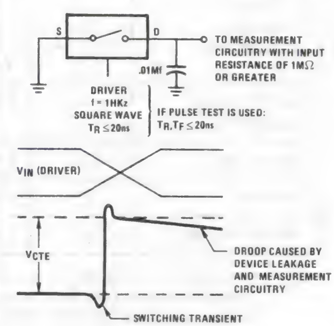
$I_{D(ON)}$



SUPPLY CURRENTS

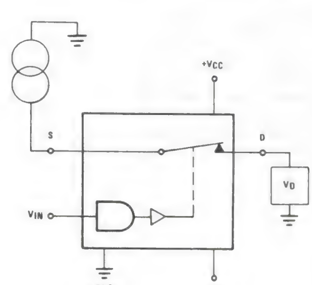


CHARGE TRANSFER ERROR

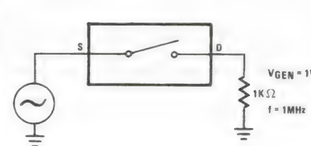


NOTE: V_{CTE} may be a positive or negative value

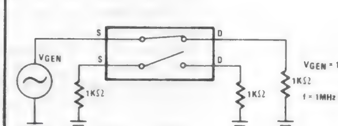
R_{DS}



OFF CHANNEL ISOLATION

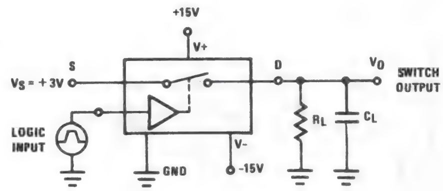


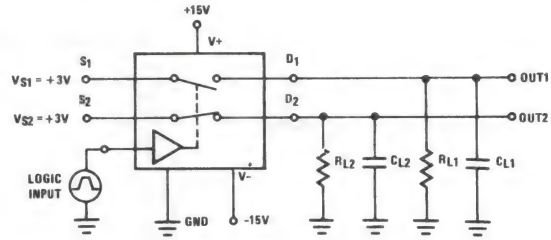
CROSSTALK BETWEEN CHANNELS

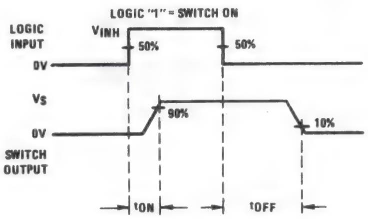


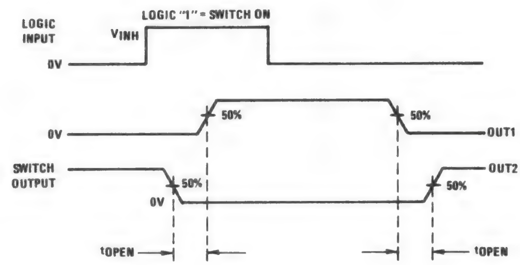
For Detail Information Refer to HI-305/883 Test Tech Brief

Test Waveforms







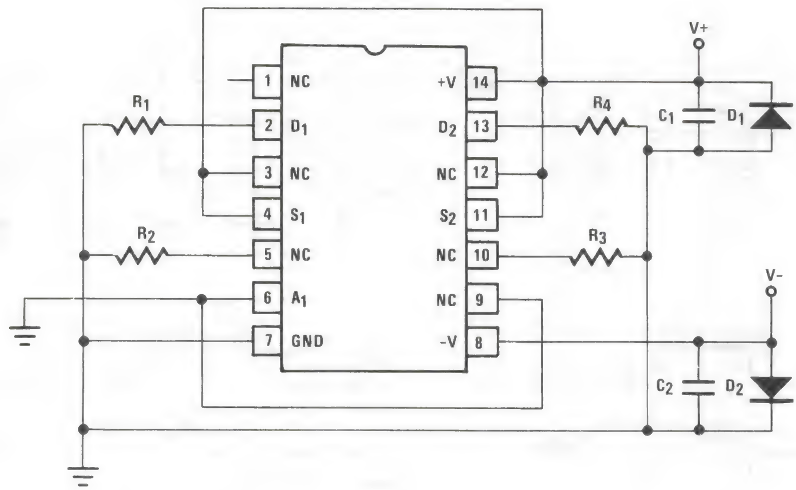


NOTES:

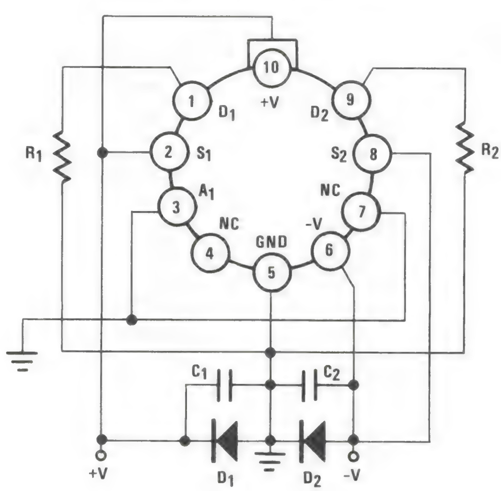
1. $R_L = R_L1 = R_L2 = 300\Omega$; $C_L = C_L1 = C_L2 = 33pF$
2. $V_{INH} = 15V$
   RISETIME (1.5V to 13.5V) $\leq$ 20ns
   FALLTIME (13.5V to 1.5V) $\leq$ 20ns

Burn-In Circuits

HI-305/883 CERAMIC DIP



HI-305/883 METAL CAN

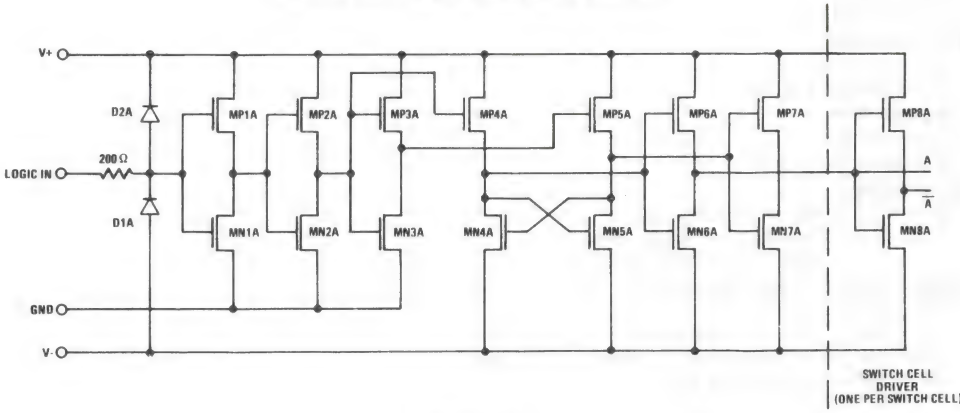


NOTES:

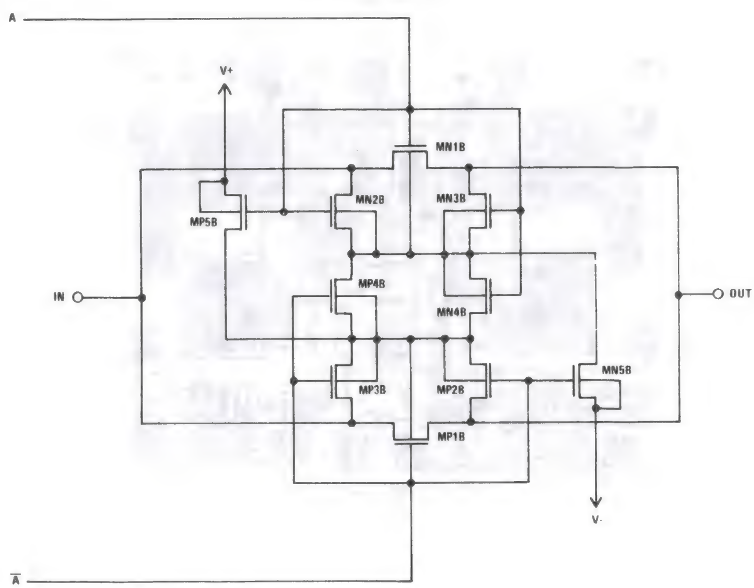
$R_1 = R_2 = R_3 = R_4 = 10k\Omega$, ± 5% (per socket)
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2$ = IN4002 or Equivalent/Board
$|(V+) - (V-)| = 30V$

Schematic Diagram

DIGITAL INPUT BUFFER AND LEVEL SHIFTER



SWITCH CELL



Die Characteristics

DIE DIMENSIONS:
76 x 60.6 x 19 mils

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

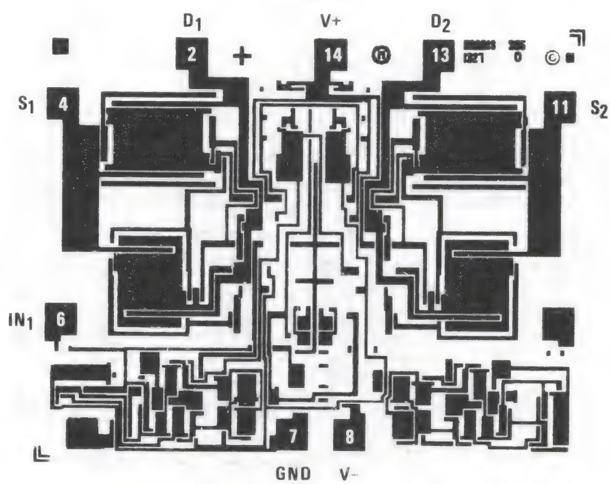
GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Metal Can — 420°C (Max)

WORST CASE CURRENT DENSITY:
$3.9 \times 10^5 A/cm^2$ at 30mA
This device meets Glassivation Integrity Test requirement per Mil-Std-883 Method 2021 and Mil-M-38510 paragraph 3.5.5.4.

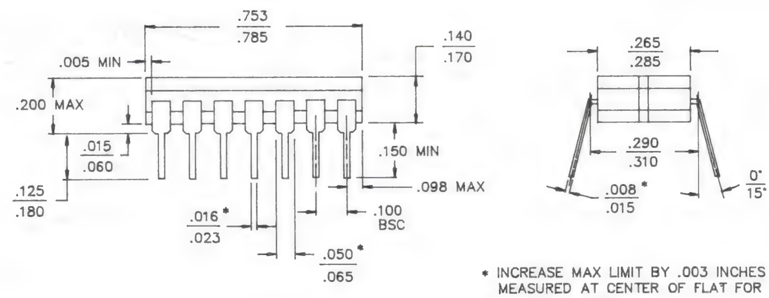
Metallization Mask Layout

HI-305/883



Packaging†

14 PIN CERAMIC DIP

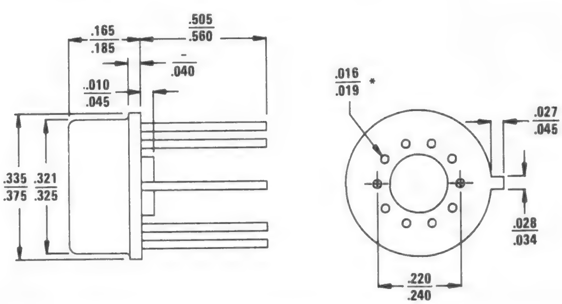


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-1

10 PIN METAL CAN



* Maximum Limits are Increased by 0.003 inches for Solder Dip Finish.

LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
Material: No Seal Material
Temperature: Room Temperature
Method: Resistance Weld

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 A-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

HI-305

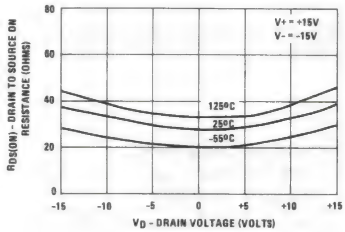
DESIGN INFORMATION

SPDT CMOS Analog Switch

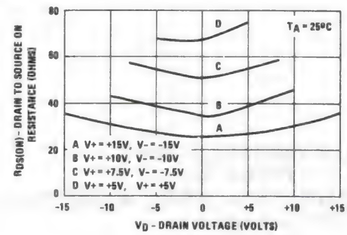
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics Unless Otherwise Specified: V+ = +15V, V- = -15V, T_A = +25°C

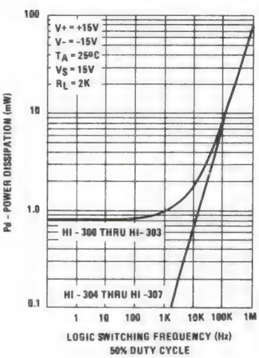
$R_{DS(ON)}$ vs. V_D AND TEMPERATURE



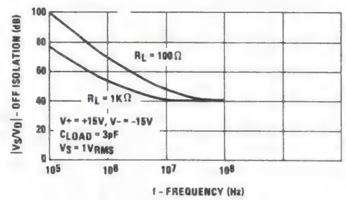
$R_{DS(ON)}$ vs. V_D AND POWER SUPPLY VOLTAGE



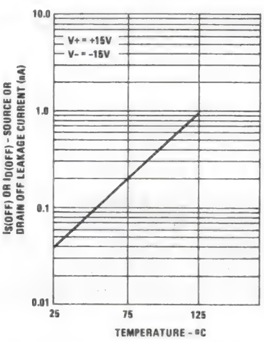
DEVICE POWER DISSIPATION vs. SWITCHING FREQUENCY SIGNAL LOGIC INPUT



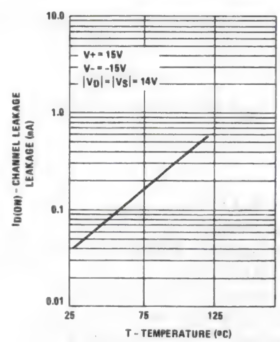
OFF ISOLATION vs. FREQUENCY



$I_{S(OFF)}$ or $I_{D(OFF)}$ vs. TEMPERATURE*



$I_{D(ON)}$ vs. TEMPERATURE*



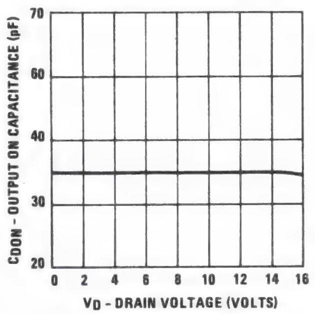
* The net leakage into the source or drain is the N-channel leakage minus the P-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

DESIGN INFORMATION (Continued)

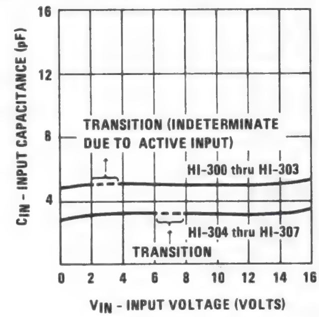
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics Unless Otherwise Specified: V+ = +15V, V- = -15V, T_A = +25°C

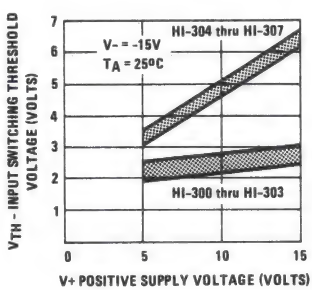
OUTPUT ON CAPACITANCE vs. DRAIN VOLTAGE



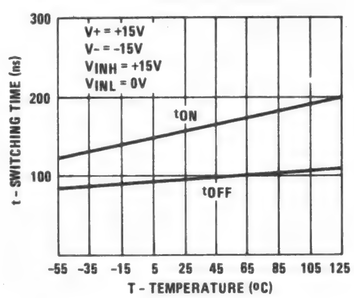
DIGITAL INPUT CAPACITANCE vs. INPUT VOLTAGE



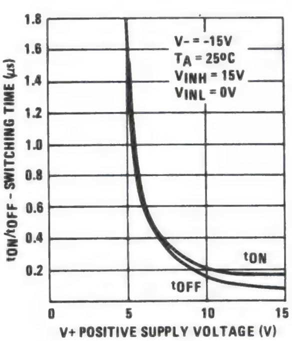
INPUT SWITCHING THRESHOLD vs. POSITIVE SUPPLY VOLTAGE



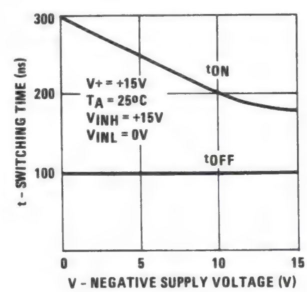
SWITCHING TIME vs. TEMPERATURE



SWITCHING TIME vs. POSITIVE SUPPLY VOLTAGE



SWITCHING TIME vs. NEGATIVE SUPPLY VOLTAGE



4 CMOS ANALOG SWITCHES

HARRIS HI-306/883

January 1989

Dual DPST CMOS Analog Switch

Features

- **This Circuit Is Processed In Accordance to Mil-Std-883 and Is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Analog Signal Range (±15V Supplies)................. ±15V**
- **Low Leakage (+25°C)....................................1nA (Max)**
- **Low Leakage (+125°C)..............................100nA (Max)**
- **Low ON Resistance..50Ω (Max)**
- **Charge Injection...30pC (Typ)**
- **CMOS Compatible**
- **Symmetrical Switch Elements**
- **Low Operating Power**
- **Compatible with DG306**

Applications

- **Sample and Hold, i.e. Low Leakage Switching**
- **Op Amp Gain Switching, i.e. Low ON Resistance**
- **Portable, Battery Operated Circuits**
- **Low Level Switching Circuits**
- **Dual or Single Supply Systems**

Description

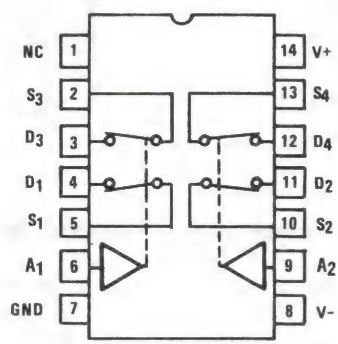
The HI-306/883 switch is a monolithic device fabricated using CMOS technology and the Harris Dielectric Isolation process. This switch features low and nearly constant ON resistance over the full analog signal range, and low power dissipation.

The HI-306/883 is CMOS compatible and has a logic "0" condition with an input less than 3.5V and a logic "1" condition with an input greater than 11.0V.

The HI-306/883 is pin-for-pin compatible with the industry standard Siliconix DG306. The device is available in a 14 pin Ceramic DIP. The HI-306/883 operates over the -55°C to +125°C temperature range.

Pinout

HI1-306/883 (CERAMIC DIP)
TOP VIEW



LOGIC	SWITCH
0	OFF
1	ON

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 44V
$\pm V_{SUPPLY}$ to Ground (V+, V-) .... ±22V
Analog Input Voltage $+V_S$ .... $+V_{SUPPLY}$ +1.5V
$-V_S$ .... $-V_{SUPPLY}$ -1.5V
Digital Input Voltage $+V_A$ .... $+V_{SUPPLY}$ +4V
$-V_A$ .... $-V_{SUPPLY}$ -4V
Peak Current (S or D)
(Pulse at 1ms, 10% Duty Cycle Max) 40mA
Continuous Current 30mA
Junction Temperature .... +175°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering 10 sec) .... ≤275°C

Thermal Information

Thermal Resistance — θ_{ja} / θ_{jc}
Ceramic DIP Package .... 88°C/W 24°C/W
Package Power Dissipation at +75°C
Ceramic DIP Package 0.85W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 11.36mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) .... ±15V
Analog Input Voltage (V_S) .... $\pm V_{SUPPLY}$
Logic Low Level (V_{AL}) .... 0V to 3.5V
Logic High Level (V_{AH}) .... 11V to $+V_{SUPPLY}$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, GND = 0V, Unless Otherwise Specified

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch "ON" Resistance	R_{DS}	V_A = 11V, V_D = 10V, I_S = -10mA S1/S2/S3/S4	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
		V_A = 11V, V_D = -10V, I_S = 10mA S1/S2/S3/S4	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = +14V, V_D = -14V, V_A = 3.5V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = -14V, V_D = +14V, V_A = 3.5V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_S = +14V, V_D = -14V, V_A = 3.5V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = -14V, V_D = +14V, V_A = 3.5V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = +14V, V_A = 11V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_D = V_S = -14V, V_A = 11V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Low Level Input Current	I_{AL}	All Channels V_A = 3.5V	1	+25°C	-1.0	1.0	µA
			2, 3	-55°C to +125°C	-1.0	1.0	µA
High Level Input Current	I_{AH}	All Channels V_A = 11V	1	+25°C	-1.0	1.0	µA
			2, 3	-55°C to +125°C	-1.0	1.0	µA
Supply Current	$+I_{CC}$	All Channels V_A = 0V	1	+25°C	-	10	µA
			2, 3	-55°C to +125°C	-	100	µA
		All Channels V_A = 15V	1	+25°C	-	10	µA
			2, 3	-55°C to +125°C	-	100	µA
Supply Current	$-I_{CC}$	All Channels V_A = 0V	1	+25°C	-10	-	µA
			2, 3	-55°C to +125°C	-100	-	µA
		All Channels V_A = 15V	1	+25°C	-10	-	µA
			2, 3	-55°C to +125°C	-100	-	µA

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Turn "ON" Time	$t_{(ON)}$	$C_L = 33pF$ $R_L = 300\Omega$	9	+25°C	-	250	ns
			10, 11	-55°C, +125°C	-	500	ns
Turn "OFF" Time	$t_{(OFF)}$	$C_L = 33pF$ $R_L = 300\Omega$	9	+25°C	-	150	ns
			10, 11	-55°C, +125°C	-	450	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Characterized at: $+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch Input Capacitance	$C_{IS(OFF)}$	Measured Source to GND	1	+25°C	-	28	pF
Driver Input Capacitance	C_{C1}	$V_A = 0V$	1	+25°C	-	10	pF
	C_{C2}	$V_A = 15V$	1	+25°C	-	10	pF
Switch Output Capacitance	C_{OS}	Measured Drain to GND	1	+25°C	-	28	pF
Off Isolation	V_{ISO}	$f = 1MHz$, $V_{GEN} = 1V_{p-p}$	1	+25°C	40	-	dB
Crosstalk	V_{CT}	$f = 1MHz$, $V_{GEN} = 1V_{p-p}$	1	+25°C	40	-	dB
Charge Transfer	V_{CTE}	$V_S = GND$, $C_L = 0.01\mu F$	1	+25°C	-	15	mV

NOTE 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

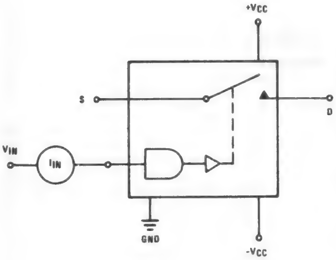
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

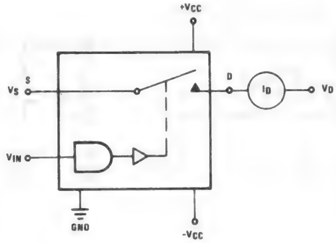
* PDA applies to Subgroup 1 only.

Test Circuits

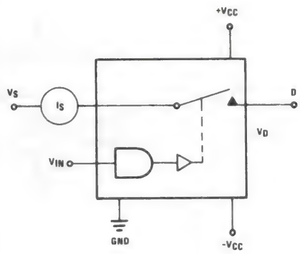
INPUT LEAKAGE CURRENT



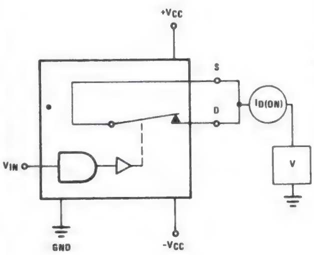
ID(OFF)



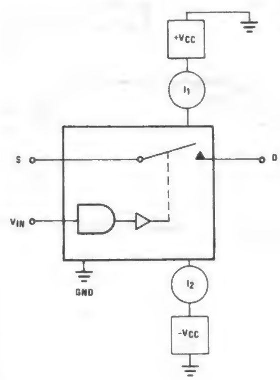
IS(OFF)



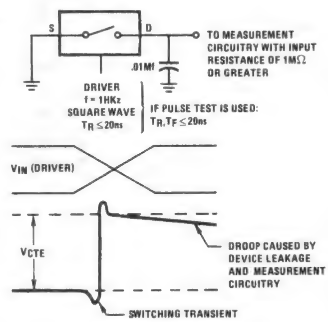
ID(ON)



SUPPLY CURRENTS

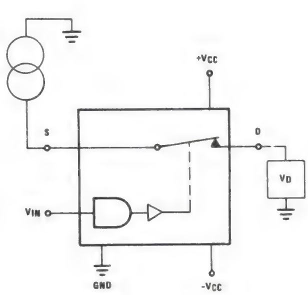


CHARGE TRANSFER ERROR

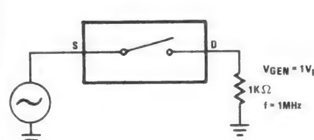


NOTE: V_{CTE} may be a positive or negative value

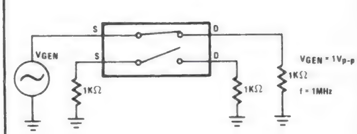
RDS



OFF CHANNEL ISOLATION

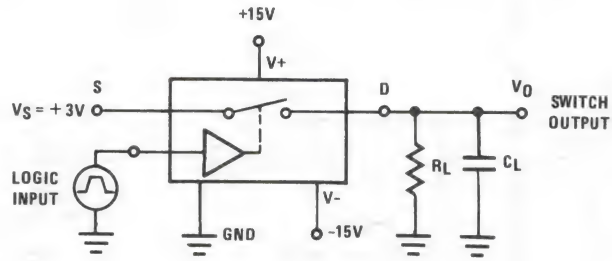


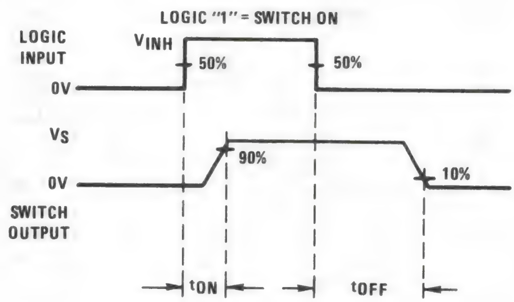
CROSSTALK BETWEEN CHANNELS



For Detail Information Refer to HI-306/883 Test Tech Brief

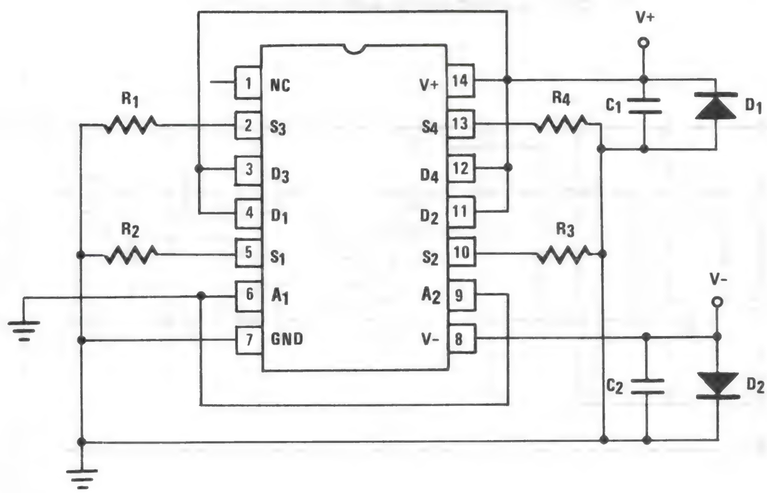
Test Waveforms





NOTES:
1. $R_L = 300\Omega$: $C_L = 33pF$
2. $V_{INH} = 15V$
   RISETIME (1.5V to 13.5V) $\leq$ 20ns
   FALLTIME (13.5V to 1.5V) $\leq$ 20ns

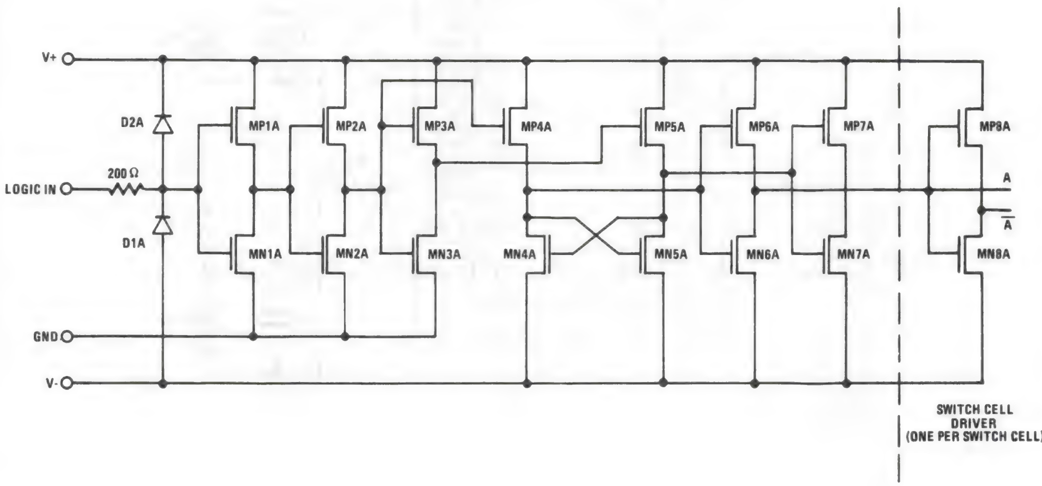
Burn-In Circuit



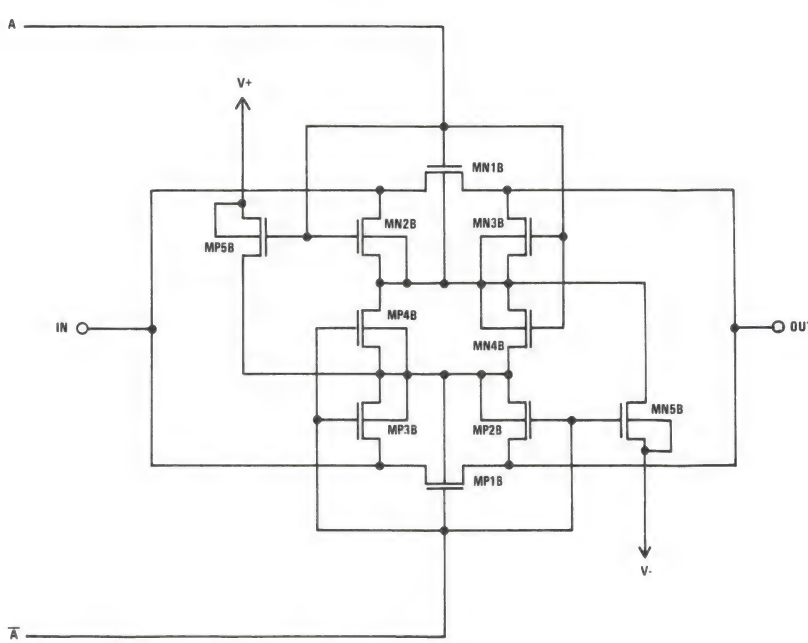
NOTES:
$R_1 = R_2 = R_3 = R_4 = 10K\Omega$, 5%, 1/4 or 1/2 watt
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2$ = IN4002 (per board)
$|(V+) - (V-)| = 30V$

Schematic Diagram

DIGITAL INPUT BUFFER AND LEVEL SHIFTER



SWITCH CELL



Die Characteristics

DIE DIMENSIONS:
76 x 83.9 x 19 mils

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

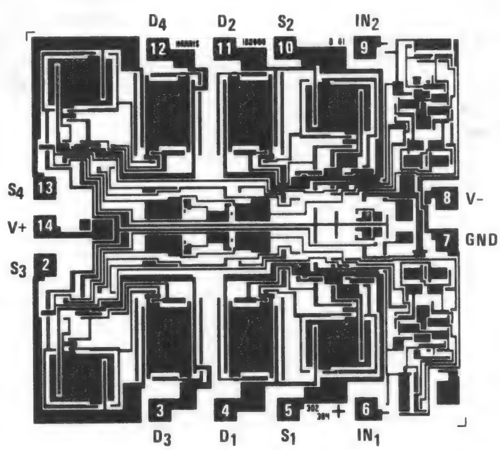
GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)

WORST CASE CURRENT DENSITY:
$3.9 \times 10^5 A/cm^2$ at 30mA
This device meets Glassivation Integrity Test requirement per Mil-Std-883 Method 2021 and Mil-M-38510 paragraph 3.5.5.4.

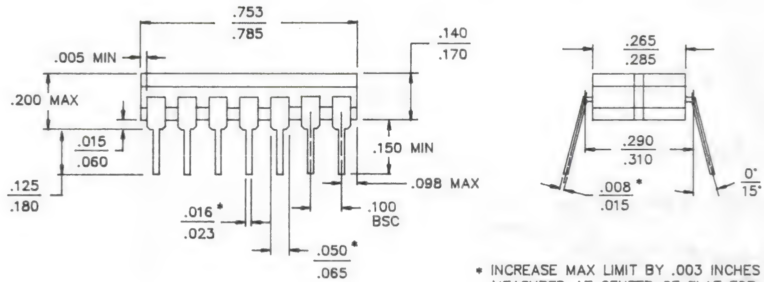
Metallization Mask Layout

HI-306/883



Packaging†

14 PIN CERAMIC DIP



* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-1

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

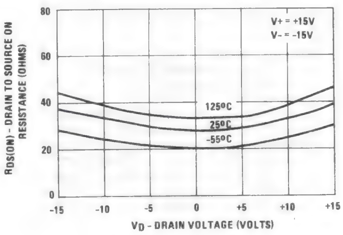
DESIGN INFORMATION

Dual DPST CMOS Analog Switch

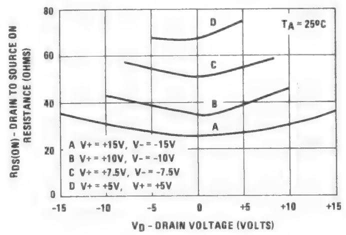
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics Unless Otherwise Specified: V+ = +15V, V- = -15V, T_A = +25°C

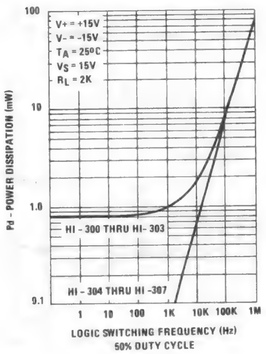
$R_{DS(ON)}$ vs. V_D AND TEMPERATURE



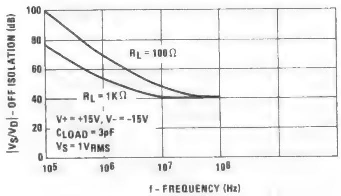
$R_{DS(ON)}$ vs. V_D AND POWER SUPPLY VOLTAGE



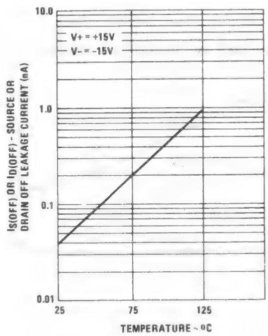
DEVICE POWER DISSIPATION vs. SWITCHING FREQUENCY SIGNAL LOGIC INPUT



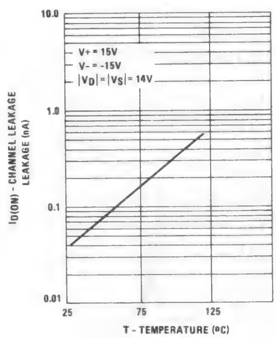
OFF ISOLATION vs. FREQUENCY



$I_{S(OFF)}$ or $I_{D(OFF)}$ vs. TEMPERATURE*



$I_{D(ON)}$ vs. TEMPERATURE*



* The net leakage into the source or drain is the N-channel leakage minus the P-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

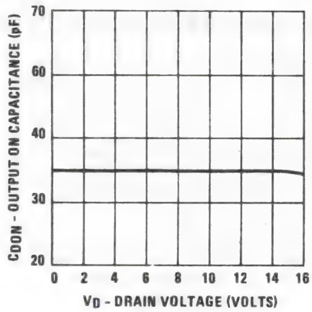
4 CMOS ANALOG SWITCHES

DESIGN INFORMATION (Continued)

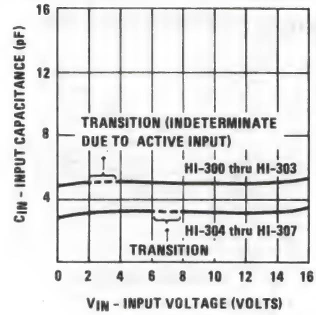
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics Unless Otherwise Specified: V+ = +15V, V- = -15V, T_A = +25°C

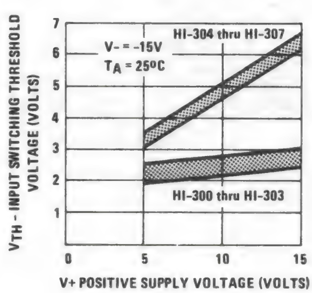
OUTPUT ON CAPACITANCE vs. DRAIN VOLTAGE



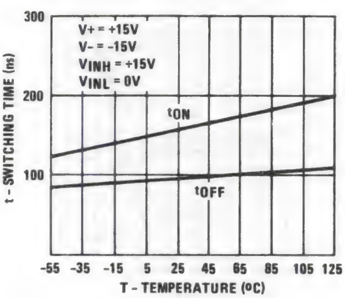
DIGITAL INPUT CAPACITANCE vs. INPUT VOLTAGE



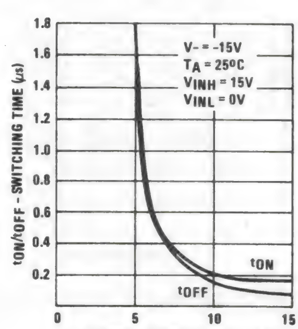
INPUT SWITCHING THRESHOLD vs. POSITIVE SUPPLY VOLTAGE



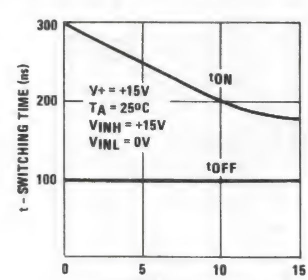
SWITCHING TIME vs. TEMPERATURE



SWITCHING TIME vs. POSITIVE SUPPLY VOLTAGE



SWITCHING TIME vs. NEGATIVE SUPPLY VOLTAGE



HARRIS HI-307/883

January 1989

Dual SPDT CMOS Analog Switch

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- Analog Signal Range (±15V Supplies) .... ±15V
- Low Leakage (+25^{o}C) .... 1nA (Max)
- Low Leakage (+125^{o}C) .... 100nA (Max)
- Low ON Resistance .... 50Ω (Max)
- Charge Injection .... 30pC (Typ)
- CMOS Compatible
- Symmetrical Switch Elements
- Low Operating Power
- Compatible with DG307

Applications

- Sample and Hold, i.e. Low Leakage Switching
- Op Amp Gain Switching, i.e. Low ON Resistance
- Portable, Battery Operated Circuits
- Low Level Switching Circuits
- Dual or Single Supply Systems

Description

The HI-307/883 switch is a monolithic device fabricated using CMOS technology and the Harris Dielectric Isolation process. This switch features break-before-make switching, low and nearly constant ON resistance over the full analog signal range, and low power dissipation.

The HI-307/883 is CMOS compatible and has a logic "0" condition with an input less than 3.5V and a logic "1" condition with an input greater than 11V.

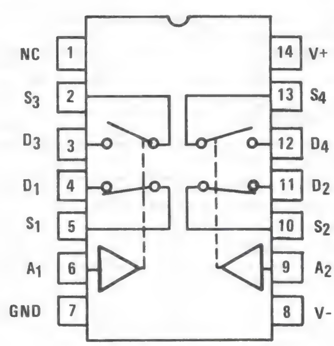
The HI-307/883 is pin-for-pin compatible with the industry standard Siliconix DG307. The device is available in a 14 pin Ceramic DIP. The HI-307/883 operates over the -55^{o}C to +125^{o}C temperature range.

4

CMOS ANALOG SWITCHES

Pinout

HI1-307/883 (CERAMIC DIP)
TOP VIEW



LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 44V
$\pm V_{SUPPLY}$ to Ground (V+, V-) .... ±22V
Analog Input Voltage $+V_S$ .... $+V_{SUPPLY}$ +1.5V
$-V_S$ .... $-V_{SUPPLY}$ -1.5V
Digital Input Voltage $+V_A$ .... $+V_{SUPPLY}$ +4V
$-V_A$ .... $-V_{SUPPLY}$ -4V
Peak Current (S or D)
(Pulse at 1ms, 10% Duty Cycle Max) 40mA
Continuous Current 30mA
Junction Temperature .... +175°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering 10 sec) .... ≤275°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	88°C/W	24°C/W

Package Power Dissipation at +75°C
Ceramic DIP Package 0.85W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 11.36mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) .... ±15V
Analog Input Voltage (V_S) .... $\pm V_{SUPPLY}$
Logic Low Level (V_{AL}) .... 0V to 3.5V
Logic High Level (V_{AH}) .... 11V to $+V_{SUPPLY}$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, GND = 0V, Unless Otherwise Specified

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch "ON" Resistance	R_{DS}	V_{A1} = 11V, V_D = 10V, I_S = -10mA V_{A2} = 3.5V S1/S2/S3/S4	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
		V_{A1} = 11V, V_D = -10V, I_S = 10mA V_{A2} = 3.5V S1/S2/S3/S4	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = +14V, V_D = -14V, V_{A1} = 3.5V V_{A2} = 11V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = -14V, V_D = +14V, V_{A1} = 3.5V V_{A2} = 11V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_S = -14V, V_D = +14V, V_{A1} = 3.5V V_{A2} = 11V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = +14V, V_D = -14V, V_{A1} = 3.5V V_{A2} = 11V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = +14V, V_{A1} = 11V V_{A2} = 3.5V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_D = V_S = -14V, V_{A1} = 11V V_{A2} = 3.5V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Low Level Input Current	I_{AL}	All Channels V_{AL} = 3.5V	1	+25°C	-1.0	1.0	μA
			2, 3	-55°C to +125°C	-1.0	1.0	μA
High Level Input Current	I_{AH}	All Channels V_{AH} = 11V	1	+25°C	-1.0	1.0	μA
			2, 3	-55°C to +125°C	-1.0	1.0	μA
Supply Current	$+I_{CC}$	All Channels V_A = 0V	1	+25°C	-	10	μA
			2, 3	-55°C to +125°C	-	100	μA
		All Channels V_A = 15V	1	+25°C	-	10	μA
			2, 3	-55°C to +125°C	-	100	μA
Supply Current	$-I_{CC}$	All Channels V_A = 0V	1	+25°C	-10	-	μA
			2, 3	-55°C to +125°C	-100	-	μA
		All Channels V_A = 15V	1	+25°C	-10	-	μA
			2, 3	-55°C to +125°C	-100	-	μA

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Turn "ON" Time	$t_{(ON)}$	$C_L = 33pF$ $R_L = 300\Omega$	9	+25°C	-	250	ns
			10, 11	-55°C, +125°C	-	500	ns
Turn "OFF" Time	$t_{(OFF)}$	$C_L = 33pF$ $R_L = 300\Omega$	9	+25°C	-	150	ns
			10, 11	-55°C, +125°C	-	450	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Characterized at: $+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch Input Capacitance	$C_{IS(OFF)}$	Measured Source to GND	1	+25°C	-	28	pF
Driver Input Capacitance	C_{C1}	$V_A = 0V$	1	+25°C	-	10	pF
	C_{C2}	$V_A = 15V$	1	+25°C	-	10	pF
Switch Output Capacitance	C_{OS}	Measured Drain to GND	1	+25°C	-	28	pF
Off Isolation	V_{ISO}	f = 1MHz, $V_{GEN} = 1V_{p-p}$	1	+25°C	40	-	dB
Crosstalk	V_{CT}	f = 1MHz, $V_{GEN} = 1V_{p-p}$	1	+25°C	40	-	dB
Charge Transfer	V_{CTE}	V_S = GND, $C_L = 0.01\mu F$	1	+25°C	-	15	mV

NOTE 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

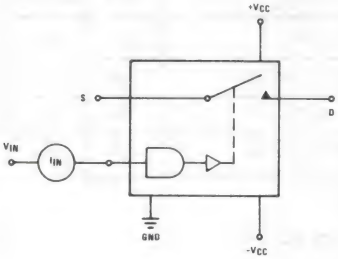
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

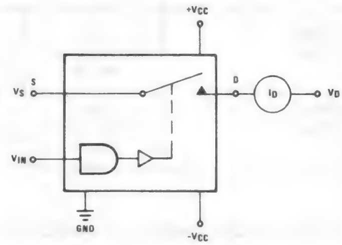
* PDA applies to Subgroup 1 only.

Test Circuits

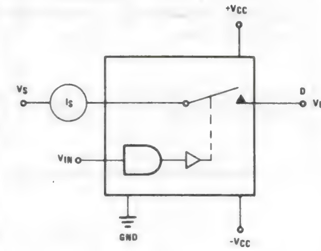
INPUT LEAKAGE CURRENT



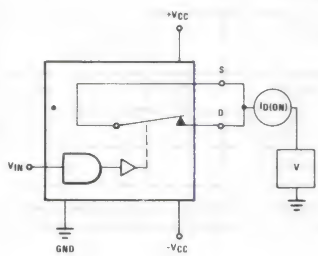
$I_{D(OFF)}$



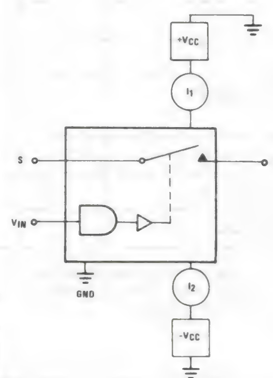
$I_{S(OFF)}$



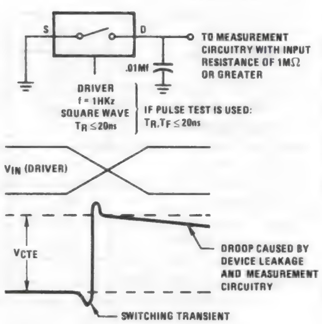
$I_{D(ON)}$



SUPPLY CURRENTS

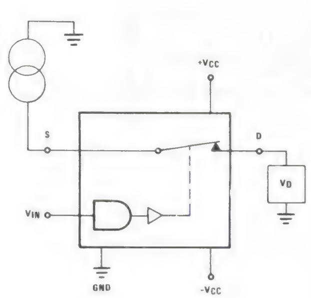


CHARGE TRANSFER ERROR

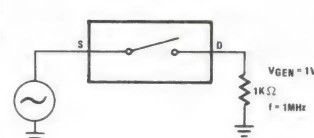


NOTE: V_{CTE} may be a positive or negative value

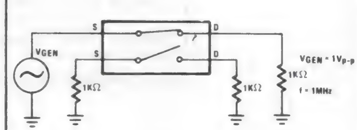
R_{DS}



OFF CHANNEL ISOLATION

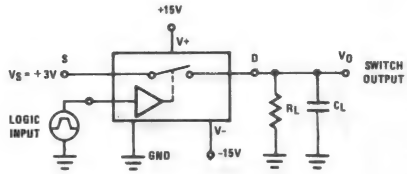


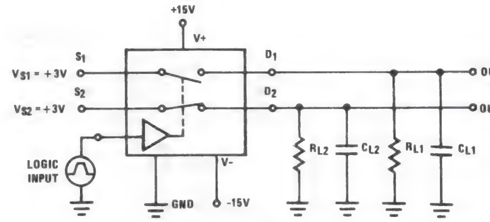
CROSSTALK BETWEEN CHANNELS

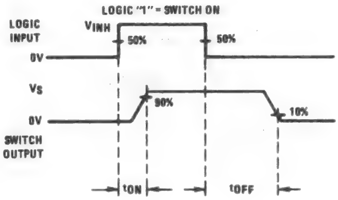


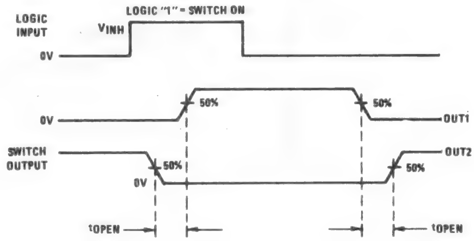
For Detail Information Refer to HI-307/883 Test Tech Brief

Test Waveforms







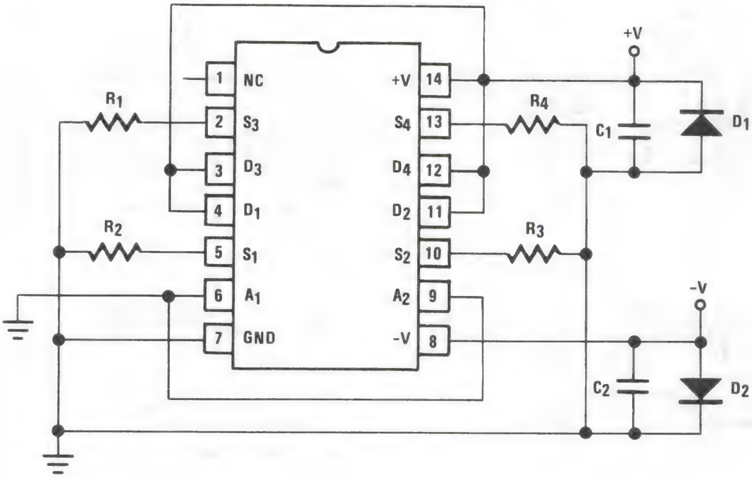


NOTES:

1. $R_L = R_L1 = R_L2 = 300\Omega$; $C_L = C_L1 = C_L2 = 33pF$
2. $V_{INH} = 15V$
   RISETIME (1.5V to 13.5V) $\leq$ 20ns
   FALLTIME (13.5V to 1.5V) $\leq$ 20ns

Burn-In Circuit

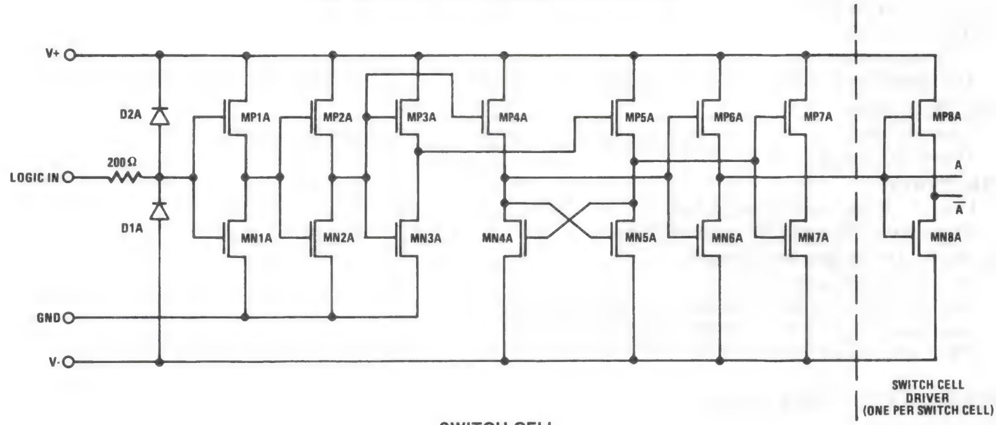
HI-307/883 CERAMIC DIP



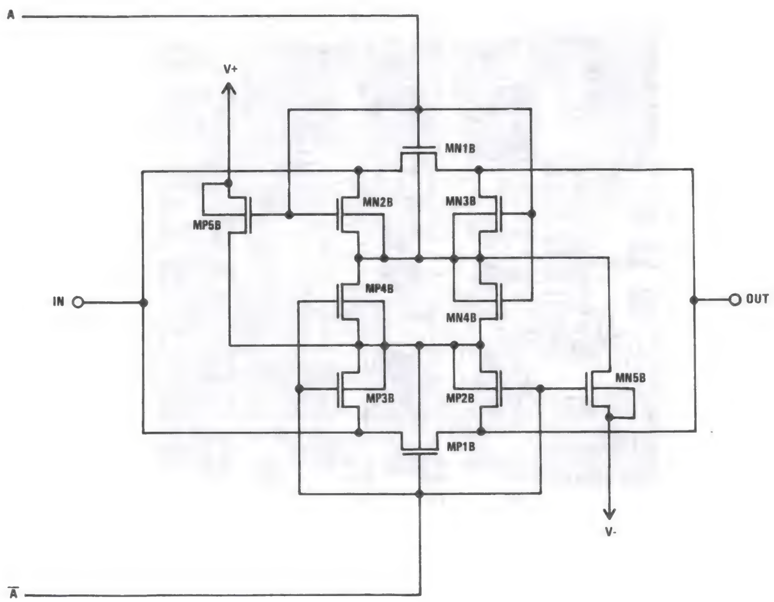
NOTES:
$R_1 = R_2 = R_3 = R_4 = 10K\Omega$, 5%, 1/4 or 1/2 watt
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2$ = IN4002 (per board)
$|(V+) - (V-)| = 30V$

Schematic Diagram

DIGITAL INPUT BUFFER AND LEVEL SHIFTER



SWITCH CELL



Die Characteristics

DIE DIMENSIONS:
76 x 83.9 x 19 mils

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

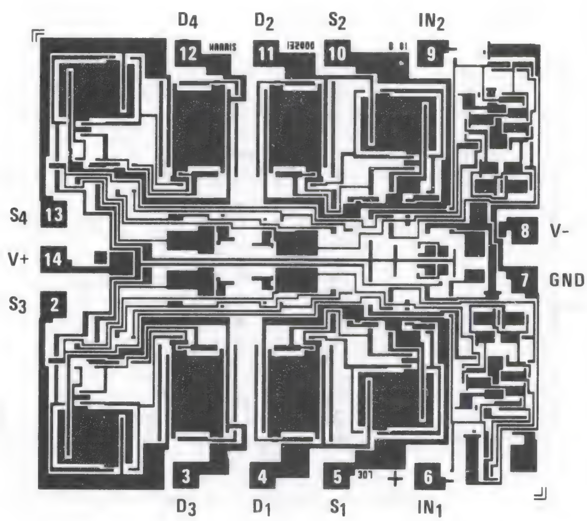
DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)

WORST CASE CURRENT DENSITY:
$3.9 \times 10^5 A/cm^2$ at 30mA

This device meets Glassivation Integrity Test requirement per Mil-Std-883 Method 2021 and Mil-M-38510 paragraph 3.5.5.4.

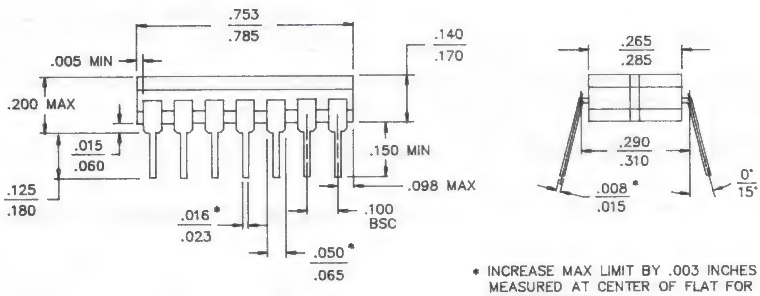
Metallization Mask Layout

HI-307/883



Packaging†

14 PIN CERAMIC DIP



* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-1

4

CMOS ANALOG SWITCHES

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

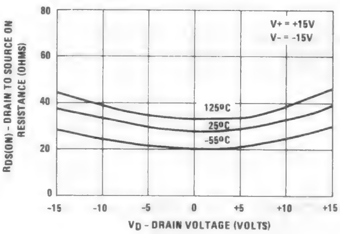
DESIGN INFORMATION

Dual SPDT CMOS Analog Switch

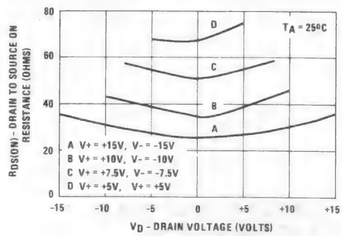
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics Unless Otherwise Specified: V+ = +15V, V- = -15V, T_A = +25°C

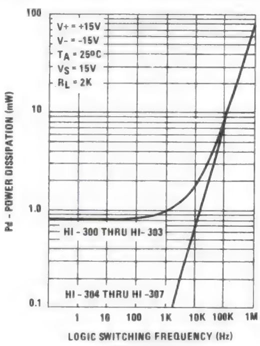
$R_{DS(ON)}$ vs. V_D AND TEMPERATURE



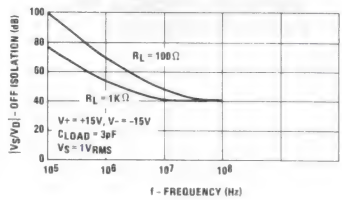
$R_{DS(ON)}$ vs. V_D AND POWER SUPPLY VOLTAGE



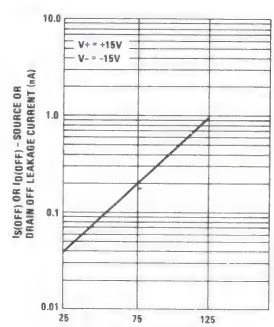
DEVICE POWER DISSIPATION vs. SWITCHING FREQUENCY SIGNAL LOGIC INPUT



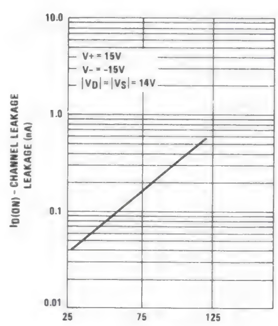
OFF ISOLATION vs. FREQUENCY



$I_{S(OFF)}$ or $I_{D(OFF)}$ vs. TEMPERATURE*



$I_{D(ON)}$ vs. TEMPERATURE*



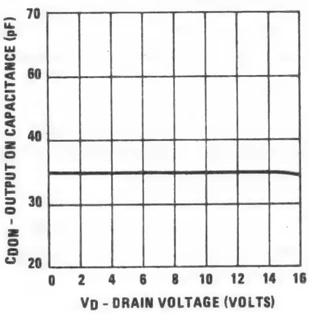
* The net leakage into the source or drain is the N-channel leakage minus the P-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

DESIGN INFORMATION (Continued)

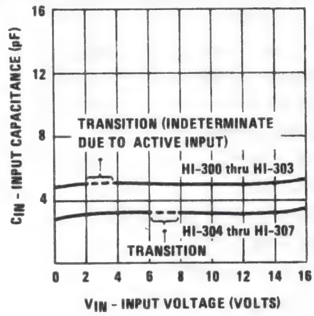
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics Unless Otherwise Specified: V+ = +15V, V- = -15V, T_A = +25°C

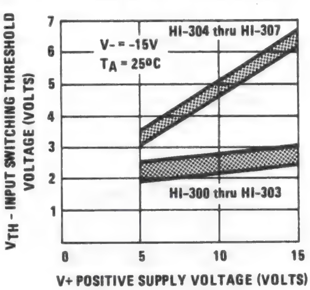
OUTPUT ON CAPACITANCE vs. DRAIN VOLTAGE



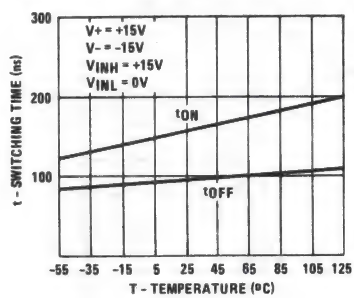
DIGITAL INPUT CAPACITANCE vs. INPUT VOLTAGE



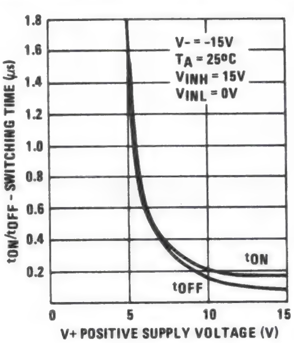
INPUT SWITCHING THRESHOLD vs. POSITIVE SUPPLY VOLTAGE



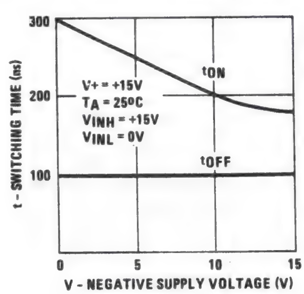
SWITCHING TIME vs. TEMPERATURE



SWITCHING TIME vs. POSITIVE SUPPLY VOLTAGE



SWITCHING TIME vs. NEGATIVE SUPPLY VOLTAGE



HARRIS

HI-381/883

January 1989

Dual SPST CMOS Analog Switch

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Analog Signal Range (±15V Supplies) .... ±15V
- Low Leakage (+25°C)....................................1nA (Max)
- Low Leakage (+125°C)..............................100nA (Max)
- Low ON Resistance...50Ω (Max)
- Charge Injection..30pC (Typ)
- TTL Compatible
- Symmetrical Switch Elements
- Low Operating Power
- Compatible with DG381

Applications

- Sample and Hold, i.e. Low Leakage Switching
- Op Amp Gain Switching, i.e. Low ON Resistance
- Portable, Battery Operated Circuits
- Low Level Switching Circuits
- Dual or Single Supply Systems

Description

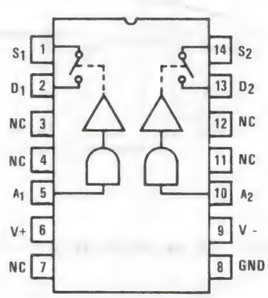
The HI-381/883 dual SPST switch is a monolithic device fabricated using CMOS technology and the Harris Dielectric Isolation process. This switch configuration is TTL compatible and is a pin-to-pin replacement for the DG381.

This switch features low leakage and supply currents, low and nearly constant ON resistance over the analog signal range, and low power dissipation.

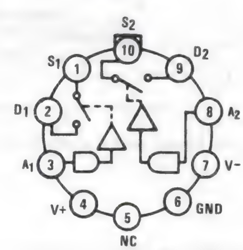
The HI-381/883 switch is available in a 14 pin Ceramic DIP or a 10 pin Metal Can and operates over the -55°C to +125°C temperature range.

Pinouts

HI1-381/883 (CERAMIC DIP)
TOP VIEW



HI2-381/883 (METAL CAN)
TOP VIEW



LOGIC	SW 1 SW 2
0	OFF
1	ON

*The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 44V
$\pm V_{SUPPLY}$ to Ground (V+, V-) .... ±22V
Analog Input Voltage $+V_S$ .... $+V_{SUPPLY}$ +1.5V
$-V_S$ .... $-V_{SUPPLY}$ -1.5V
Digital Input Voltage $+V_A$ .... $+V_{SUPPLY}$ +4V
$-V_A$ .... $-V_{SUPPLY}$ -4V
Peak Current (S or D)
(Pulse at 1ms, 10% Duty Cycle Max) 40mA
Continuous Current 30mA
Junction Temperature .... +175°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering 10 sec) .... ≤275°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	98°C/W	30°C/W
Metal Can Package	117°C/W	35°C/W

Package Power Dissipation at +75°C
Ceramic DIP Package 0.77W
Metal Can Package 0.64W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 10.32mW/°C
Metal Can Package .... 8.56mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) .... ±15V
Analog Input Voltage (V_S) .... $\pm V_{SUPPLY}$
Logic Low Level (V_{AL}) .... 0V to 0.8V
Logic High Level (V_{AH}) .... 4.0V to $+V_{SUPPLY}$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, GND = 0V, Unless Otherwise Specified

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch "ON" Resistance	R_{DS}	V_A = 0.8V, V_D = 10V, I_S = -10mA S1/S2	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
		V_A = 0.8V, V_D = -10V, I_S = 10mA S1/S2	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = +14V, V_D = -14V, V_A = 4.0V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = -14V, V_D = +14V, V_A = 4.0V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_S = +14V, V_D = -14V, V_A = 4.0V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = -14V, V_D = +14V, V_A = 4.0V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = +14V, V_A = 0.8V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_D = V_S = -14V, V_A = 0.8V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Low Level Input Current	I_{AL}	All Channels V_A = 0.8V	1	+25°C	-1.0	1.0	µA
			2, 3	-55°C to +125°C	-1.0	1.0	µA
High Level Input Current	I_{AH}	All Channels V_A = 4.0V	1	+25°C	-1.0	1.0	µA
			2, 3	-55°C to +125°C	-1.0	1.0	µA
Supply Current	$+I_{CC}$	All Channels V_A = 0.8V	1	+25°C	-	10	µA
			2, 3	-55°C to +125°C	-	100	µA
		V_{A1} = 4.0V, V_{A2} = 0V and V_{A1} = 0V, V_{A2} = 4.0V	1	+25°C	-	0.5	mA
			2, 3	-55°C to +125°C	-	1.0	mA
Supply Current	$-I_{CC}$	All Channels V_A = 0.8V	1	+25°C	-10	-	µA
			2, 3	-55°C to +125°C	-100	-	µA
		V_{A1} = 4.0V, V_{A2} = 0V and V_{A1} = 0V, V_{A2} = 4.0V	1	+25°C	-10	-	µA
			2, 3	-55°C to +125°C	-100	-	µA

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Turn "ON" Time	$t_{(ON)}$	$C_L = 33pF$ $R_L = 300\Omega$	9	$+25^oC$	-	300	ns
			10, 11	$-55^oC, +125^oC$	-	500	ns
Turn "OFF" Time	$t_{(OFF)}$	$C_L = 33pF$ $R_L = 300\Omega$	9	$+25^oC$	-	250	ns
			10, 11	$-55^oC, +125^oC$	-	450	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Characterized at: $+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch Input Capacitance	$C_{IS(OFF)}$	Measured Source to GND	1	$+25^oC$	-	28	pF
Driver Input Capacitance	C_{C1}	$V_A = 0V$	1	$+25^oC$	-	10	pF
	C_{C2}	$V_A = 15V$	1	$+25^oC$	-	10	pF
Switch Output Capacitance	C_{OS}	Measured Drain to GND	1	$+25^oC$	-	28	pF
Off Isolation	V_{ISO}	$f = 1MHz, V_{GEN} = 1V_{p-p}$	1	$+25^oC$	40	-	dB
Crosstalk	V_{CT}	$f = 1MHz, V_{GEN} = 1V_{p-p}$	1	$+25^oC$	40	-	dB
Charge Transfer	V_{CTE}	$V_S = GND, C_L = 0.01\mu F$	1	$+25^oC$	-	15	mV

NOTE 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

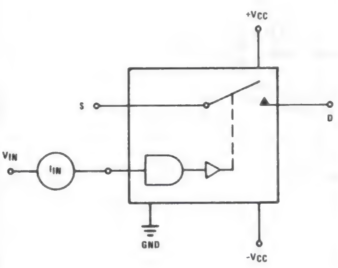
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

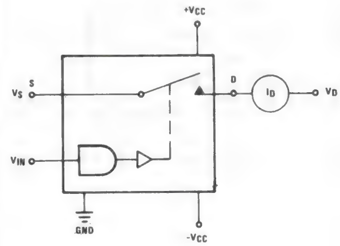
* PDA applies to Subgroup 1 only.

Test Circuits

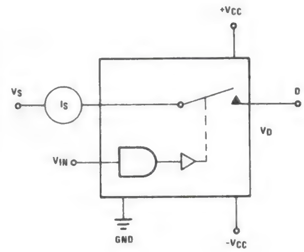
INPUT LEAKAGE CURRENT



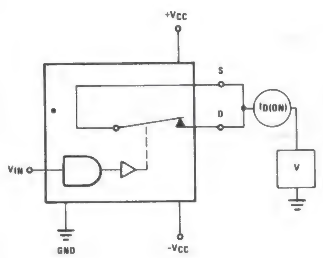
$I_{D(OFF)}$



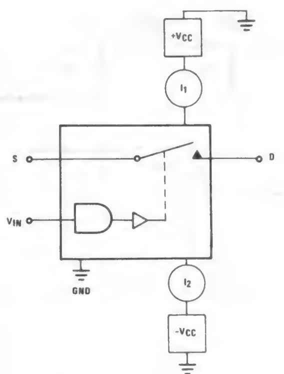
$I_{S(OFF)}$



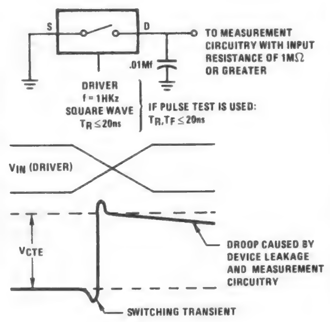
$I_{D(ON)}$



SUPPLY CURRENTS

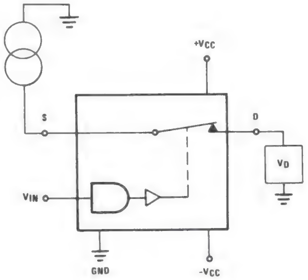


CHARGE TRANSFER ERROR

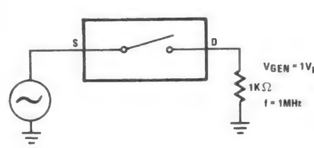


NOTE: V_{CTE} may be a positive or negative value

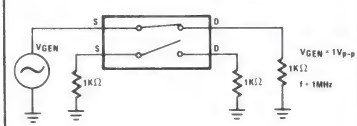
R_{DS}



OFF CHANNEL ISOLATION

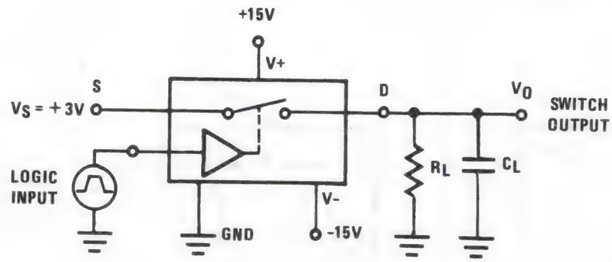


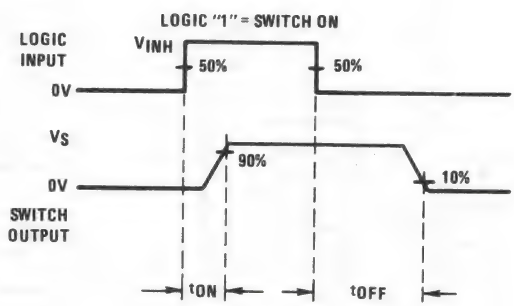
CROSSTALK BETWEEN CHANNELS



For Detail Information Refer to HI-381/883 Test Tech Brief

Test Waveforms

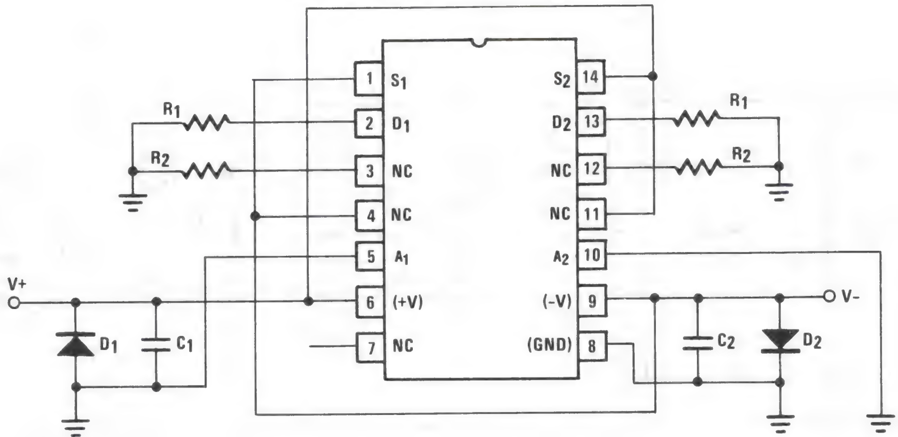




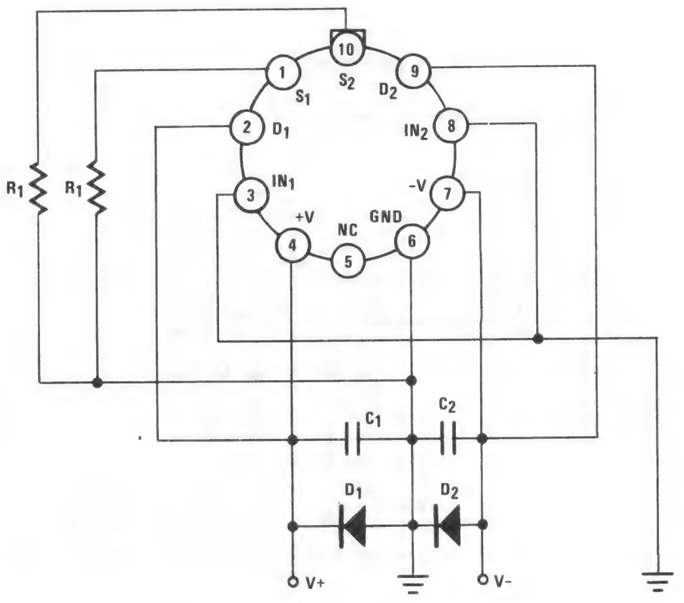
NOTES:
1. $R_L = 300\Omega$: $C_L = 33pF$
2. $V_{INH} = 4V$
   RISETIME (0.4V to 3.6V) $\leq$ 20ns
   FALLTIME (3.6V to 0.4V) $\leq$ 20ns

Burn-In Circuits

HI-381/883 CERAMIC DIP



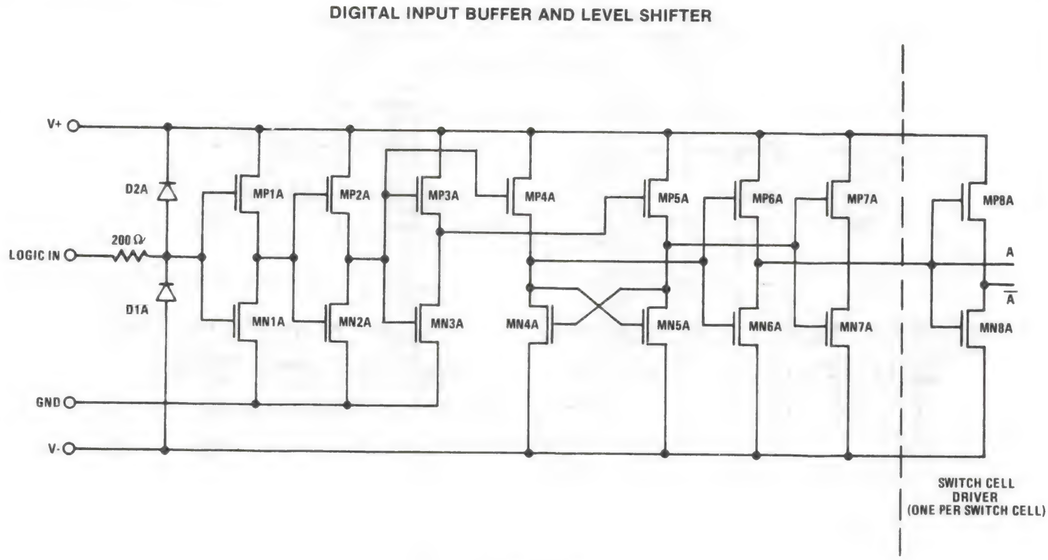
HI-381/883 METAL CAN

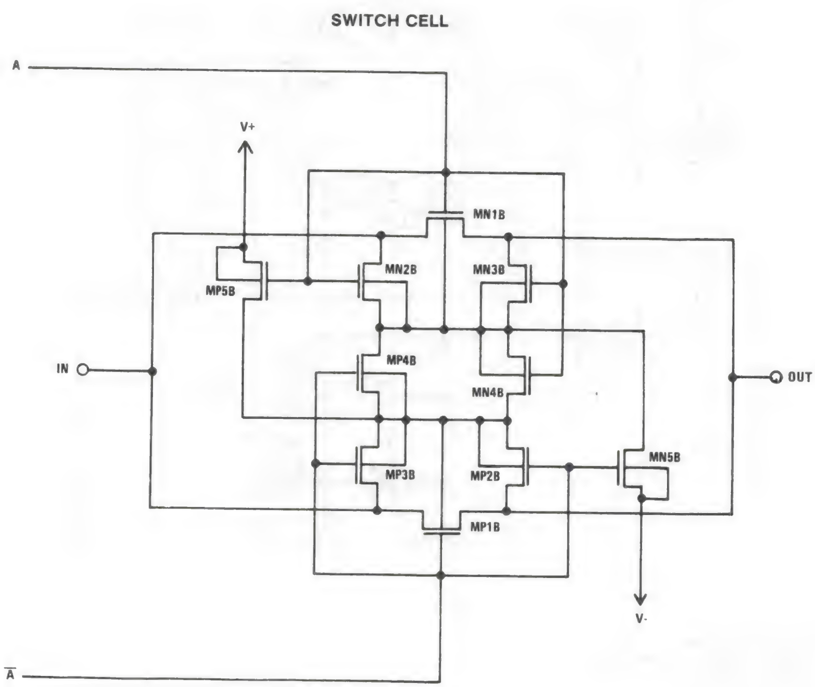


NOTES:
$R_1 = R_2 = 10K\Omega$, 5%, (per socket)
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2$ = IN4002 Equivalent (per board)
$|(V+) - (V-)| = 30V$

4
CMOS ANALOG SWITCHES

Schematic Diagram





Die Characteristics

DIE DIMENSIONS:
76 x 60.6 x 19 mils

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

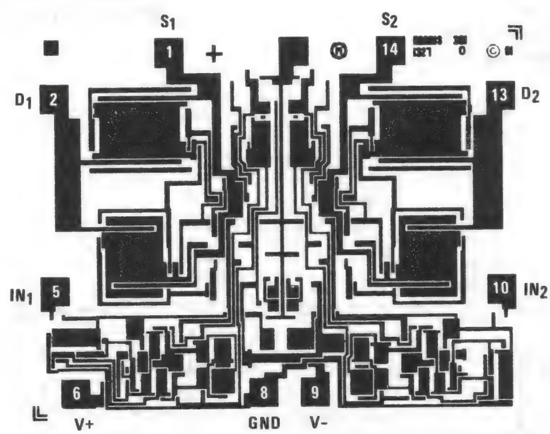
GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Metal Can — 420°C (Max)

WORST CASE CURRENT DENSITY:
$3.9 \times 10^5 A/cm^2$ at 20mA
This device meets Glassivation Integrity Test requirement per Mil-Std-883 Method 2021 and Mil-M-38510 paragraph 3.5.5.4.

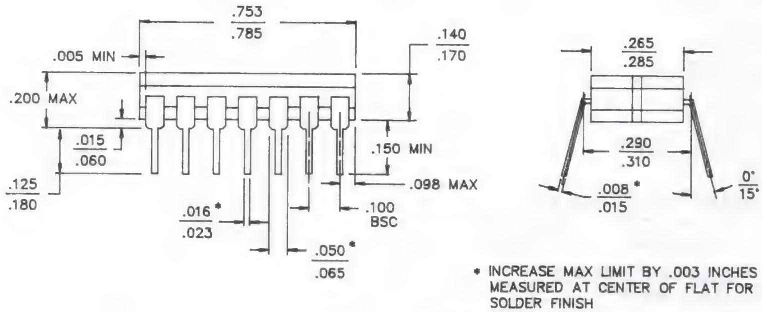
Metallization Mask Layout

HI-381/883



Packaging†

14 PIN CERAMIC DIP

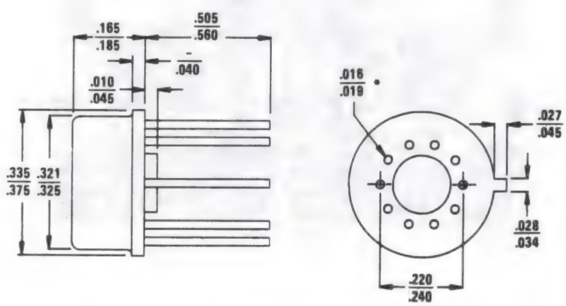


LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
- Material: Glass Frit
- Temperature: 450°C ± 10°C
- Method: Furnace Seal

INTERNAL LEAD WIRE:
- Material: Aluminum
- Diameter: 1.25 Mil
- Bonding Method: Ultrasonic

COMPLIANT OUTLINE: 38510 D-1

10 PIN METAL CAN



* Maximum Limits are Increased by 0.003 inches for Solder Dip Finish.

LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
- Material: No Seal Material
- Temperature: Room Temperature
- Method: Resistance Weld

INTERNAL LEAD WIRE:
- Material: Aluminum
- Diameter: 1.25 Mil
- Bonding Method: Ultrasonic

COMPLIANT OUTLINE: 38510 A-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

DESIGN INFORMATION

Dual SPST CMOS Analog Switch

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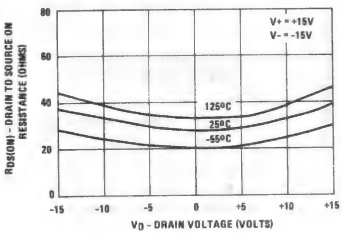
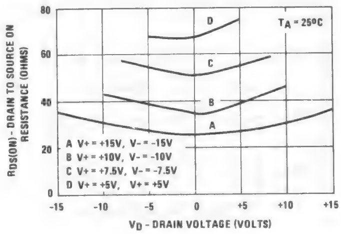
Typical Performance Characteristics Unless Otherwise Specified: V+ = +15V, V- = -15V, T_A = +25°C

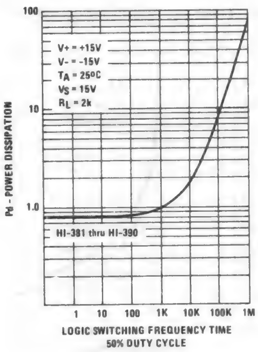
$R_{DS(ON)}$ vs. V_D AND TEMPERATURE



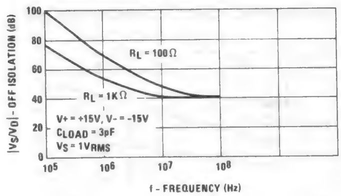
$R_{DS(ON)}$ vs. V_D AND POWER SUPPLY VOLTAGE



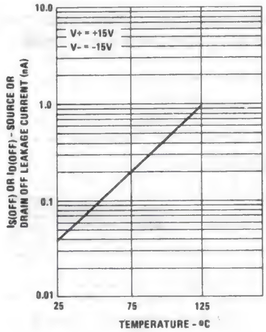
DEVICE POWER DISSIPATION vs. SWITCHING FREQUENCY SIGNAL LOGIC INPUT



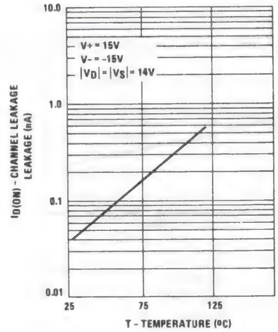
OFF ISOLATION vs. FREQUENCY



$I_{S(OFF)}$ or $I_{D(OFF)}$ vs. TEMPERATURE*



$I_{D(ON)}$ vs. TEMPERATURE*



* The net leakage into the source or drain is the N-channel leakage minus the P-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

DESIGN INFORMATION (Continued)

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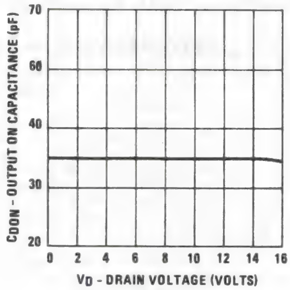
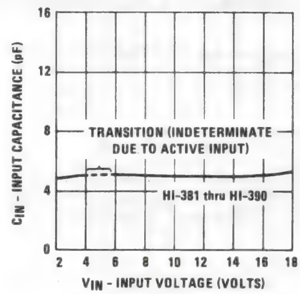
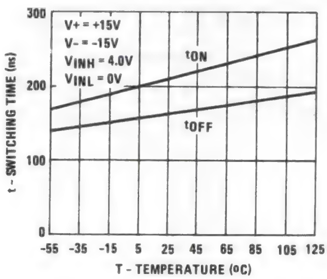
OUTPUT ON CAPACITANCE vs. DRAIN VOLTAGE



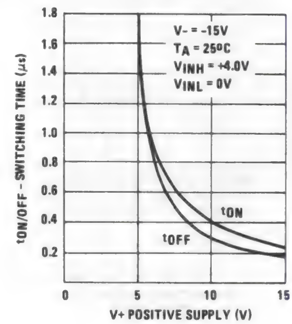
DIGITAL INPUT CAPACITANCE vs. INPUT VOLTAGE



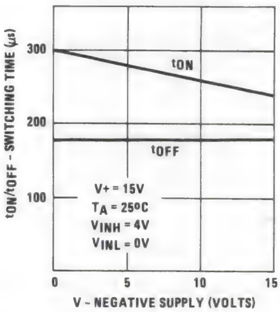
SWITCHING TIME vs. TEMPERATURE



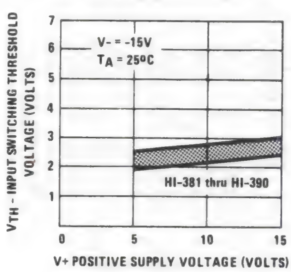
SWITCHING TIME vs. POSITIVE SUPPLY VOLTAGE



SWITCHING TIME vs. NEGATIVE SUPPLY VOLTAGE



INPUT SWITCHING THRESHOLD vs. POSITIVE SUPPLY VOLTAGE



HARRIS

HI-384/883

January 1989

Dual DPST CMOS Analog Switch

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Analog Signal Range (±15V Supplies) .... ±15V**
- **Low Leakage (+25°C) .... 1nA (Max)**
- **Low Leakage (+125°C) .... 100nA (Max)**
- **Low ON Resistance .... 50Ω (Max)**
- **Charge Injection .... 30pC (Typ)**
- **TTL Compatible**
- **Symmetrical Switch Elements**
- **Low Operating Power**
- **Compatible with DG384**

Applications

- **Sample and Hold, i.e. Low Leakage Switching**
- **Op Amp Gain Switching, i.e. Low ON Resistance**
- **Portable, Battery Operated Circuits**
- **Low Level Switching Circuits**
- **Dual or Single Supply Systems**

Description

The HI-384/883 dual DPST switch is a monolithic device fabricated using CMOS technology and the Harris Dielectric Isolation process. This switch configuration is TTL compatible and is a pin-to-pin replacement for the DG384.

This switch features low leakage and supply currents, low and nearly constant ON resistance over the analog signal range, and low power dissipation.

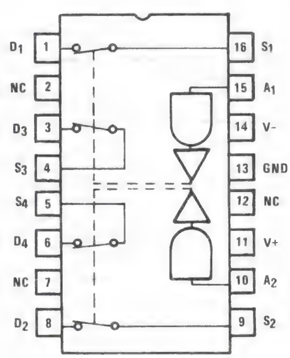
The HI-384/883 switch is available in a 16 pin Ceramic DIP and operates over the -55°C to +125°C temperature range.

4

CMOS ANALOG SWITCHES

Pinout

HI1-384/883 (CERAMIC DIP)
TOP VIEW



LOGIC	SW 1 - SW 4
0	OFF
1	ON

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 44V
$\pm V_{SUPPLY}$ to Ground (V+, V-) .... ±22V
Analog Input Voltage $+V_S$ .... $+V_{SUPPLY}$ +1.5V
$-V_S$ .... $-V_{SUPPLY}$ -1.5V
Digital Input Voltage $+V_A$ .... $+V_{SUPPLY}$ +4V
$-V_A$ .... $-V_{SUPPLY}$ -4V
Peak Current (S or D)
(Pulse at 1ms, 10% Duty Cycle Max) 40mA
Continuous Current 30mA
Junction Temperature .... +175°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering 10 sec) .... ≤275°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	88°C/W	24°C/W

Package Power Dissipation at +75°C
Ceramic DIP Package 0.85W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 11.36mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) .... ±15V
Analog Input Voltage (V_S) .... $\pm V_{SUPPLY}$
Logic Low Level (V_{AL}) .... 0V to 0.8V
Logic High Level (V_{AH}) .... 4.0V to $+V_{SUPPLY}$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, GND = 0V, Unless Otherwise Specified

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch "ON" Resistance	R_{DS}	V_A = 4.0V, V_D = 10V, I_S = -10mA S1/S2/S3/S4	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
		V_A = 4.0V, V_D = -10V, I_S = 10mA S1/S2/S3/S4	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = +14V, V_D = -14V, V_A = 0.8V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = -14V, V_D = +14V, V_A = 0.8V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_S = +14V, V_D = -14V, V_A = 0.8V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = -14V, V_D = +14V, V_A = 0.8V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = ±14V, V_A = 4.0V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_D = V_S = ±14V, V_A = 4.0V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Low Level Input Current	I_{AL}	All Channels V_A = 0.8V	1	+25°C	-1.0	1.0	μA
			2, 3	-55°C to +125°C	-1.0	1.0	μA
High Level Input Current	I_{AH}	All Channels V_A = 4.0V	1	+25°C	-1.0	1.0	μA
			2, 3	-55°C to +125°C	-1.0	1.0	μA
Supply Current	$+I_{CC}$	All Channels V_A = 0.8V	1	+25°C	-	10	μA
			2, 3	-55°C to +125°C	-	100	μA
		V_{A1} = 0V, V_{A2} = 4.0V and V_{A1} = 4.0V, V_{A2} = 0V	1	+25°C	-	0.5	mA
			2, 3	-55°C to +125°C	-	1.0	mA
Supply Current	$-I_{CC}$	All Channels V_A = 0.8V	1	+25°C	-10	-	μA
			2, 3	-55°C to +125°C	-100	-	μA
		V_{A1} = 0V, V_{A2} = 4.0V and V_{A1} = 4.0V, V_{A2} = 0V	1	+25°C	-10	-	μA
			2, 3	-55°C to +125°C	-100	-	μA

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Turn "ON" Time	$t_{(ON)}$	$C_L = 33pF$, $R_L = 300\Omega$	9	+25°C	-	300	ns
			10, 11	-55°C, +125°C	-	500	ns
Turn "OFF" Time	$t_{(OFF)}$	$C_L = 33pF$, $R_L = 300\Omega$	9	+25°C	-	250	ns
			10, 11	-55°C, +125°C	-	450	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Characterized at: $+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch Input Capacitance	$C_{IS(OFF)}$	Measured Source to GND	1	+25°C	-	28	pF
Driver Input Capacitance	C_{C1}	$V_A = 0V$	1	+25°C	-	10	pF
	C_{C2}	$V_A = 15V$	1	+25°C	-	10	pF
Switch Output Capacitance	C_{OS}	Measured Drain to GND	1	+25°C	-	28	pF
Off Isolation	V_{ISO}	f = 1MHz, $V_{GEN} = 1V_{p-p}$	1	+25°C	40	-	dB
Crosstalk	V_{CT}	f = 1MHz, $V_{GEN} = 1V_{p-p}$	1	+25°C	40	-	dB
Charge Transfer	V_{CTE}	V_S = GND, $C_L = 0.01\mu F$	1	+25°C	-	15	mV

NOTE 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

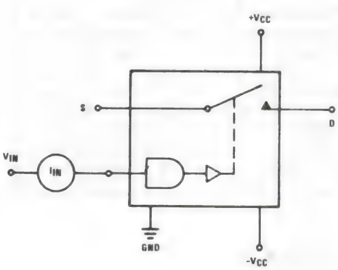
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

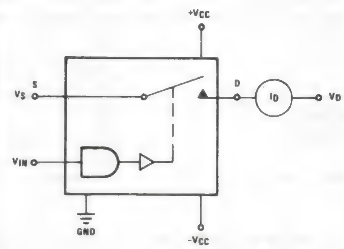
* PDA applies to Subgroup 1 only.

Test Circuits

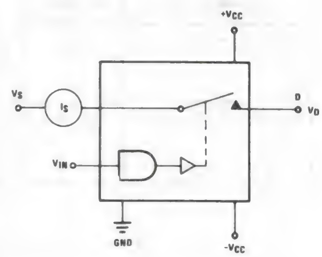
INPUT LEAKAGE CURRENT



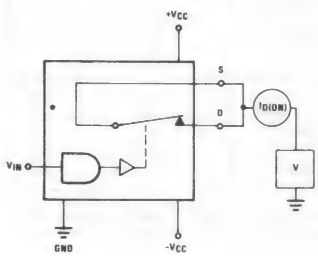
$I_{D(OFF)}$



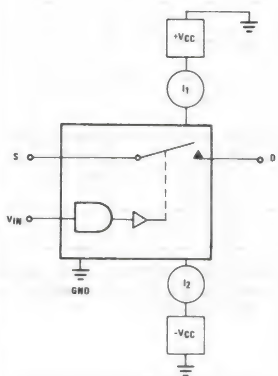
$I_{S(OFF)}$



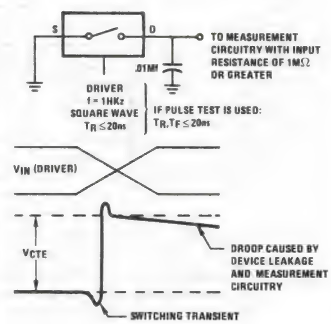
$I_{D(ON)}$



SUPPLY CURRENTS

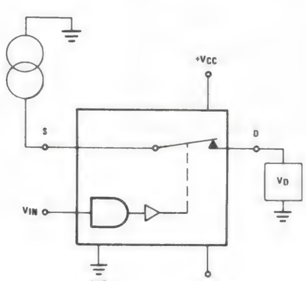


CHARGE TRANSFER ERROR

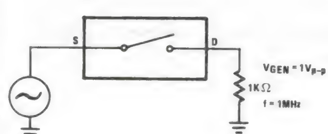


NOTE: V_{CTE} may be a positive or negative value

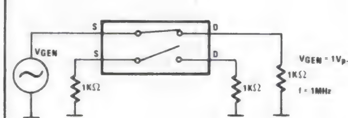
R_{DS}



OFF CHANNEL ISOLATION

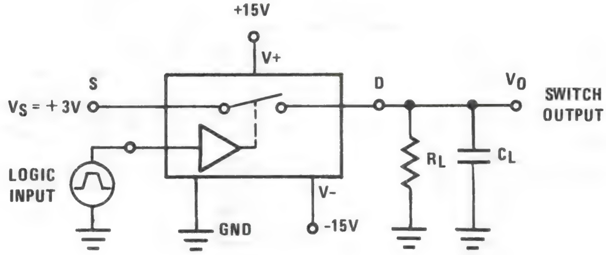


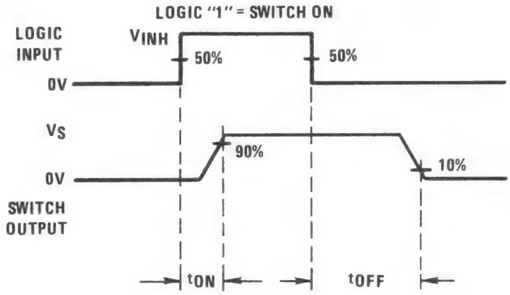
CROSSTALK BETWEEN CHANNELS



For Detail Information Refer to HI-384/883 Test Tech Brief

Test Waveforms

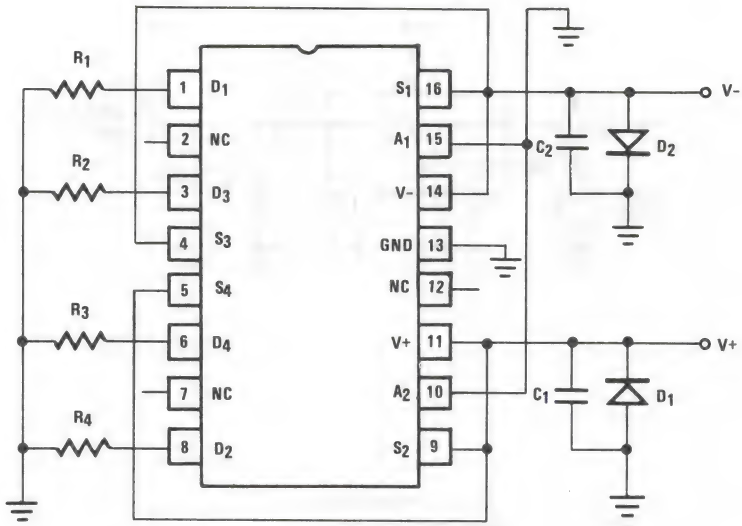




NOTES:
1. $R_L = 300\Omega$: $C_L = 33pF$
2. $V_{INH} = 4V$
   RISETIME (0.4V to 3.6V) $\leq$ 20ns
   FALLTIME (3.6V to 0.4V) $\leq$ 20ns

Burn-In Circuit

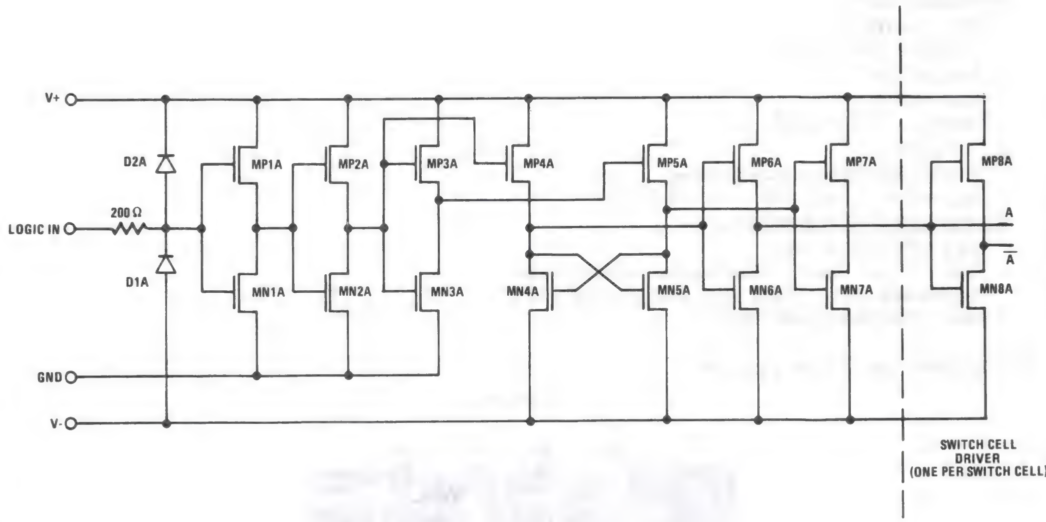
HI-384/883 CERAMIC DIP



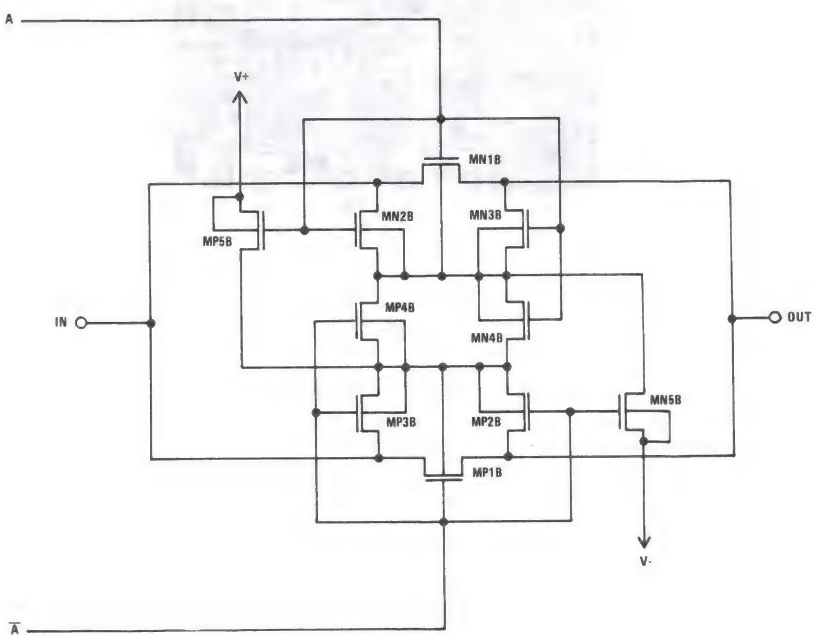
NOTES:
$R_1 = R_2 = R_3 = R_4 = 10k\Omega$, 5%, 1/4 or 1/2 watt
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2$ = IN4002 or Equivalent (per board)
$|(V+) - (V-)| = 30V$

Schematic Diagram

DIGITAL INPUT BUFFER AND LEVEL SHIFTER



SWITCH CELL



Die Characteristics

DIE DIMENSIONS:
76 x 83.9 x 19 mils

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

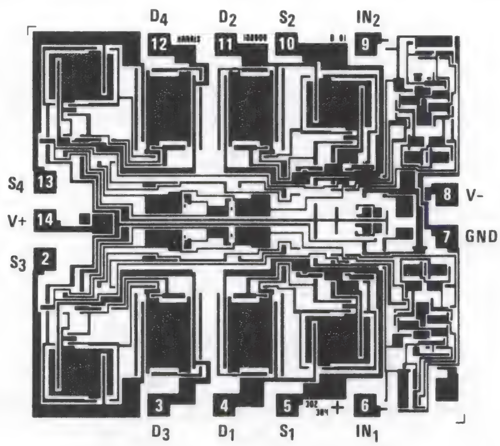
GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)

WORST CASE CURRENT DENSITY:
$3.9 \times 10^5 A/cm^2$ at 30mA
This device meets Glassivation Integrity Test requirement per Mil-Std-883 Method 2021 and Mil-M-38510 paragraph 3.5.5.4.

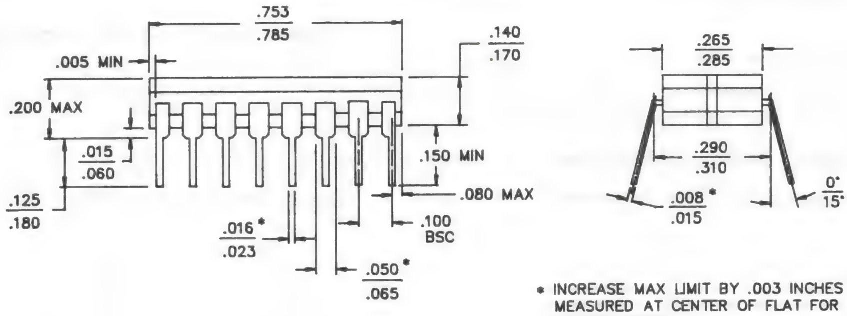
Metallization Mask Layout

HI-384/883



Packaging†

16 PIN CERAMIC DIP



* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

HI-384

DESIGN INFORMATION

Dual DPST CMOS Analog Switch

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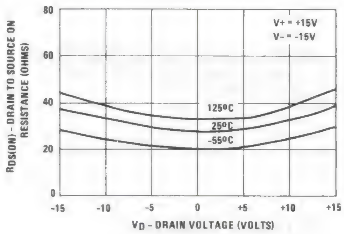
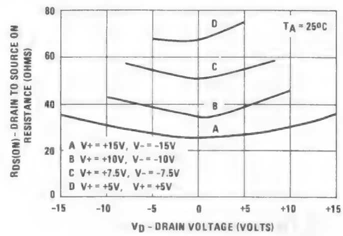
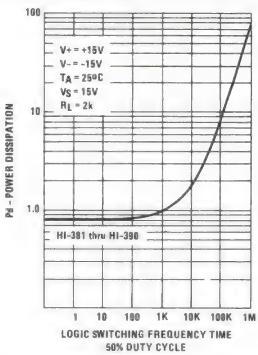
$R_{DS(ON)}$ vs. V_D AND TEMPERATURE



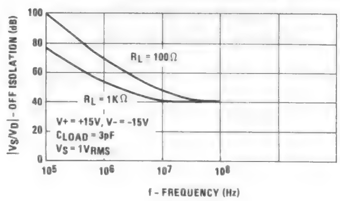
$R_{DS(ON)}$ vs. V_D AND POWER SUPPLY VOLTAGE



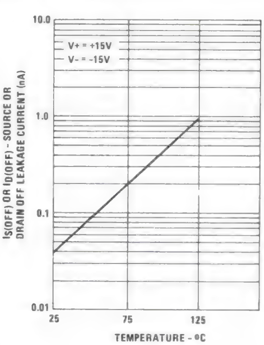
DEVICE POWER DISSIPATION vs.
SWITCHING FREQUENCY SIGNAL LOGIC INPUT



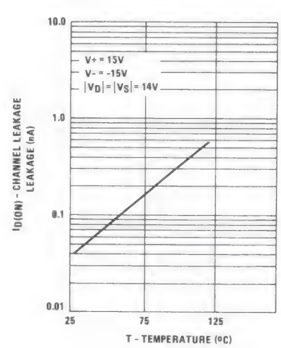
OFF ISOLATION vs. FREQUENCY



$I_{S(OFF)}$ or $I_{D(OFF)}$ vs. TEMPERATURE*



$I_{D(ON)}$ vs. TEMPERATURE*



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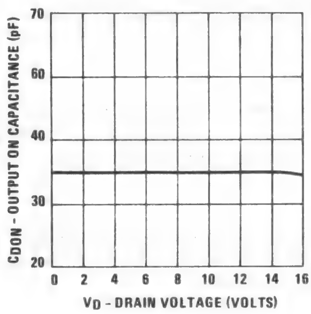
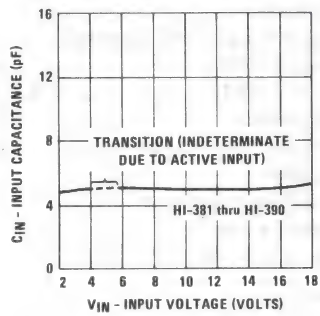
Typical Performance Characteristics Unless Otherwise Specified: V+ = +15V, V- = -15V, T_A = +25°C

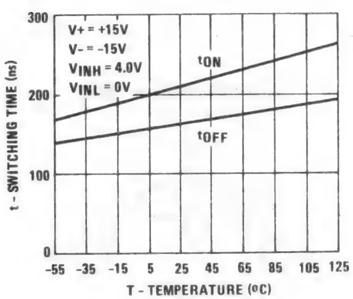
OUTPUT ON CAPACITANCE vs. DRAIN VOLTAGE



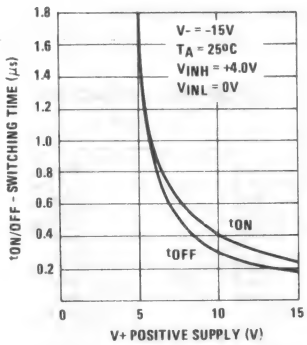
DIGITAL INPUT CAPACITANCE vs. INPUT VOLTAGE



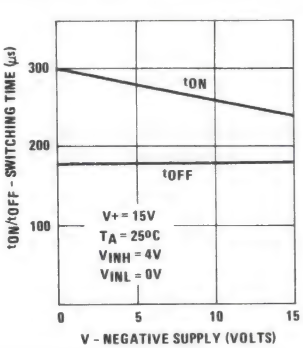
SWITCHING TIME vs. TEMPERATURE



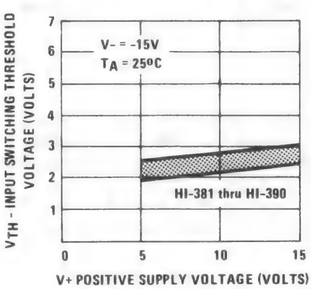
SWITCHING TIME vs. POSITIVE SUPPLY VOLTAGE



SWITCHING TIME vs. NEGATIVE SUPPLY VOLTAGE



INPUT SWITCHING THRESHOLD vs. POSITIVE SUPPLY VOLTAGE



HI-387/883

January 1989

SPDT CMOS Analog Switch

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Analog Signal Range (±15V Supplies) .... ±15V
- Low Leakage (+25°C) .... 1nA (Max)
- Low Leakage (+125°C) .... 100nA (Max)
- Low ON Resistance .... 50Ω (Max)
- Charge Injection .... 30pC (Typ)
- TTL Compatible
- Symmetrical Switch Elements
- Low Operating Power
- Compatible with DG387

Applications

- Sample and Hold, i.e. Low Leakage Switching
- Op Amp Gain Switching, i.e. Low ON Resistance
- Portable, Battery Operated Circuits
- Low Level Switching Circuits
- Dual or Single Supply Systems

Description

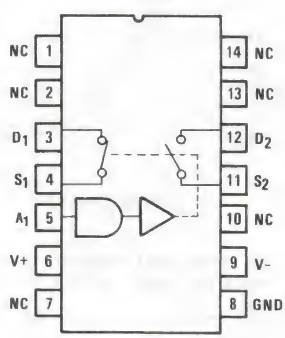
The HI-387/883 SPDT switch is a monolithic device fabricated using CMOS technology and the Harris Dielectric Isolation process. This switch configuration is TTL compatible and is a pin-to-pin replacement for the DG387.

This switch features low leakage and supply currents, low and nearly constant ON resistance over the analog signal range, break-before-make switching and low power dissipation.

The HI-387/883 switch is available in a 14 pin Ceramic DIP or a 10 pin Metal Can and operates over the -55°C to +125°C temperature range.

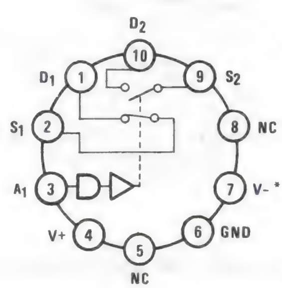
Pinouts

HI1-387/883 (CERAMIC DIP)
TOP VIEW



LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

HI2-387/883 (METAL CAN)
TOP VIEW



*The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 44V
$\pm V_{SUPPLY}$ to Ground (V+, V-) .... ±22V
Analog Input Voltage $+V_S$ .... $+V_{SUPPLY}$ +1.5V
$-V_S$ .... $-V_{SUPPLY}$ -1.5V
Digital Input Voltage $+V_A$ .... $+V_{SUPPLY}$ +4V
$-V_A$ .... $-V_{SUPPLY}$ -4V
Peak Current (S or D)
(Pulse at 1ms, 10% Duty Cycle Max) 40mA
Continuous Current 30mA
Junction Temperature .... +175°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering 10 sec) .... ≤275°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	98°C/W	30°C/W
Metal Can Package	117°C/W	35°C/W

Package Power Dissipation at +75°C
Ceramic DIP Package 0.77W
Metal Can Package 0.64W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 10.32mW/°C
Metal Can Package .... 8.56mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) .... ±15V
Analog Input Voltage (V_S) .... $\pm V_{SUPPLY}$
Logic Low Level (V_{AL}) .... 0V to 0.8V
Logic High Level (V_{AH}) .... 4.0V to $+V_{SUPPLY}$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, GND = 0V, Unless Otherwise Specified

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	MAX	UNITS
Switch "ON" Resistance	R_{DS}	V_A = 4.0V, V_D = 10V, I_S = -10mA S1/S2	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
		V_A = 4.0V, V_D = -10V, I_S = 10mA S1/S2	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = +14V, V_D = -14V, V_A = 0.8V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = -14V, V_D = +14V, V_A = 0.8V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_S = +14V, V_D = -14V, V_A = 0.8V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = -14V, V_D = +14V, V_A = 0.8V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = +14V, V_A = 4.0V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_D = V_S = -14V, V_A = 4.0V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Low Level Input Current	I_{AL}	All Channels V_A = 0.8V	1	+25°C	-1.0	1.0	μA
			2, 3	-55°C to +125°C	-1.0	1.0	μA
High Level Input Current	I_{AH}	All Channels V_A = 4.0V	1	+25°C	-1.0	1.0	μA
			2, 3	-55°C to +125°C	-1.0	1.0	μA
Supply Current	$+I_{CC}$	All Channels V_A = 0.8V	1	+25°C	-	10	μA
			2, 3	-55°C to +125°C	-	100	μA
		V_A = 4.0V	1	+25°C	-	0.5	mA
			2, 3	-55°C to +125°C	-	1.0	mA
Supply Current	$-I_{CC}$	All Channels V_A = 0.8V	1	+25°C	-10	-	μA
			2, 3	-55°C to +125°C	-100	-	μA
		V_A = 4.0V	1	+25°C	-10	-	μA
			2, 3	-55°C to +125°C	-100	-	μA

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Turn "ON" Time	$t_{(ON)}$	$C_L = 33pF$, $R_L = 300\Omega$	9	+25°C	-	300	ns
			10, 11	-55°C, +125°C	-	500	ns
Turn "OFF" Time	$t_{(OFF)}$	$C_L = 33pF$, $R_L = 300\Omega$	9	+25°C	-	250	ns
			10, 11	-55°C, +125°C	-	450	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Characterized at: $+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch Input Capacitance	$C_{IS(OFF)}$	Measured Source to GND	1	+25°C	-	28	pF
Driver Input Capacitance	C_{C1}	$V_A = 0V$	1	+25°C	-	10	pF
	C_{C2}	$V_A = 15V$	1	+25°C	-	10	pF
Switch Output Capacitance	C_{OS}	Measured Drain to GND	1	+25°C	-	28	pF
Off Isolation	V_{ISO}	f = 1MHz, $V_{GEN} = 1V_{p-p}$	1	+25°C	40	-	dB
Crosstalk	V_{CT}	f = 1MHz, $V_{GEN} = 1V_{p-p}$	1	+25°C	40	-	dB
Charge Transfer	V_{CTE}	V_S = GND, $C_L = 0.01\mu F$	1	+25°C	-	15	mV

NOTE 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

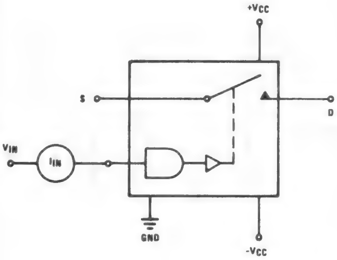
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

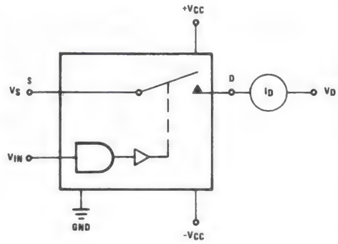
* PDA applies to Subgroup 1 only.

Test Circuits

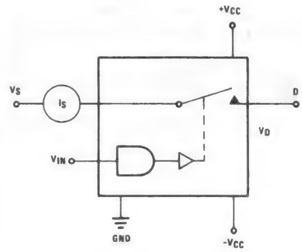
INPUT LEAKAGE CURRENT



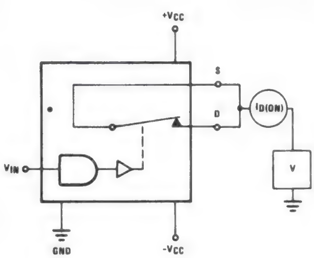
ID(OFF)



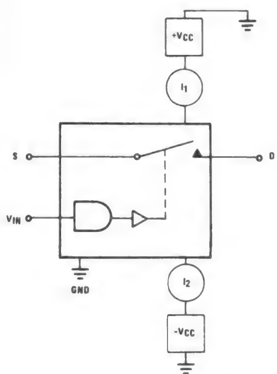
IS(OFF)



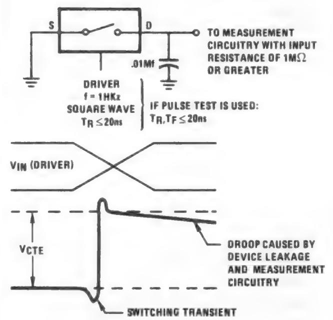
ID(ON)



SUPPLY CURRENTS

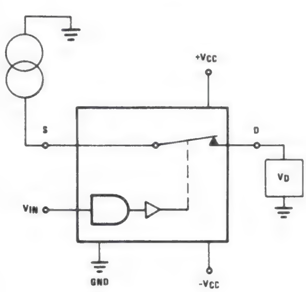


CHARGE TRANSFER ERROR

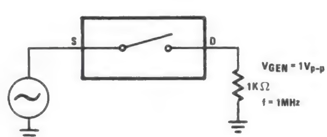


NOTE: V_{CTE} may be a positive or negative value

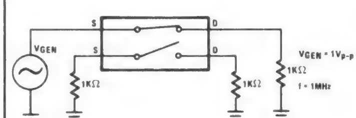
RDS



OFF CHANNEL ISOLATION

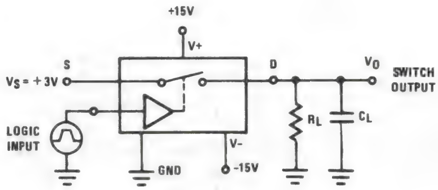


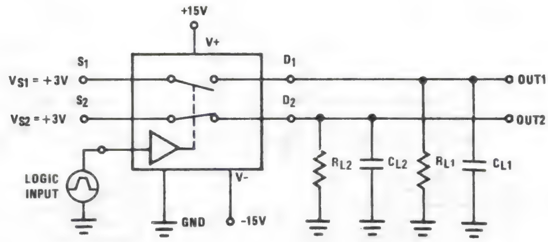
CROSSTALK BETWEEN CHANNELS

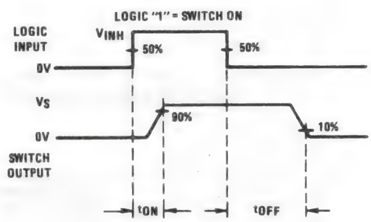


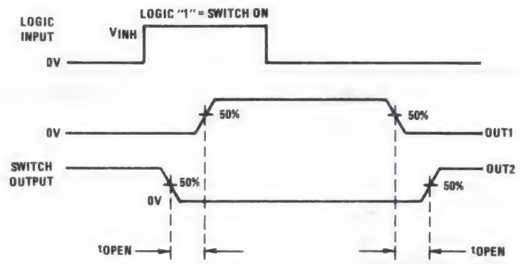
For Detail Information Refer to HI-387/883 Test Tech Brief

Test Waveforms







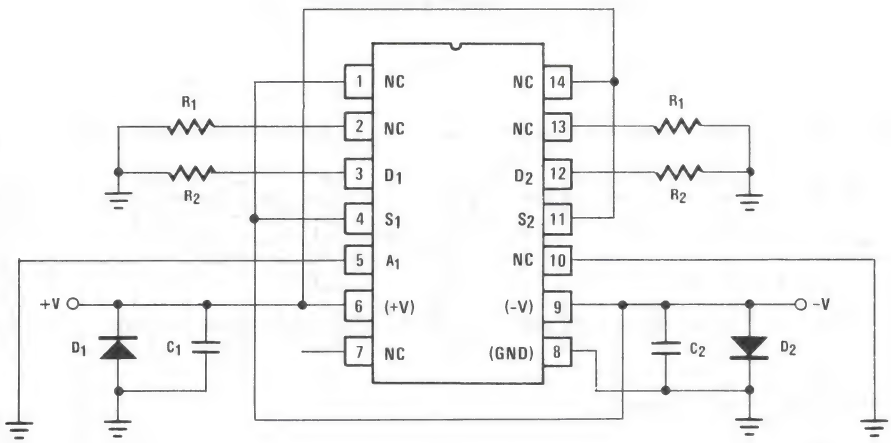


NOTES:

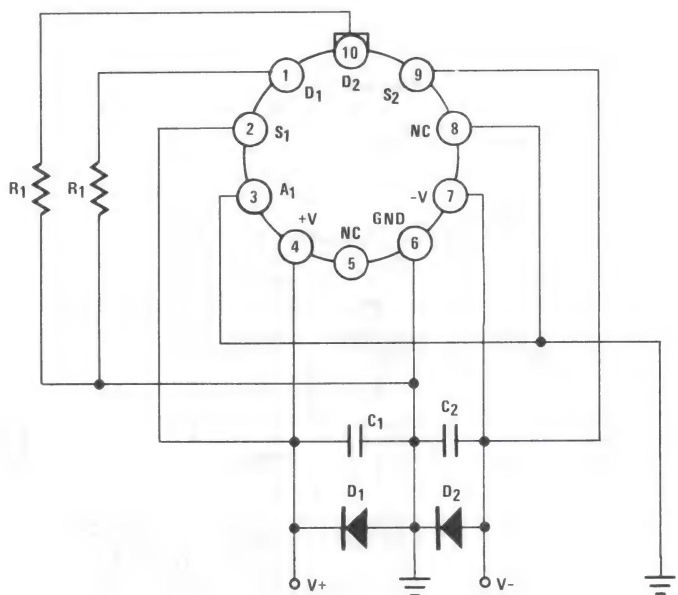
1. $R_L = R_L1 = R_L2 = 300\Omega$; $C_L = C_L1 = C_L2 = 33pF$
2. $V_{INH} = 4V$
   RISETIME (0.4V to 3.6V) $\leq$ 20ns
   FALLTIME (3.6V to 0.4V) $\leq$ 20ns

Burn-In Circuits

HI-387/883 CERAMIC DIP



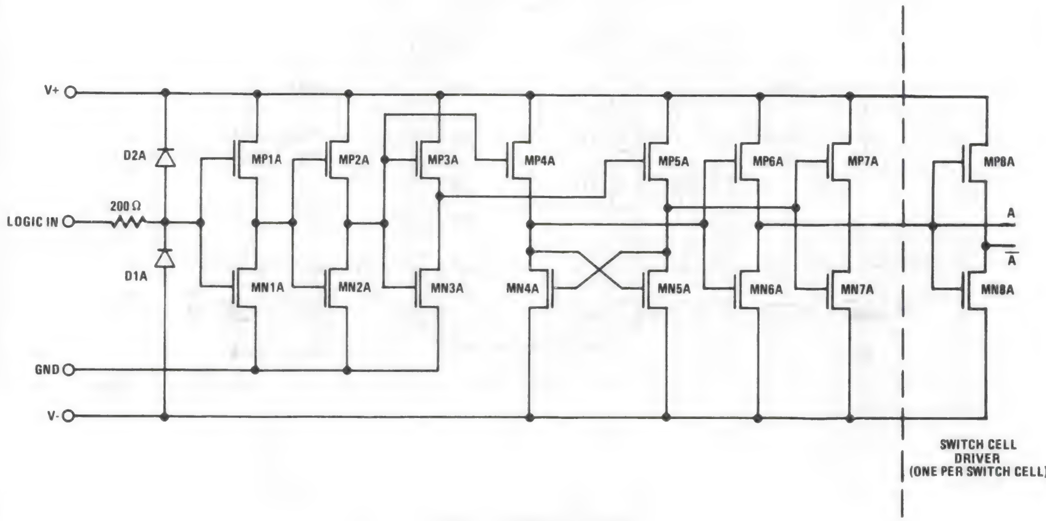
HI-387/883 METAL CAN



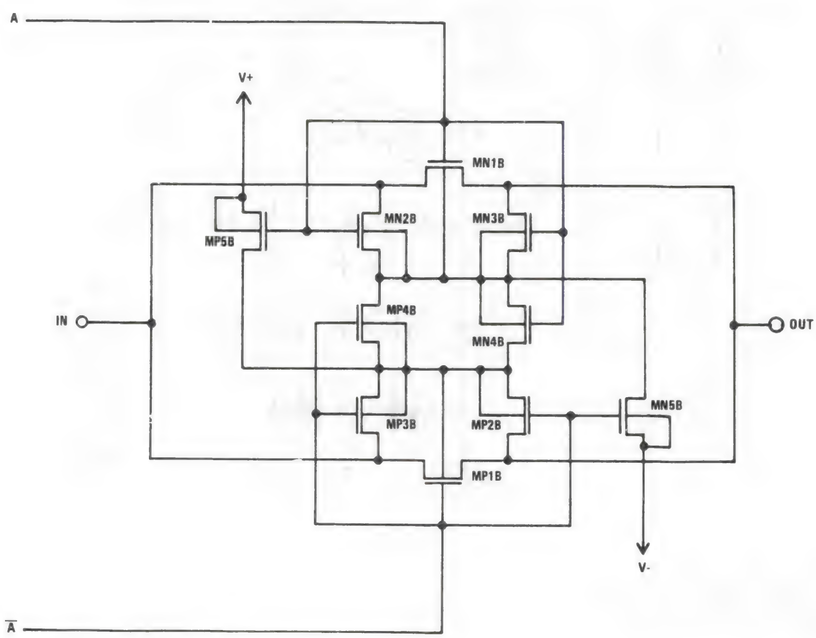
NOTES:
$R_1 = R_2 = 10K\Omega$, 5%, (per socket)
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2$ = IN4002 Equivalent (per board)
$|(V+) - (V-)| = 30V$

Schematic Diagram

DIGITAL INPUT BUFFER AND LEVEL SHIFTER



SWITCH CELL



Die Characteristics

DIE DIMENSIONS:
76 x 60.6 x 19 mils

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

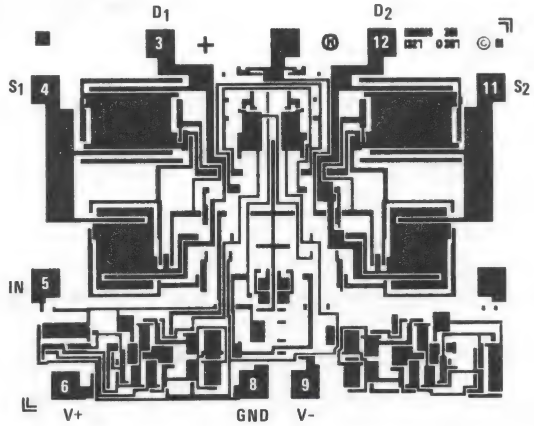
GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Metal Can — 420°C (Max)

WORST CASE CURRENT DENSITY:
$3.9 \times 10^5 A/cm^2$ at 30mA
This device meets Glassivation Integrity Test requirement per Mil-Std-883 Method 2021 and Mil-M-38510 paragraph 3.5.5.4.

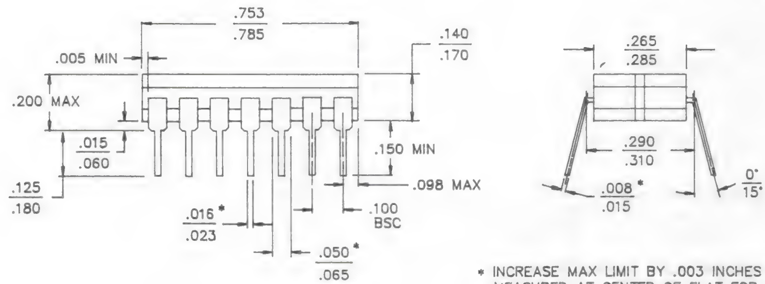
Metallization Mask Layout

HI-387/883



Packaging†

14 PIN CERAMIC DIP

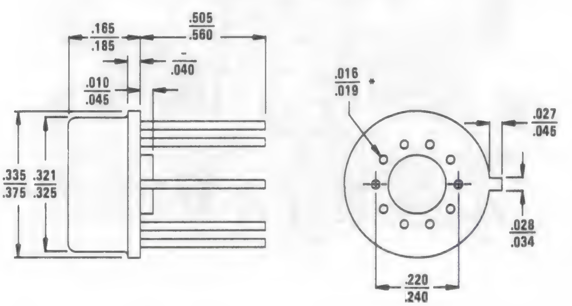


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-1

10 PIN METAL CAN



* Maximum Limits are Increased by 0.003 inches for Solder Dip Finish.

LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
Material: No Seal Material
Temperature: Room Temperature
Method: Resistance Weld

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 A-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

HI-387

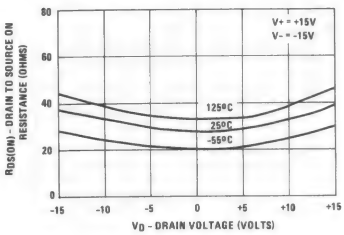
DESIGN INFORMATION

SPDT CMOS Analog Switch

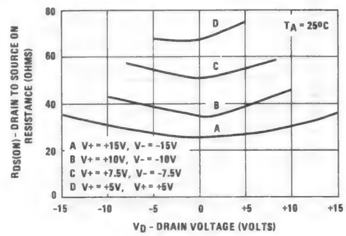
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics Unless Otherwise Specified: V+ = +15V, V- = -15V, T_A = +25°C

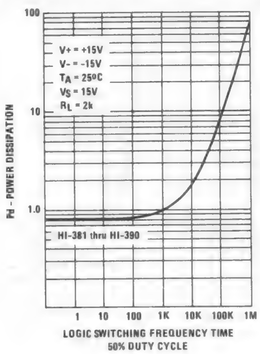
$R_{DS(ON)}$ vs. V_D AND TEMPERATURE



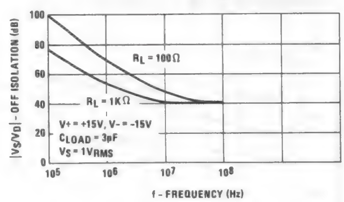
$R_{DS(ON)}$ vs. V_D AND POWER SUPPLY VOLTAGE



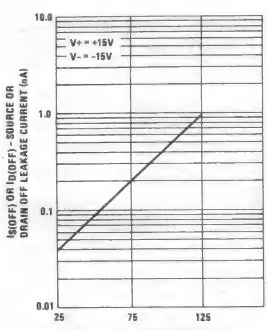
DEVICE POWER DISSIPATION vs. SWITCHING FREQUENCY SIGNAL LOGIC INPUT



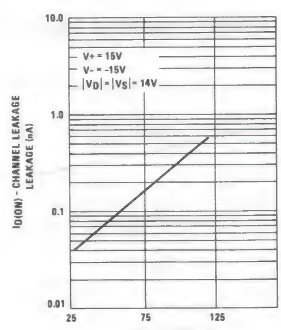
OFF ISOLATION vs. FREQUENCY



$I_{S(OFF)}$ or $I_{D(OFF)}$ vs. TEMPERATURE*



$I_{D(ON)}$ vs. TEMPERATURE*



* The net leakage into the source or drain is the N-channel leakage minus the P-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

4

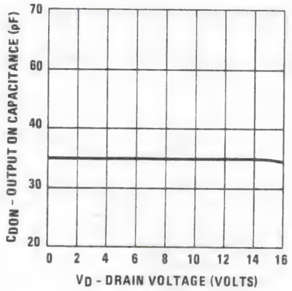
CMOS ANALOG SWITCHES

DESIGN INFORMATION (Continued)

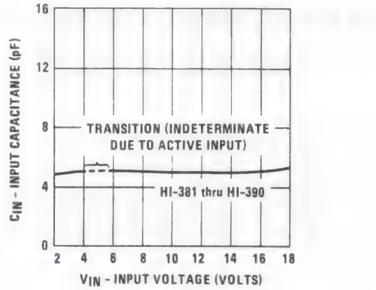
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics Unless Otherwise Specified: V+ = +15V, V- = -15V, T_A = +25°C

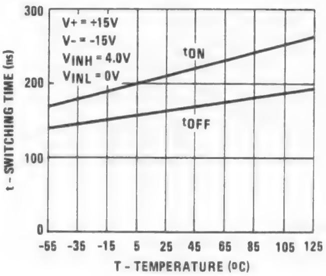
OUTPUT ON CAPACITANCE vs. DRAIN VOLTAGE



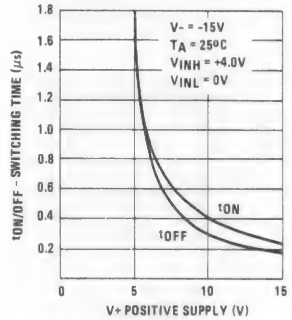
DIGITAL INPUT CAPACITANCE vs. INPUT VOLTAGE



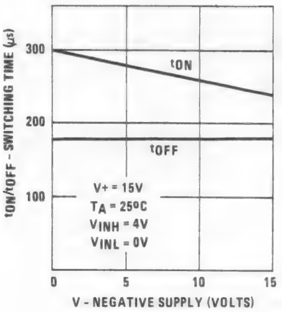
SWITCHING TIME vs. TEMPERATURE



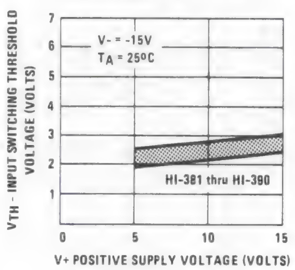
SWITCHING TIME vs. POSITIVE SUPPLY VOLTAGE



SWITCHING TIME vs. NEGATIVE SUPPLY VOLTAGE



INPUT SWITCHING THRESHOLD vs. POSITIVE SUPPLY VOLTAGE



HARRIS

HI-390/883

January 1989

Dual SPDT CMOS Analog Switch

Features

- **This Circuit Is Processed in Accordance to Mil-Std-883 and Is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Analog Signal Range (±15V Supplies) .... ±15V**
- **Low Leakage (+25°C) .... 1nA (Max)**
- **Low Leakage (+125°C) .... 100nA (Max)**
- **Low ON Resistance .... 50Ω (Max)**
- **Charge Injection .... 30pC (Typ)**
- **TTL Compatible**
- **Symmetrical Switch Elements**
- **Low Operating Power**
- **Compatible with DG390**

Applications

- **Sample and Hold, i.e. Low Leakage Switching**
- **Op Amp Gain Switching, i.e. Low ON Resistance**
- **Portable, Battery Operated Circuits**
- **Low Level Switching Circuits**
- **Dual or Single Supply Systems**

Description

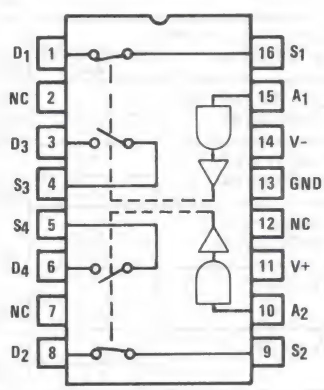
The HI-390/883 dual SPDT switch is a monolithic device fabricated using CMOS technology and the Harris Dielectric Isolation process. This switch configuration is TTL compatible and is a pin-to-pin replacement for the DG390.

This switch features low leakage and supply currents, low and nearly constant ON resistance over the analog signal range, break-before-make switching and low power dissipation.

The HI-390/883 switch is available in a 16 pin Ceramic DIP and operates over the -55°C to +125°C temperature range.

Pinout

HI1-390/883 (CERAMIC DIP)
TOP VIEW



LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 44V
$\pm V_{SUPPLY}$ to Ground (V+, V-) .... ±22V
Analog Input Voltage $+V_S$ .... $+V_{SUPPLY}$ +1.5V
$-V_S$ .... $-V_{SUPPLY}$ -1.5V
Digital Input Voltage $+V_A$ .... $+V_{SUPPLY}$ +4V
$-V_A$ .... $-V_{SUPPLY}$ -4V
Peak Current (S or D)
(Pulse at 1ms, 10% Duty Cycle Max) 40mA
Continuous Current 30mA
Junction Temperature .... +175°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering 10 sec) .... ≤275°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	88°C/W	24°C/W

Package Power Dissipation at +75°C
Ceramic DIP Package 0.85W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 11.36mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) .... ±15V
Analog Input Voltage (V_S) .... $\pm V_{SUPPLY}$
Logic Low Level (V_{AL}) .... 0V to 0.8V
Logic High Level (V_{AH}) .... 4.0V to $+V_{SUPPLY}$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, GND = 0V, Unless Otherwise Specified

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch "ON" Resistance	R_{DS}	V_{A1} = 4.0V, V_D = 10V, I_S = -10mA V_{A2} = 0.8V S1/S2/S3/S4	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
		V_{A1} = 11V, V_D = -10V, I_S = 10mA V_{A2} = 0.8V S1/S2/S3/S4	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = +14V, V_D = -14V, V_{A1} = 0.8V V_{A2} = 4.0V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = -14V, V_D = +14V, V_{A1} = 0.8V V_{A2} = 4.0V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_S = +14V, V_D = -14V, V_{A1} = 0.8V V_{A2} = 4.0V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = -14V, V_D = +14V, V_{A1} = 0.8V V_{A2} = 4.0V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = +14V, V_{A1} = 4.0V V_{A2} = 0.8V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_D = V_S = -14V, V_{A1} = 4.0V V_{A2} = 0.8V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Low Level Input Current	I_{AL}	All Channels V_A = 0.8V	1	+25°C	-1.0	1.0	µA
			2, 3	-55°C to +125°C	-1.0	1.0	µA
High Level Input Current	I_{AH}	All Channels V_A = 4.0V	1	+25°C	-1.0	1.0	µA
			2, 3	-55°C to +125°C	-1.0	1.0	µA
Supply Current	$+I_{CC}$	All Channels V_A = 0.8V	1	+25°C	-	10	µA
			2, 3	-55°C to +125°C	-	100	µA
		V_{A1} = 0V, V_{A2} = 4.0V and V_{A1} = 4.0V, V_{A2} = 0V	1	+25°C	-	0.5	mA
			2, 3	-55°C to +125°C	-	1.0	mA
Supply Current	$-I_{CC}$	All Channels V_A = 0.8V	1	+25°C	-10	-	µA
			2, 3	-55°C to +125°C	-100	-	µA
		V_{A1} = 0V, V_{A2} = 4.0V and V_{A1} = 4.0V, V_{A2} = 0V	1	+25°C	-10	-	µA
			2, 3	-55°C to +125°C	-100	-	µA

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = −15V, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Turn "ON" Time	$t_{(ON)}$	C_L = 33pF R_L = 300Ω	9	+25°C	-	300	ns
			10, 11	-55°C, +125°C	-	500	ns
Turn "OFF" Time	$t_{(OFF)}$	C_L = 33pF R_L = 300Ω	9	+25°C	-	250	ns
			10, 11	-55°C, +125°C	-	450	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Characterized at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = −15V, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Switch Input Capacitance	$C_{IS(OFF)}$	Measured Source to GND	1	+25°C	-	28	pF
Driver Input Capacitance	C_{C1}	V_A = 0V	1	+25°C	-	10	pF
	C_{C2}	V_A = 15V	1	+25°C	-	10	pF
Switch Output Capacitance	C_{OS}	Measured Drain to GND	1	+25°C	-	28	pF
Off Isolation	V_{ISO}	f = 1MHz, V_{GEN} = $1V_{p-p}$	1	+25°C	40	-	dB
Crosstalk	V_{CT}	f = 1MHz, V_{GEN} = $1V_{p-p}$	1	+25°C	40	-	dB
Charge Transfer	V_{CTE}	V_S = GND, C_L = 0.01µF	1	+25°C	-	15	mV

NOTE 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

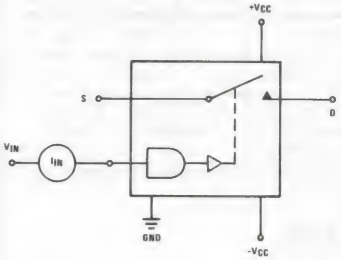
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

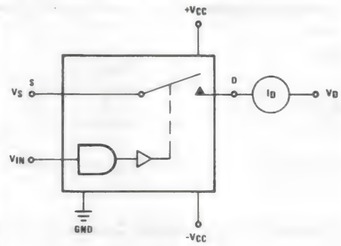
* PDA applies to Subgroup 1 only.

Test Circuits

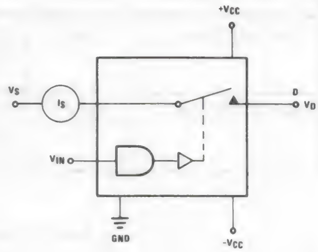
INPUT LEAKAGE CURRENT



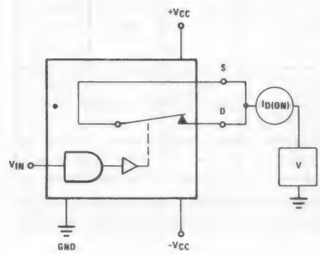
$I_{D(OFF)}$



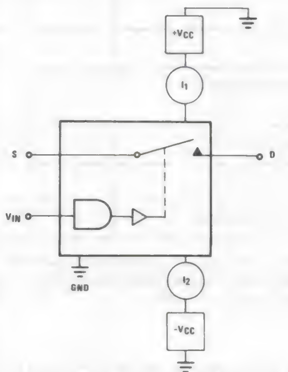
$I_{S(OFF)}$



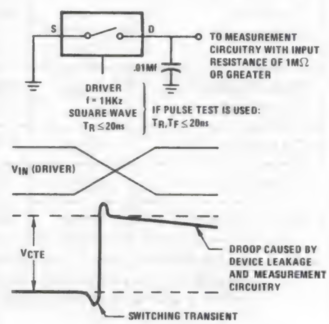
$I_{D(ON)}$



SUPPLY CURRENTS

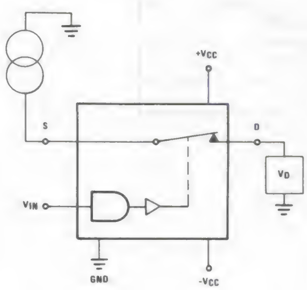


CHARGE TRANSFER ERROR

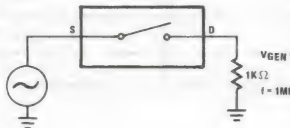


NOTE: V_{CTE} may be a positive or negative value

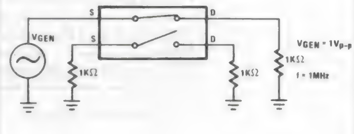
R_{DS}



OFF CHANNEL ISOLATION

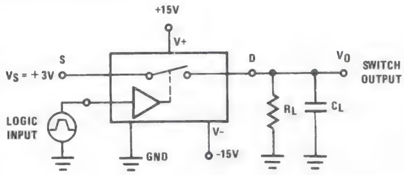


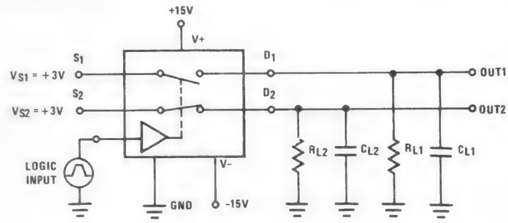
CROSSTALK BETWEEN CHANNELS

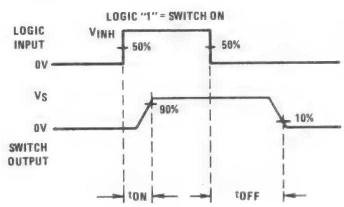


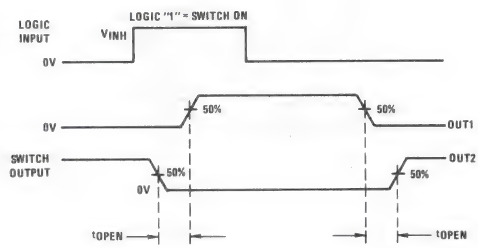
For Detail Information Refer to HI-390/883 Test Tech Brief

Test Waveforms







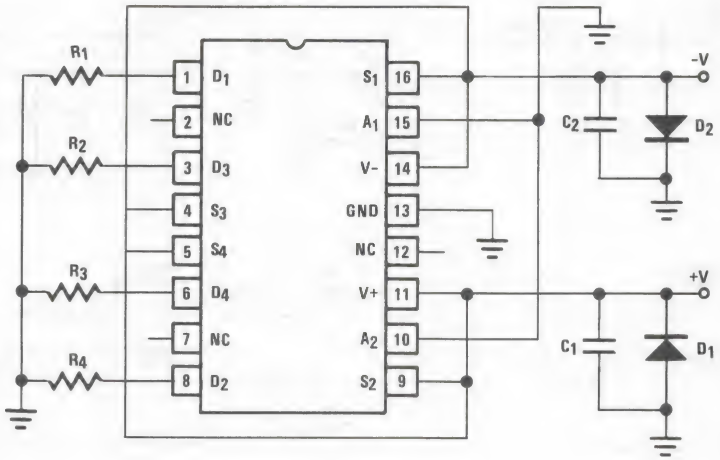


NOTES:

1. $R_L = R_L1 = R_L2 = 300\Omega$; $C_L = C_L1 = C_L2 = 33pF$
2. $V_{INH} = 4V$
   RISETIME (0.4V to 3.6V) $\leq$ 20ns
   FALLTIME (3.6V to 0.4V) $\leq$ 20ns

Burn-In Circuit

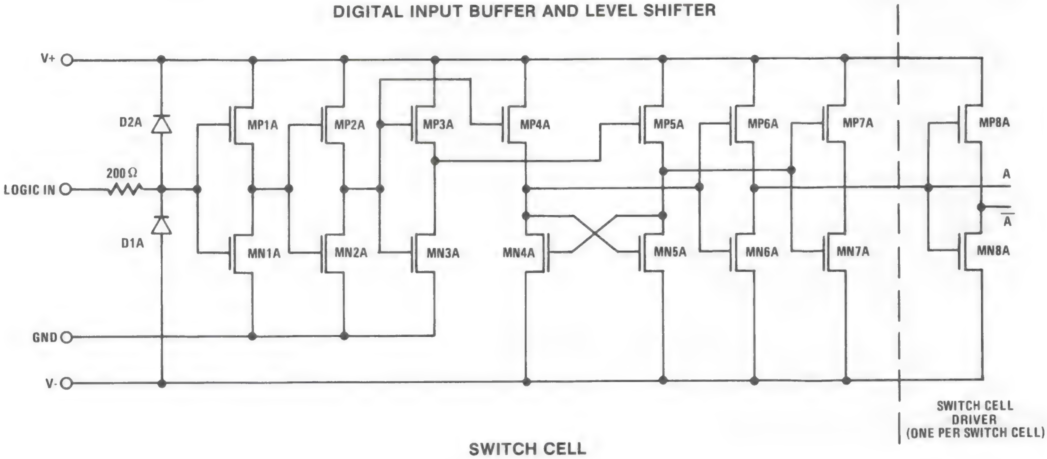
HI-390/883 CERAMIC DIP



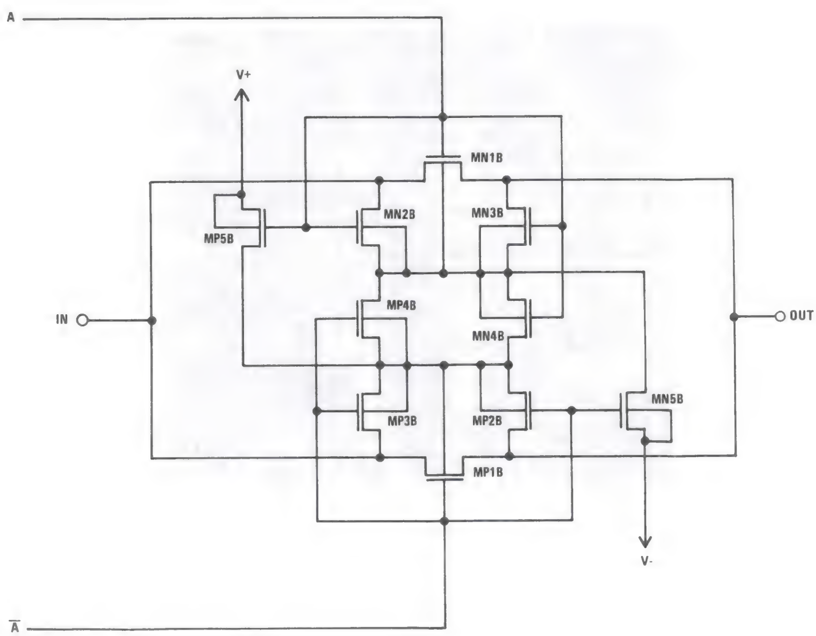
NOTES:
$R_1 = R_2 = R_3 = R_4 = 10k\Omega$, 5%, 1/4 or 1/2 watt
$C_1 = C_2 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
$D_1 = D_2$ = IN4002 or Equivalent (per board)
$|(V+) - (V-)| = 30V$

Schematic Diagram

DIGITAL INPUT BUFFER AND LEVEL SHIFTER



SWITCH CELL



Die Characteristics

DIE DIMENSIONS:
76 x 83.9 x 19 mils

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

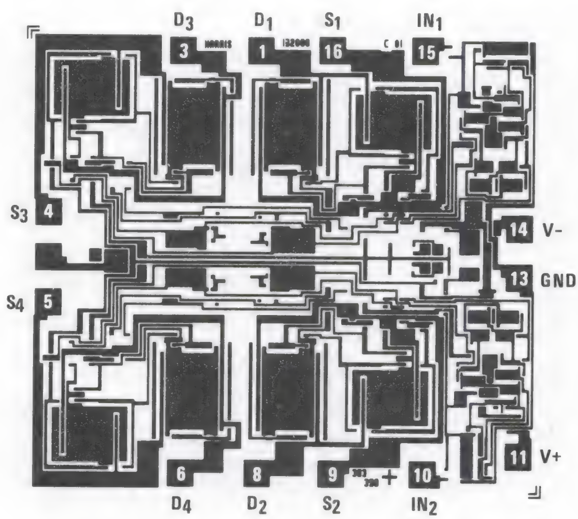
DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)

WORST CASE CURRENT DENSITY:
$3.9 \times 10^5 A/cm^2$ at 30mA

This device meets Glassivation Integrity Test requirement per Mil-Std-883 Method 2021 and Mil-M-38510 paragraph 3.5.5.4.

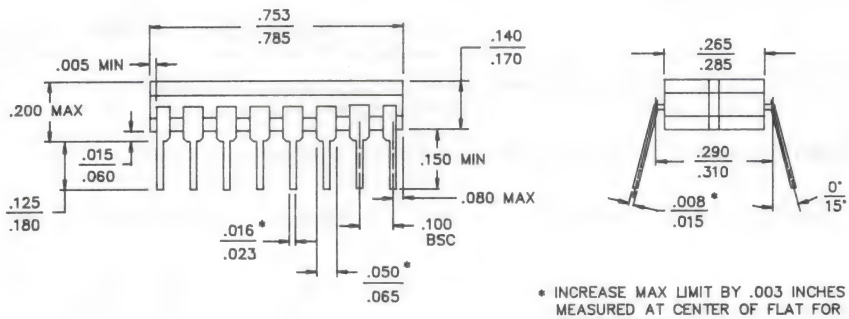
Metallization Mask Layout

HI-390/883



Packaging†

16 PIN CERAMIC DIP



* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-2

4
CMOS ANALOG SWITCHES

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

HI-390

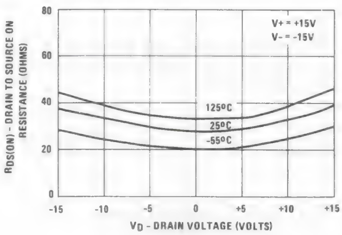
DESIGN INFORMATION

Dual SPDT CMOS Analog Switch

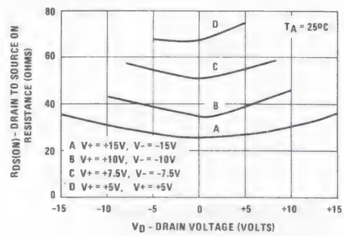
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics Unless Otherwise Specified: V+ = +15V, V- = -15V, T_A = +25°C

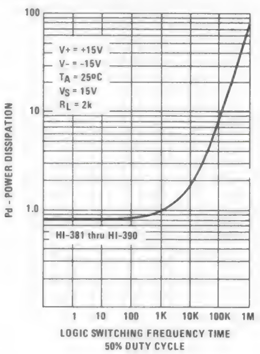
$R_{DS(ON)}$ vs. V_D AND TEMPERATURE



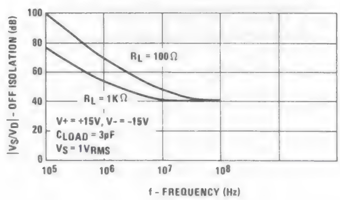
$R_{DS(ON)}$ vs. V_D AND POWER SUPPLY VOLTAGE



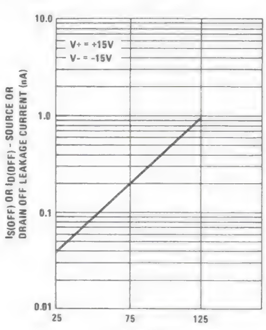
DEVICE POWER DISSIPATION vs. SWITCHING FREQUENCY SIGNAL LOGIC INPUT



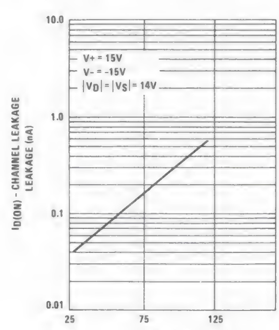
OFF ISOLATION vs. FREQUENCY



$I_{S(OFF)}$ or $I_{D(OFF)}$ vs. TEMPERATURE*



$I_{D(ON)}$ vs. TEMPERATURE*



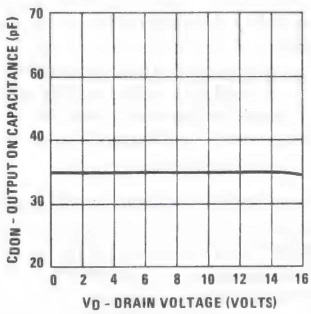
* The net leakage into the source or drain is the N-channel leakage minus the P-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

DESIGN INFORMATION (Continued)

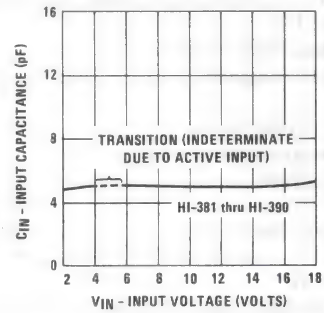
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics Unless Otherwise Specified: V+ = +15V, V- = -15V, T_A = +25°C

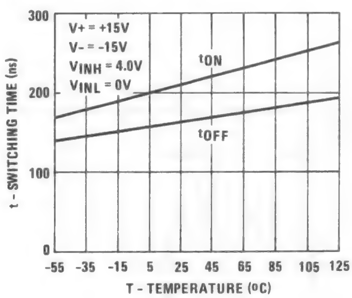
OUTPUT ON CAPACITANCE vs. DRAIN VOLTAGE



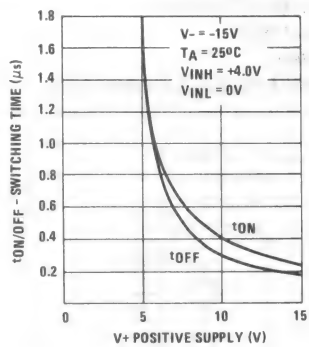
DIGITAL INPUT CAPACITANCE vs. INPUT VOLTAGE



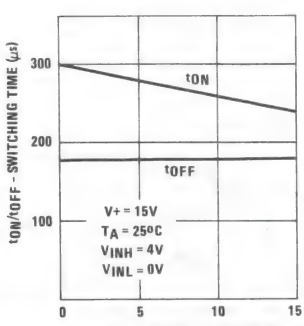
SWITCHING TIME vs. TEMPERATURE



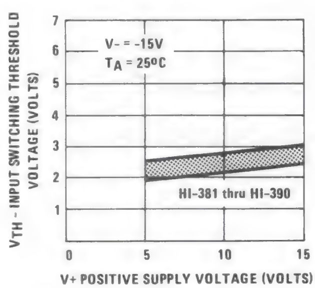
SWITCHING TIME vs. POSITIVE SUPPLY VOLTAGE



SWITCHING TIME vs. NEGATIVE SUPPLY VOLTAGE



INPUT SWITCHING THRESHOLD vs. POSITIVE SUPPLY VOLTAGE



HARRIS

HI-5040/883

January 1989

SPST CMOS Analog Switch

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Wide Analog Signal Range .... ±15V
- Low "ON" Resistance .... 50Ω (Typ) 150Ω (Max)
- High Current Capability .... 70mA (Max)
- Break-Before-Make Switching
  - Turn-On Time .... 370ns (Typ) 800ns (Max)
  - Turn-Off Time .... 280ns (Typ) 400ns (Max)
- No Latch-Up
- Input MOS Gates Are Protected From Electrostatic Discharge
- DTL, TTL, CMOS, PMOS Compatible

Applications

- High Frequency Switching
- Sample and Hold
- Digital Filters
- Operational Amplifier Gain Switching

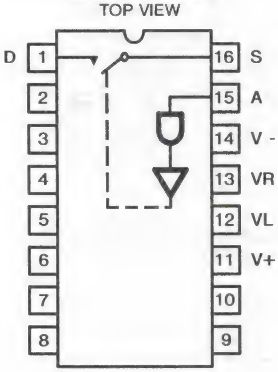
Description

This CMOS analog switch offers low-resistance switching performance for analog voltages up to the supply rails and for signal currents up to 70mA. "ON" resistance is low and stays reasonably constant over the full range of operating signal voltage and current. R_{ON} remains exceptionally constant for input voltages between +5V and -5V and currents up to 50mA. Switch impedance also changes very little over temperature, particularly between 0°C and +75°C. R_{ON} is nominally 50Ω.

This device provides break-before-make switching and is TTL and CMOS compatible for maximum application versatility. Performance is further enhanced by Dielectric Isolation processing which insures latch-free operation with very low input and output leakage currents (0.8nA at +25°C). This switch also features very low power operation (1.5mW at +25°C). The HI-5040/883 is available in a 16 pin Ceramic DIP and operates over the -55°C to +125°C temperature range.

Pinout

LOGIC "0" INPUT
TOP VIEW

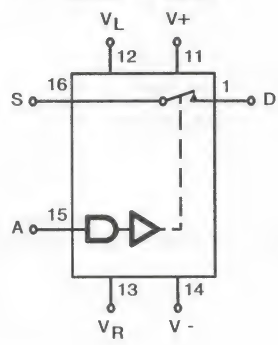


HI1-5040/883 (CERAMIC DIP)

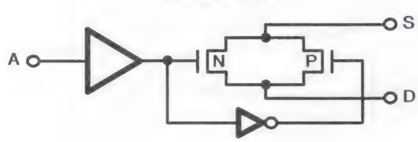
NOTE: Unused pins may be internally connected. Ground all unused pins.

Functional Diagram

LOGIC "1" INPUT



TYPICAL SWITCH



NOTE: Source and Drain are arbitrarily depicted as Analog Input and Output respectively. They may be interchanged without affecting performance.

Absolute Maximum Ratings

Voltage Between V+ and V− Terminals 36V
$\pm V_{SUPPLY}$ to Ground (V+, V−) .... ±18V
V_R to Ground .... $-V_{SUPPLY}$
V_L to Ground .... $+V_{SUPPLY}$
Digital and Analog Input Voltage (V_A, V_S, V_D) ..... $+V_{SUPPLY}$ +4V
$-V_{SUPPLY}$ −4V
Peak Current (Source to Drain)
(Pulse at 1ms, 10% Duty Cycle Max) 70mA
Continuous Current (Any Pin) 20mA
Junction Temperature .... +175°C
Storage Temperature Range .... −65°C to +150°C
ESD Rating .... < 2000V
Lead Temperature (Soldering 10 sec) .... 300°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	82°C/W	20°C/W

Package Power Dissipation Limit at +75°C for $T_J \leq$ +175°C
Ceramic DIP Package 1.0W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 12.3mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range .... −55°C to +125°C
Operating Supply Voltage .... ±15V
Logic Supply Voltage (V_L) .... +5.0V
Logic Reference Voltage (V_R) 0.0V
Analog Input Voltage (V_S) .... $\pm V_{SUPPLY}$
Address Low Level (V_{AL}) .... 0V to 0.8V
Address High Level (V_{AH}) .... 2.4V to +5.0V

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = 2.4V, V_{AL} = +0.8V, Unused Pins are Grounded, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch "ON" Resistance	R_{DS}	V_D = −10V, I_S = 10mA	1	+25°C	-	75	Ω
			2, 3	−55°C to +125°C	-	150	Ω
		V_D = 10V, I_S = −10mA	1	+25°C	-	75	Ω
			2, 3	−55°C to +125°C	-	150	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = −10V, V_D = 10V	1	+25°C	−1	1	nA
			2, 3	−55°C to +125°C	−100	100	nA
		V_S = 10V, V_D = −10V	1	+25°C	−1	1	nA
			2, 3	−55°C to +125°C	−100	100	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_D = −10V, V_S = 10V	1	+25°C	−1	1	nA
			2, 3	−55°C to +125°C	−100	100	nA
		V_D = 10V, V_S = −10V	1	+25°C	−1	1	nA
			2, 3	−55°C to +125°C	−100	100	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = 10V	1	+25°C	−2	2	nA
			2, 3	−55°C to +125°C	−200	200	nA
		V_D = V_S = −10V	1	+25°C	−2	2	nA
			2, 3	−55°C to +125°C	−200	200	nA
Low Level Address Current	I_{AL}	V_A = 0V	1	+25°C	−1	1	μA
			2, 3	−55°C to +125°C	−10	1	μA
High Level Address Current	I_{AH}	V_A = 2.4V, 5V	1	+25°C	−1	1	μA
			2, 3	−55°C to +125°C	−1	10	μA
Positive Supply Current	$+I_{CC}$	V_A = 0V, 5V	1	+25°C	-	200	μA
			2, 3	−55°C to +125°C	-	300	μA
Negative Supply Current	$-I_{CC}$	V_A = 0V, 5V	1	+25°C	−200	-	μA
			2, 3	−55°C to +125°C	−300	-	μA
Logic Supply Current	$+I_L$	V_A = 0V, 5V	1	+25°C	-	200	μA
			2, 3	−55°C to +125°C	-	300	μA
Reference Supply Current	$+I_R$	V_A = 0V, 5V	1	+25°C	−200	-	μA
			2, 3	−55°C to +125°C	−300	-	μA

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = +5.0V, V_{AL} = +0.0V, Unused Pins are Grounded, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Turn "ON" Time	t_{ON}	V_S = 10V, -10V C_L = 10pF R_L = 1kΩ	11	-55°C	-	450	ns
			9	+25°C	-	500	ns
			10	+125°C	-	800	ns
Turn "OFF" Time	t_{OFF}	V_S = 10V, -10V C_L = 10pF R_L = 1kΩ	11	-55°C	-	350	ns
			9	+25°C	-	450	ns
			10	+125°C	-	600	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Characterized at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = 4.0V, V_{AL} = 0.8V, Unused Pins are Grounded, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
"On" Resistance Match (Channel to Channel)	R_{ON} Match	V_D = ±10V I_D = 10mA	1	+25°C	-	10	Ω
Address Capacitance	C_A	V_A = 0V, 5V	1	+25°C	-	45	pF
Switch Input Capacitance	$C_{S(OFF)}$	Switch Off: V_A = 0V	1	+25°C	-	60	pF
Switch Output Capacitance	$C_{D(OFF)}$	Switch Off: V_A = 0V	1	+25°C	-	60	pF
	$C_{D(ON)}$	Switch On: V_A = 5V	1	+25°C	-	60	pF
Drain to Source Capacitance	$C_{DS(OFF)}$	Switch Off: V_A = 0V	1	+25°C	-	10	pF
Off Isolation	V_{ISO}	$V_S = 2V_{p-p}$ @ f = 100kHz R_L = 100Ω	1	+25°C	-	60	dB
Charge Transfer Error	V_{CTE}	V_S = GND, C_L = 10,000pF V_A = 0 to 4V @ f = 200kHz	1	+25°C	-	30	mV

NOTE 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

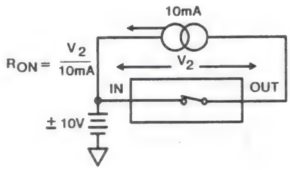
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

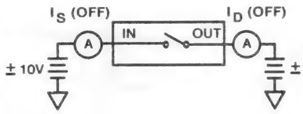
* PDA applies to Subgroup 1 only.

Test Circuits

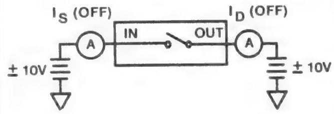
R_{DS}



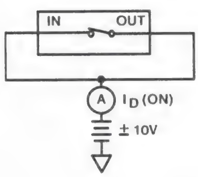
$I_{S(OFF)}$



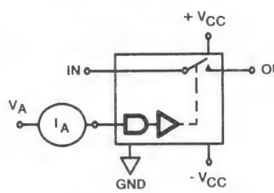
$I_{D(OFF)}$



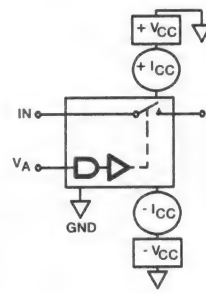
$I_{D(ON)}$



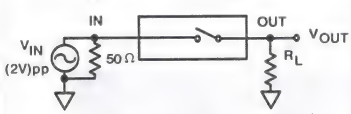
ADDRESS CURRENT



SUPPLY CURRENTS

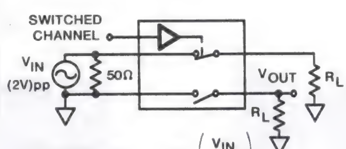


OFF ISOLATION



$$\text{"OFF" ISOLATION} = 20 \text{ LOG} \left(\frac{V_{IN}}{V_{OUT}}\right)$$

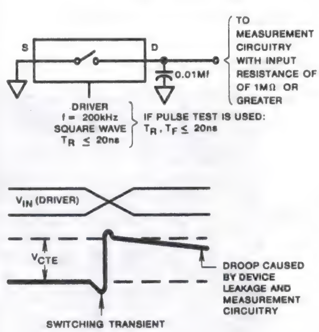
CROSSTALK



$$\text{"CROSSTALK"} = 20 \text{ LOG} \left(\frac{V_{IN}}{V_{OUT}}\right)$$

NOTE: Applies only to DUAL or DOUBLE THROW switches.

CHARGE TRANSFER



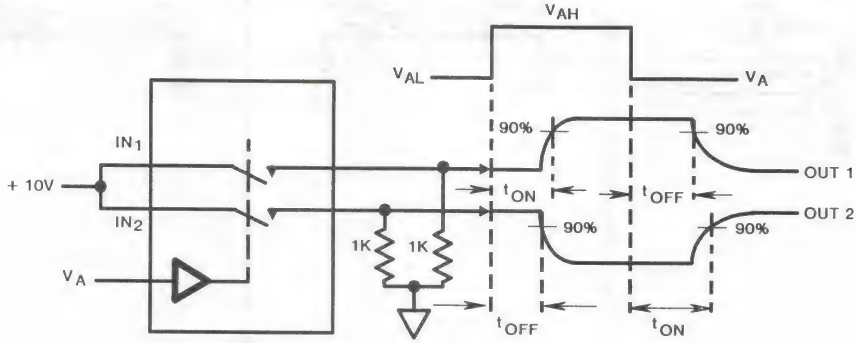
NOTE: V_{CTE} may be a positive or negative value.

4

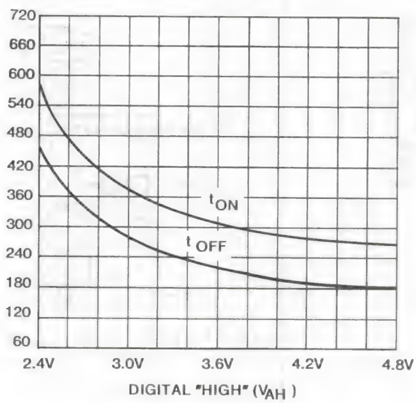
CMOS ANALOG SWITCHES

Test Characteristics

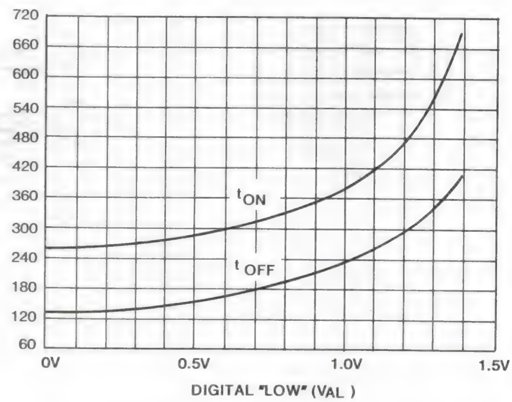
ON/OFF SWITCH TIME (t_{ON}, t_{OFF})



SWITCHING TIMES FOR POSITIVE DIGITAL TRANSITION



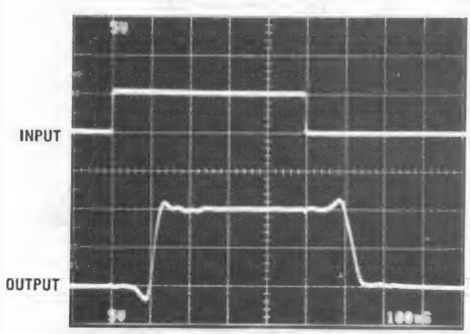
SWITCHING TIMES FOR NEGATIVE DIGITAL TRANSITION



Test Waveforms

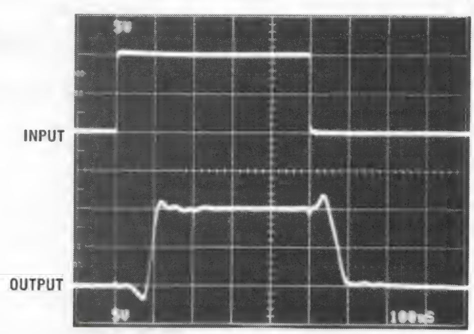
Vertical Scale: Input = 5V/Div., (TTL; V_{AH} = 5V, V_{AL} = 0V)
Output = 5V/Div.

Horizontal Scale: 100ns/Div.



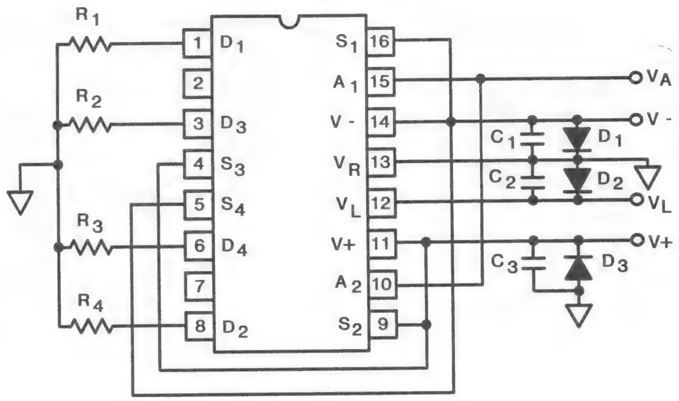
Vertical Scale: Input = 5V/Div., (CMOS; V_{AH} = 10V, V_{AL} = 0V)
Output = 5V/Div.

Horizontal Scale: 100ns/Div.



Burn-In Circuit

HI-5040/883 CERAMIC DIP



NOTES:

R_1 thru R_4 = 10kΩ, ±5%, 1/4W (Min)

C_1, C_2, C_3 = 0.01μF/Socket (Min) or 0.1μF/Row, (Min)

D_1, D_2, D_3 = IN4002 or Equivalent/Board

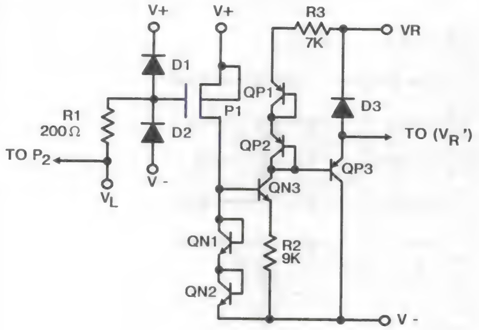
V_L = 5.5 ± 0.5V

A_1 = A_2 = 5.5 ± 0.5V

$|(V+) - (V-)|$ = 30V

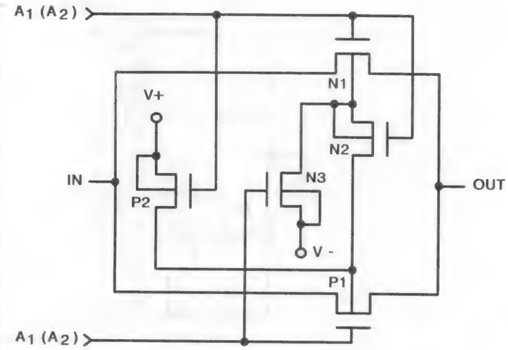
Schematic Diagram

TTL/CMOS REFERENCE CIRCUIT *

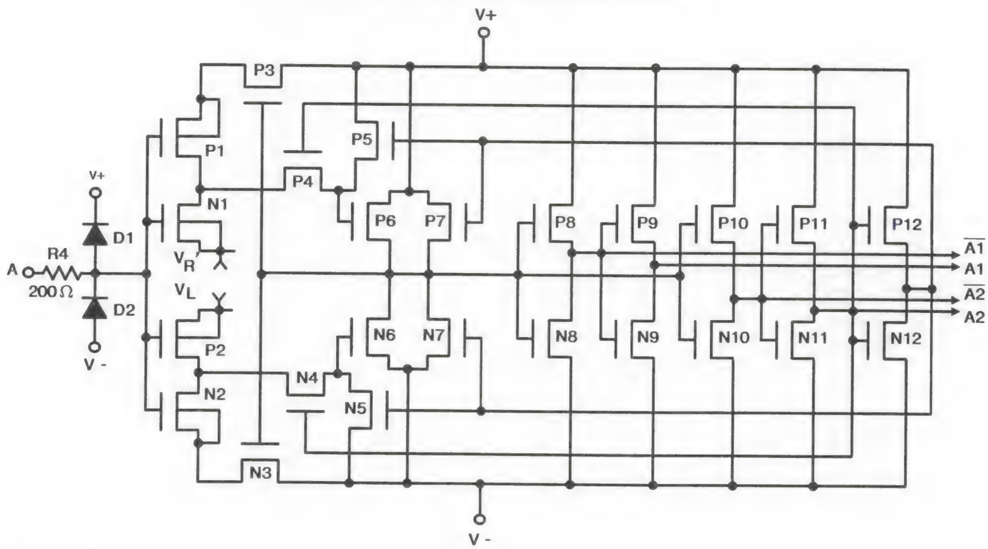


* Connect V+ to V_L for minimizing power consumption when driving from CMOS circuits.

SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



All N-Channel Bodies to V–
All P-Channel Bodies to V+
Except as Shown

Die Characteristics

DIE DIMENSIONS:
96 x 81 x 19mils
(2430 x 2050 x 480μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride over Silox
Silox Thickness: 12kÅ ± 2kÅ
Nitride Thickness: 3.5kÅ ± 1kÅ

SUBSTRATE POTENTIAL (Powered-up): V-

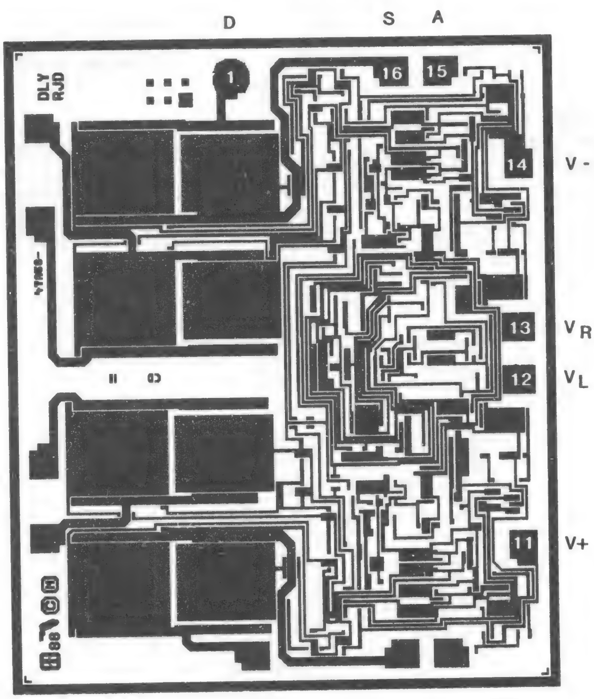
DEVICE COUNT: 82

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)

WORST CASE CURRENT DENSITY:
$1.0 \times 10^5 A/cm^2$ @ 20mA

Metallization Mask Layout

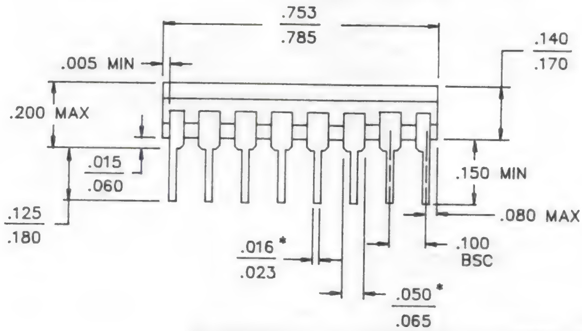
HI-5040/883

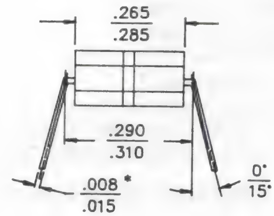


NOTE: Pin Numbers Correspond to DIP Package Only. Unused Pins May Be Connected. Ground All Unused Pins.

Packaging†

16 PIN CERAMIC DIP





* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
  Material: Glass Frit
  Temperature: 450°C ± 10°C
  Method: Furnace Seal

INTERNAL LEAD WIRE:
  Material: Aluminum
  Diameter: 1.25 Mil
  Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

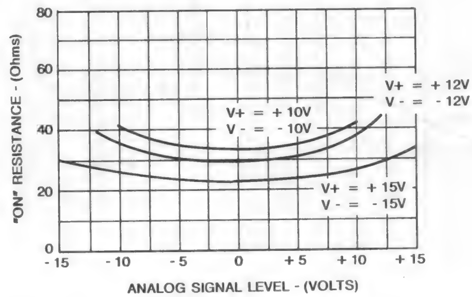
DESIGN INFORMATION

SPST CMOS Analog Switch

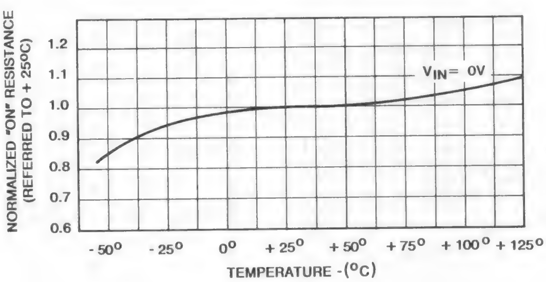
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

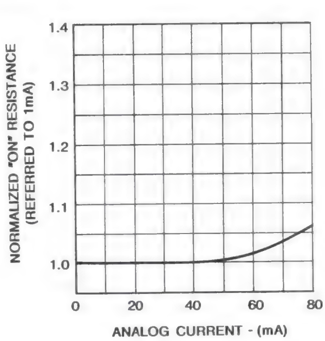
"ON" RESISTANCE vs. ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE



NORMALIZED "ON" RESISTANCE vs. TEMPERATURE



NORMALIZED "ON" RESISTANCE vs. ANALOG CURRENT



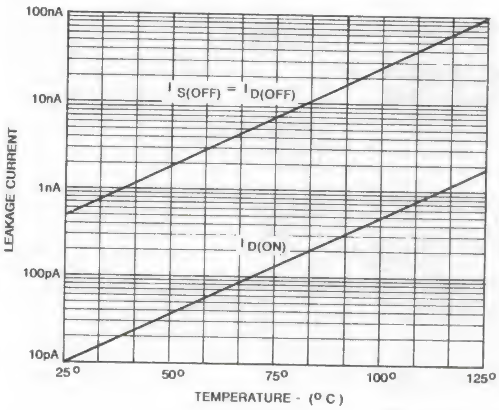
4 CMOS ANALOG SWITCHES

DESIGN INFORMATION (Continued)

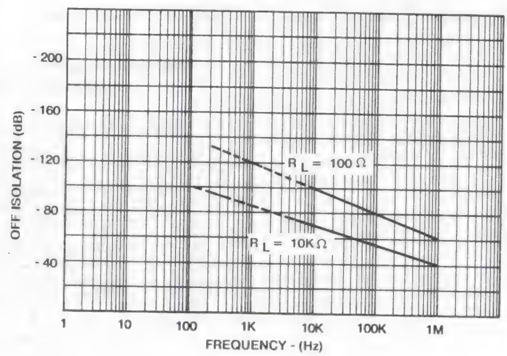
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

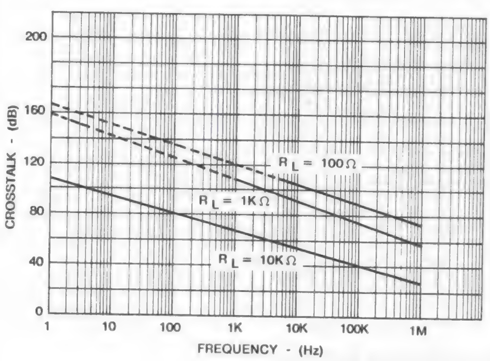
ON/OFF LEAKAGE CURRENT vs. TEMPERATURE



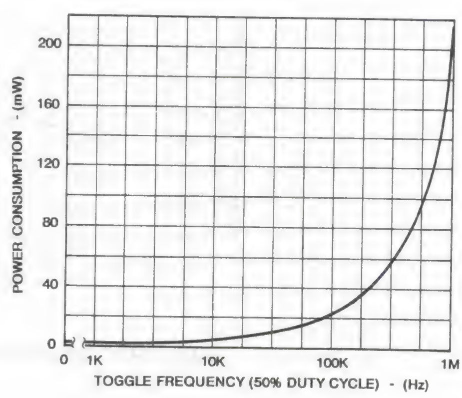
"OFF" ISOLATION vs. FREQUENCY



CROSSTALK vs. FREQUENCY



POWER CONSUMPTION vs. FREQUENCY



HARRIS

HI-5041/883

January 1989

Dual SPST CMOS Analog Switch

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Wide Analog Signal Range .... ±15V
- Low "ON" Resistance .... 50Ω (Typ) 150Ω (Max)
- High Current Capability.................70mA (Max)
- Break-Before-Make Switching
  - Turn-On Time.........................370ns (Typ) 800ns (Max)
  - Turn-Off Time.........................280ns (Typ) 400ns (Max)
- No Latch-Up
- Input MOS Gates Are Protected From Electrostatic Discharge
- DTL, TTL, CMOS, PMOS Compatible

Applications

- High Frequency Switching
- Sample and Hold
- Digital Filters
- Operational Amplifier Gain Switching

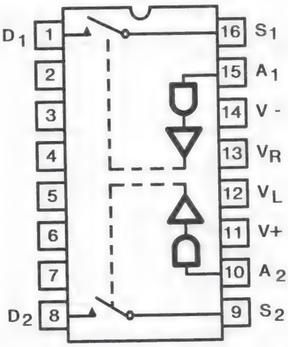
Description

This CMOS analog switch offers low-resistance switching performance for analog voltages up to the supply rails and for signal currents up to 70mA. "ON" resistance is low and stays reasonably constant over the full range of operating signal voltage and current. R_{ON} remains exceptionally constant for input voltages between +5V and -5V and currents up to 50mA. Switch impedance also changes very little over temperature, particularly between 0°C and +75°C. R_{ON} is nominally 50Ω.

This device provides break-before-make switching and is TTL and CMOS compatible for maximum application versatility. Performance is further enhanced by Dielectric Isolation processing which insures latch-free operation with very low input and output leakage currents (0.8nA at +25°C). This switch also features very low power operation (1.5mW at +25°C). The HI-5041/883 is available in a 16 pin Ceramic DIP and operates over the -55°C to +125°C temperature range.

Pinout

LOGIC "0" INPUT
TOP VIEW

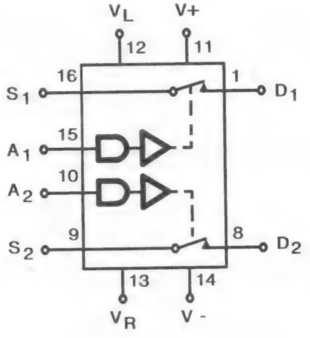


HI1-5041/883 (CERAMIC DIP)

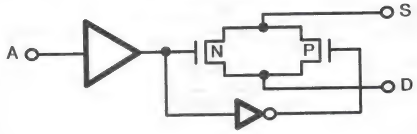
NOTE: Unused pins may be internally connected. Ground all unused pins.

Functional Diagram

LOGIC "1" INPUT



TYPICAL SWITCH



NOTE: Source and Drain are arbitrarily depicted as Analog Input and Output respectively. They may be interchanged without affecting performance.

4

CMOS ANALOG SWITCHES

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 36V
$\pm V_{SUPPLY}$ to Ground (V+, V-) .... ±18V
V_R to Ground .... $-V_{SUPPLY}$
V_L to Ground .... $+V_{SUPPLY}$
Digital and Analog Input Voltage (V_A, V_S, V_D) ..... $+V_{SUPPLY}$ +4V
$-V_{SUPPLY}$ -4V
Peak Current (Source to Drain)
(Pulse at 1ms, 10% Duty Cycle Max) 70mA
Continuous Current (Any Pin) 20mA
Junction Temperature .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... < 2000V
Lead Temperature (Soldering 10 sec) .... 300°C

Thermal Information

Thermal Resistance — θ_{ja} / θ_{jc}
Ceramic DIP Package .... 82°C/W 20°C/W
Package Power Dissipation Limit at +75°C for $T_J \leq$ +175°C
Ceramic DIP Package 1.0W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 12.3mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±15V
Logic Supply Voltage (V_L) .... +5.0V
Logic Reference Voltage (V_R) 0.0V
Analog Input Voltage (V_S) .... $\pm V_{SUPPLY}$
Address Low Level (V_{AL}) .... 0V to 0.8V
Address High Level (V_{AH}) .... 2.4V to +5.0V

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = 2.4V, V_{AL} = +0.8V, Unused Pins are Grounded, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch "ON" Resistance	R_{DS}	V_D = -10V, I_S = 10mA S1/S2	1	+25°C	-	75	Ω
			2, 3	-55°C to +125°C	-	150	Ω
		V_D = 10V, I_S = -10mA S1/S2	1	+25°C	-	75	Ω
			2, 3	-55°C to +125°C	-	150	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = -10V, V_D = 10V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = 10V, V_D = -10V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_D = -10V, V_S = 10V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_D = 10V, V_S = -10V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = 10V S1/S2	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-200	200	nA
		V_D = V_S = -10V S1/S2	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-200	200	nA
Low Level Address Current	I_{AL}	V_A = 0V A_1, A_2	1	+25°C	-1	1	μA
			2, 3	-55°C to +125°C	-10	1	μA
High Level Address Current	I_{AH}	V_A = 2.4V, 5V A_1, A_2	1	+25°C	-1	1	μA
			2, 3	-55°C to +125°C	-1	10	μA
Positive Supply Current	$+I_{CC}$	V_A = 0V, 5V A_1, A_2	1	+25°C	-	200	μA
			2, 3	-55°C to +125°C	-	300	μA
Negative Supply Current	$-I_{CC}$	V_A = 0V, 5V A_1, A_2	1	+25°C	-200	-	μA
			2, 3	-55°C to +125°C	-300	-	μA
Logic Supply Current	$+I_L$	V_A = 0V, 5V	1	+25°C	-	200	μA
			2, 3	-55°C to +125°C	-	300	μA
Reference Supply Current	$+I_R$	V_A = 0V, 5V	1	+25°C	-200	-	μA
			2, 3	-55°C to +125°C	-300	-	μA

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = +5.0V, V_{AL} = +0.0V, Unused Pins are Grounded, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Turn "ON" Time	t_{ON}	V_S = 10V, -10V C_L = 10pF R_L = 1kΩ	11	-55°C	-	450	ns
			9	+25°C	-	500	ns
			10	+125°C	-	800	ns
Turn "OFF" Time	t_{OFF}	V_S = 10V, -10V C_L = 10pF R_L = 1kΩ	11	-55°C	-	350	ns
			9	+25°C	-	450	ns
			10	+125°C	-	600	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Characterized at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = 4.0V, V_{AL} = 0.8V, Unused Pins are Grounded, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
"On" Resistance Match (Channel to Channel)	R_{ON} Match	V_D = ±10V I_D = 10mA	1	+25°C	-	10	Ω
Address Capacitance	C_A	V_A = 0V, 5V	1	+25°C	-	45	pF
Switch Input Capacitance	$C_{S(OFF)}$	Switch Off: V_A = 0V	1	+25°C	-	60	pF
Switch Output Capacitance	$C_{D(OFF)}$	Switch Off: V_A = 0V	1	+25°C	-	60	pF
	$C_{D(ON)}$	Switch On: V_A = 5V	1	+25°C	-	60	pF
Drain to Source Capacitance	$C_{DS(OFF)}$	Switch Off: V_A = 0V	1	+25°C	-	10	pF
Off Isolation	V_{ISO}	V_S = 2V_{p-p} @ f = 100kHz R_L = 100Ω	1	+25°C	-	60	dB
Crosstalk	V_{CT}	V_S = 2V_{p-p} @ f = 100kHz R_L = 100Ω	1	+25°C	-	60	dB
Charge Transfer Error	V_{CTE}	V_S = GND, C_L = 10,000pF V_A = 0 to 4V @ f = 200kHz	1	+25°C	-	30	mV

NOTE 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

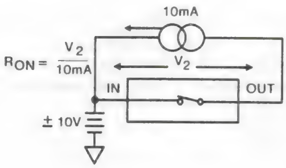
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

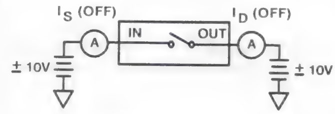
* PDA applies to Subgroup 1 only.

Test Circuits

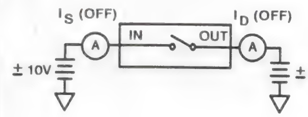
R_{DS}



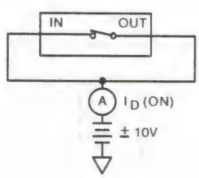
$I_{S(OFF)}$



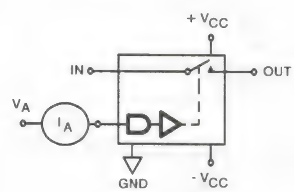
$I_{D(OFF)}$



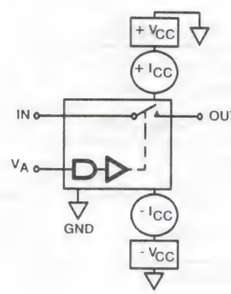
$I_{D(ON)}$



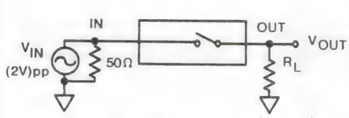
ADDRESS CURRENT



SUPPLY CURRENTS

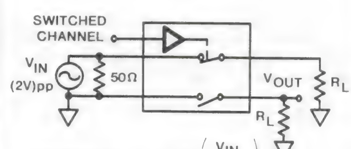


OFF ISOLATION



"OFF" ISOLATION = 20 LOG $\left(\frac{V_{IN}}{V_{OUT}}\right)$

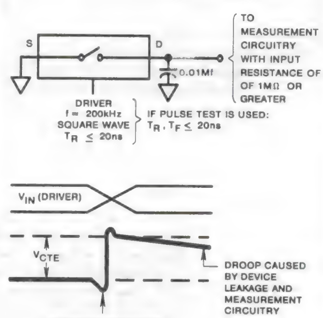
CROSSTALK



"CROSSTALK" = 20 LOG $\left(\frac{V_{IN}}{V_{OUT}}\right)$

NOTE: Applies only to DUAL or DOUBLE THROW switches.

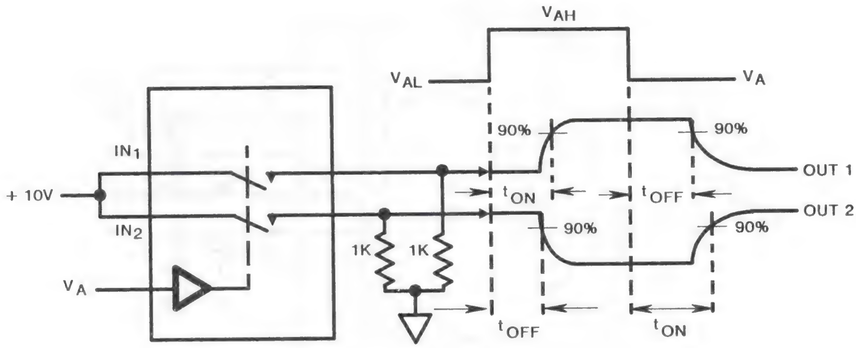
CHARGE TRANSFER

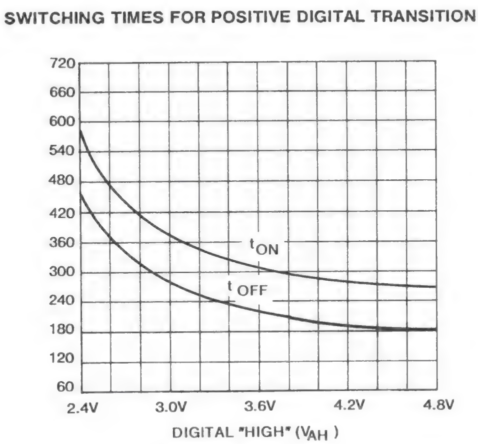


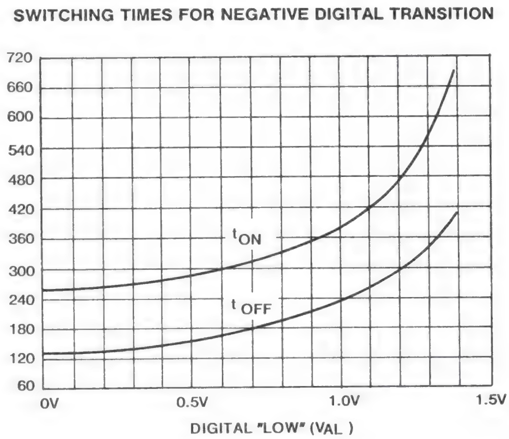
NOTE: V_{CTE} may be a positive or negative value.

Test Characteristics

ON/OFF SWITCH TIME (t_{ON}, t_{OFF})



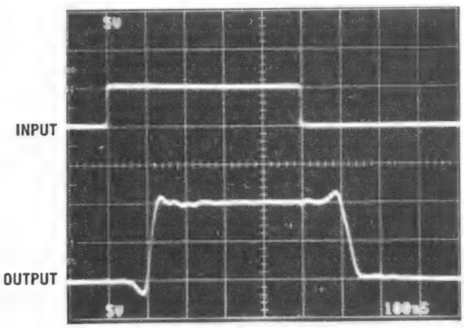




Test Waveforms

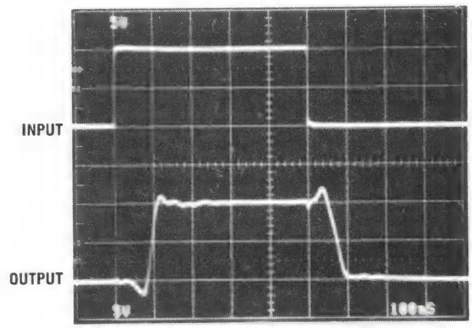
Vertical Scale: Input = 5V/Div., (TTL; V_{AH} = 5V, V_{AL} = 0V)
Output = 5V/Div.

Horizontal Scale: 100ns/Div.



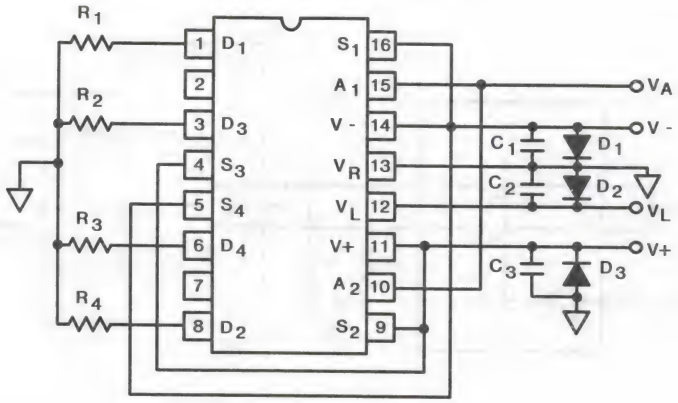
Vertical Scale: Input = 5V/Div., (CMOS; V_{AH} = 10V, V_{AL} = 0V)
Output = 5V/Div.

Horizontal Scale: 100ns/Div.



Burn-In Circuit

HI-5041/883 CERAMIC DIP



NOTES:

R_1 thru R_4 = 10kΩ, ±5%, 1/4W (Min)

C_1, C_2, C_3, = 0.01μF/Socket (Min) or 0.1μF/Row, (Min)

D_1, D_2, D_3 = IN4002 or Equivalent/Board

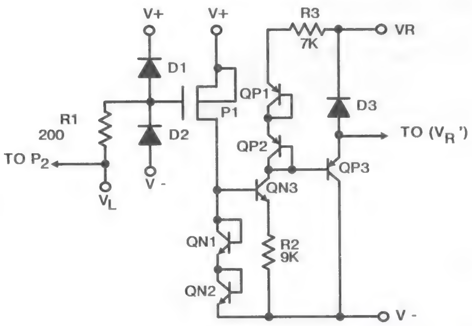
V_L = 5.5 ± 0.5V

A_1 = A_2 = 5.5 ± 0.5V

$|(V+) - (V-)|$ = 30V

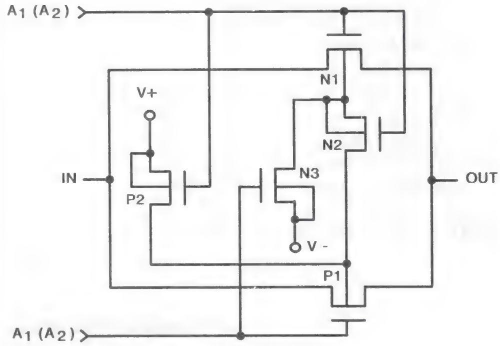
Schematic Diagram

TTL/CMOS REFERENCE CIRCUIT *

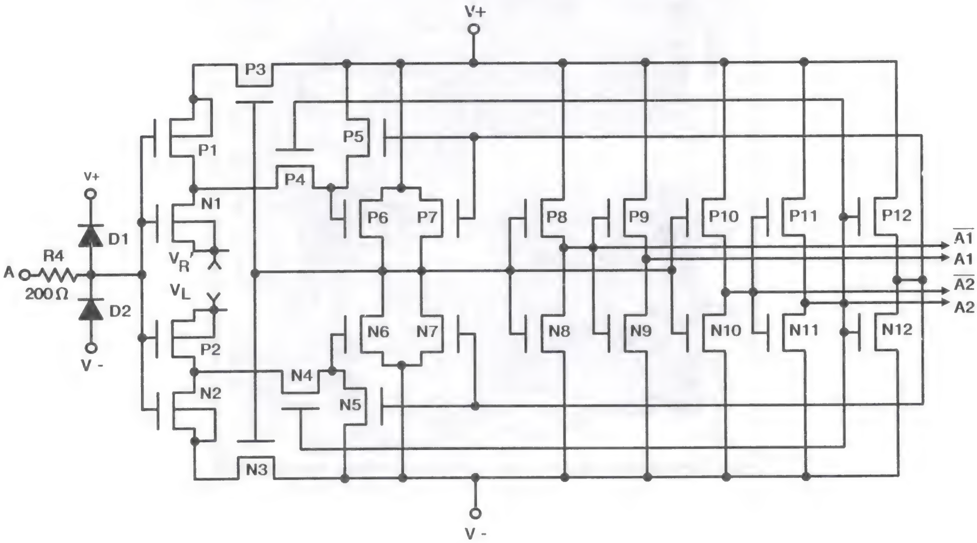


* Connect V+ to V_L for minimizing power consumption when driving from CMOS circuits.

SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



All N-Channel Bodies to V−
All P-Channel Bodies to V+
Except as Shown

Die Characteristics

DIE DIMENSIONS:
96 x 81 x 19mils
(2430 x 2050 x 480μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride over Silox
Silox Thickness: 12kÅ ± 2kÅ
Nitride Thickness: 3.5kÅ ± 1kÅ

SUBSTRATE POTENTIAL (Powered-up): V-

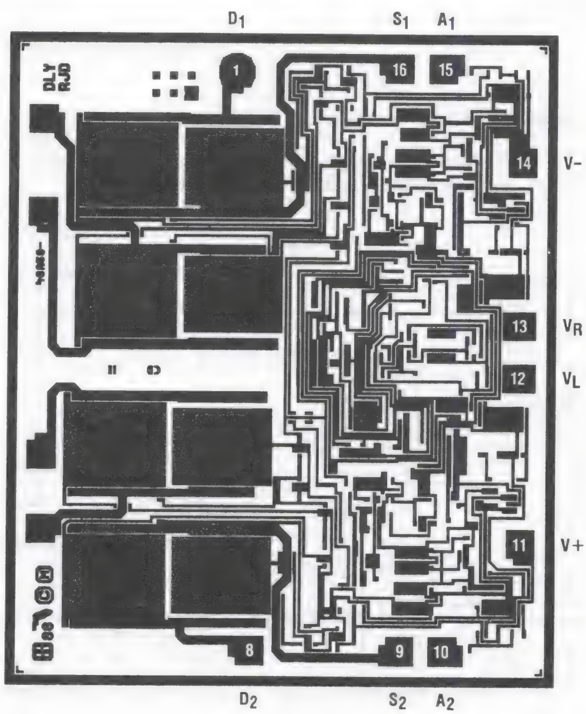
DEVICE COUNT: 82

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)

WORST CASE CURRENT DENSITY:
$1.0 \times 10^5 A/cm^2$ @ 20mA

Metallization Mask Layout

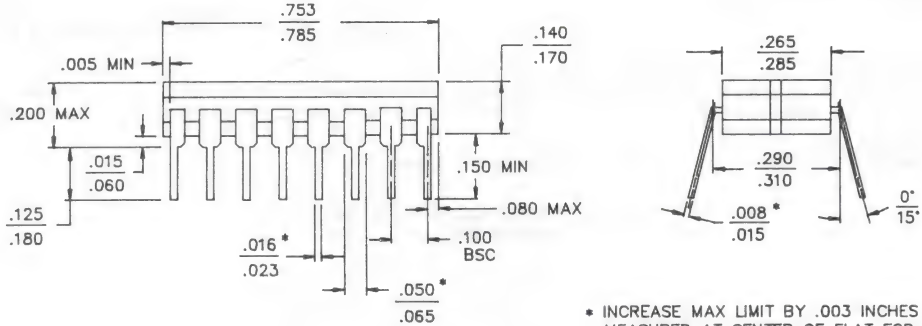
HI-5041/883



NOTE: Pin Numbers Correspond to DIP Package Only. Unused Pins May Be Connected. Ground All Unused Pins.

Packaging†

16 PIN CERAMIC DIP



* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

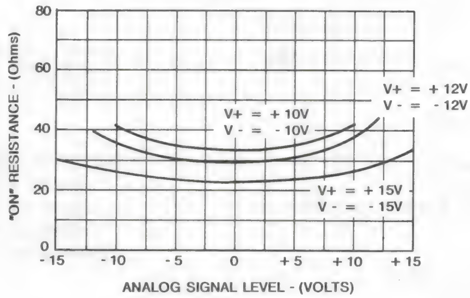
DESIGN INFORMATION

Dual SPST CMOS Analog Switch

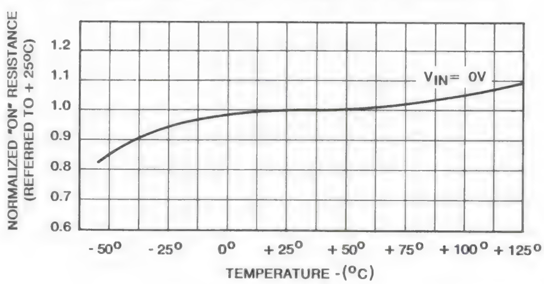
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

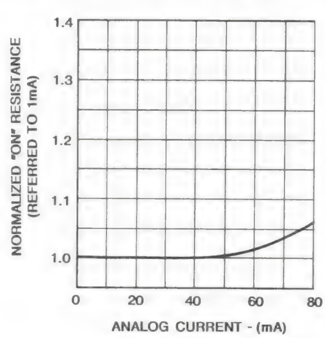
"ON" RESISTANCE vs. ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE



NORMALIZED "ON" RESISTANCE vs. TEMPERATURE



NORMALIZED "ON" RESISTANCE vs. ANALOG CURRENT

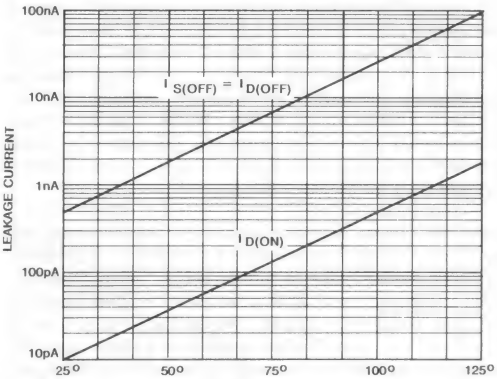


DESIGN INFORMATION (Continued)

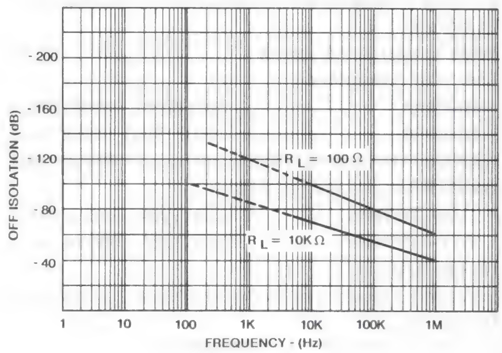
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

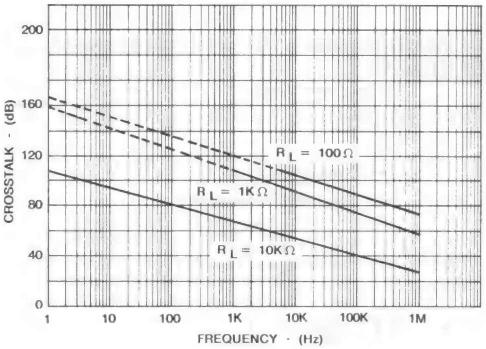
ON/OFF LEAKAGE CURRENT vs. TEMPERATURE



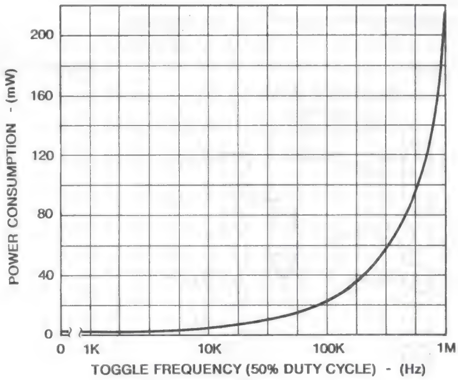
"OFF" ISOLATION vs. FREQUENCY



CROSSTALK vs. FREQUENCY



POWER CONSUMPTION vs. FREQUENCY



HARRIS

HI-5042/883
HI-5050/883

January 1989

SPDT CMOS Analog Switch

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Wide Analog Signal Range .... ±15V
- Low "ON" Resistance
  - HI-5042 .... 50Ω (Typ) 150Ω (Max)
  - HI-5050 .... 25Ω (Typ) 50Ω (Max)
- High Current Capability .... 70mA (Max)
- Break-Before-Make Switching
  - Turn-On Time .... 370ns (Typ) 800ns (Max)
  - Turn-Off Time .... 280ns (Typ) 400ns (Max)
- No Latch-Up
- Input MOS Gates Are Protected From Electrostatic Discharge
- DTL, TTL, CMOS, PMOS Compatible

Applications

- High Frequency Switching
- Sample and Hold
- Digital Filters
- Operational Amplifier Gain Switching

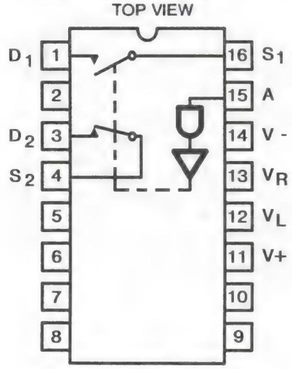
Description

These CMOS analog switches offer low-resistance switching performance for analog voltages up to the supply rails and for signal currents up to 70mA. "ON" resistance is low and stays reasonably constant over the full range of operating signal voltage and current. R_{ON} remains exceptionally constant for input voltages between +5V and -5V and currents up to 50mA. Switch impedance also changes very little over temperature, particularly between 0°C and +75°C. R_{ON} is nominally 50Ω for the HI-5042/883 and 25Ω for the HI-5050/883.

These devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. Performance is further enhanced by Dielectric Isolation processing which insures latch-free operation with very low input and output leakage currents (0.8nA at +25°C). They also feature very low power operation (1.5mW at +25°C). The HI-5042/883 and HI-5050/883 are available in a 16 pin Ceramic DIP and operate over the -55°C to +125°C temperature range.

Pinout

LOGIC "0" INPUT
TOP VIEW

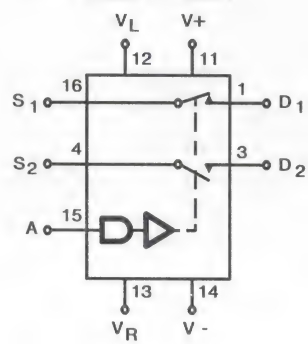


HI1-5042/883 (CERAMIC DIP)
HI1-5050/883 (CERAMIC DIP)

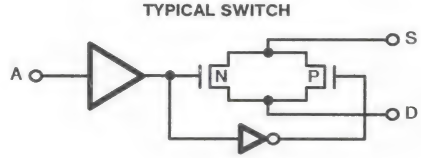
NOTE: Unused pins may be internally connected. Ground all unused pins.

Functional Diagram

LOGIC "1" INPUT



TYPICAL SWITCH



NOTE: Source and Drain are arbitrarily depicted as Analog Input and Output respectively. They may be interchanged without affecting performance.

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 36V
$\pm V_{SUPPLY}$ to Ground (V+, V-) .... ±18V
V_R to Ground .... $-V_{SUPPLY}$
V_L to Ground .... $+V_{SUPPLY}$
Digital and Analog Input Voltage (V_A, V_S, V_D) ..... $+V_{SUPPLY}$ +4V
$-V_{SUPPLY}$ -4V
Peak Current (Source to Drain)
(Pulse at 1ms, 10% Duty Cycle Max) 70mA
Continuous Current (Any Pin) 20mA
Junction Temperature .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... <2000V
Lead Temperature (Soldering 10 sec) .... 300°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	82°C/W	20°C/W

Package Power Dissipation at +75°C
Ceramic DIP Package 1.0W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 12.3mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±15V
Logic Supply Voltage (V_L) .... +5.0V
Logic Reference Voltage (V_R) 0.0V
Analog Input Voltage (V_S) .... $\pm V_{SUPPLY}$
Address Low Level (V_{AL}) .... 0V to 0.8V
Address High Level (V_{AH}) .... 2.4V to +5.0V

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = 2.4V, V_{AL} = +0.8V, Unused Pins are Grounded, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch "ON" Resistance For HI-5042/883	R_{DS}	V_D = -10V, I_S = 10mA S1/S2	1	+25°C	-	75	Ω
			2, 3	-55°C to +125°C	-	150	Ω
		V_D = 10V, I_S = -10mA S1/S2	1	+25°C	-	75	Ω
			2, 3	-55°C to +125°C	-	150	Ω
Switch "ON" Resistance For HI-5050/883	R_{DS}	V_D = -10V, I_S = 10mA S1/S2	1	+25°C	-	45	Ω
			2, 3	-55°C to +125°C	-	50	Ω
		V_D = 10V, I_S = -10mA S1/S2	1	+25°C	-	45	Ω
			2, 3	-55°C to +125°C	-	50	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = -10V, V_D = 10V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = 10V, V_D = -10V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_D = -10V, V_S = 10V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_D = 10V, V_S = -10V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = 10V S1/S2	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-200	200	nA
		V_D = V_S = -10V S1/S2	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-200	200	nA

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = 2.4V, V_{AL} = +0.8V, Unused Pins are Grounded, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Low Level Address Current	I_{AL}	V_A = 0V	1	+25°C	-1	1	μA
			2, 3	-55°C to +125°C	-10	1	μA
High Level Address Current	I_{AH}	V_A = 2.4V, 5V	1	+25°C	-1	1	μA
			2, 3	-55°C to +125°C	-1	10	μA
Positive Supply Current	$+I_{CC}$	V_A = 0V, 5V	1	+25°C	-	200	μA
			2, 3	-55°C to +125°C	-	300	μA
Negative Supply Current	$-I_{CC}$	V_A = 0V, 5V	1	+25°C	-200	-	μA
			2, 3	-55°C to +125°C	-300	-	μA
Logic Supply Current	$+I_L$	V_A = 0V, 5V	1	+25°C	-	200	μA
			2, 3	-55°C to +125°C	-	300	μA
Reference Supply Current	$+I_R$	V_A = 0V, 5V	1	+25°C	-200	-	μA
			2, 3	-55°C to +125°C	-300	-	μA

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = +5.0V, V_{AL} = +0.0V, Unused Pins are Grounded, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Turn "ON" Time	t_{ON}	V_S = 10V, -10V C_L = 10pF R_L = 1kΩ	11	-55°C	-	450	ns
			9	+25°C	-	500	ns
			10	+125°C	-	800	ns
Turn "OFF" Time	t_{OFF}	V_S = 10V, -10V C_L = 10pF R_L = 1kΩ	11	-55°C	-	350	ns
			9	+25°C	-	450	ns
			10	+125°C	-	600	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Characterized at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = 4.0V, V_{AL} = 0.8V, Unused Pins are Grounded, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
"On" Resistance Match (Channel to Channel) for HI-5042/883	R_{ON1} Match	V_D = ±10V I_D = 10mA	1	+25°C	-	10	Ω
"On" Resistance Match (Channel to Channel) for HI-5050/883	R_{ON2} Match	V_D = ±10V I_D = 10mA	1	+25°C	-	10	Ω
Address Capacitance	C_A	V_A = 0V, 5V	1	+25°C	-	45	pF
Switch Input Capacitance	$C_{S(OFF)}$	Switch Off: V_A = 0V	1	+25°C	-	60	pF
Switch Output Capacitance	$C_{D(OFF)}$	Switch Off: V_A = 0V	1	+25°C	-	60	pF
	$C_{D(ON)}$	Switch On: V_A = 5V	1	+25°C	-	60	pF
Drain to Source Capacitance	$C_{DS(OFF)}$	Switch Off: V_A = 0V	1	+25°C	-	10	pF
Off Isolation	V_{ISO}	V_S = $2V_{p-p}$ @ f = 100kHz R_L = 100Ω	1	+25°C	-	60	dB
Crosstalk	V_{CT}	V_S = $2V_{p-p}$ @ f = 100kHz R_L = 100Ω	1	+25°C	-	60	dB
Charge Transfer Error	V_{CTE}	V_S = GND, C_L = 10,000pF V_A = 0 to 4V @ f = 200kHz	1	+25°C	-	30	mV

NOTE 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

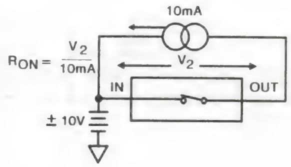
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

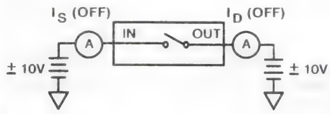
* PDA applies to Subgroup 1 only.

Test Circuits

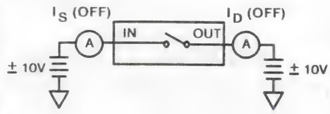
R_{DS}



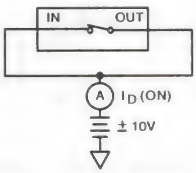
$I_{S(OFF)}$



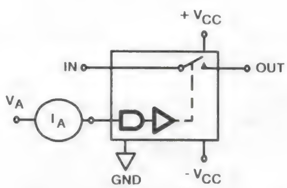
$I_{D(OFF)}$



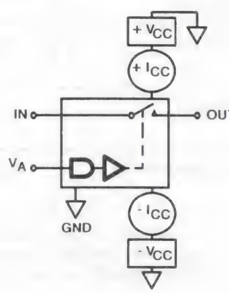
$I_{D(ON)}$



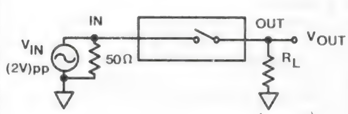
ADDRESS CURRENT



SUPPLY CURRENTS

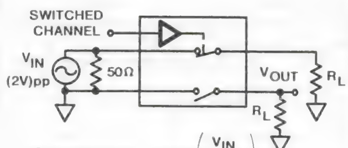


OFF ISOLATION



"OFF" ISOLATION = $20 \text{ LOG} \left(\frac{V_{IN}}{V_{OUT}} \right)$

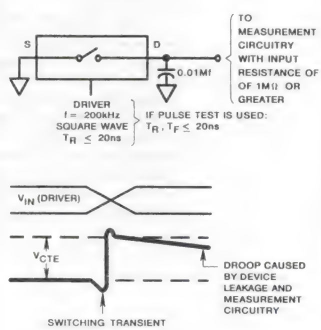
CROSSTALK



"CROSSTALK" = $20 \text{ LOG} \left(\frac{V_{IN}}{V_{OUT}} \right)$

NOTE: Applies only to DUAL or DOUBLE THROW switches.

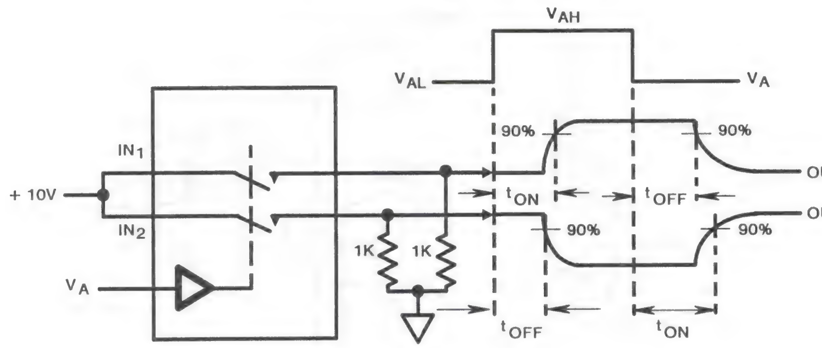
CHARGE TRANSFER



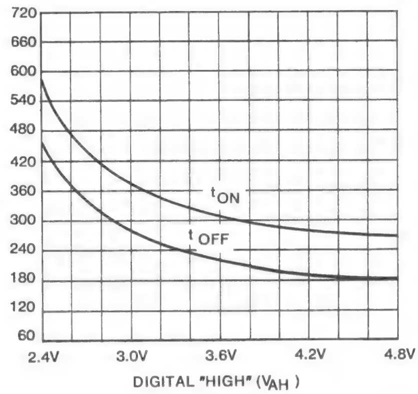
NOTE: V_{CTE} may be a positive or negative value.

Test Characteristics

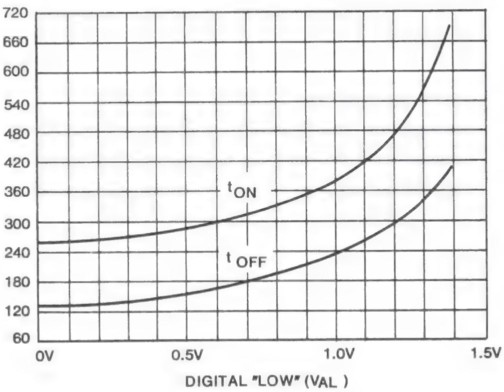
ON/OFF SWITCH TIME (t_{ON}, t_{OFF})



SWITCHING TIMES FOR POSITIVE DIGITAL TRANSITION



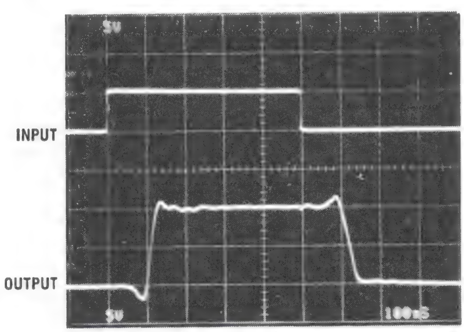
SWITCHING TIMES FOR NEGATIVE DIGITAL TRANSITION



Test Waveforms

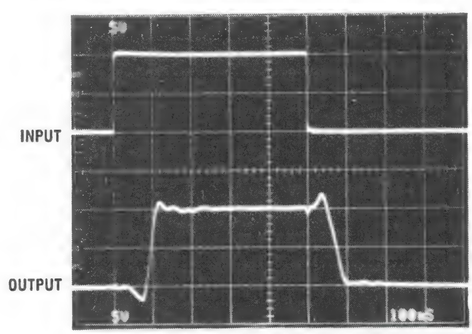
Vertical Scale: Input = 5V/Div., (TTL; V_{AH} = 5V, V_{AL} = 0V)
Output = 5V/Div.

Horizontal Scale: 100ns/Div.



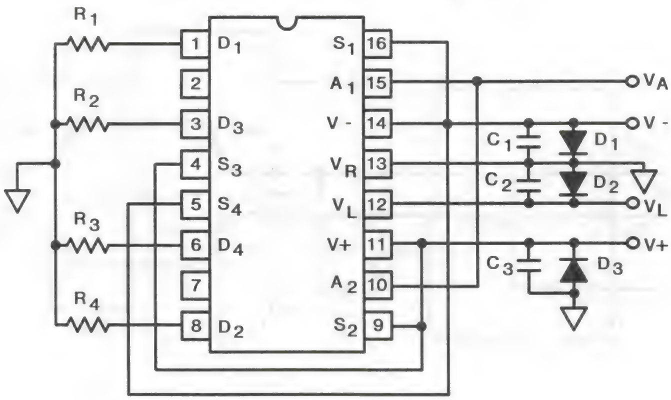
Vertical Scale: Input = 5V/Div., (CMOS; V_{AH} = 10V, V_{AL} = 0V)
Output = 5V/Div.

Horizontal Scale: 100ns/Div.



Burn-In Circuit

HI-5042/883 HI-5050/883 CERAMIC DIP



NOTES:

R_1 thru R_4 = 10kΩ, ±5%, 1/4W (Min)

C_1, C_2, C_3, = 0.01µF/Socket (Min) or 0.1µF/Row, (Min)

D_1, D_2, D_3 = IN4002 or Equivalent/Board

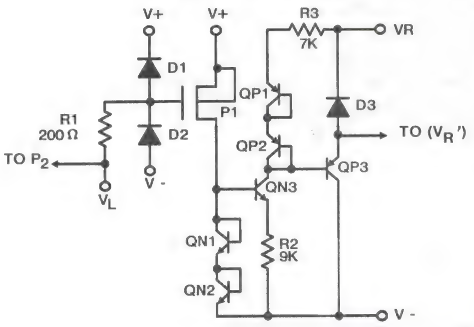
V_L = 5.5 ± 0.5V

A_1 = A_2 = 5.5 ± 0.5V

$|(V+) - (V-)|$ = 30V

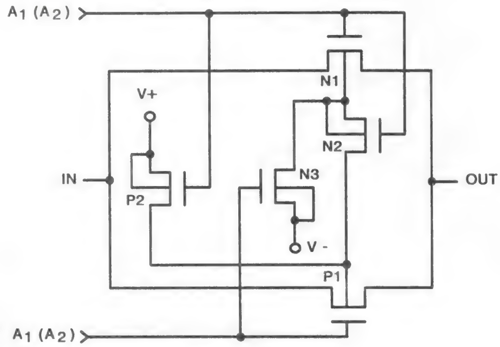
Schematic Diagram

TTL/CMOS REFERENCE CIRCUIT *

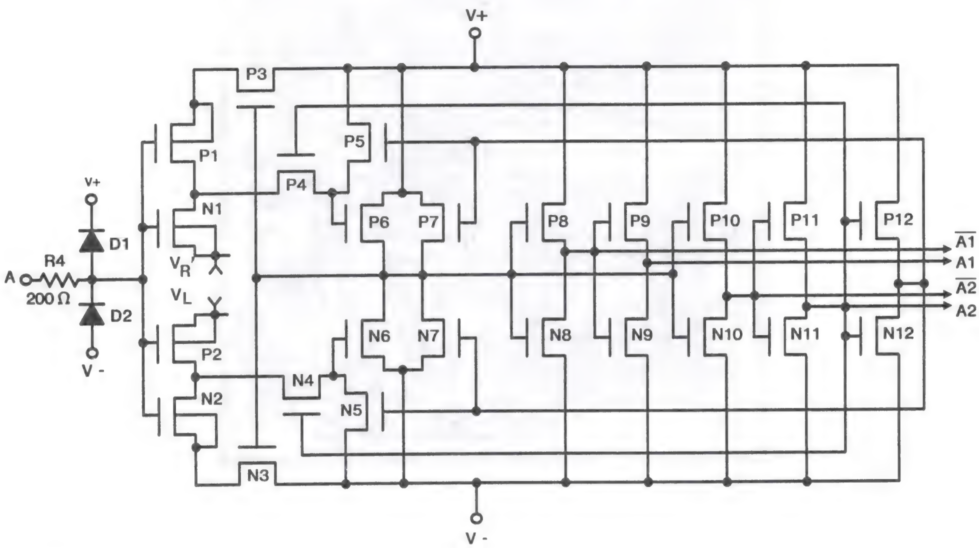


* Connect V+ to V_L for minimizing power consumption when driving from CMOS circuits.

SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



All N-Channel Bodies to V-
All P-Channel Bodies to V+
Except as Shown

Die Characteristics

DIE DIMENSIONS:
96 x 81 x 19mils
(2430 x 2050 x 480μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride over Silox
Silox Thickness: 12kÅ ± 2kÅ
Nitride Thickness: 3.5kÅ ± 1kÅ

SUBSTRATE POTENTIAL (Powered-up): V-

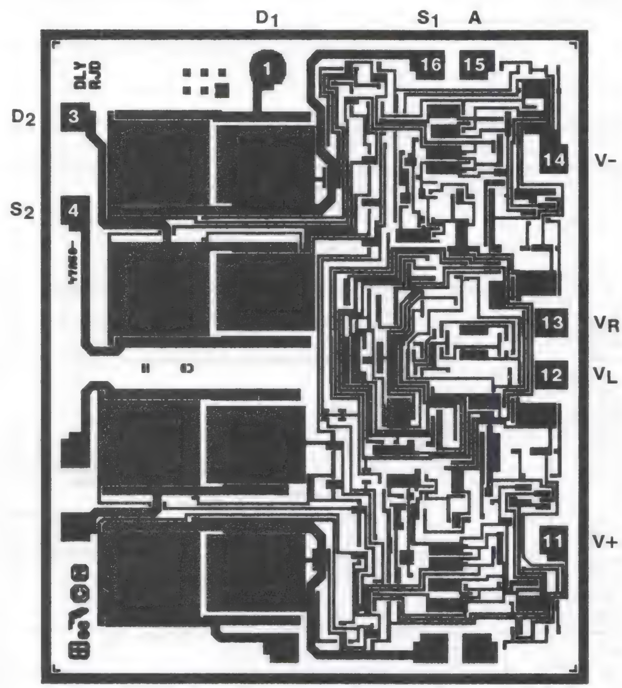
DEVICE COUNT: 82

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)

WORST CASE CURRENT DENSITY:
$1.0 \times 10^5 A/cm^2$ @ 20mA

Metallization Mask Layout

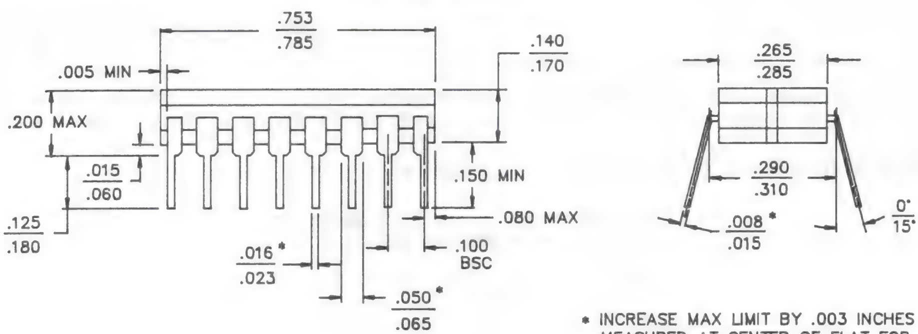
HI-5042/883 HI-5050/883



NOTE: Pin Numbers Correspond to DIP Package Only. Unused Pins May Be Connected. Ground All Unused Pins.

Packaging†

16 PIN CERAMIC DIP



* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

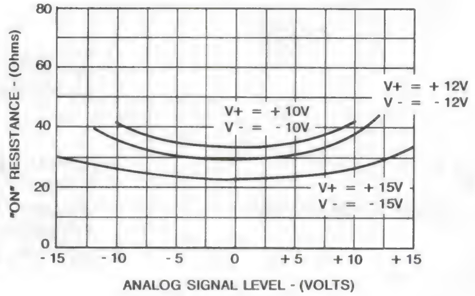
DESIGN INFORMATION

SPDT CMOS Analog Switch

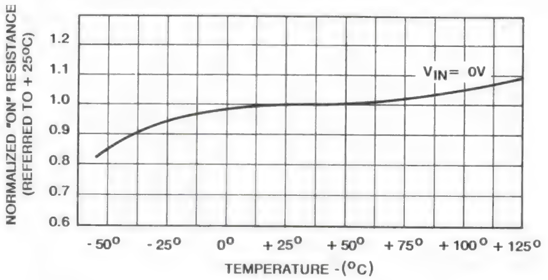
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

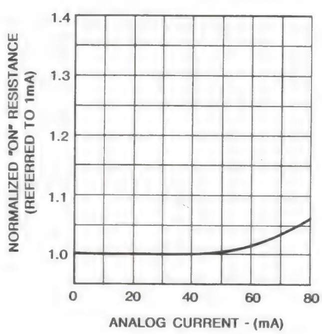
"ON" RESISTANCE vs. ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE



NORMALIZED "ON" RESISTANCE vs. TEMPERATURE



NORMALIZED "ON" RESISTANCE vs. ANALOG CURRENT

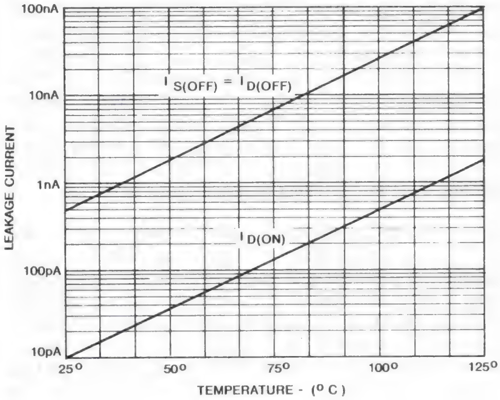


DESIGN INFORMATION (Continued)

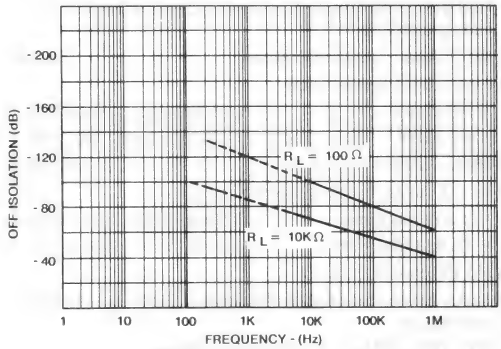
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

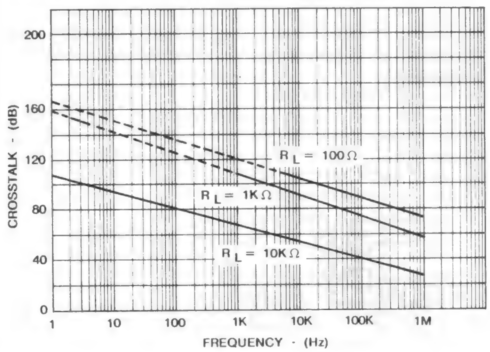
ON/OFF LEAKAGE CURRENT vs. TEMPERATURE



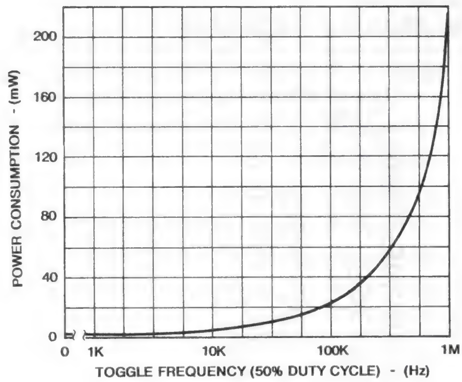
"OFF" ISOLATION vs. FREQUENCY



CROSSTALK vs. FREQUENCY



POWER CONSUMPTION vs. FREQUENCY



HARRIS

HI-5043/883
HI-5051/883

January 1989

Dual SPDT CMOS Analog Switch

Features

- This Circuit Is Processed In Accordance to Mil-Std-883 and Is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Wide Analog Signal Range .... ±15V
- Low "ON" Resistance
  - HI-5043 .... 50Ω (Typ) 150Ω (Max)
  - HI-5051 .... 25Ω (Typ) 50Ω (Max)
- High Current Capability .... 70mA (Max)
- Break-Before-Make Switching
  - Turn-On Time .... 370ns (Typ) 800ns (Max)
  - Turn-Off Time .... 280ns (Typ) 400ns (Max)
- No Latch-Up
- Input MOS Gates Are Protected From Electrostatic Discharge
- DTL, TTL, CMOS, PMOS Compatible

Applications

- High Frequency Switching
- Sample and Hold
- Digital Filters
- Operational Amplifier Gain Switching

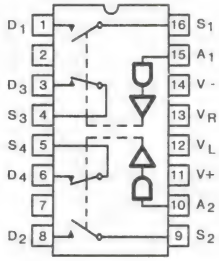
Description

These CMOS analog switches offer low-resistance switching performance for analog voltages up to the supply rails and for signal currents up to 70mA. "ON" resistance is low and stays reasonably constant over the full range of operating signal voltage and current. R_{ON} remains exceptionally constant for input voltages between +5V and -5V and currents up to 50mA. Switch impedance also changes very little over temperature, particularly between 0°C and +75°C. R_{ON} is nominally 50Ω for the HI-5043/883 and 25Ω for the HI-5051/883.

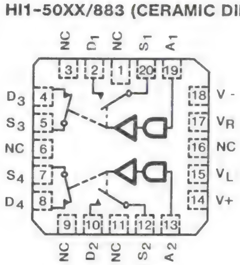
These devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. Performance is further enhanced by Dielectric Isolation processing which insures latch-free operation with very low input and output leakage currents (0.8nA at +25°C). They also feature very low power operation (1.5mW at +25°C). The HI-5043/883 and HI-5051/883 are available in a 16 pin Ceramic DIP or a 20 pin LCC and operate over the -55°C to +125°C temperature range.

Pinouts

LOGIC "0" INPUT
TOP VIEWS



HI1-50XX/883 (CERAMIC DIP)

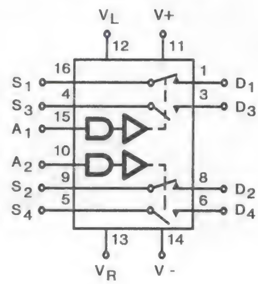


HI4-50XX/883 (CERAMIC LCC)

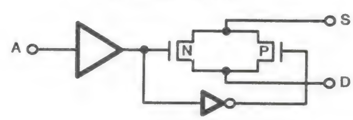
NOTE: Unused pins may be internally connected. Ground all unused pins.

Functional Diagram

LOGIC "1" INPUT



TYPICAL SWITCH



NOTE: Source and Drain are arbitrarily depicted as Analog Input and Output respectively. They may be interchanged without affecting performance.

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 36V
$\pm V_{SUPPLY}$ to Ground (V+, V-) .... ±18V
V_R to Ground .... $-V_{SUPPLY}$
V_L to Ground .... $+V_{SUPPLY}$
Digital and Analog Input Voltage (V_A, V_S, V_D) ..... $+V_{SUPPLY}$ +4V
$-V_{SUPPLY}$ -4V
Peak Current (Source to Drain)
(Pulse at 1ms, 10% Duty Cycle Max) 70mA
Continuous Current (Any Pin) 20mA
Junction Temperature .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... <2000V
Lead Temperature (Soldering 10 sec) .... 300°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	82°C/W	20°C/W
Ceramic LCC Package	80°C/W	20°C/W

Package Power Dissipation at +75°C
Ceramic DIP Package 1.0W
Ceramic LCC Package 1.0W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 12.3mW/°C
Ceramic LCC Package .... 12.5mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±15V
Logic Supply Voltage (V_L) .... +5.0V
Logic Reference Voltage (V_R) 0.0V
Analog Input Voltage (V_S) .... $\pm V_{SUPPLY}$
Address Low Level (V_{AL}) .... 0V to 0.8V
Address High Level (V_{AH}) .... 2.4V to +5.0V

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = 2.4V, V_{AL} = +0.8V, Unused Pins are Grounded, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch "ON" Resistance For HI-5043/883	R_{DS1}	V_D = -10V, I_S = 10mA S1/S2/S3/S4	1	+25°C	-	75	Ω
			2, 3	-55°C to +125°C	-	150	Ω
		V_D = 10V, I_S = -10mA S1/S2/S3/S4	1	+25°C	-	75	Ω
			2, 3	-55°C to +125°C	-	150	Ω
Switch "ON" Resistance For HI-5051/883	R_{DS2}	V_D = -10V, I_S = 10mA S1/S2/S3/S4	1	+25°C	-	45	Ω
			2, 3	-55°C to +125°C	-	50	Ω
		V_D = 10V, I_S = -10mA S1/S2/S3/S4	1	+25°C	-	45	Ω
			2, 3	-55°C to +125°C	-	50	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = -10V, V_D = 10V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = 10V, V_D = -10V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_D = -10V, V_S = 10V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_D = 10V, V_S = -10V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = 10V S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-200	200	nA
		V_D = V_S = -10V S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-200	200	nA

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = 2.4V, V_{AL} = +0.8V, Unused Pins are Grounded, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	MAX	UNITS
Low Level Address Current	I_{AL}	$V_A = 0V$ A_1, A_2	1	+25°C	-1	1	μA
			2, 3	-55°C to +125°C	-10	1	μA
High Level Address Current	I_{AH}	$V_A = 2.4V, 5V$ A_1, A_2	1	+25°C	-1	1	μA
			2, 3	-55°C to +125°C	-1	10	μA
Positive Supply Current	$+I_{CC}$	$V_A = 0V, 5V$ A_1, A_2	1	+25°C	-	200	μA
			2, 3	-55°C to +125°C	-	300	μA
Negative Supply Current	$-I_{CC}$	$V_A = 0V, 5V$ A_1, A_2	1	+25°C	-200	-	μA
			2, 3	-55°C to +125°C	-300	-	μA
Logic Supply Current	$+I_L$	$V_A = 0V, 5V$	1	+25°C	-	200	μA
			2, 3	-55°C to +125°C	-	300	μA
Reference Supply Current	$+I_R$	$V_A = 0V, 5V$	1	+25°C	-200	-	μA
			2, 3	-55°C to +125°C	-300	-	μA

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = +5.0V, V_{AL} = +0.0V, Unused Pins are Grounded, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	MAX	UNITS
Turn "ON" Time	t_{ON}	$V_S = 10V, -10V$ $C_L = 10pF$ $R_L = 1k\Omega$	11	-55°C	-	450	ns
			9	+25°C	-	500	ns
			10	+125°C	-	800	ns
Turn "OFF" Time	t_{OFF}	$V_S = 10V, -10V$ $C_L = 10pF$ $R_L = 1k\Omega$	11	-55°C	-	350	ns
			9	+25°C	-	450	ns
			10	+125°C	-	600	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Characterized at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = 4.0V, V_{AL} = 0.8V, Unused Pins are Grounded, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
"On" Resistance Match (Channel to Channel) for HI-5043/883	R_{ON1} Match	V_D = ±10V I_D = 10mA	1	+25°C	-	10	Ω
"On" Resistance Match (Channel to Channel) for HI-5051/883	R_{ON2} Match	V_D = ±10V I_D = 10mA	1	+25°C	-	10	Ω
Address Capacitance	C_A	V_A = 0V, 5V	1	+25°C	-	45	pF
Switch Input Capacitance	$C_{S(OFF)}$	Switch Off: V_A = 0V	1	+25°C	-	60	pF
Switch Output Capacitance	$C_{D(OFF)}$	Switch Off: V_A = 0V	1	+25°C	-	60	pF
	$C_{D(ON)}$	Switch On: V_A = 5V	1	+25°C	-	60	pF
Drain to Source Capacitance	$C_{DS(OFF)}$	Switch Off: V_A = 0V	1	+25°C	-	10	pF
Off Isolation	V_{ISO}	V_S = $2V_{p-p}$ @ f = 100kHz R_L = 100Ω	1	+25°C	-	60	dB
Crosstalk	V_{CT}	V_S = $2V_{p-p}$ @ f = 100kHz R_L = 100Ω	1	+25°C	-	60	dB
Charge Transfer Error	V_{CTE}	V_S = GND, C_L = 10,000pF V_A = 0 to 4V @ f = 200kHz	1	+25°C	-	30	mV

NOTE 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

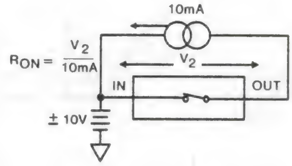
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

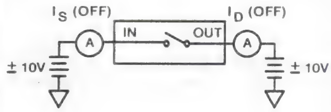
* PDA applies to Subgroup 1 only.

Test Circuits

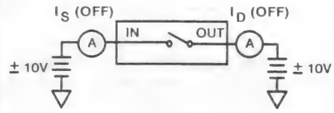
R_{DS}



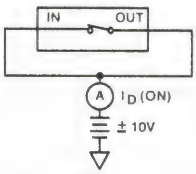
$I_{S(OFF)}$



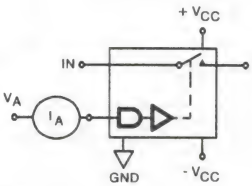
$I_{D(OFF)}$



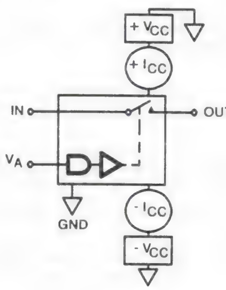
$I_{D(ON)}$



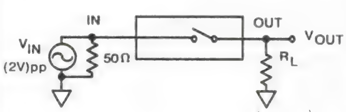
ADDRESS CURRENT



SUPPLY CURRENTS

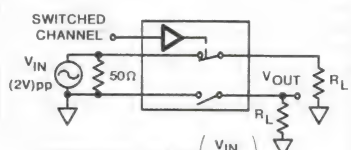


OFF ISOLATION



$$\text{"OFF" ISOLATION} = 20 \text{ LOG} \left(\frac{V_{IN}}{V_{OUT}}\right)$$

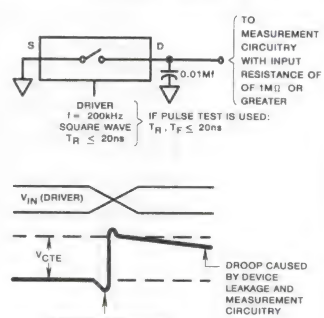
CROSSTALK



$$\text{"CROSSTALK"} = 20 \text{ LOG} \left(\frac{V_{IN}}{V_{OUT}}\right)$$

NOTE: Applies only to DUAL or DOUBLE THROW switches.

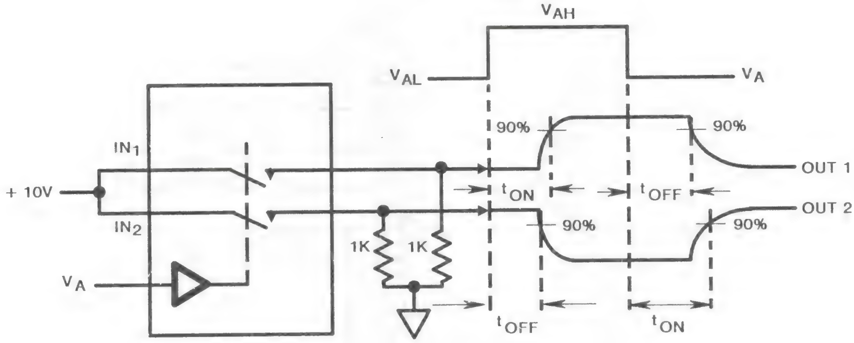
CHARGE TRANSFER



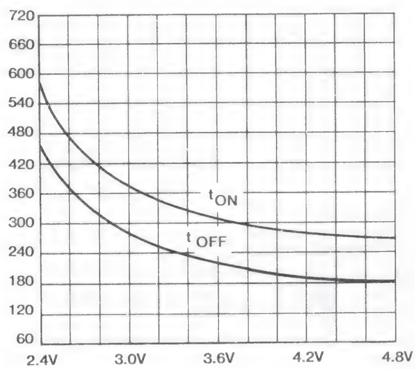
NOTE: V_{CTE} may be a positive or negative value.

Test Characteristics

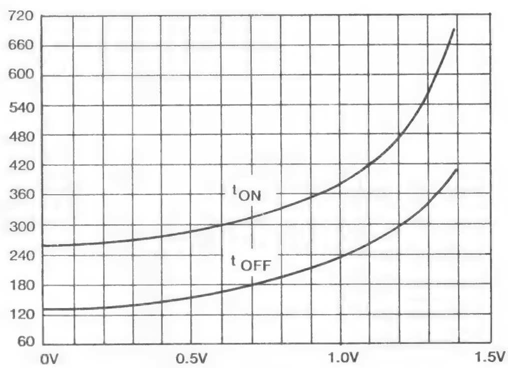
ON/OFF SWITCH TIME (t_{ON}, t_{OFF})



SWITCHING TIMES FOR POSITIVE DIGITAL TRANSITION

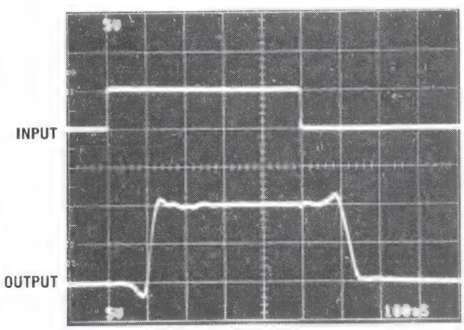


SWITCHING TIMES FOR NEGATIVE DIGITAL TRANSITION

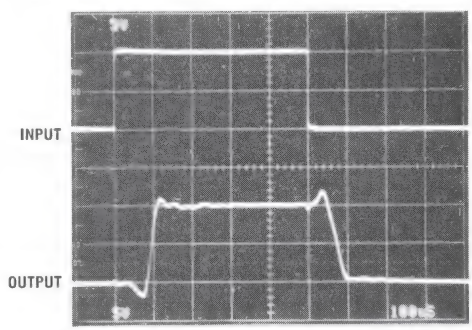


Test Waveforms

Vertical Scale: Input = 5V/Div., (TTL; V_{AH} = 5V, V_{AL} = 0V)
Output = 5V/Div.
Horizontal Scale: 100ns/Div.

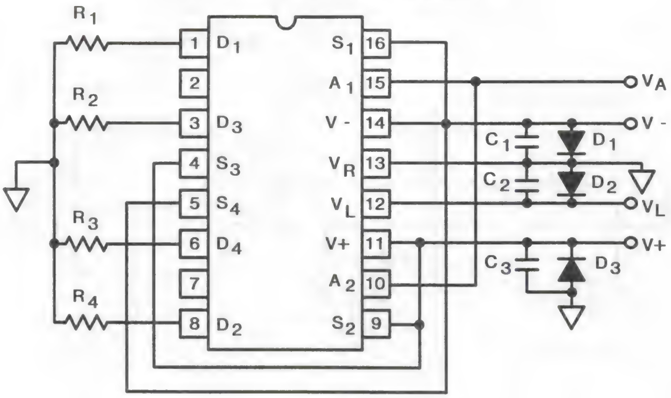


Vertical Scale: Input = 5V/Div., (CMOS; V_{AH} = 10V, V_{AL} = 0V)
Output = 5V/Div.
Horizontal Scale: 100ns/Div.

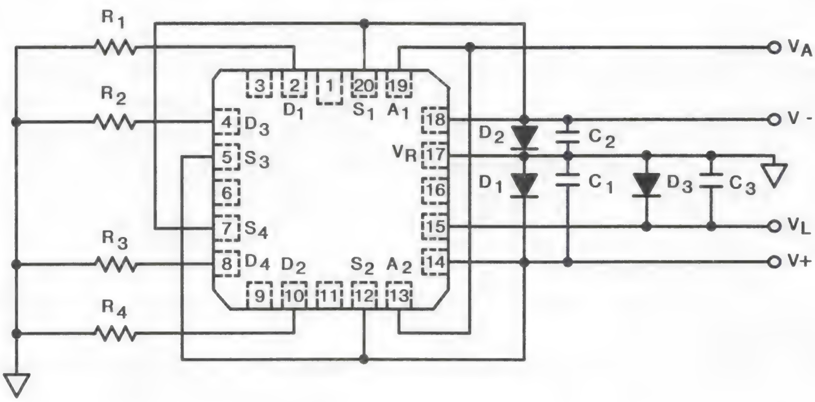


Burn-In Circuits

HI-5043/883 HI-5051/883 CERAMIC DIP



HI-5043/883 HI-5051/883 CERAMIC LCC

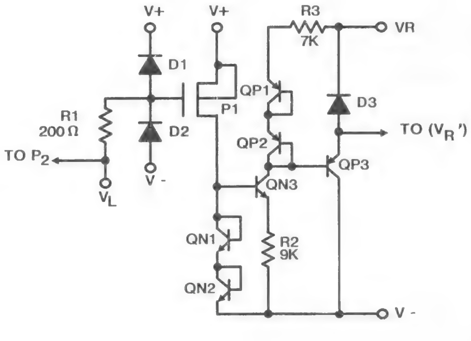


NOTES:

R_1 thru R_4 = 10kΩ, ±5%, 1/4W (Min)
C_1, C_2, C_3, = 0.01µF/Socket (Min) or 0.1µF/Row, (Min)
D_1, D_2, D_3 = IN4002 or Equivalent/Board
V_L = 5.5 ± 0.5V
A_1 = A_2 = 5.5 ± 0.5V
$|(V+) - (V-)|$ = 30V

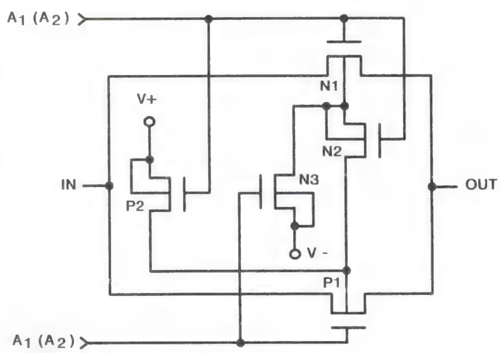
Schematic Diagram

TTL/CMOS REFERENCE CIRCUIT *

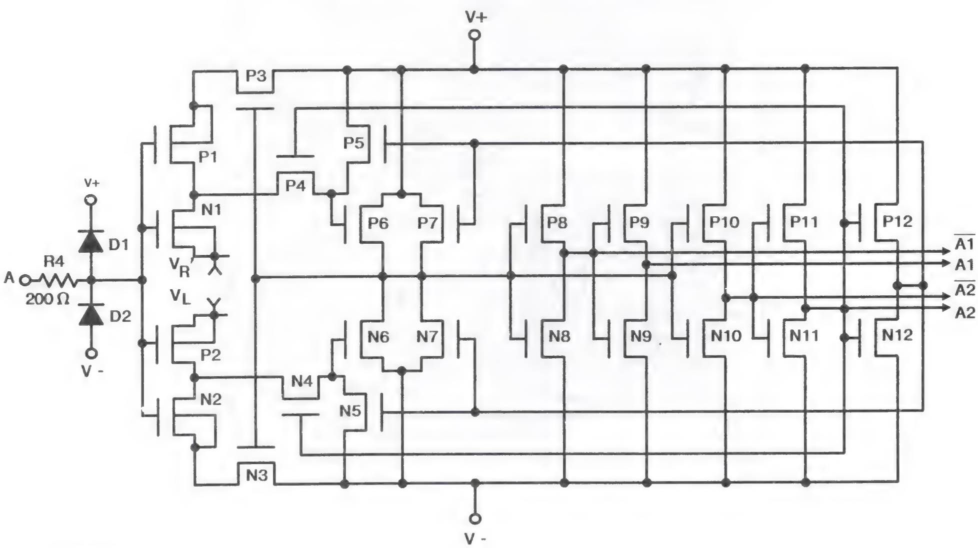


* Connect V+ to V_L for minimizing power consumption when driving from CMOS circuits.

SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



All N-Channel Bodies to V–
All P-Channel Bodies to V+
Except as Shown

Die Characteristics

DIE DIMENSIONS:
96 x 81 x 19mils
(2430 x 2050 x 480μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride over Silox
Silox Thickness: 12kÅ ± 2kÅ
Nitride Thickness: 3.5kÅ ± 1kÅ

SUBSTRATE POTENTIAL (Powered-up): V-

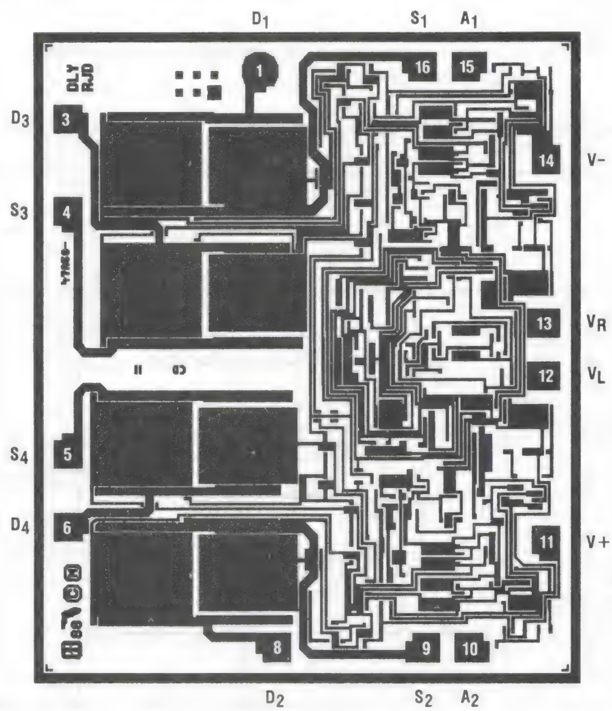
DEVICE COUNT: 82

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:
$1.0 \times 10^5 A/cm^2$ @ 20mA

Metallization Mask Layout

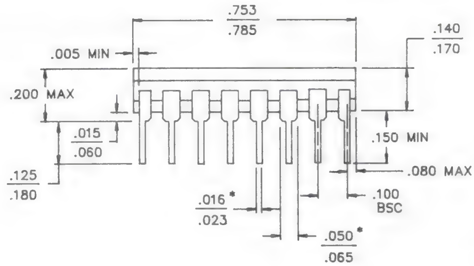
HI-5043/883 HI-5051/883

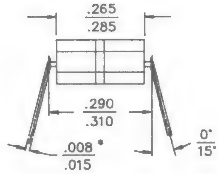


NOTE: Pin Numbers Correspond to DIP Package Only. Unused Pins May Be Connected. Ground All Unused Pins.

Packaging†

16 PIN CERAMIC DIP



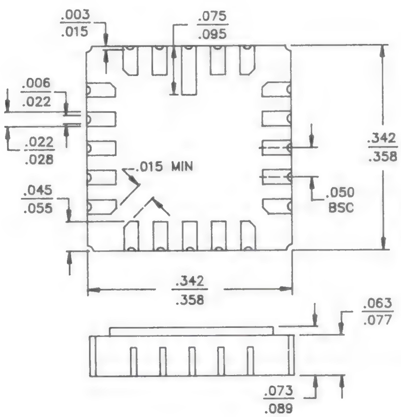


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-2

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

HI-5043
HI-5051

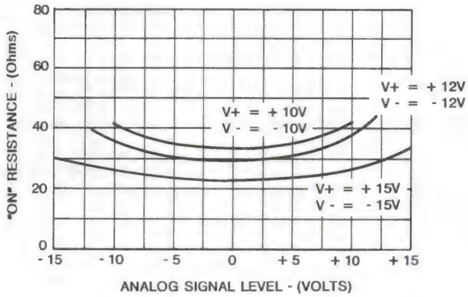
DESIGN INFORMATION

Dual SPDT CMOS Analog Switch

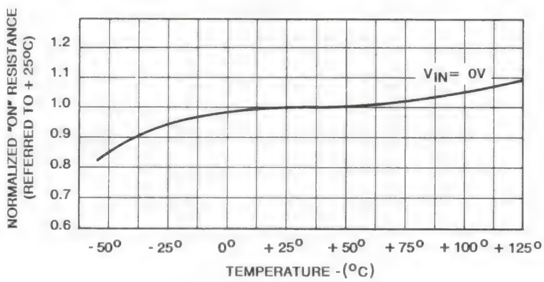
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

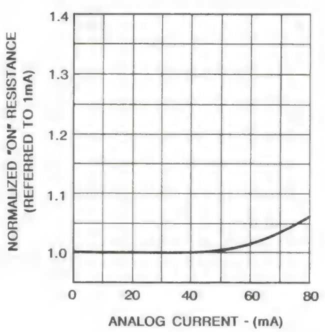
"ON" RESISTANCE vs. ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE



NORMALIZED "ON" RESISTANCE vs. TEMPERATURE



NORMALIZED "ON" RESISTANCE vs. ANALOG CURRENT

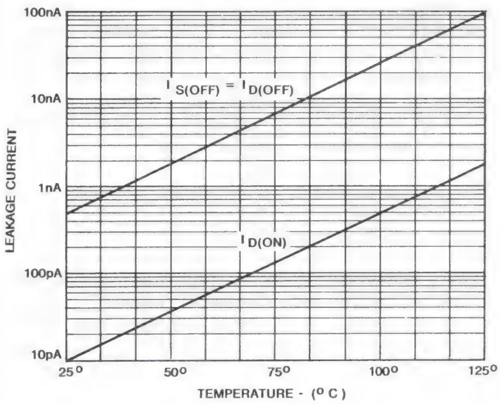


DESIGN INFORMATION (Continued)

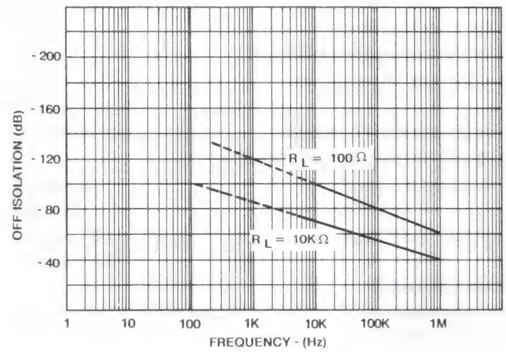
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

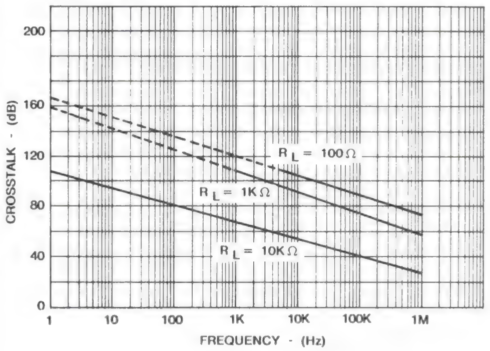
ON/OFF LEAKAGE CURRENT vs. TEMPERATURE



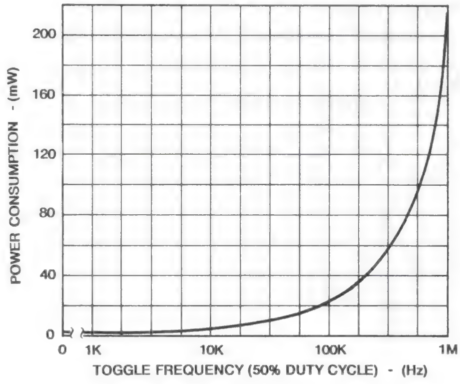
"OFF" ISOLATION vs. FREQUENCY



CROSSTALK vs. FREQUENCY



POWER CONSUMPTION vs. FREQUENCY



4

CMOS ANALOG SWITCHES

HI-5044/883

January 1989

DPST CMOS Analog Switch

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Wide Analog Signal Range .... ±15V
- Low "ON" Resistance .... 50Ω (Typ) 150Ω (Max)
- High Current Capability .... 70mA (Max)
- Break-Before-Make Switching
  - Turn-On Time .... 370ns (Typ) 800ns (Max)
  - Turn-Off Time .... 280ns (Typ) 400ns (Max)
- No Latch-Up
- Input MOS Gates Are Protected From Electrostatic Discharge
- DTL, TTL, CMOS, PMOS Compatible

Applications

- High Frequency Switching
- Sample and Hold
- Digital Filters
- Operational Amplifier Gain Switching

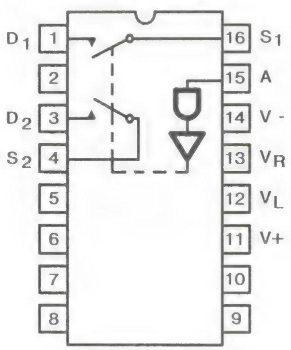
Description

This CMOS analog switch offers low-resistance switching performance for analog voltages up to the supply rails and for signal currents up to 70mA. "ON" resistance is low and stays reasonably constant over the full range of operating signal voltage and current. R_{ON} remains exceptionally constant for input voltages between +5V and -5V and currents up to 50mA. Switch impedance also changes very little over temperature, particularly between 0°C and +75°C. R_{ON} is nominally 50Ω.

This device provides break-before-make switching and is TTL and CMOS compatible for maximum application versatility. Performance is further enhanced by Dielectric Isolation processing which insures latch-free operation with very low input and output leakage currents (0.8nA at +25°C). This switch also features very low power operation (1.5mW at +25°C). The HI-5044/883 is available in a 16 pin Ceramic DIP and operates over the -55°C to +125°C temperature range.

Pinout

LOGIC "0" INPUT
TOP VIEW

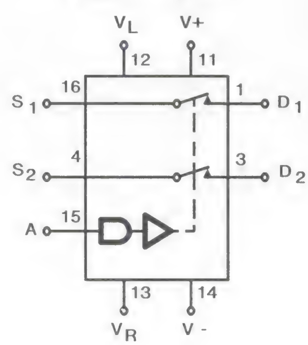


HI1-5044/883 (CERAMIC DIP)

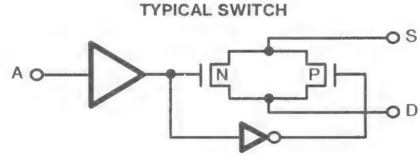
NOTE: Unused pins may be internally connected. Ground all unused pins.

Functional Diagram

LOGIC "1" INPUT



TYPICAL SWITCH



NOTE: Source and Drain are arbitrarily depicted as Analog Input and Output respectively. They may be interchanged without affecting performance.

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 36V
$\pm V_{SUPPLY}$ to Ground (V+, V-) .... ±18V
V_R to Ground .... $-V_{SUPPLY}$
V_L to Ground .... $+V_{SUPPLY}$
Digital and Analog Input Voltage (V_A, V_S, V_D) ..... $+V_{SUPPLY}$ +4V
$-V_{SUPPLY}$ -4V
Peak Current (Source to Drain)
(Pulse at 1ms, 10% Duty Cycle Max) 70mA
Continuous Current (Any Pin) 20mA
Junction Temperature .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... < 2000V
Lead Temperature (Soldering 10 sec) .... 300°C

Thermal Information

Thermal Resistance θ_{ja} θ_{jc}
Ceramic DIP Package .... 82°C/W 20°C/W
Package Power Dissipation Limit at +75°C for $T_J \leq$ +175°C
Ceramic DIP Package 1.0W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 12.3mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±15V
Logic Supply Voltage (V_L) .... +5.0V
Logic Reference Voltage (V_R) 0.0V
Analog Input Voltage (V_S) .... $\pm V_{SUPPLY}$
Address Low Level (V_{AL}) .... 0V to 0.8V
Address High Level (V_{AH}) .... 2.4V to +5.0V

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = 2.4V, V_{AL} = +0.8V, Unused Pins are Grounded, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch "ON" Resistance	R_{DS}	V_D = -10V, I_S = 10mA S1/S2	1	+25°C	-	75	Ω
			2, 3	-55°C to +125°C	-	150	Ω
		V_D = 10V, I_S = -10mA S1/S2	1	+25°C	-	75	Ω
			2, 3	-55°C to +125°C	-	150	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = -10V, V_D = 10V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = 10V, V_D = -10V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_D = -10V, V_S = 10V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_D = 10V, V_S = -10V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = 10V S1/S2	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-200	200	nA
		V_D = V_S = -10V S1/S2	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-200	200	nA
Low Level Address Current	I_{AL}	V_A = 0V	1	+25°C	-1	1	µA
			2, 3	-55°C to +125°C	-10	1	µA
High Level Address Current	I_{AH}	V_A = 2.4V, 5V	1	+25°C	-1	1	µA
			2, 3	-55°C to +125°C	-1	10	µA
Positive Supply Current	$+I_{CC}$	V_A = 0V, 5V	1	+25°C	-	200	µA
			2, 3	-55°C to +125°C	-	300	µA
Negative Supply Current	$-I_{CC}$	V_A = 0V, 5V	1	+25°C	-200	-	µA
			2, 3	-55°C to +125°C	-300	-	µA
Logic Supply Current	$+I_L$	V_A = 0V, 5V	1	+25°C	-	200	µA
			2, 3	-55°C to +125°C	-	300	µA
Reference Supply Current	$+I_R$	V_A = 0V, 5V	1	+25°C	-200	-	µA
			2, 3	-55°C to +125°C	-300	-	µA

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = +5.0V, V_{AL} = +0.0V, Unused Pins are Grounded, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Turn "ON" Time	t_{ON}	V_S = 10V, -10V C_L = 10pF R_L = 1kΩ	11	-55°C	-	450	ns
			9	+25°C	-	500	ns
			10	+125°C	-	800	ns
Turn "OFF" Time	t_{OFF}	V_S = 10V, -10V C_L = 10pF R_L = 1kΩ	11	-55°C	-	350	ns
			9	+25°C	-	450	ns
			10	+125°C	-	600	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Characterized at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = 4.0V, V_{AL} = 0.8V, Unused Pins are Grounded, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
"On" Resistance Match (Channel to Channel)	R_{ON} Match	V_D = ±10V I_D = 10mA	1	+25°C	-	10	Ω
Address Capacitance	C_A	V_A = 0V, 5V	1	+25°C	-	45	pF
Switch Input Capacitance	$C_{S(OFF)}$	Switch Off: V_A = 0V	1	+25°C	-	60	pF
Switch Output Capacitance	$C_{D(OFF)}$	Switch Off: V_A = 0V	1	+25°C	-	60	pF
	$C_{D(ON)}$	Switch On: V_A = 5V	1	+25°C	-	60	pF
Drain to Source Capacitance	$C_{DS(OFF)}$	Switch Off: V_A = 0V	1	+25°C	-	10	pF
Off Isolation	V_{ISO}	$V_S = 2V_{p-p}$ @ f = 100kHz R_L = 100Ω	1	+25°C	-	60	dB
Charge Transfer Error	V_{CTE}	V_S = GND, C_L = 10,000pF V_A = 0 to 4V @ f = 200kHz	1	+25°C	-	30	mV

NOTE 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

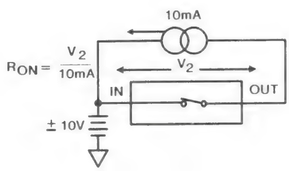
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

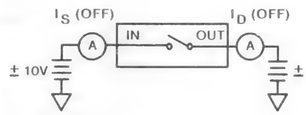
* PDA applies to Subgroup 1 only.

Test Circuits

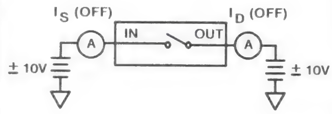
R_{DS}



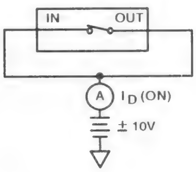
$I_{S(OFF)}$



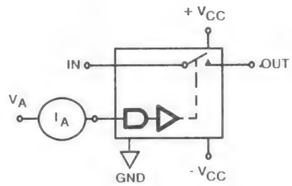
$I_{D(OFF)}$



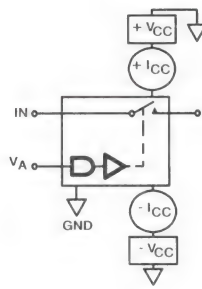
$I_{D(ON)}$



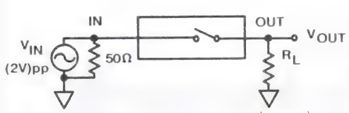
ADDRESS CURRENT



SUPPLY CURRENTS

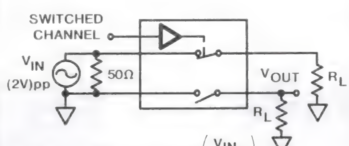


OFF ISOLATION



"OFF" ISOLATION = $20 \text{ LOG} \left(\frac{V_{IN}}{V_{OUT}} \right)$

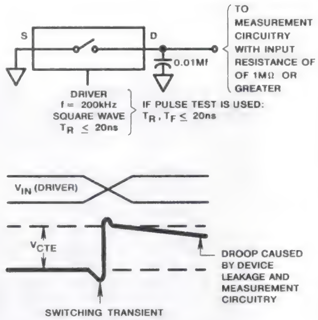
CROSSTALK



"CROSSTALK" = $20 \text{ LOG} \left(\frac{V_{IN}}{V_{OUT}} \right)$

NOTE: Applies only to DUAL or DOUBLE THROW switches.

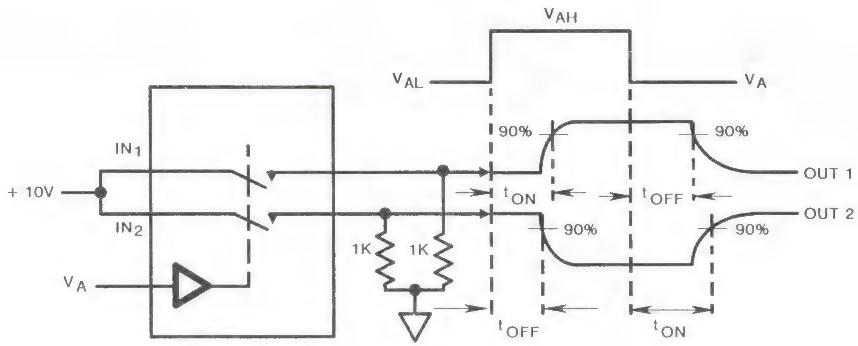
CHARGE TRANSFER



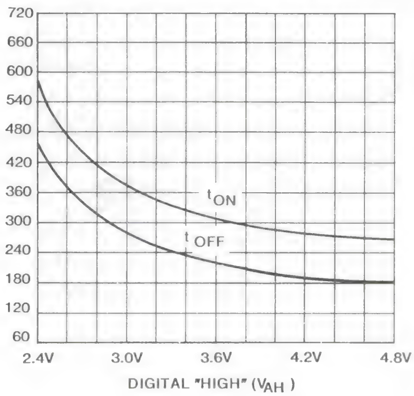
NOTE: V_{CTE} may be a positive or negative value.

Test Characteristics

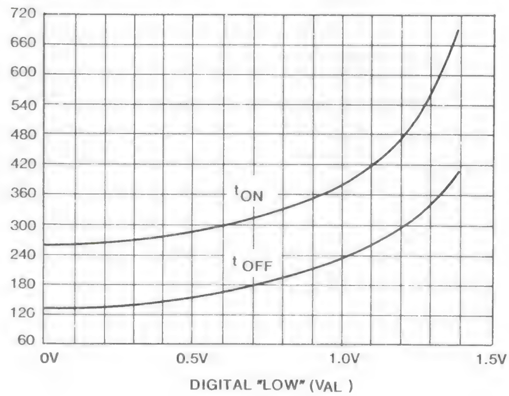
ON/OFF SWITCH TIME (t_{ON}, t_{OFF})



SWITCHING TIMES FOR POSITIVE DIGITAL TRANSITION



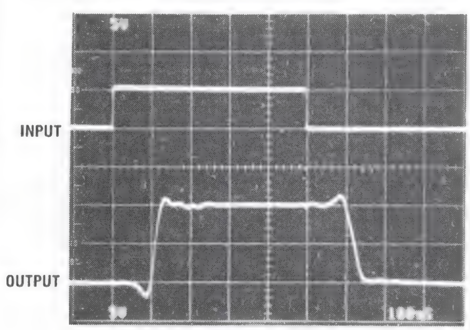
SWITCHING TIMES FOR NEGATIVE DIGITAL TRANSITION



Test Waveforms

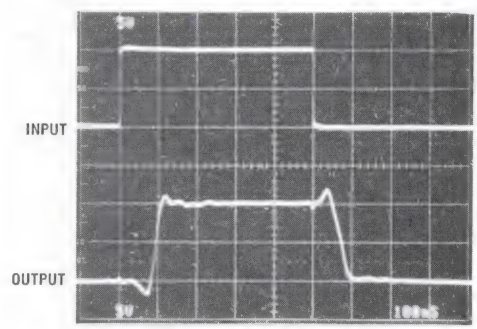
Vertical Scale: Input = 5V/Div., (TTL; V_{AH} = 5V, V_{AL} = 0V)
Output = 5V/Div.

Horizontal Scale: 100ns/Div.



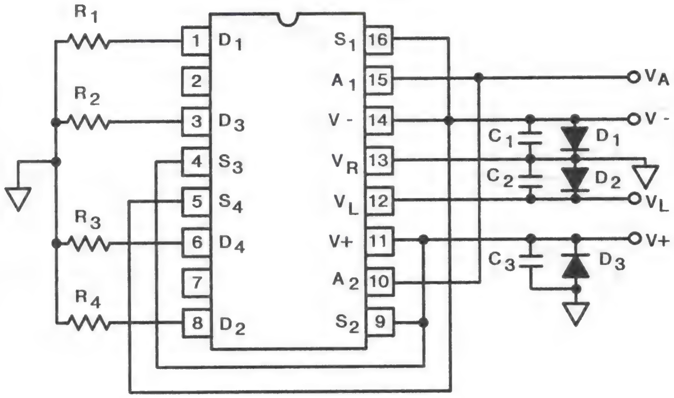
Vertical Scale: Input = 5V/Div., (CMOS; V_{AH} = 10V, V_{AL} = 0V)
Output = 5V/Div.

Horizontal Scale: 100ns/Div.



Burn-In Circuit

HI-5044/883 CERAMIC DIP



NOTES:

R_1 thru R_4 = 10kΩ, ±5%, 1/4W (Min)

C_1, C_2, C_3, = 0.01μF/Socket (Min) or 0.1μF/Row, (Min)

D_1, D_2, D_3 = IN4002 or Equivalent/Board

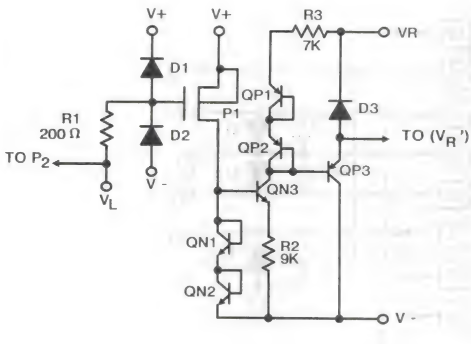
V_L = 5.5 ± 0.5V

A_1 = A_2 = 5.5 ± 0.5V

$|(V+) - (V-)| = 30V$

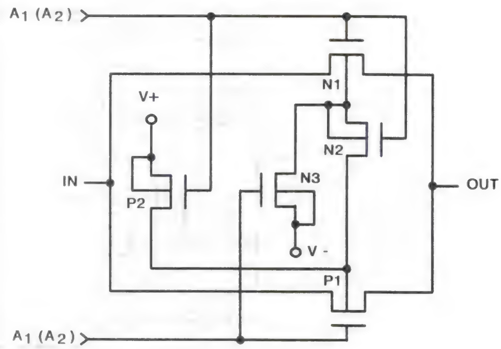
Schematic Diagram

TTL/CMOS REFERENCE CIRCUIT *

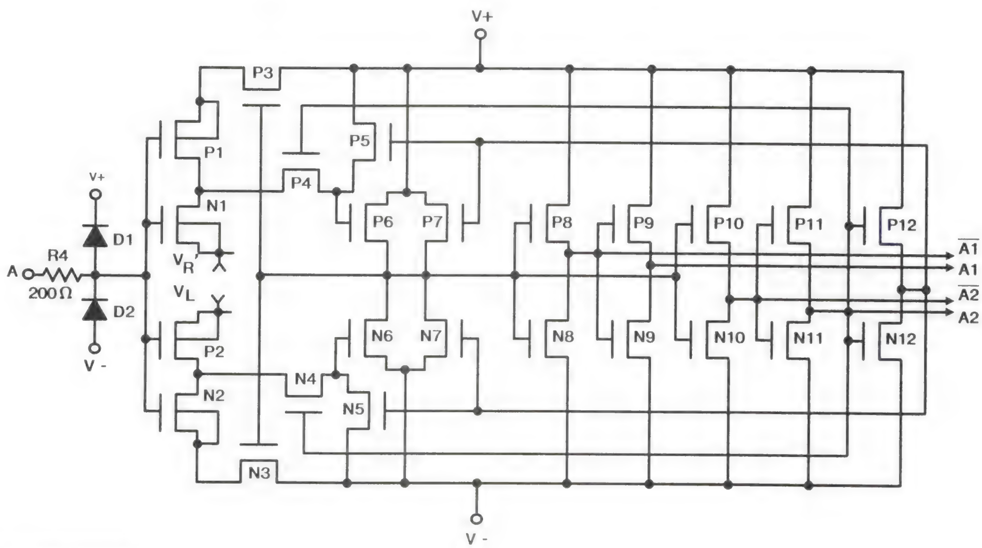


* Connect V+ to V_L for minimizing power consumption when driving from CMOS circuits.

SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



All N-Channel Bodies to V-
All P-Channel Bodies to V+
Except as Shown

Die Characteristics

DIE DIMENSIONS:
96 x 81 x 19mils
(2430 x 2050 x 480μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride over Silox
Silox Thickness: 12kÅ ± 2kÅ
Nitride Thickness: 3.5kÅ ± 1kÅ

SUBSTRATE POTENTIAL (Powered-up): V-

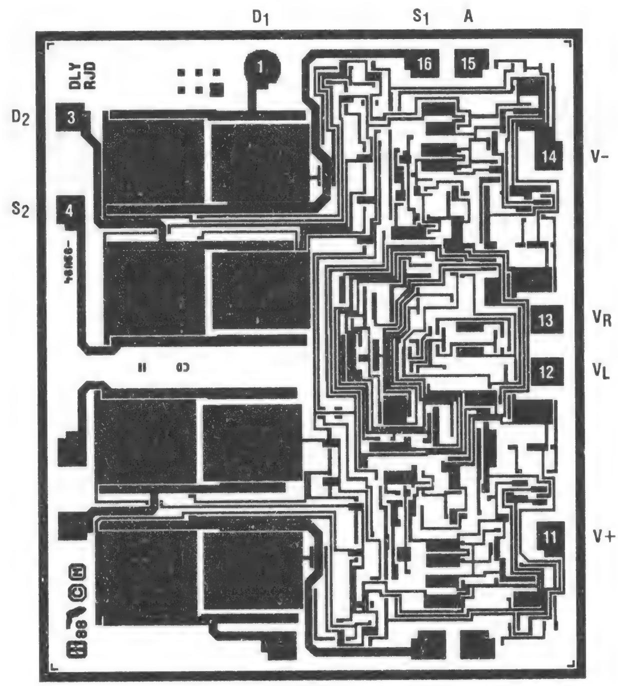
DEVICE COUNT: 82

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)

WORST CASE CURRENT DENSITY:
$1.0 \times 10^5 A/cm^2$ @ 20mA

Metallization Mask Layout

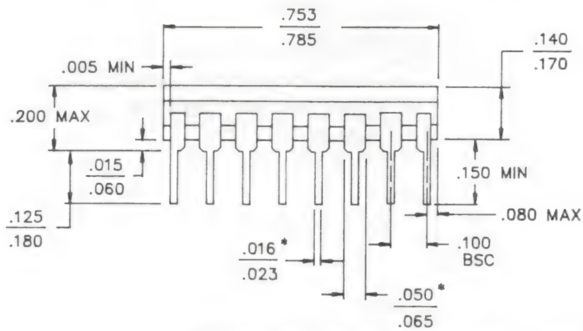
HI-5044/883

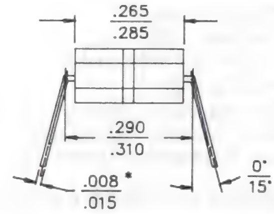


NOTE: Pin Numbers Correspond to DIP Package Only. Unused Pins May Be Connected. Ground All Unused Pins.

Packaging†

16 PIN CERAMIC DIP





* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
- Material: Glass Frit
- Temperature: 450°C ± 10°C
- Method: Furnace Seal

INTERNAL LEAD WIRE:
- Material: Aluminum
- Diameter: 1.25 Mil
- Bonding Method: Ultrasonic

COMPLIANT OUTLINE: 38510 D-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

HI-5044

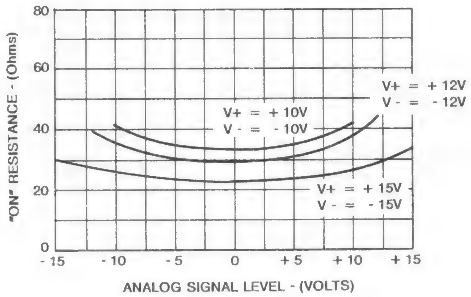
DESIGN INFORMATION

DPST CMOS Analog Switch

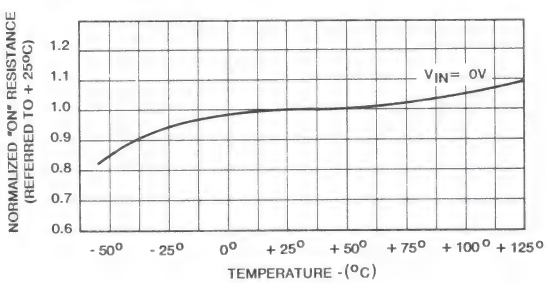
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

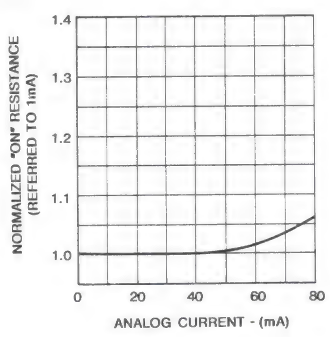
"ON" RESISTANCE vs. ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE



NORMALIZED "ON" RESISTANCE vs. TEMPERATURE



NORMALIZED "ON" RESISTANCE vs. ANALOG CURRENT



4

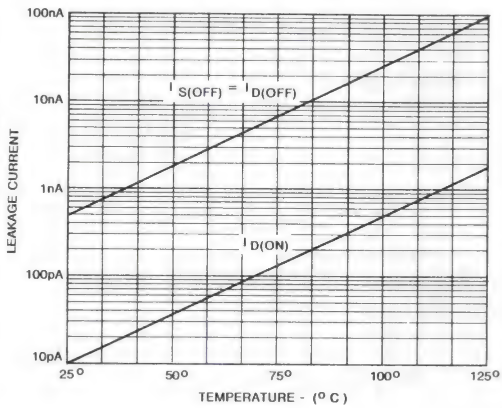
CMOS ANALOG SWITCHES

DESIGN INFORMATION (Continued)

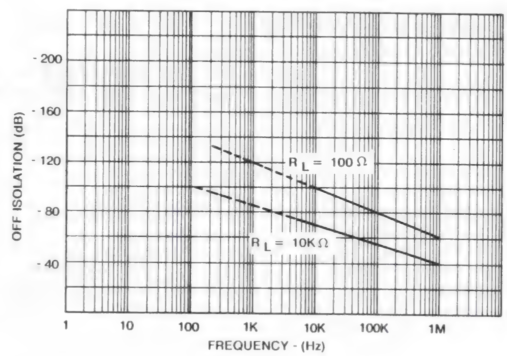
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

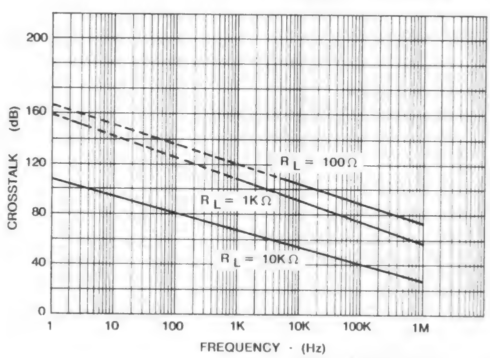
ON/OFF LEAKAGE CURRENT vs. TEMPERATURE



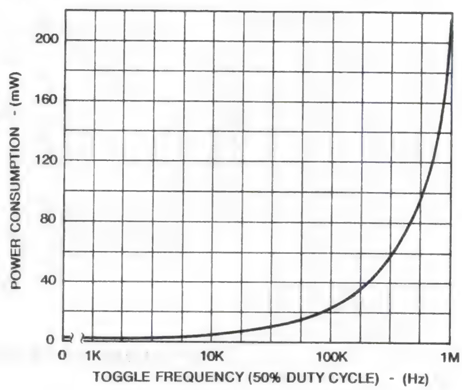
"OFF" ISOLATION vs. FREQUENCY



CROSSTALK vs. FREQUENCY



POWER CONSUMPTION vs. FREQUENCY



HARRIS

HI-5045/883
HI-5049/883

January 1989

Dual DPST CMOS Analog Switch

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Wide Analog Signal Range .... ±15V
- Low "ON" Resistance
  - HI-5045 .... 50Ω (Typ) 150Ω (Max)
  - HI-5049 .... 25Ω (Typ) 50Ω (Max)
- High Current Capability .... 70mA (Max)
- Break-Before-Make Switching
  - Turn-On Time .... 370ns (Typ) 800ns (Max)
  - Turn-Off Time .... 280ns (Typ) 400ns (Max)
- No Latch-Up
- Input MOS Gates Are Protected From Electrostatic Discharge
- DTL, TTL, CMOS, PMOS Compatible

Applications

- High Frequency Switching
- Sample and Hold
- Digital Filters
- Operational Amplifier Gain Switching

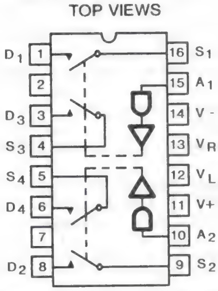
Description

These CMOS analog switches offer low-resistance switching performance for analog voltages up to the supply rails and for signal currents up to 70mA. "ON" resistance is low and stays reasonably constant over the full range of operating signal voltage and current. R_{ON} remains exceptionally constant for input voltages between +5V and -5V and currents up to 50mA. Switch impedance also changes very little over temperature, particularly between 0°C and +75°C. R_{ON} is nominally 50Ω for the HI-5045/883 and 25Ω for the HI-5049/883.

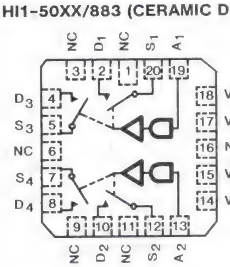
These devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. Performance is further enhanced by Dielectric Isolation processing which insures latch-free operation with very low input and output leakage currents (0.8nA at +25°C). They also feature very low power operation (1.5mW at +25°C). The HI-5045/883 and HI-5049/883 are available in a 16 pin Ceramic DIP or a 20 pin LCC and operate over the -55°C to +125°C temperature range.

Pinouts

LOGIC "0" INPUT
TOP VIEWS



HI1-50XX/883 (CERAMIC DIP)

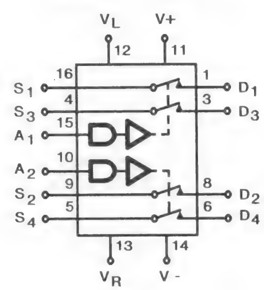


HI4-50XX/883 (CERAMIC LCC)

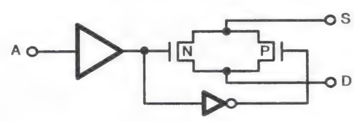
NOTE: Unused pins may be internally connected. Ground all unused pins.

Functional Diagram

LOGIC "1" INPUT



TYPICAL SWITCH



NOTE: Source and Drain are arbitrarily depicted as Analog Input and Output respectively. They may be interchanged without affecting performance.

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 36V
$\pm V_{SUPPLY}$ to Ground (V+, V-) .... ±18V
V_R to Ground .... $-V_{SUPPLY}$
V_L to Ground .... $+V_{SUPPLY}$
Digital and Analog Input Voltage (V_A, V_S, V_D) ..... $+V_{SUPPLY}$ +4V
$-V_{SUPPLY}$ -4V
Peak Current (Source to Drain)
(Pulse at 1ms, 10% Duty Cycle Max) 70mA
Continuous Current (Any Pin) 20mA
Junction Temperature .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... <2000V
Lead Temperature (Soldering 10 sec) .... 300°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	82°C/W	20°C/W
Ceramic LCC Package	80°C/W	20°C/W

Package Power Dissipation at +75°C
Ceramic DIP Package 1.0W
Ceramic LCC Package 1.0W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 12.3mW/°C
Ceramic LCC Package .... 12.5mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±15V
Logic Supply Voltage (V_L) .... +5.0V
Logic Reference Voltage (V_R) 0.0V
Analog Input Voltage (V_S) .... $\pm V_{SUPPLY}$
Address Low Level (V_{AL}) .... 0V to 0.8V
Address High Level (V_{AH}) .... 2.4V to +5.0V

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = 2.4V, V_{AL} = +0.8V, Unused Pins are Grounded, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch "ON" Resistance For HI-5045/883	R_{DS1}	V_D = -10V, I_S = 10mA S1/S2/S3/S4	1	+25°C	-	75	Ω
			2, 3	-55°C to +125°C	-	150	Ω
		V_D = 10V, I_S = -10mA S1/S2/S3/S4	1	+25°C	-	75	Ω
			2, 3	-55°C to +125°C	-	150	Ω
Switch "ON" Resistance For HI-5049/883	R_{DS2}	V_D = -10V, I_S = 10mA S1/S2/S3/S4	1	+25°C	-	45	Ω
			2, 3	-55°C to +125°C	-	50	Ω
		V_D = 10V, I_S = -10mA S1/S2/S3/S4	1	+25°C	-	45	Ω
			2, 3	-55°C to +125°C	-	50	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = -10V, V_D = 10V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = 10V, V_D = -10V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_D = -10V, V_S = 10V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_D = 10V, V_S = -10V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = 10V S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-200	200	nA
		V_D = V_S = -10V S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-200	200	nA

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = 2.4V, V_{AL} = +0.8V, Unused Pins are Grounded, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Low Level Address Current	I_{AL}	V_A = 0V A_1, A_2	1	+25°C	-1	1	µA
			2, 3	-55°C to +125°C	-10	1	µA
High Level Address Current	I_{AH}	V_A = 2.4V, 5V A_1, A_2	1	+25°C	-1	1	µA
			2, 3	-55°C to +125°C	-1	10	µA
Positive Supply Current	$+I_{CC}$	V_A = 0V, 5V A_1, A_2	1	+25°C	-	200	µA
			2, 3	-55°C to +125°C	-	300	µA
Negative Supply Current	$-I_{CC}$	V_A = 0V, 5V A_1, A_2	1	+25°C	-200	-	µA
			2, 3	-55°C to +125°C	-300	-	µA
Logic Supply Current	$+I_L$	V_A = 0V, 5V	1	+25°C	-	200	µA
			2, 3	-55°C to +125°C	-	300	µA
Reference Supply Current	$+I_R$	V_A = 0V, 5V	1	+25°C	-200	-	µA
			2, 3	-55°C to +125°C	-300	-	µA

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = +5.0V, V_{AL} = +0.0V, Unused Pins are Grounded, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Turn "ON" Time	t_{ON}	V_S = 10V, -10V C_L = 10pF R_L = 1kΩ	11	-55°C	-	450	ns
			9	+25°C	-	500	ns
			10	+125°C	-	800	ns
Turn "OFF" Time	t_{OFF}	V_S = 10V, -10V C_L = 10pF R_L = 1kΩ	11	-55°C	-	350	ns
			9	+25°C	-	450	ns
			10	+125°C	-	600	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Characterized at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = 4.0V, V_{AL} = 0.8V, Unused Pins are Grounded, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
"On" Resistance Match (Channel to Channel) for HI-5045/883	R_{ON1} Match	$V_D = \pm10V$ $I_D = 10mA$	1	+25°C	-	10	Ω
"On" Resistance Match (Channel to Channel) for HI-5049/883	R_{ON2} Match	$V_D = \pm10V$ $I_D = 10mA$	1	+25°C	-	10	Ω
Address Capacitance	C_A	$V_A = 0V, 5V$	1	+25°C	-	45	pF
Switch Input Capacitance	$C_{S(OFF)}$	Switch Off: $V_A = 0V$	1	+25°C	-	60	pF
Switch Output Capacitance	$C_{D(OFF)}$	Switch Off: $V_A = 0V$	1	+25°C	-	60	pF
	$C_{D(ON)}$	Switch On: $V_A = 5V$	1	+25°C	-	60	pF
Drain to Source Capacitance	$C_{DS(OFF)}$	Switch Off: $V_A = 0V$	1	+25°C	-	10	pF
Off Isolation	V_{ISO}	$V_S = 2V_{p-p}$ @ f = 100kHz $R_L = 100\Omega$	1	+25°C	-	60	dB
Crosstalk	V_{CT}	$V_S = 2V_{p-p}$ @ f = 100kHz $R_L = 100\Omega$	1	+25°C	-	60	dB
Charge Transfer Error	V_{CTE}	V_S = GND, C_L = 10,000pF V_A = 0 to 4V @ f = 200kHz	1	+25°C	-	30	mV

NOTE 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

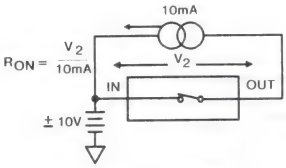
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

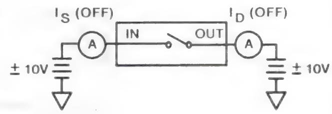
* PDA applies to Subgroup 1 only.

Test Circuits

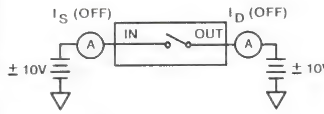
R_{DS}



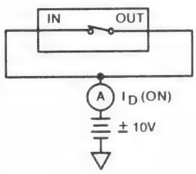
$I_{S(OFF)}$



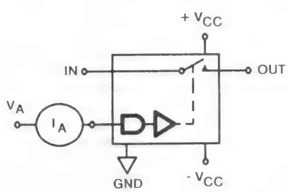
$I_{D(OFF)}$



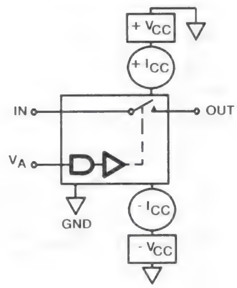
$I_{D(ON)}$



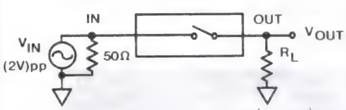
ADDRESS CURRENT



SUPPLY CURRENTS

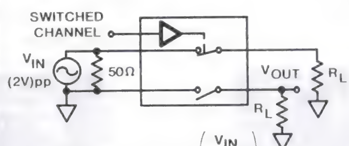


OFF ISOLATION



"OFF" ISOLATION = $20 \text{ LOG} \left(\frac{V_{IN}}{V_{OUT}} \right)$

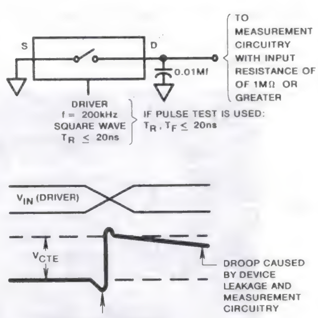
CROSSTALK



"CROSSTALK" = $20 \text{ LOG} \left(\frac{V_{IN}}{V_{OUT}} \right)$

NOTE: Applies only to DUAL or DOUBLE THROW switches.

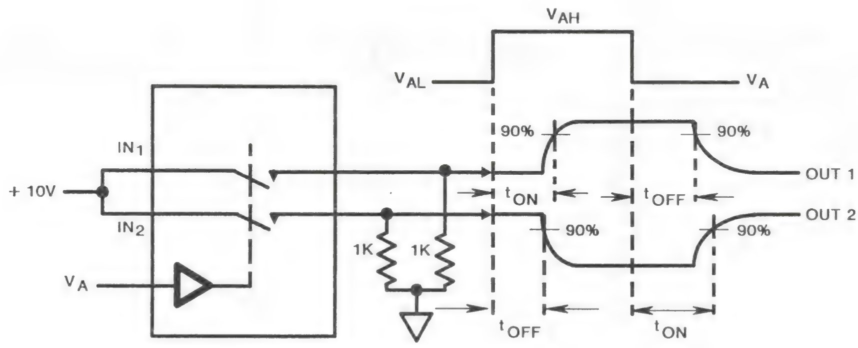
CHARGE TRANSFER



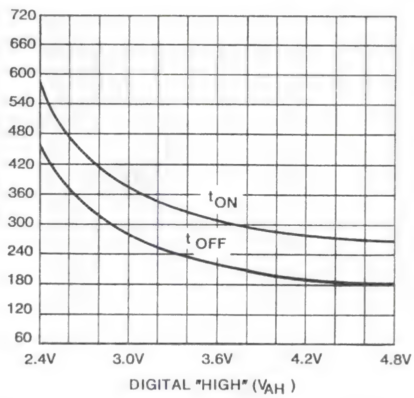
NOTE: V_{CTE} may be a positive or negative value.

Test Characteristics

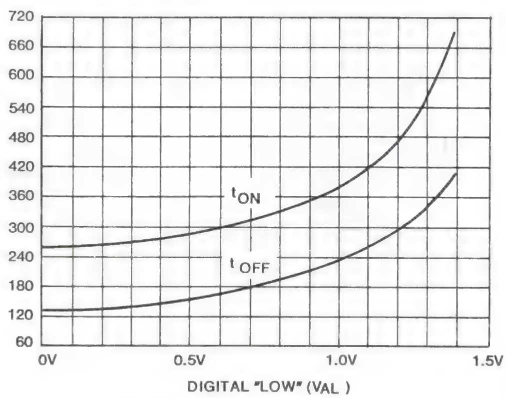
ON/OFF SWITCH TIME (t_{ON}, t_{OFF})



SWITCHING TIMES FOR POSITIVE DIGITAL TRANSITION



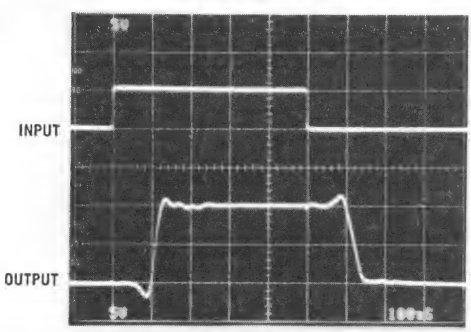
SWITCHING TIMES FOR NEGATIVE DIGITAL TRANSITION



Test Waveforms

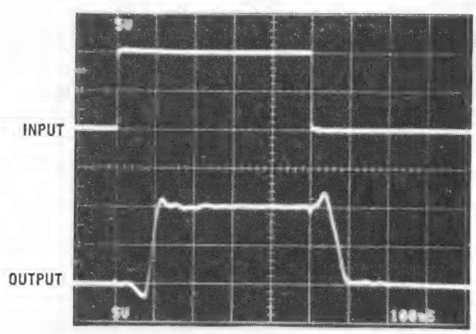
Vertical Scale: Input = 5V/Div., (TTL; V_{AH} = 5V, V_{AL} = 0V)
Output = 5V/Div.

Horizontal Scale: 100ns/Div.



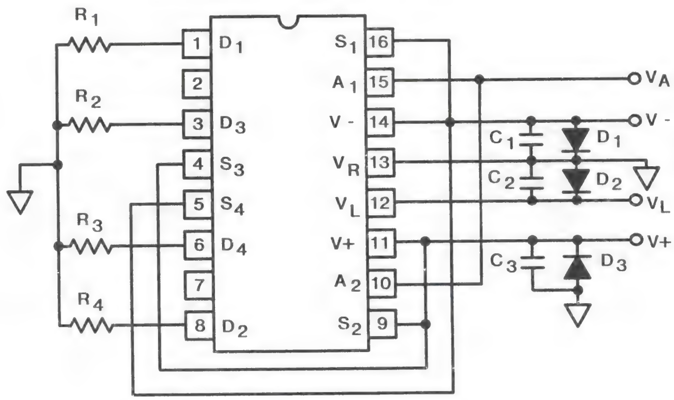
Vertical Scale: Input = 5V/Div., (CMOS; V_{AH} = 10V, V_{AL} = 0V)
Output = 5V/Div.

Horizontal Scale: 100ns/Div.

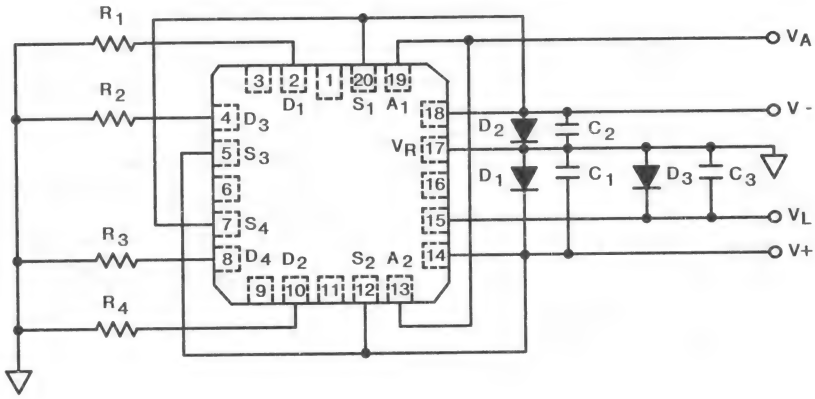


Burn-In Circuits

HI-5045/883 HI-5049/883 CERAMIC DIP



HI-5045/883 HI-5049/883 CERAMIC LCC



NOTES:

R_1 thru R_4 = 10kΩ, ±5%, 1/4W (Min)

C_1, C_2, C_3, = 0.01μF/Socket (Min) or 0.1μF/Row, (Min)

D_1, D_2, D_3 = IN4002 or Equivalent/Board

V_L = 5.5 ± 0.5V

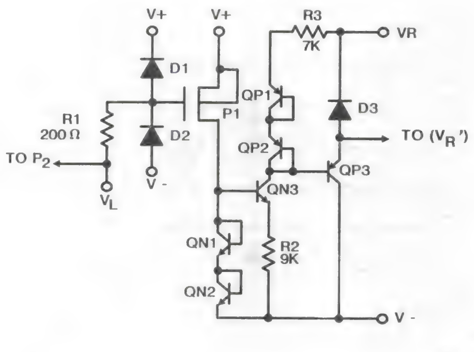
A_1 = A_2 = 5.5 ± 0.5V

$|(V+) - (V-)| = 30V$

4 CMOS ANALOG SWITCHES

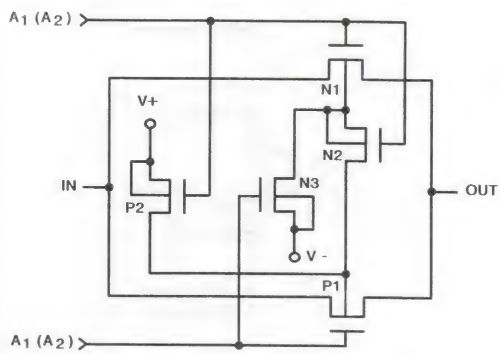
Schematic Diagram

TTL/CMOS REFERENCE CIRCUIT *

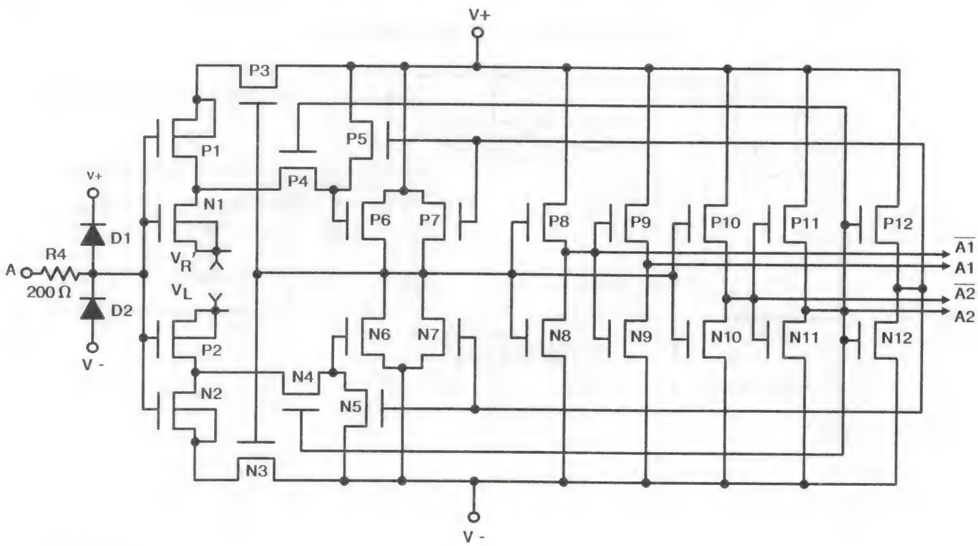


* Connect V+ to V_L for minimizing power consumption when driving from CMOS circuits.

SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



All N-Channel Bodies to V-
All P-Channel Bodies to V+
Except as Shown

Die Characteristics

DIE DIMENSIONS:
96 x 81 x 19mils
(2430 x 2050 x 480μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride over Silox
Silox Thickness: 12kÅ ± 2kÅ
Nitride Thickness: 3.5kÅ ± 1kÅ

SUBSTRATE POTENTIAL (Powered-up): V-

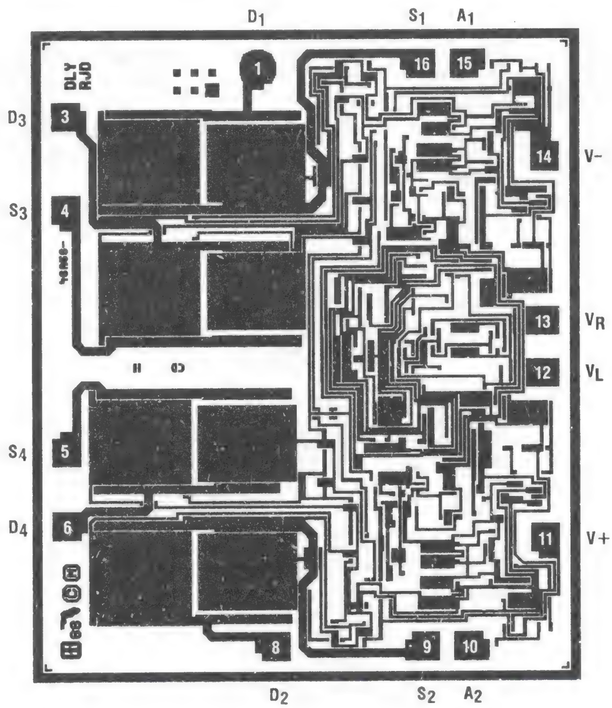
DEVICE COUNT: 82

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:
$1.0 \times 10^5 A/cm^2$ @ 20mA

Metallization Mask Layout

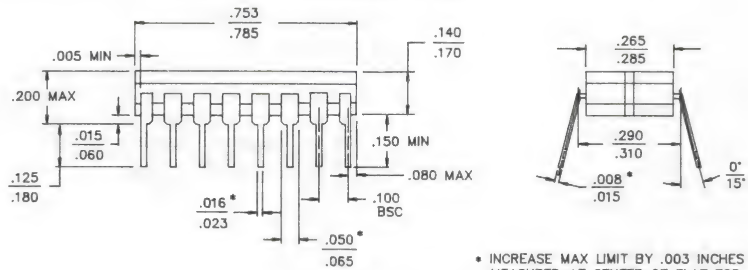
HI-5045/883 HI-5049/883



NOTE: Pin Numbers Correspond to DIP Package Only. Unused Pins May Be Connected. Ground All Unused Pins.

Packaging†

16 PIN CERAMIC DIP

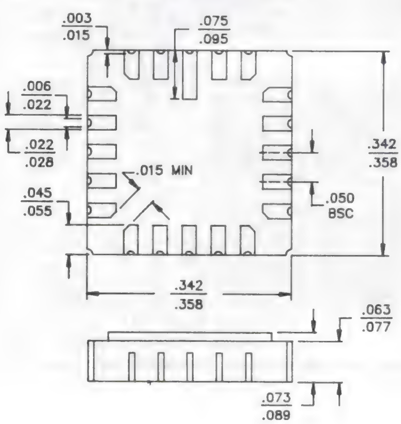


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-2

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

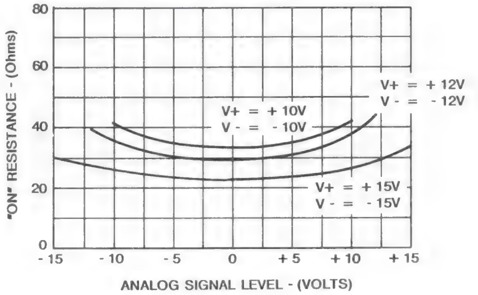
DESIGN INFORMATION

Dual DPST CMOS Analog Switch

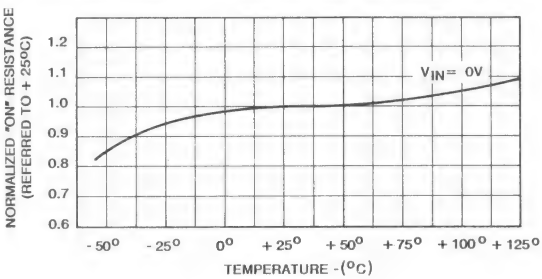
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

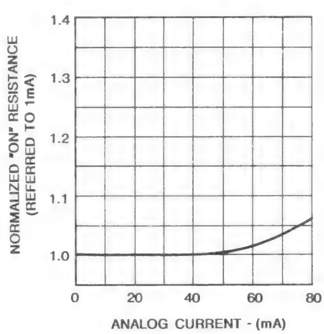
"ON" RESISTANCE vs. ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE



NORMALIZED "ON" RESISTANCE vs. TEMPERATURE



NORMALIZED "ON" RESISTANCE vs. ANALOG CURRENT



4

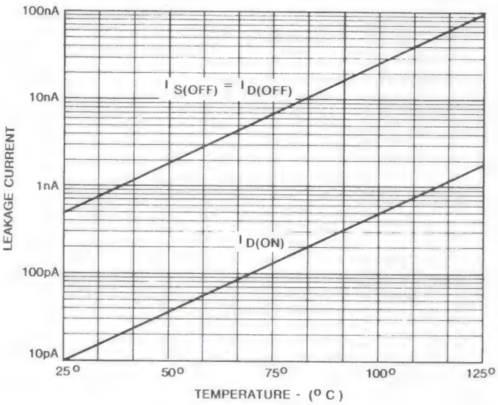
CMOS ANALOG SWITCHES

DESIGN INFORMATION (Continued)

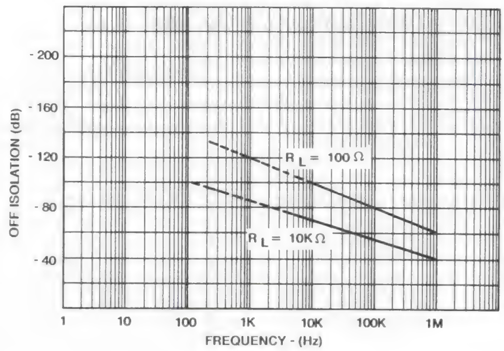
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

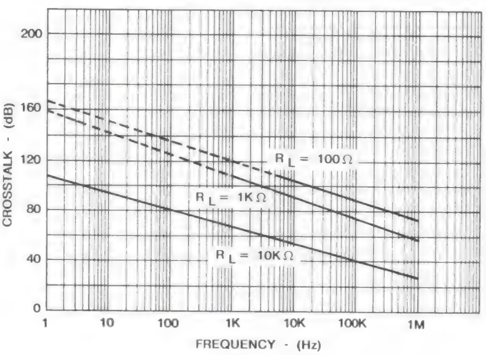
ON/OFF LEAKAGE CURRENT vs. TEMPERATURE



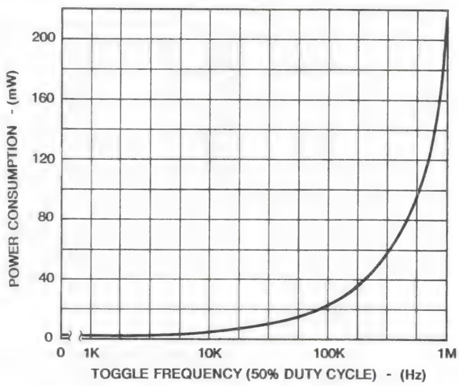
"OFF" ISOLATION vs. FREQUENCY



CROSSTALK vs. FREQUENCY



POWER CONSUMPTION vs. FREQUENCY



HARRIS

HI-5046/883
HI-5046A/883

January 1989

DPDT CMOS Analog Switch

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Wide Analog Signal Range .... ±15V
- Low "ON" Resistance
  - ▸ HI-5046 .... 50Ω (Typ) 150Ω (Max)
  - ▸ HI-5046A .... 25Ω (Typ) 50Ω (Max)
- High Current Capability .... 70mA (Max)
- Break-Before-Make Switching
  - ▸ Turn-On Time .... 370ns (Typ) 800ns (Max)
  - ▸ Turn-Off Time .... 280ns (Typ) 400ns (Max)
- No Latch-Up
- Input MOS Gates Are Protected From Electrostatic Discharge
- DTL, TTL, CMOS, PMOS Compatible

Applications

- High Frequency Switching
- Sample and Hold
- Digital Filters
- Operational Amplifier Gain Switching

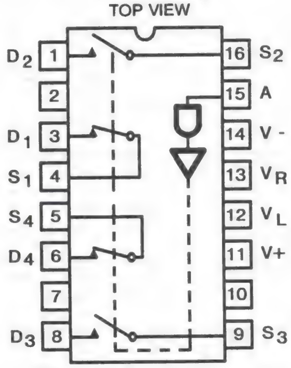
Description

These CMOS analog switches offer low-resistance switching performance for analog voltages up to the supply rails and for signal currents up to 70mA. "ON" resistance is low and stays reasonably constant over the full range of operating signal voltage and current. R_{ON} remains exceptionally constant for input voltages between +5V and -5V and currents up to 50mA. Switch impedance also changes very little over temperature, particularly between 0°C and +75°C. R_{ON} is nominally 50Ω for the HI-5046/883 and 25Ω for the HI-5046A/883.

These devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. Performance is further enhanced by Dielectric Isolation processing which insures latch-free operation with very low input and output leakage currents (0.8nA at +25°C). They also feature very low power operation (1.5mW at +25°C). The HI-5046/883 and HI-5046A/883 are available in a 16 pin Ceramic DIP and operate over the -55°C to +125°C temperature range.

Pinout

LOGIC "0" INPUT
TOP VIEW

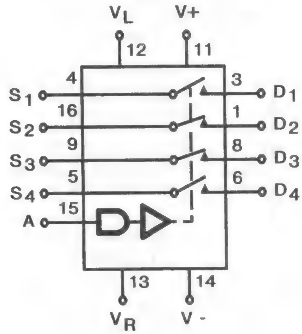


HI1-5046/883 (CERAMIC DIP)
HI1-5046A/883 (CERAMIC DIP)

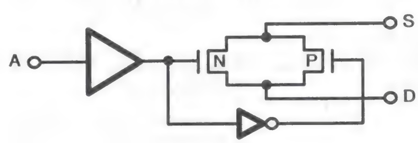
NOTE: Unused pins may be internally connected. Ground all unused pins.

Functional Diagram

LOGIC "1" INPUT



TYPICAL SWITCH



NOTE: Source and Drain are arbitrarily depicted as Analog Input and Output respectively. They may be interchanged without affecting performance.

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 36V
$\pm V_{SUPPLY}$ to Ground (V+, V-) .... ±18V
V_R to Ground .... $-V_{SUPPLY}$
V_L to Ground .... $+V_{SUPPLY}$
Digital and Analog Input Voltage (V_A, V_S, V_D) ..... $+V_{SUPPLY}$ +4V
$-V_{SUPPLY}$ -4V
Peak Current (Source to Drain)
(Pulse at 1ms, 10% Duty Cycle Max) 70mA
Continuous Current (Any Pin) 20mA
Junction Temperature .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... <2000V
Lead Temperature (Soldering 10 sec) .... 300°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	82°C/W	20°C/W

Package Power Dissipation at +75°C
Ceramic DIP Package 1.0W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 12.3mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±15V
Logic Supply Voltage (V_L) .... +5.0V
Logic Reference Voltage (V_R) 0.0V
Analog Input Voltage (V_S) .... $\pm V_{SUPPLY}$
Address Low Level (V_{AL}) .... 0V to 0.8V
Address High Level (V_{AH}) .... 2.4V to +5.0V

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = 2.4V, V_{AL} = +0.8V, Unused Pins are Grounded, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch "ON" Resistance For HI-5046/883	R_{DS1}	V_D = -10V, I_S = 10mA S1/S2/S3/S4	1	+25°C	-	75	Ω
			2, 3	-55°C to +125°C	-	150	Ω
		V_D = 10V, I_S = -10mA S1/S2/S3/S4	1	+25°C	-	75	Ω
			2, 3	-55°C to +125°C	-	150	Ω
Switch "ON" Resistance For HI-5046A/883	R_{DS2}	V_D = -10V, I_S = 10mA S1/S2/S3/S4	1	+25°C	-	45	Ω
			2, 3	-55°C to +125°C	-	50	Ω
		V_D = 10V, I_S = -10mA S1/S2/S3/S4	1	+25°C	-	45	Ω
			2, 3	-55°C to +125°C	-	50	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = -10V, V_D = 10V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = 10V, V_D = -10V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_D = -10V, V_S = 10V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_D = 10V, V_S = -10V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = 10V S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-200	200	nA
		V_D = V_S = -10V S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-200	200	nA

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = 2.4V, V_{AL} = +0.8V, Unused Pins are Grounded, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Low Level Address Current	I_{AL}	V_A = 0V	1	+25°C	-1	1	µA
			2, 3	-55°C to +125°C	-10	1	µA
High Level Address Current	I_{AH}	V_A = 2.4V, 5V	1	+25°C	-1	1	µA
			2, 3	-55°C to +125°C	-1	10	µA
Positive Supply Current	$+I_{CC}$	V_A = 0V, 5V	1	+25°C	-	200	µA
			2, 3	-55°C to +125°C	-	300	µA
Negative Supply Current	$-I_{CC}$	V_A = 0V, 5V	1	+25°C	-200	-	µA
			2, 3	-55°C to +125°C	-300	-	µA
Logic Supply Current	$+I_L$	V_A = 0V, 5V	1	+25°C	-	200	µA
			2, 3	-55°C to +125°C	-	300	µA
Reference Supply Current	$+I_R$	V_A = 0V, 5V	1	+25°C	-200	-	µA
			2, 3	-55°C to +125°C	-300	-	µA

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = +5.0V, V_{AL} = +0.0V, Unused Pins are Grounded, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Turn "ON" Time	t_{ON}	V_S = 10V, -10V C_L = 10pF R_L = 1kΩ	11	-55°C	-	450	ns
			9	+25°C	-	500	ns
			10	+125°C	-	800	ns
Turn "OFF" Time	t_{OFF}	V_S = 10V, -10V C_L = 10pF R_L = 1kΩ	11	-55°C	-	350	ns
			9	+25°C	-	450	ns
			10	+125°C	-	600	ns

4

CMOS ANALOG SWITCHES

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Characterized at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = 4.0V, V_{AL} = 0.8V, Unused Pins are Grounded, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
"On" Resistance Match (Channel to Channel) for HI-5046/883	R_{ON1} Match	V_D = ±10V I_D = 10mA	1	+25°C	-	10	Ω
"On" Resistance Match (Channel to Channel) for HI-5046A/883	R_{ON2} Match	V_D = ±10V I_D = 10mA	1	+25°C	-	10	Ω
Address Capacitance	C_A	V_A = 0V, 5V	1	+25°C	-	45	pF
Switch Input Capacitance	$C_{S(OFF)}$	Switch Off: V_A = 0V	1	+25°C	-	60	pF
Switch Output Capacitance	$C_{D(OFF)}$	Switch Off: V_A = 0V	1	+25°C	-	60	pF
	$C_{D(ON)}$	Switch On: V_A = 5V	1	+25°C	-	60	pF
Drain to Source Capacitance	$C_{DS(OFF)}$	Switch Off: V_A = 0V	1	+25°C	-	10	pF
Off Isolation	V_{ISO}	$V_S = 2V_{p-p}$ @ f = 100kHz R_L = 100Ω	1	+25°C	-	60	dB
Crosstalk	V_{CT}	$V_S = 2V_{p-p}$ @ f = 100kHz R_L = 100Ω	1	+25°C	-	60	dB
Charge Transfer Error	V_{CTE}	V_S = GND, C_L = 10,000pF V_A = 0 to 4V @ f = 200kHz	1	+25°C	-	30	mV

NOTE 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

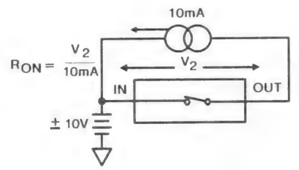
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

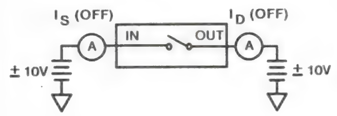
* PDA applies to Subgroup 1 only.

Test Circuits

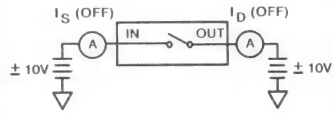
R_{DS}



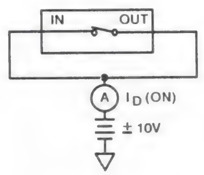
$I_{S(OFF)}$



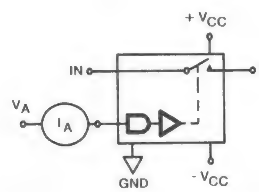
$I_{D(OFF)}$



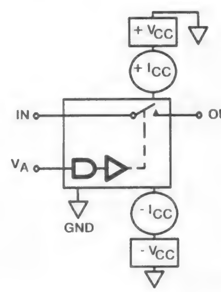
$I_{D(ON)}$



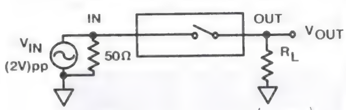
ADDRESS CURRENT



SUPPLY CURRENTS

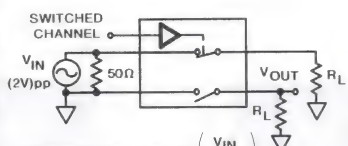


OFF ISOLATION



"OFF" ISOLATION = $20 \text{ LOG} \left(\frac{V_{IN}}{V_{OUT}}\right)$

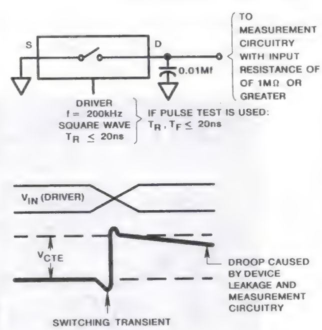
CROSSTALK



"CROSSTALK" = $20 \text{ LOG} \left(\frac{V_{IN}}{V_{OUT}}\right)$

NOTE: Applies only to DUAL or DOUBLE THROW switches.

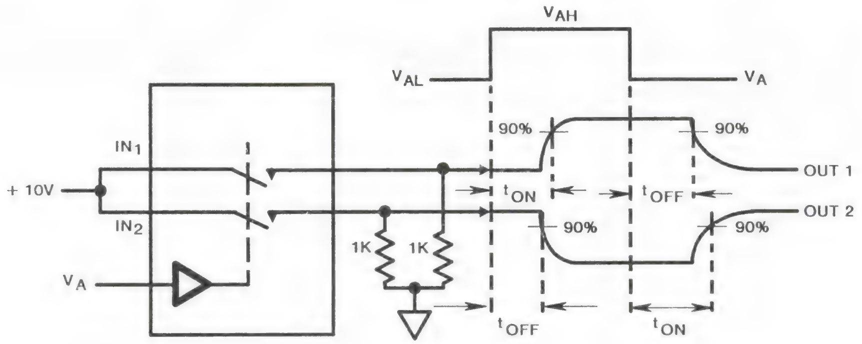
CHARGE TRANSFER



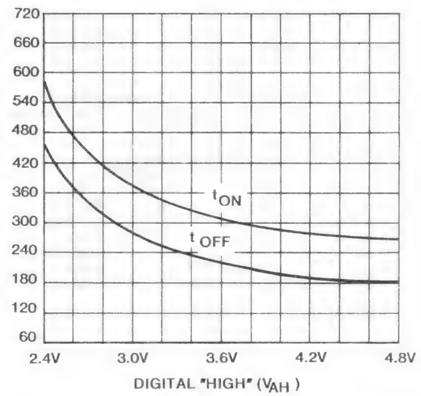
NOTE: V_{CTE} may be a positive or negative value.

Test Characteristics

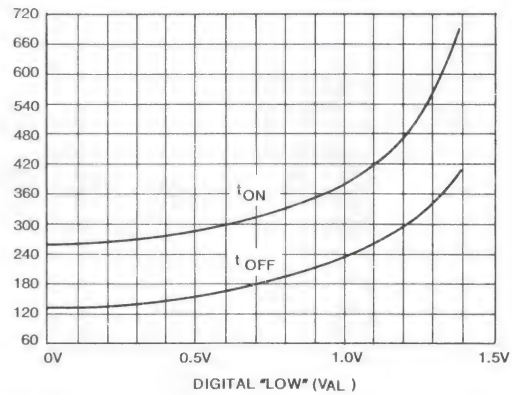
ON/OFF SWITCH TIME (t_{ON}, t_{OFF})



SWITCHING TIMES FOR POSITIVE DIGITAL TRANSITION



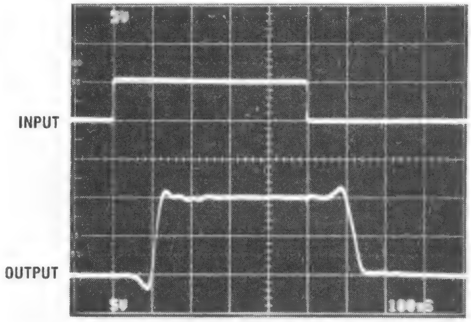
SWITCHING TIMES FOR NEGATIVE DIGITAL TRANSITION



Test Waveforms

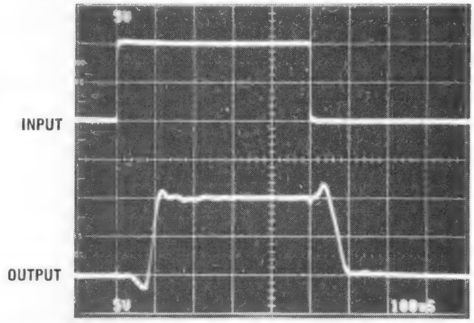
Vertical Scale: Input = 5V/Div., (TTL; V_{AH} = 5V, V_{AL} = 0V)
Output = 5V/Div.

Horizontal Scale: 100ns/Div.



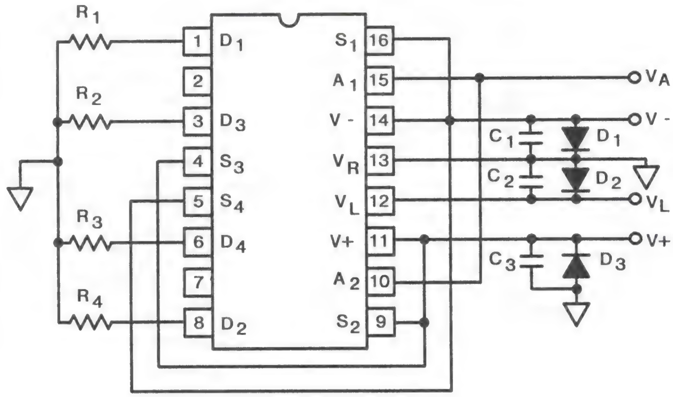
Vertical Scale: Input = 5V/Div., (CMOS; V_{AH} = 10V, V_{AL} = 0V)
Output = 5V/Div.

Horizontal Scale: 100ns/Div.



Burn-In Circuit

HI-5046/883 HI-5046A/883 CERAMIC DIP



NOTES:

R_1 thru R_4 = 10kΩ, ±5%, 1/4W (Min)

C_1, C_2, C_3, = 0.01μF/Socket (Min) or 0.1μF/Row, (Min)

D_1, D_2, D_3 = IN4002 or Equivalent/Board

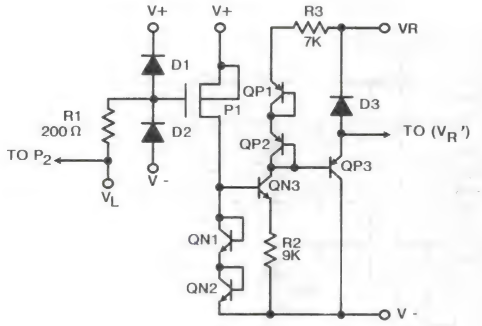
V_L = 5.5 ± 0.5V

A_1 = A_2 = 5.5 ± 0.5V

|(V+) - (V-)| = 30V

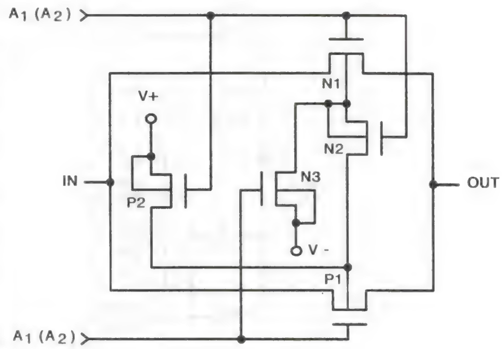
Schematic Diagram

TTL/CMOS REFERENCE CIRCUIT *

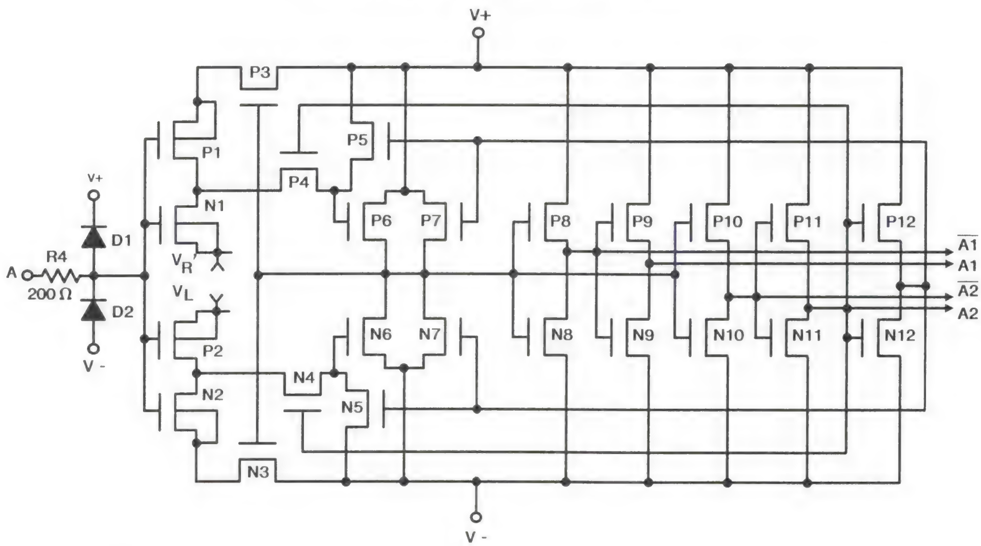


* Connect V+ to V_L for minimizing power consumption when driving from CMOS circuits.

SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



All N-Channel Bodies to V-
All P-Channel Bodies to V+
Except as Shown

Die Characteristics

DIE DIMENSIONS:
96 x 81 x 19mils
(2430 x 2050 x 480μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride over Silox
Silox Thickness: 12kÅ ± 2kÅ
Nitride Thickness: 3.5kÅ ± 1kÅ

SUBSTRATE POTENTIAL (Powered-up): V-

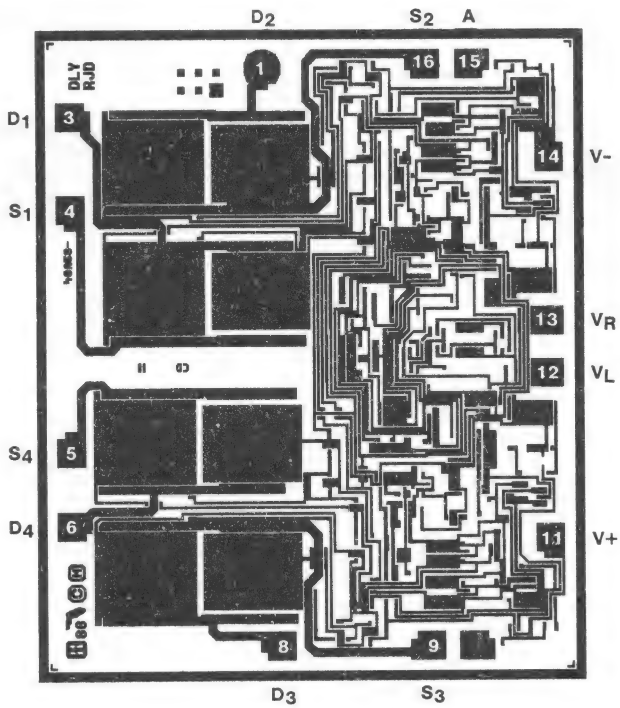
DEVICE COUNT: 82

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)

WORST CASE CURRENT DENSITY:
$1.0 \times 10^5 A/cm^2$ @ 20mA

Metallization Mask Layout

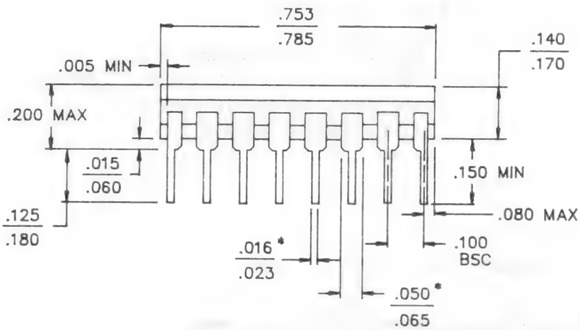
HI-5046/883 HI-5046A/883

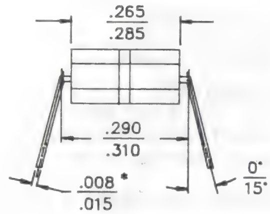


NOTE: Pin Numbers Correspond to DIP Package Only. Unused Pins May Be Connected. Ground All Unused Pins.

Packaging †

16 PIN CERAMIC DIP





* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

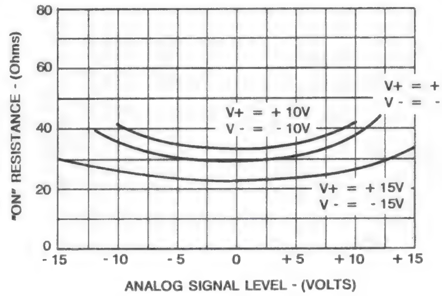
DESIGN INFORMATION

DPDT CMOS Analog Switch

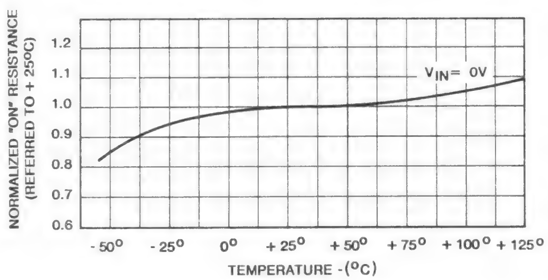
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

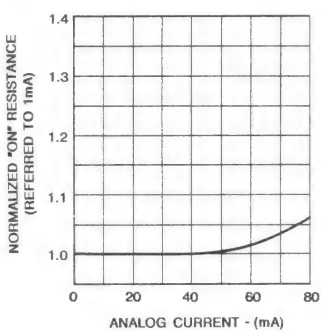
"ON" RESISTANCE vs. ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE



NORMALIZED "ON" RESISTANCE vs. TEMPERATURE



NORMALIZED "ON" RESISTANCE vs. ANALOG CURRENT



4

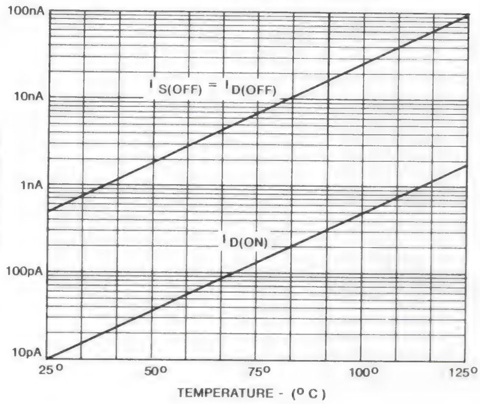
CMOS ANALOG SWITCHES

DESIGN INFORMATION (Continued)

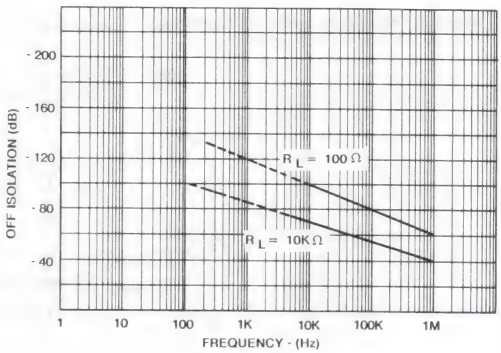
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

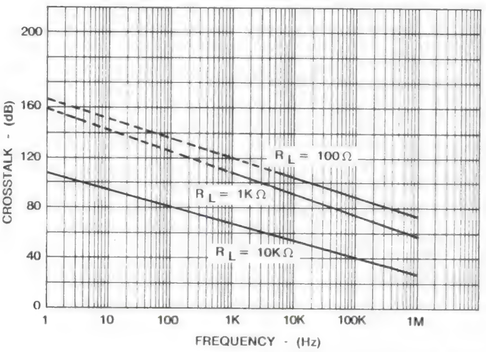
ON/OFF LEAKAGE CURRENT vs. TEMPERATURE



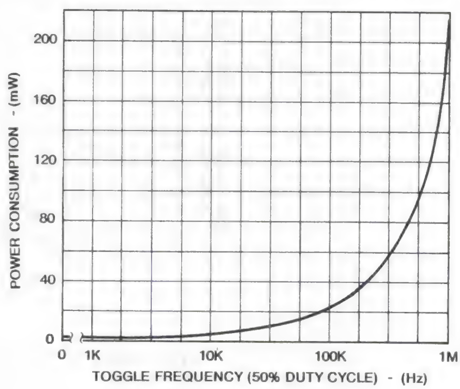
"OFF" ISOLATION vs. FREQUENCY



CROSSTALK vs. FREQUENCY



POWER CONSUMPTION vs. FREQUENCY



HARRIS

HI-5047/883
HI-5047A/883

January 1989

4PST CMOS Analog Switch

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Wide Analog Signal Range .... ±15V
- Low "ON" Resistance
  - HI-5047 .... 50Ω (Typ) 150Ω (Max)
  - HI-5047A .... 25Ω (Typ) 50Ω (Max)
- High Current Capability .... 70mA (Max)
- Break-Before-Make Switching
  - Turn-On Time .... 370ns (Typ) 800ns (Max)
  - Turn-Off Time .... 280ns (Typ) 400ns (Max)
- No Latch-Up
- Input MOS Gates Are Protected From Electrostatic Discharge
- DTL, TTL, CMOS, PMOS Compatible

Applications

- High Frequency Switching
- Sample and Hold
- Digital Filters
- Operational Amplifier Gain Switching

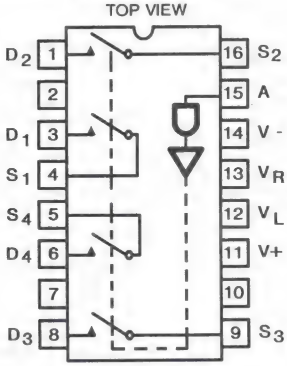
Description

These CMOS analog switches offer low-resistance switching performance for analog voltages up to the supply rails and for signal currents up to 70mA. "ON" resistance is low and stays reasonably constant over the full range of operating signal voltage and current. R_{ON} remains exceptionally constant for input voltages between +5V and -5V and currents up to 50mA. Switch impedance also changes very little over temperature, particularly between 0°C and +75°C. R_{ON} is nominally 50Ω for the HI-5047/883 and 25Ω for the HI-5047A/883.

These devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. Performance is further enhanced by Dielectric Isolation processing which insures latch-free operation with very low input and output leakage currents (0.8nA at +25°C). They also feature very low power operation (1.5mW at +25°C). The HI-5047/883 and HI-5047A/883 are available in a 16 pin Ceramic DIP and operate over the -55°C to +125°C temperature range.

Pinout

LOGIC "0" INPUT
TOP VIEW

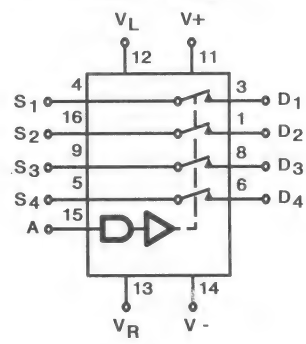


HI1-5047/883 (CERAMIC DIP)
HI1-5047A/883 (CERAMIC DIP)

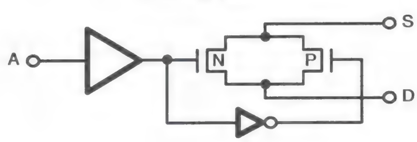
NOTE: Unused pins may be internally connected. Ground all unused pins.

Functional Diagram

LOGIC "1" INPUT



TYPICAL SWITCH



NOTE: Source and Drain are arbitrarily depicted as Analog Input and Output respectively. They may be interchanged without affecting performance.

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 36V
$\pm V_{SUPPLY}$ to Ground (V+, V-) .... ±18V
V_R to Ground .... $-V_{SUPPLY}$
V_L to Ground .... $+V_{SUPPLY}$
Digital and Analog Input Voltage (V_A, V_S, V_D) .... $+V_{SUPPLY}$ +4V
$-V_{SUPPLY}$ -4V
Peak Current (Source to Drain)
(Pulse at 1ms, 10% Duty Cycle Max) 70mA
Continuous Current (Any Pin) 20mA
Junction Temperature .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... <2000V
Lead Temperature (Soldering 10 sec) .... 300°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	82°C/W	20°C/W

Package Power Dissipation at +75°C
Ceramic DIP Package 1.0W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 12.3mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±15V
Logic Supply Voltage (V_L) .... +5.0V
Logic Reference Voltage (V_R) 0.0V
Analog Input Voltage (V_S) .... $\pm V_{SUPPLY}$
Address Low Level (V_{AL}) .... 0V to 0.8V
Address High Level (V_{AH}) .... 2.4V to +5.0V

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = 2.4V, V_{AL} = +0.8V, Unused Pins are Grounded, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch "ON" Resistance For HI-5047/883	R_{DS1}	V_D = -10V, I_S = 10mA S1/S2/S3/S4	1	+25°C	-	75	Ω
			2, 3	-55°C to +125°C	-	150	Ω
		V_D = 10V, I_S = -10mA S1/S2/S3/S4	1	+25°C	-	75	Ω
			2, 3	-55°C to +125°C	-	150	Ω
Switch "ON" Resistance For HI-5047A/883	R_{DS2}	V_D = -10V, I_S = 10mA S1/S2/S3/S4	1	+25°C	-	45	Ω
			2, 3	-55°C to +125°C	-	50	Ω
		V_D = 10V, I_S = -10mA S1/S2/S3/S4	1	+25°C	-	45	Ω
			2, 3	-55°C to +125°C	-	50	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = -10V, V_D = 10V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = 10V, V_D = -10V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_D = -10V, V_S = 10V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_D = 10V, V_S = -10V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = 10V S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-200	200	nA
		V_D = V_S = -10V S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-200	200	nA

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = 2.4V, V_{AL} = +0.8V, Unused Pins are Grounded, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Low Level Address Current	I_{AL}	V_A = 0V	1	+25°C	-1	1	μA
			2, 3	-55°C to +125°C	-10	1	μA
High Level Address Current	I_{AH}	V_A = 2.4V, 5V	1	+25°C	-1	1	μA
			2, 3	-55°C to +125°C	-1	10	μA
Positive Supply Current	$+I_{CC}$	V_A = 0V, 5V	1	+25°C	-	200	μA
			2, 3	-55°C to +125°C	-	300	μA
Negative Supply Current	$-I_{CC}$	V_A = 0V, 5V	1	+25°C	-200	-	μA
			2, 3	-55°C to +125°C	-300	-	μA
Logic Supply Current	$+I_L$	V_A = 0V, 5V	1	+25°C	-	200	μA
			2, 3	-55°C to +125°C	-	300	μA
Reference Supply Current	$+I_R$	V_A = 0V, 5V	1	+25°C	-200	-	μA
			2, 3	-55°C to +125°C	-300	-	μA

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = +5.0V, V_{AL} = +0.0V, Unused Pins are Grounded, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Turn "ON" Time	t_{ON}	V_S = 10V, -10V C_L = 10pF R_L = 1kΩ	11	-55°C	-	450	ns
			9	+25°C	-	500	ns
			10	+125°C	-	800	ns
Turn "OFF" Time	t_{OFF}	V_S = 10V, -10V C_L = 10pF R_L = 1kΩ	11	-55°C	-	350	ns
			9	+25°C	-	450	ns
			10	+125°C	-	600	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Characterized at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = 4.0V, V_{AL} = 0.8V, Unused Pins are Grounded, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
"On" Resistance Match (Channel to Channel) for HI-5047/883	R_{ON1} Match	V_D = ±10V I_D = 10mA	1	+25°C	-	10	Ω
"On" Resistance Match (Channel to Channel) for HI-5047A/883	R_{ON2} Match	V_D = ±10V I_D = 10mA	1	+25°C	-	10	Ω
Address Capacitance	C_A	V_A = 0V, 5V	1	+25°C	-	45	pF
Switch Input Capacitance	$C_{S(OFF)}$	Switch Off: V_A = 0V	1	+25°C	-	60	pF
Switch Output Capacitance	$C_{D(OFF)}$	Switch Off: V_A = 0V	1	+25°C	-	60	pF
	$C_{D(ON)}$	Switch On: V_A = 5V	1	+25°C	-	60	pF
Drain to Source Capacitance	$C_{DS(OFF)}$	Switch Off: V_A = 0V	1	+25°C	-	10	pF
Off Isolation	V_{ISO}	$V_S = 2V_{p-p}$ @ f = 100kHz R_L = 100Ω	1	+25°C	-	60	dB
Charge Transfer Error	V_{CTE}	V_S = GND, C_L = 10,000pF V_A = 0 to 4V @ f = 200kHz	1	+25°C	-	30	mV

NOTE 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

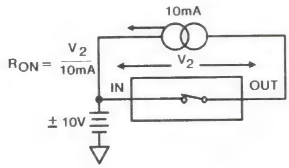
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

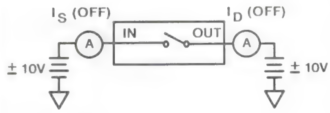
* PDA applies to Subgroup 1 only.

Test Circuits

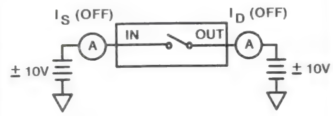
R_{DS}



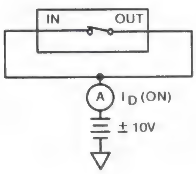
$I_{S(OFF)}$



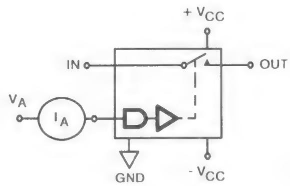
$I_{D(OFF)}$



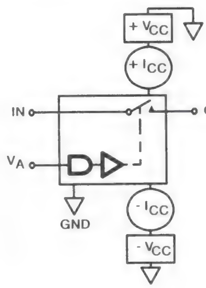
$I_{D(ON)}$



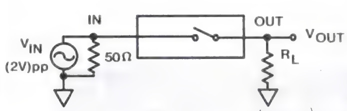
ADDRESS CURRENT



SUPPLY CURRENTS

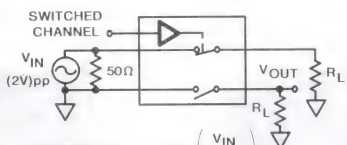


OFF ISOLATION



"OFF" ISOLATION = $20 \text{ LOG} \left(\frac{V_{IN}}{V_{OUT}} \right)$

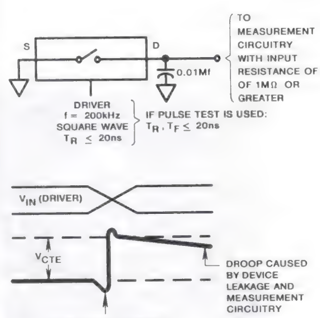
CROSSTALK



"CROSSTALK" = $20 \text{ LOG} \left(\frac{V_{IN}}{V_{OUT}} \right)$

NOTE: Applies only to DUAL or DOUBLE THROW switches.

CHARGE TRANSFER

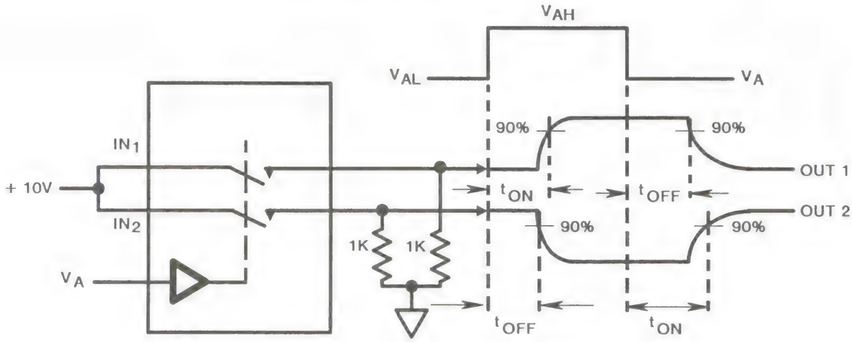


NOTE: V_{CTE} may be a positive or negative value.

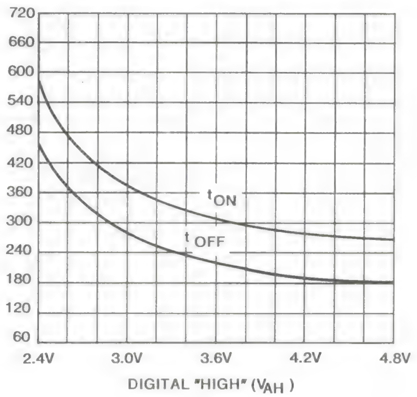
4
CMOS ANALOG SWITCHES

Test Characteristics

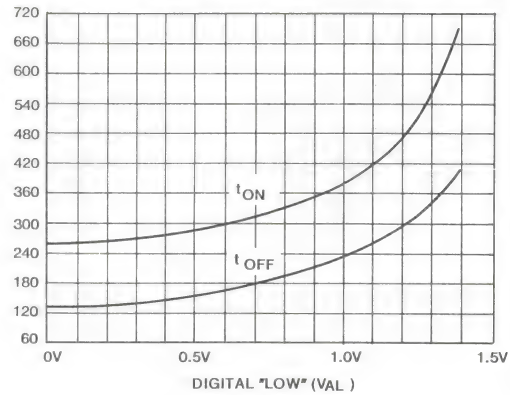
ON/OFF SWITCH TIME (t_{ON}, t_{OFF})



SWITCHING TIMES FOR POSITIVE DIGITAL TRANSITION



SWITCHING TIMES FOR NEGATIVE DIGITAL TRANSITION



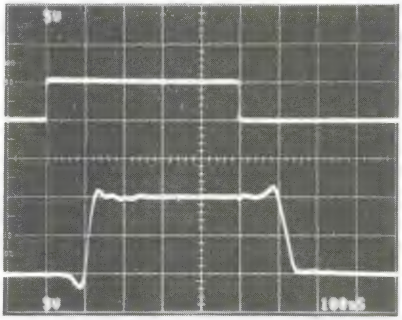
Test Waveforms

Vertical Scale: Input = 5V/Div., (TTL; V_{AH} = 5V, V_{AL} = 0V)
Output = 5V/Div.

Horizontal Scale: 100ns/Div.

INPUT

OUTPUT

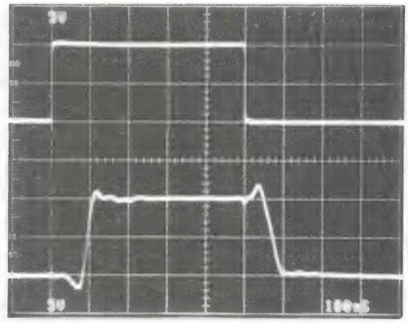


Vertical Scale: Input = 5V/Div., (CMOS; V_{AH} = 10V, V_{AL} = 0V)
Output = 5V/Div.

Horizontal Scale: 100ns/Div.

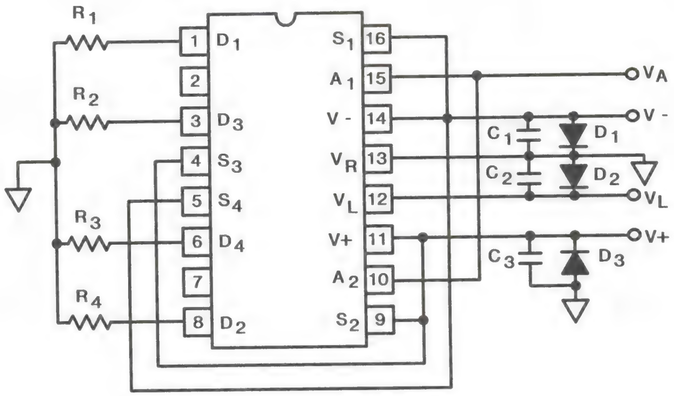
INPUT

OUTPUT



Burn-In Circuit

HI-5047/883 HI-5047A/883 CERAMIC DIP



NOTES:

R_1 thru R_4 = 10kΩ, ±5%, 1/4W (Min)

C_1, C_2, C_3, = 0.01µF/Socket (Min) or 0.1µF/Row, (Min)

D_1, D_2, D_3 = IN4002 or Equivalent/Board

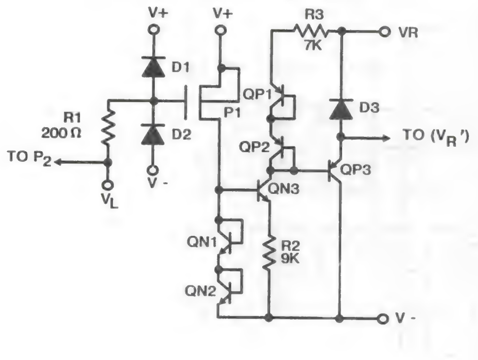
V_L = 5.5 ± 0.5V

A_1 = A_2 = 5.5 ± 0.5V

$|(V+) - (V-)|$ = 30V

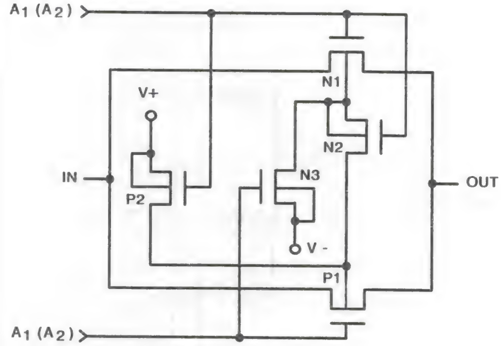
Schematic Diagram

TTL/CMOS REFERENCE CIRCUIT *

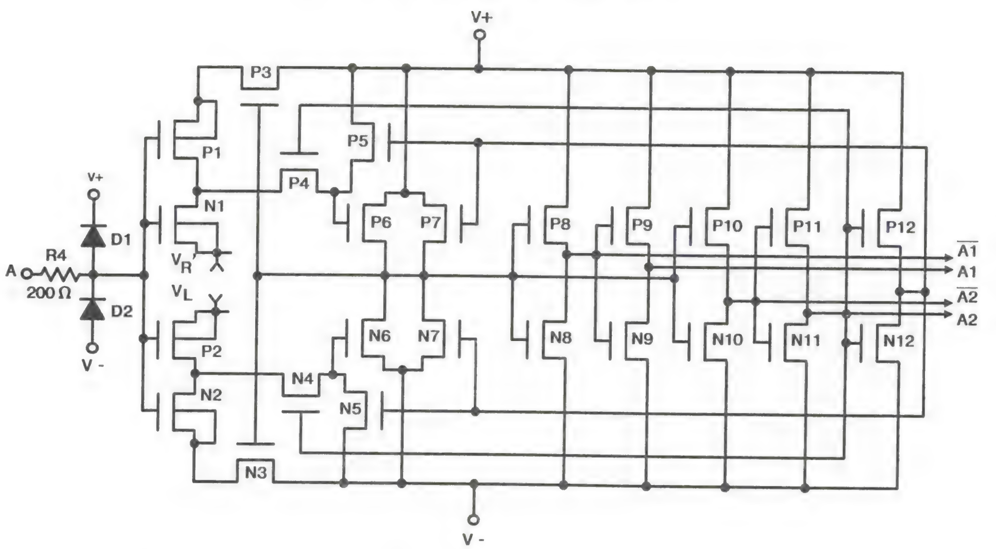


* Connect V+ to V_L for minimizing power consumption when driving from CMOS circuits.

SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



All N-Channel Bodies to V−
All P-Channel Bodies to V+
Except as Shown

Die Characteristics

DIE DIMENSIONS:
96 x 81 x 19mils
(2430 x 2050 x 480μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride over Silox
Silox Thickness: 12kÅ ± 2kÅ
Nitride Thickness: 3.5kÅ ± 1kÅ

SUBSTRATE POTENTIAL (Powered-up): V-

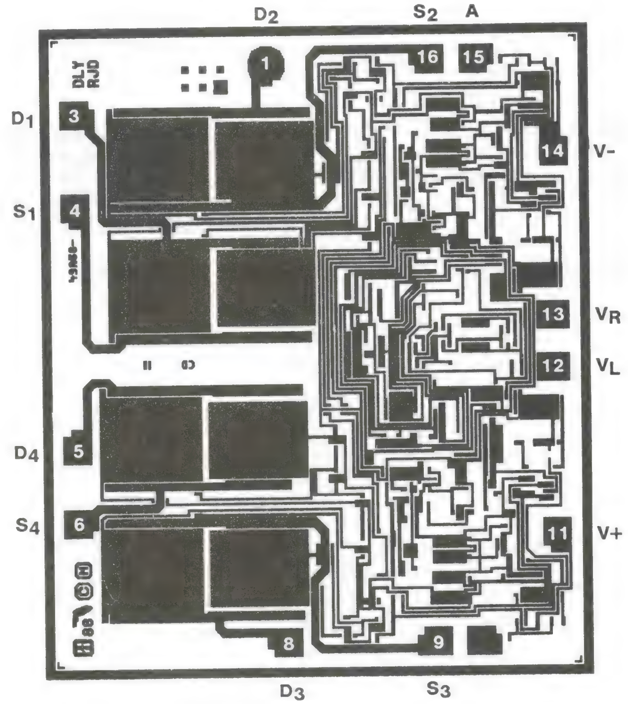
DEVICE COUNT: 82

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)

WORST CASE CURRENT DENSITY:
$1.0 \times 10^5 A/cm^2$ @ 20mA

Metallization Mask Layout

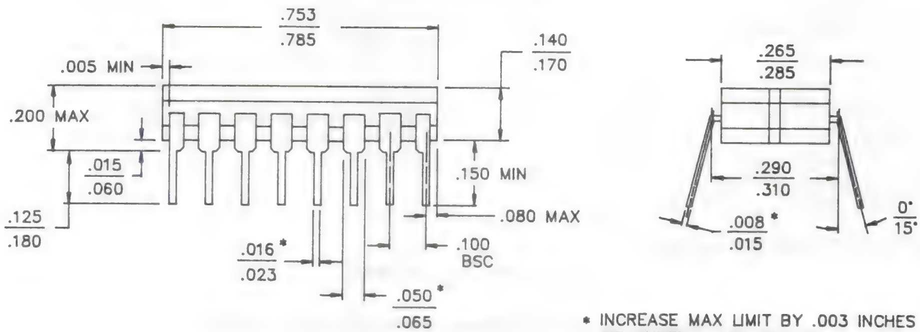
HI-5047/883 HI-5047A/883



NOTE: Pin Numbers Correspond to DIP Package Only. Unused Pins May Be Connected. Ground All Unused Pins.

Packaging†

16 PIN CERAMIC DIP



* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

DESIGN INFORMATION

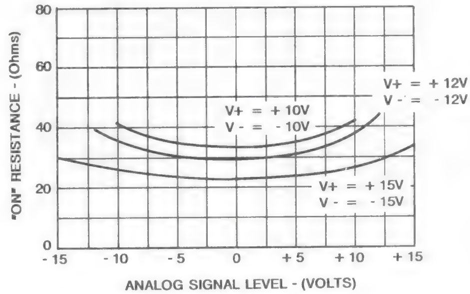
4PST CMOS Analog Switch

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

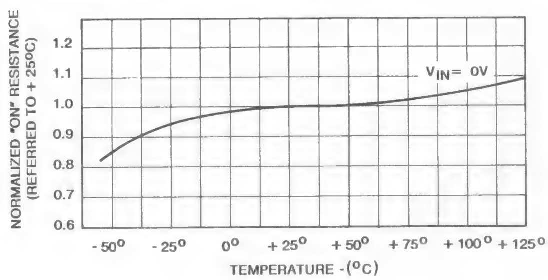
Typical Performance Curves

Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

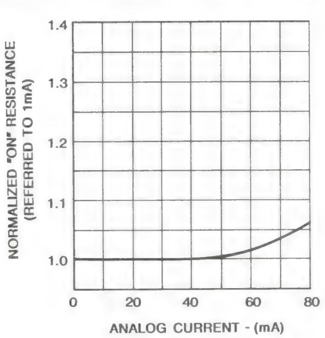
"ON" RESISTANCE vs. ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE



NORMALIZED "ON" RESISTANCE vs. TEMPERATURE



NORMALIZED "ON" RESISTANCE vs. ANALOG CURRENT



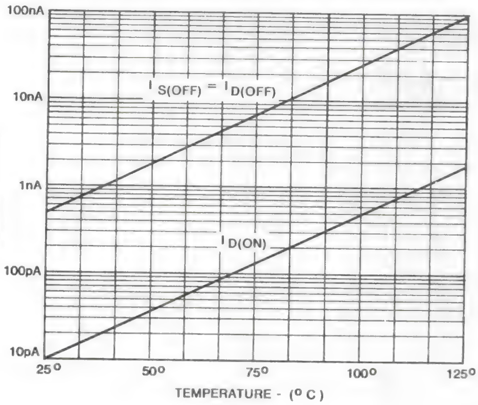
4 CMOS ANALOG SWITCHES

DESIGN INFORMATION (Continued)

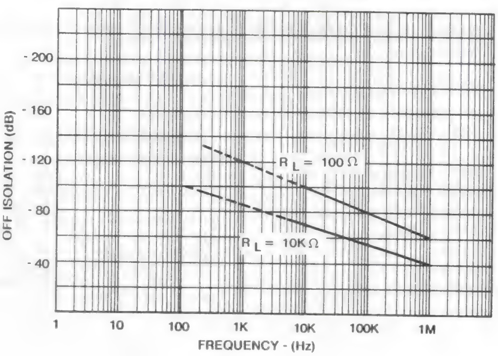
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

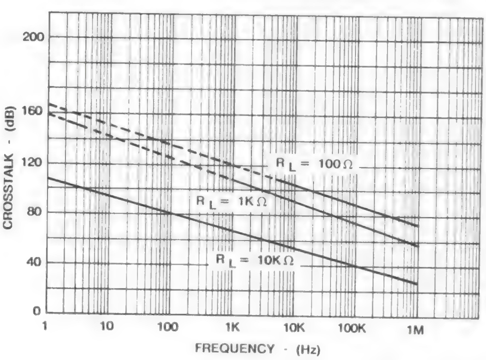
ON/OFF LEAKAGE CURRENT vs. TEMPERATURE



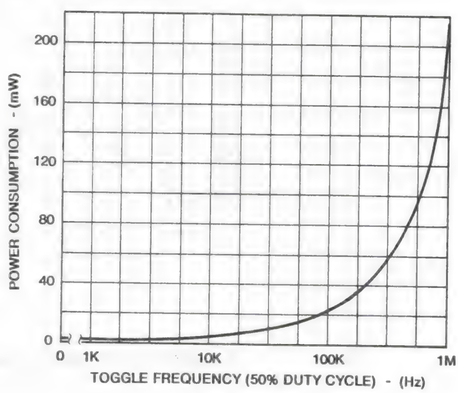
"OFF" ISOLATION vs. FREQUENCY



CROSSTALK vs. FREQUENCY



POWER CONSUMPTION vs. FREQUENCY



HARRIS

HI-5048/883

January 1989

Dual SPST CMOS Analog Switch

Features

- This Circuit Is Processed In Accordance to Mil-Std-883 and Is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Wide Analog Signal Range .... ±15V
- Low "ON" Resistance .... 25Ω (Typ) 50Ω (Max)
- High Current Capability.................70mA (Max)
- Break-Before-Make Switching
  - Turn-On Time.........................370ns (Typ) 800ns (Max)
  - Turn-Off Time........................280ns (Typ) 400ns (Max)
- No Latch-Up
- Input MOS Gates Are Protected From Electrostatic Discharge
- DTL, TTL, CMOS, PMOS Compatible

Applications

- High Frequency Switching
- Sample and Hold
- Digital Filters
- Operational Amplifier Gain Switching

Description

This CMOS analog switch offers low-resistance switching performance for analog voltages up to the supply rails and for signal currents up to 70mA. "ON" resistance is low and stays reasonably constant over the full range of operating signal voltage and current. R_{ON} remains exceptionally constant for input voltages between +5V and -5V and currents up to 50mA. Switch impedance also changes very little over temperature, particularly between 0°C and +75°C. R_{ON} is nominally 25Ω.

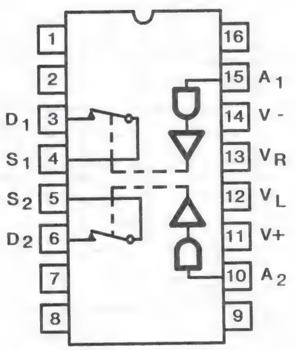
This device provides break-before-make switching and is TTL and CMOS compatible for maximum application versatility. Performance is further enhanced by Dielectric Isolation processing which insures latch-free operation with very low input and output leakage currents (0.8nA at +25°C). This switch also features very low power operation (1.5mW at +25°C). The HI-5048/883 is available in a 16 pin Ceramic DIP and operates over the -55°C to +125°C temperature range.

4

CMOS ANALOG SWITCHES

Pinout

LOGIC "0" INPUT
TOP VIEW

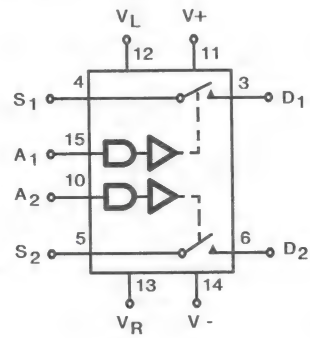


HI1-5048/883 (CERAMIC DIP)

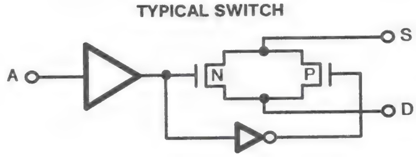
NOTE: Unused pins may be internally connected. Ground all unused pins.

Functional Diagram

LOGIC "1" INPUT



TYPICAL SWITCH



NOTE: Source and Drain are arbitrarily depicted as Analog Input and Output respectively. They may be interchanged without affecting performance.

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 36V
$\pm V_{SUPPLY}$ to Ground (V+, V-) .... ±18V
V_R to Ground .... $-V_{SUPPLY}$
V_L to Ground .... $+V_{SUPPLY}$
Digital and Analog Input Voltage (V_A, V_S, V_D) ..... $+V_{SUPPLY}$ +4V
$-V_{SUPPLY}$ -4V
Peak Current (Source to Drain)
(Pulse at 1ms, 10% Duty Cycle Max) 70mA
Continuous Current (Any Pin) 20mA
Junction Temperature .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... < 2000V
Lead Temperature (Soldering 10 sec) .... 300°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	82°C/W	20°C/W

Package Power Dissipation Limit at +75°C for $T_J \leq$ +175°C
Ceramic DIP Package 1.0W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 12.3mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±15V
Logic Supply Voltage (V_L) .... +5.0V
Logic Reference Voltage (V_R) 0.0V
Analog Input Voltage (V_S) .... $\pm V_{SUPPLY}$
Address Low Level (V_{AL}) .... 0V to 0.8V
Address High Level (V_{AH}) .... 2.4V to +5.0V

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = 2.4V, V_{AL} = +0.8V, Unused Pins are Grounded, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch "ON" Resistance	R_{DS}	V_D = -10V, I_S = 10mA S1/S2	1	+25°C	-	45	Ω
			2, 3	-55°C to +125°C	-	50	Ω
		V_D = 10V, I_S = -10mA S1/S2	1	+25°C	-	45	Ω
			2, 3	-55°C to +125°C	-	50	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = -10V, V_D = 10V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_S = 10V, V_D = -10V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_D = -10V, V_S = 10V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
		V_D = 10V, V_S = -10V S1/S2	1	+25°C	-1	1	nA
			2, 3	-55°C to +125°C	-100	100	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = 10V S1/S2	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-200	200	nA
		V_D = V_S = -10V S1/S2	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-200	200	nA
Low Level Address Current	I_{AL}	V_A = 0V A_1, A_2	1	+25°C	-1	1	µA
			2, 3	-55°C to +125°C	-10	1	µA
High Level Address Current	I_{AH}	V_A = 2.4V, 5V A_1, A_2	1	+25°C	-1	1	µA
			2, 3	-55°C to +125°C	-1	10	µA
Positive Supply Current	$+I_{CC}$	V_A = 0V, 5V A_1, A_2	1	+25°C	-	200	µA
			2, 3	-55°C to +125°C	-	300	µA
Negative Supply Current	$-I_{CC}$	V_A = 0V, 5V A_1, A_2	1	+25°C	-200	-	µA
			2, 3	-55°C to +125°C	-300	-	µA
Logic Supply Current	$+I_L$	V_A = 0V, 5V	1	+25°C	-	200	µA
			2, 3	-55°C to +125°C	-	300	µA
Reference Supply Current	$+I_R$	V_A = 0V, 5V	1	+25°C	-200	-	µA
			2, 3	-55°C to +125°C	-300	-	µA

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = +5.0V, V_{AL} = +0.0V, Unused Pins are Grounded, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Turn "ON" Time	t_{ON}	V_S = 10V, -10V C_L = 10pF R_L = 1kΩ	11	-55°C	-	450	ns
			9	+25°C	-	500	ns
			10	+125°C	-	800	ns
Turn "OFF" Time	t_{OFF}	V_S = 10V, -10V C_L = 10pF R_L = 1kΩ	11	-55°C	-	350	ns
			9	+25°C	-	450	ns
			10	+125°C	-	600	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Characterized at: Supply Voltage = ±15V, V_L = +5.0V, V_R = 0.0V, V_{AH} = 4.0V, V_{AL} = 0.8V, Unused Pins are Grounded, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
"On" Resistance Match (Channel to Channel)	R_{ON} Match	V_D = ±10V I_D = 10mA	1	+25°C	-	10	Ω
Address Capacitance	C_A	V_A = 0V, 5V	1	+25°C	-	45	pF
Switch Input Capacitance	$C_{S(OFF)}$	Switch Off: V_A = 0V	1	+25°C	-	60	pF
Switch Output Capacitance	$C_{D(OFF)}$	Switch Off: V_A = 0V	1	+25°C	-	60	pF
	$C_{D(ON)}$	Switch On: V_A = 5V	1	+25°C	-	60	pF
Drain to Source Capacitance	$C_{DS(OFF)}$	Switch Off: V_A = 0V	1	+25°C	-	10	pF
Off Isolation	V_{ISO}	$V_S = 2V_{p-p}$ @ f = 100kHz R_L = 100Ω	1	+25°C	-	60	dB
Crosstalk	V_{CT}	$V_S = 2V_{p-p}$ @ f = 100kHz R_L = 100Ω	1	+25°C	-	60	dB
Charge Transfer Error	V_{CTE}	V_S = GND, C_L = 10,000pF V_A = 0 to 4V @ f = 200kHz	1	+25°C	-	30	mV

NOTE 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

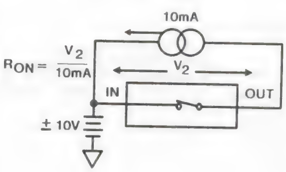
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

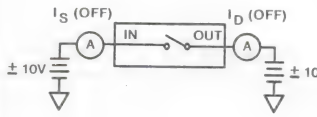
* PDA applies to Subgroup 1 only.

Test Circuits

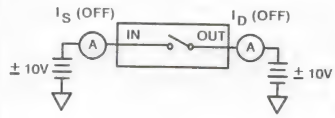
R_{DS}



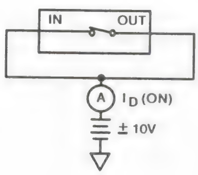
$I_{S(OFF)}$



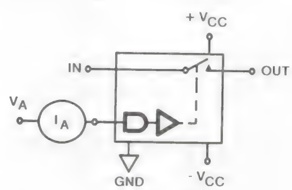
$I_{D(OFF)}$



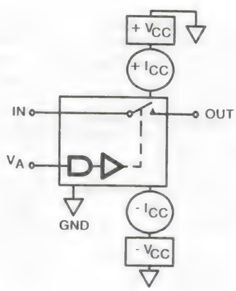
$I_{D(ON)}$



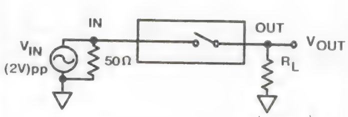
ADDRESS CURRENT



SUPPLY CURRENTS

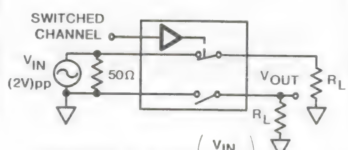


OFF ISOLATION



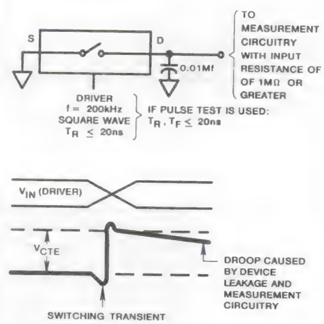
"OFF" ISOLATION = 20 LOG $\left(\frac{V_{IN}}{V_{OUT}}\right)$

CROSSTALK



"CROSSTALK" = 20 LOG $\left(\frac{V_{IN}}{V_{OUT}}\right)$

CHARGE TRANSFER

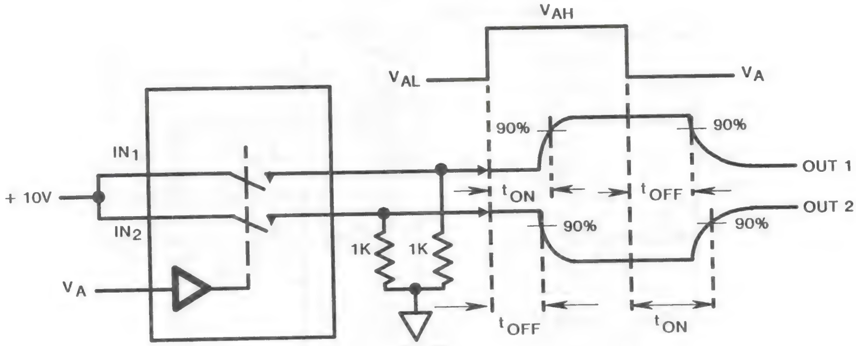


NOTE: Applies only to DUAL or DOUBLE THROW switches.

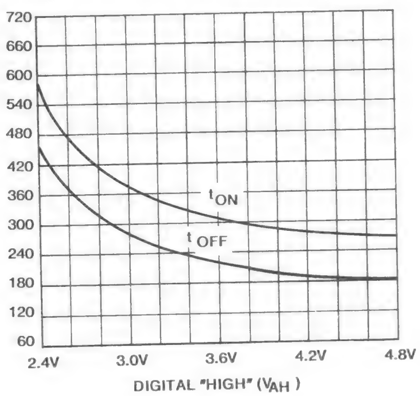
NOTE: V_{CTE} may be a positive or negative value.

Test Characteristics

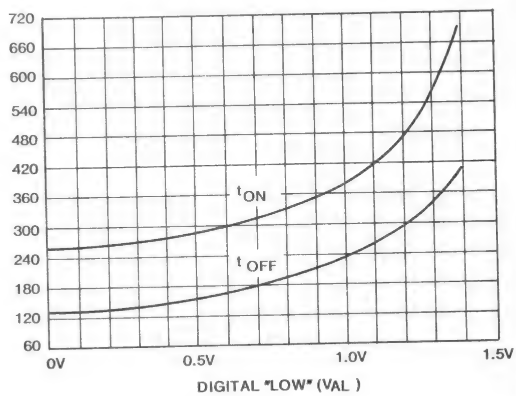
ON/OFF SWITCH TIME (t_{ON}, t_{OFF})



SWITCHING TIMES FOR POSITIVE DIGITAL TRANSITION



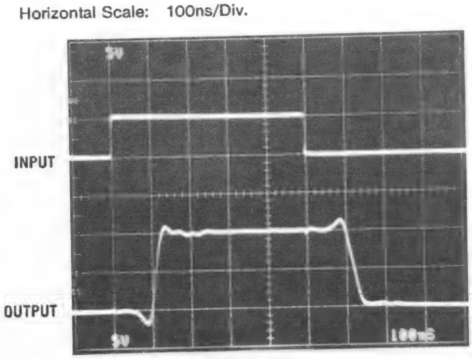
SWITCHING TIMES FOR NEGATIVE DIGITAL TRANSITION



Test Waveforms

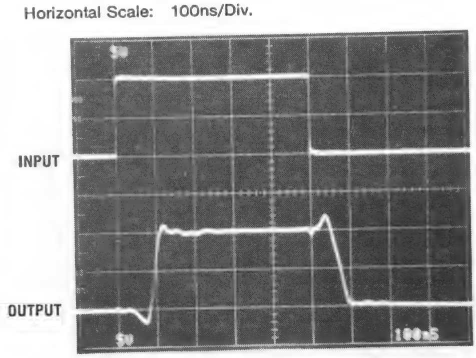
Vertical Scale: Input = 5V/Div., (TTL; V_{AH} = 5V, V_{AL} = 0V)
Output = 5V/Div.

Horizontal Scale: 100ns/Div.



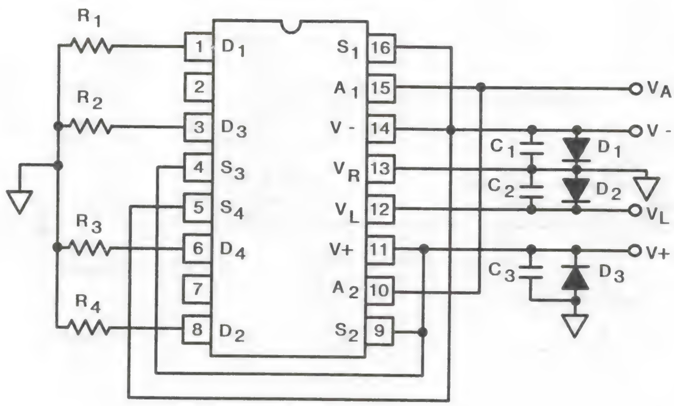
Vertical Scale: Input = 5V/Div., (CMOS; V_{AH} = 10V, V_{AL} = 0V)
Output = 5V/Div.

Horizontal Scale: 100ns/Div.



Burn-In Circuit

HI-5048/883 CERAMIC DIP



NOTES:

R_1 thru R_4 = 10kΩ, ±5%, 1/4W (Min)

C_1, C_2, C_3, = 0.01μF/Socket (Min) or 0.1μF/Row, (Min)

D_1, D_2, D_3 = IN4002 or Equivalent/Board

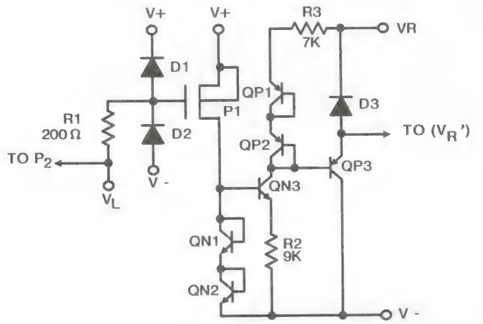
$V_L = 5.5 \pm 0.5V$

$A_1 = A_2 = 5.5 \pm 0.5V$

$|(V+) - (V-)| = 30V$

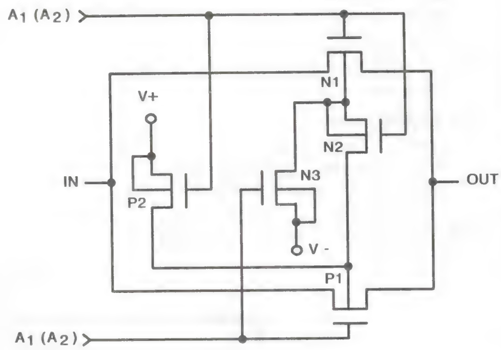
Schematic Diagram

TTL/CMOS REFERENCE CIRCUIT *

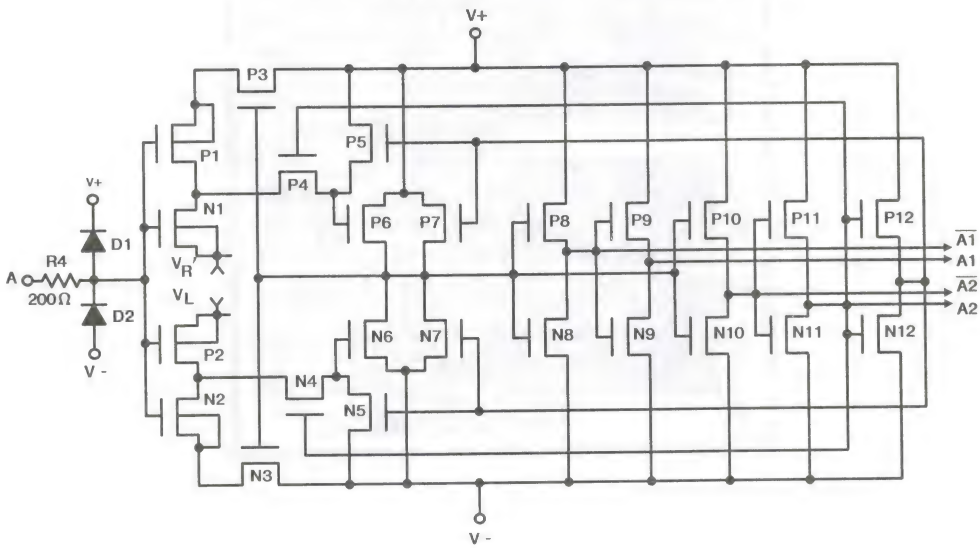


* Connect V+ to V_L for minimizing power consumption when driving from CMOS circuits.

SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



All N-Channel Bodies to V-
All P-Channel Bodies to V+
Except as Shown

Die Characteristics

DIE DIMENSIONS:
96 x 81 x 19mils
(2430 x 2050 x 480μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride over Silox
Silox Thickness: 12kÅ ± 2kÅ
Nitride Thickness: 3.5kÅ ± 1kÅ

SUBSTRATE POTENTIAL (Powered-up): V-

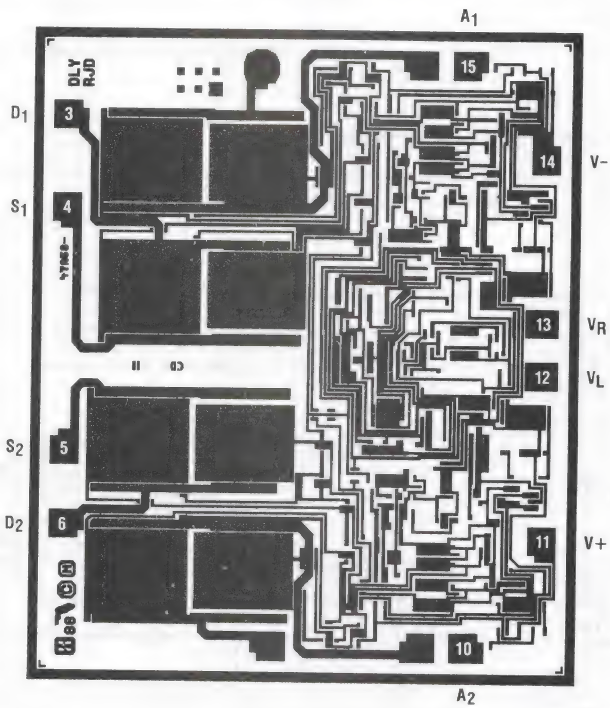
DEVICE COUNT: 82

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)

WORST CASE CURRENT DENSITY:
$1.0 \times 10^5 A/cm^2$ @ 20mA

Metallization Mask Layout

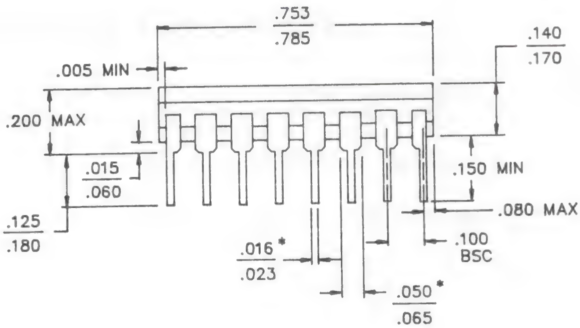
HI-5048/883

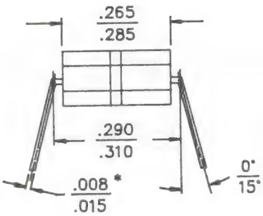


NOTE: Pin Numbers Correspond to DIP Package Only. Unused Pins May Be Connected. Ground All Unused Pins.

Packaging†

16 PIN CERAMIC DIP





* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

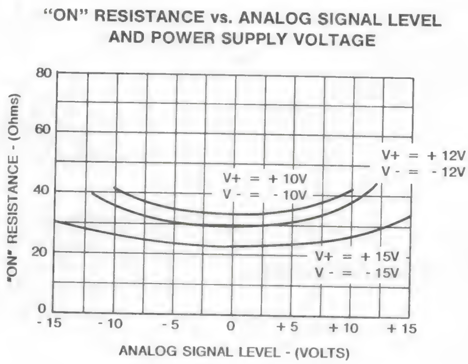
HI-5048

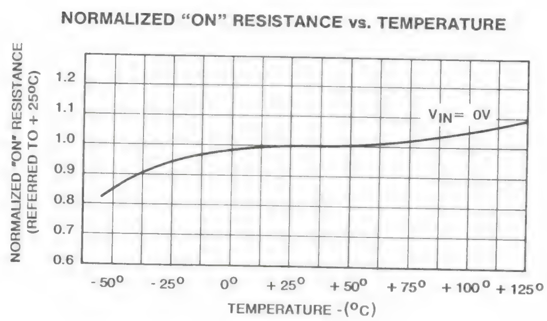
DESIGN INFORMATION

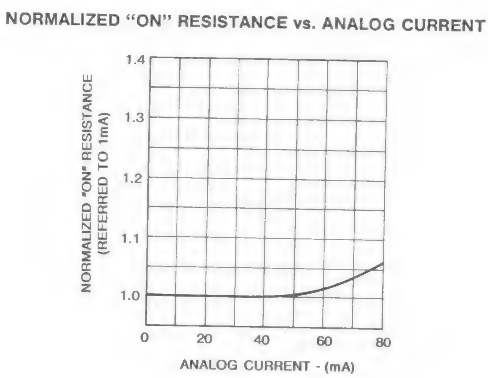
Dual SPST CMOS Analog Switch

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$





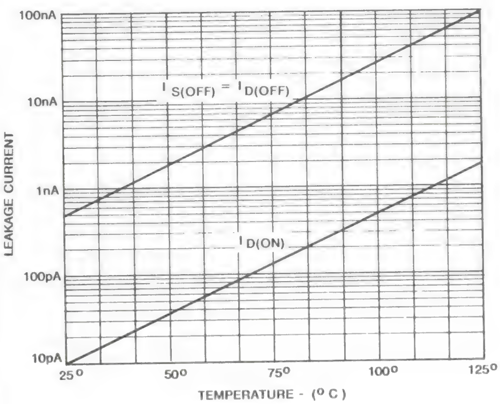


DESIGN INFORMATION (Continued)

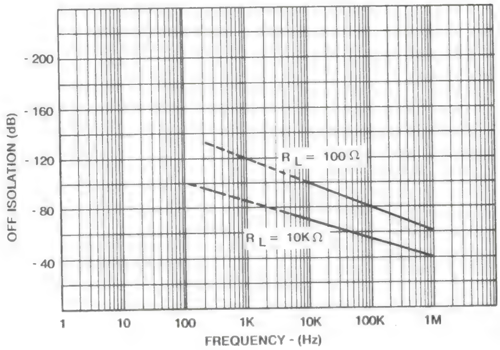
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

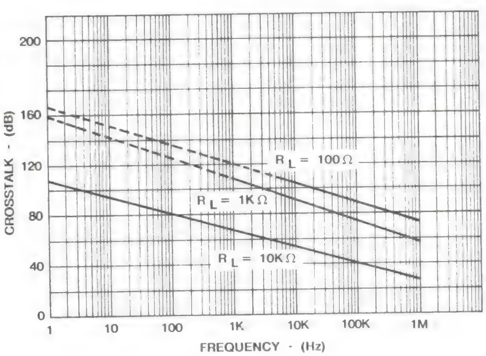
ON/OFF LEAKAGE CURRENT vs. TEMPERATURE



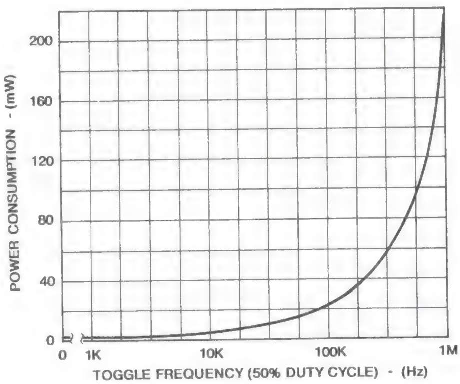
"OFF" ISOLATION vs. FREQUENCY



CROSSTALK vs. FREQUENCY



POWER CONSUMPTION vs. FREQUENCY



ANALOG

CMOS Analog Multiplexers

5

CMOS ANALOG MULTIPLEXER DATA SHEETS **PAGE**

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

HARRIS

HI-506/883
HI-507/883

Single 16/Differential 8 Channel CMOS Analog Multiplexer

January 1989

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Low On Resistance (Max.) 400Ω**
- **Wide Analog Signal Range .... ±15V**
- **TTL/CMOS Compatible .... 2.4V (Logic "1")**
- **Access Time (Max.) 1000ns**
- **44V Maximum Power Supply**
- **Break-Before-Make Switching**
- **No Latch-up**
- **Replaces DG506A/DG506AA and DG507A/DG507AA**

Applications

- **Data Acquisition Systems**
- **Precision Instrumentation**
- **Demultiplexing**
- **Selector Switch**

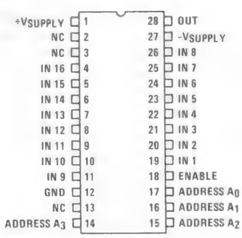
Description

These monolithic CMOS multiplexers each include an array of sixteen analog switches, a digital decode circuit for channel selection, voltage reference for logic thresholds, and an ENABLE input for device selection when several multiplexers are present.

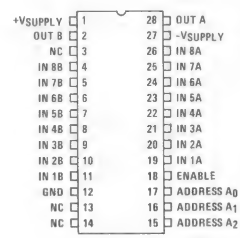
The Dielectric Isolation (DI) process used in fabrication of these devices eliminates the problem of latchup. Also, DI offers much lower substrate leakage and parasitic capacitance than conventional junction isolated CMOS. The switching threshold for each digital input is established by an internal +5V reference, providing a guaranteed minimum 2.4V for logic "1" and maximum 0.8V for logic "0". This allows direct interface without pullup resistors to signals from most logic families: CMOS, TTL, DTL and some PMOS. For protection against transient overvoltage, the digital inputs include a series 200Ω resistor and diode clamp to each supply. The HI-506/883 is a sixteen channel single-ended multiplexer, and the HI-507/883 is an eight channel differential version. If input overvoltage protection is needed, the HI-546/833 or HI-547/883 multiplexers are recommended. For further information see Application Notes 520 and 521.

Pinouts

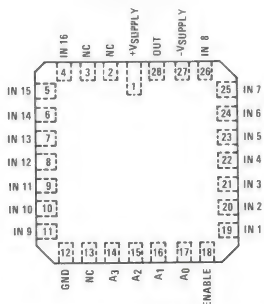
HI1-506/883 (CERAMIC DIP)
TOP VIEW



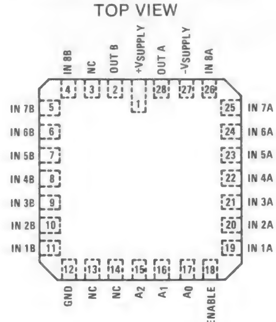
HI1-507/883 (CERAMIC DIP)
TOP VIEW



HI4-506/883 (CERAMIC LCC)
TOP VIEW

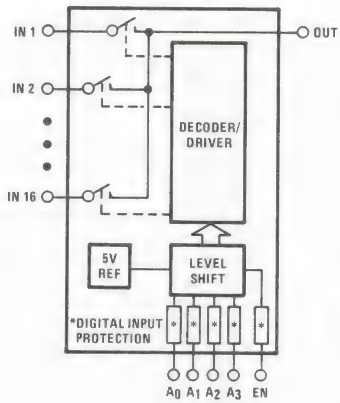


HI4-507/883 (CERAMIC LCC)
TOP VIEW



Functional Diagrams

HI-506/883

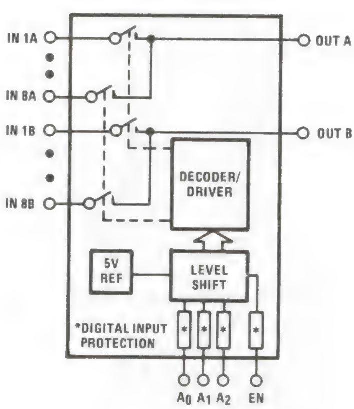


TRUTH TABLES

HI-506/883

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	None
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507/883



HI-507/883

A_2	A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

Absolute Maximum Ratings

Voltage Between Supply Pins 44V
$+V_{SUPPLY}$ to Ground 22V
$-V_{SUPPLY}$ to Ground 25V
Analog Input Voltage
$+V_S$ .... $+V_{SUPPLY}$ +2V
$-V_S$ .... $-V_{SUPPLY}$ -2V
Digital Input Voltage
$+V_{EN}$, $+V_A$ .... $+V_{SUPPLY}$ +4V
$-V_{EN}$, $-V_A$ .... $-V_{SUPPLY}$ -4V
or 20mA, whichever occurs first.
Continuous Current, S or D 20mA
Peak Current, S or D
(Pulsed at 1ms, 10% Duty Cycle Max.) 40mA
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering 10 Seconds) .... 275°C

Junction Temperature .... +175°C
Thermal Resistance, Junction-to-Case (θjc)
Ceramic DIP Package .... 18°C/W
Ceramic LCC Package .... 20°C/W
Thermal Resistance, Junction-to-Ambient (θja)
Ceramic DIP Package .... 51°C/W
Ceramic LCC Package .... 74°C/W
Power Dissipation at 75°C
Ceramic DIP Package 1.97W
Ceramic LCC Package 1.35W
Power Dissipation Derating Factor (Above +75°C)
Ceramic DIP Package .... 19.8mW/°C
Ceramic LCC Package .... 13.5mW/°C
ESD Classification .... ≤2000V

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) .... ±15V
Analog Input Voltage (V_S) .... $\pm V_{SUPPLY}$

Logic Low Level (V_{AL}) .... 0V to 0.8V
Logic High Level (V_{AH}) .... 2.4V to $+V_{SUPPLY}$
Max RMS Current, S or D 8mA

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISITICS

Devices Tested at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 2.4V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current	I_{IH}	Measure Inputs Sequentially, Connect All Unused Inputs to GND	1, 2, 3	+25°C, +125°C, -55°C	-1.0	1.0	µA
	I_{IL}		1, 2, 3	+25°C, +125°C, -55°C	-1.0	1.0	µA
Leakage Current Into the Source Terminal of an "OFF" Switch	$+I_{S(OFF)}$	V_S = +10V, V_D = -10V, V_{EN} = 0.8V	1	+25°C	-10	+10	nA
		All Unused Inputs = -10V	2, 3	+125°C, -55°C	-50	+50	nA
	$-I_{S(OFF)}$	V_S = -10V, V_D = +10V, V_{EN} = 0.8V	1	+25°C	-10	+10	nA
		All Unused Inputs = +10V	2, 3	+125°C, -55°C	-50	+50	nA
Leakage Current Into the Drain Terminal of an "OFF" Switch	$+I_{D(OFF)}$	V_D = +10V, V_{EN} = 0.8V	1	+25°C	-10	+10	nA
		All Unused Inputs = -10V HI-506/883	2, 3	+125°C, -55°C	-300	+300	nA
		HI-507/883	2, 3	+125°C, -55°C	-200	+200	nA
	$-I_{D(OFF)}$	V_D = -10V, V_{EN} = 0.8V	1	+25°C	-10	+10	nA
		All Unused Inputs = +10V HI-506/883	2, 3	+125°C, -55°C	-300	+300	nA
		HI-507/883	2, 3	+125°C, -55°C	-200	+200	nA
Leakage Current From an "ON" Driver Into the Switch (Drain)	$+I_{D(ON)}$	V_S = V_D = +10V	1	+25°C	-10	+10	nA
		All Unused Inputs = -10V HI-506/883	2, 3	+125°C, -55°C	-300	+300	nA
		HI-507/883	2, 3	+125°C, -55°C	-200	+200	nA
	$-I_{D(ON)}$	V_S = V_D = -10V	1	+25°C	-10	+10	nA
		All Unused Inputs = +10V HI-506/883	2, 3	+125°C, -55°C	-300	+300	nA
		HI-507/883	2, 3	+125°C, -55°C	-200	+200	nA
Positive Supply Current	I(+)	V_A = 0V, V_{EN} = 2.4V	1, 2, 3	+25°C, +125°C, -55°C		3.0	mA
Negative Supply Current	I(-)	V_A = 0V, V_{EN} = 2.4V	1, 2, 3	+25°C, +125°C, -55°C	-1.0		mA
Standby Positive Supply Current	$+I_{SBY}$	V_A = 0V, V_{EN} = 0V	1, 2, 3	+25°C, +125°C, -55°C		3.0	mA
Standby Negative Supply Current	$-I_{SBY}$	V_A = 0V, V_{EN} = 0V	1, 2, 3	+25°C, +125°C, -55°C	-1.0		mA
Switch "ON" Resistance	$+R_{DS1}$	V_S = 10V	1	+25°C		300	Ω
		I_D = 1mA	2, 3	+125°C, -55°C		400	Ω
	$-R_{DS1}$	V_S = -10V	1	+25°C		300	Ω
		I_D = -1mA	2, 3	+125°C, -55°C		400	Ω
Logic Level Voltage	V_{AL}	Note 1	1, 2, 3	+25°C, +125°C, -55°C		0.8	V
	V_{AH}	Note 1	1, 2, 3	+25°C, +125°C, -55°C	2.4		V V

NOTE 1. Use for forcing conditions for all DC tests unless otherwise specified.

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 2.4V, Unless Otherwise Specified.

A.C. PARAMETERS	SYMBOL	CONDITIONS	SUBGROUP	TEMP	LIMITS MIN	LIMITS MAX	UNITS
Break-Before-Make Time Delay	t_D	$R_L = 200\Omega$, $C_L = 12.5pF$	9	+25°C	25		ns
Propagation Delay Times: Address Inputs to I/O Channel Times	t_A	$R_L = 10M\Omega$, $C_L = 14pF$	9	+25°C		500	ns
			10, 11	+125°C, -55°C		1000	ns
Enable to I/O	$t_{ON(EN)}$	$R_L = 200\Omega$, $C_L = 12.5pF$	9	+25°C		500	ns
			10, 11	+125°C, -55°C		1000	ns
	$t_{OFF(EN)}$	$R_L = 200\Omega$, $C_L = 12.5pF$	9	+25°C		500	ns
			10, 11	+125°C, -55°C		1000	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Characterized at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 2.4V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTE	TEMP	LIMITS MIN	LIMITS MAX	UNITS
Capacitance: Address Input	C_A	V+ = V- = 0V f = 1MHz	2	+25°C		12	pF
Capacitance: Output Switch	C_{OS}	V+ = V- = 0V HI-506/883	2	+25°C		90	pF
		f = 1MHz HI-507/883	2	+25°C		50	pF
Capacitance Input Switch	C_{IS}	V+ = V- = 0V f = 1MHz	2	+25°C		12	pF
Charge Transfer Error	V_{CTE}	V_S = GND V_{GEN} = 0V to 5V	2	+25°C		10	mV
Off Isolation	V_{ISO}	$V_{EN} = 0.8V$, $R_L = 1k\Omega$, $C_L = 15pF$, $V_S = 7V_{RMS}$, f = 100kHz	2, 3	+25°C	-50		dB

NOTE 2. The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

3. Worst case isolation occurs on channel 8B due to proximity of the output pins.

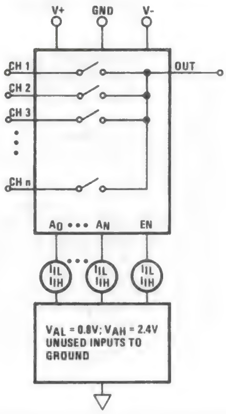
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1, 2 & 3)
Interim Electrical Parameters (Pre-Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

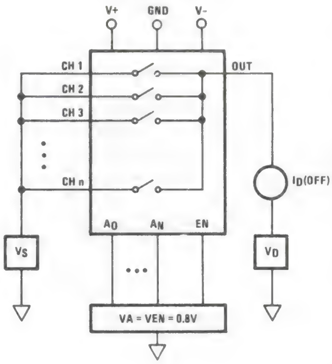
*PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

Test Circuits

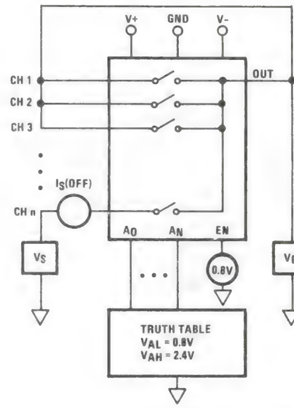
INPUT LEAKAGE CURRENT



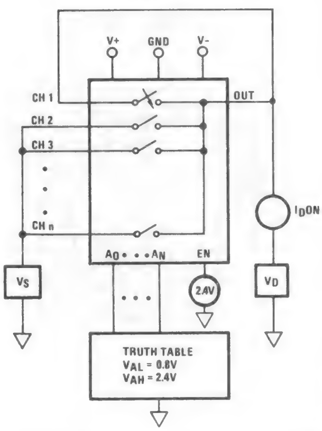
$I_{D(OFF)}$



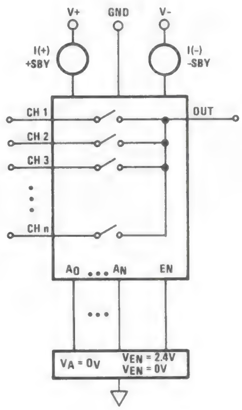
$I_{S(OFF)}$



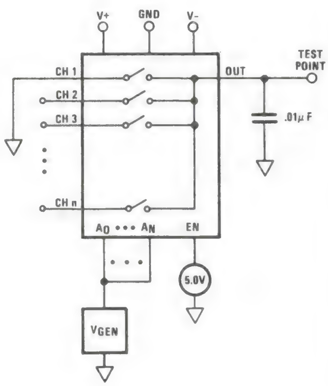
$I_{D(ON)}$



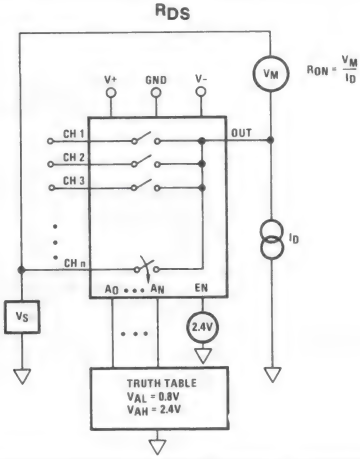
SUPPLY CURRENTS



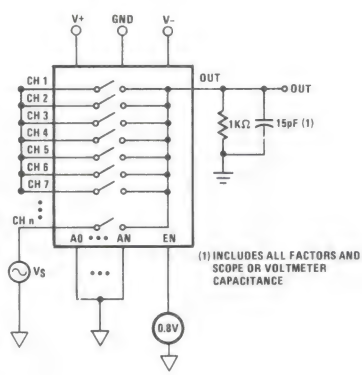
CHARGE TRANSFER ERROR



R_{DS}

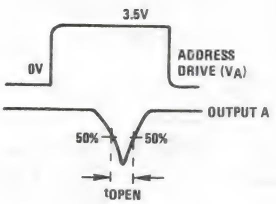


OFF CHANNEL ISOLATION

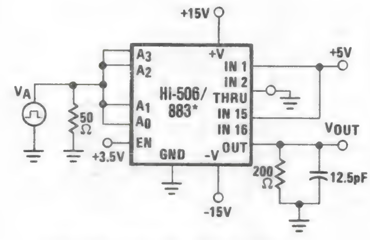


(1) INCLUDES ALL FACTORS AND SCOPE OR VOLTMETER CAPACITANCE

Switching Waveforms

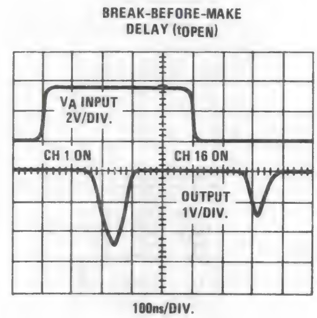


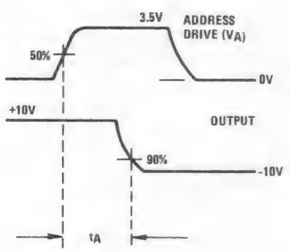
BREAK-BEFORE-MAKE DELAY (t_{OPEN})



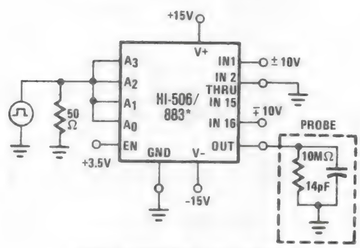
*SIMILAR CONNECTION FOR HI-507/883

BREAK-BEFORE-MAKE DELAY (t_{OPEN})



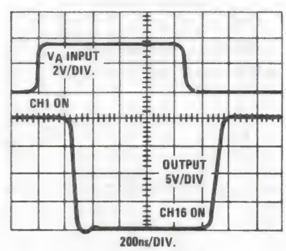


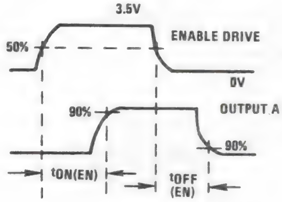
ACCESS TIME vs. LOGIC LEVEL (HIGH)



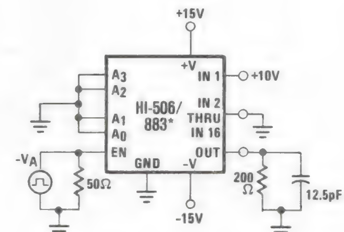
*SIMILAR CONNECTION FOR HI-507/883

ACCESS TIME



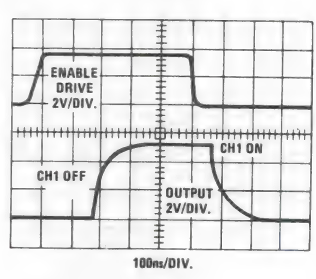


ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$



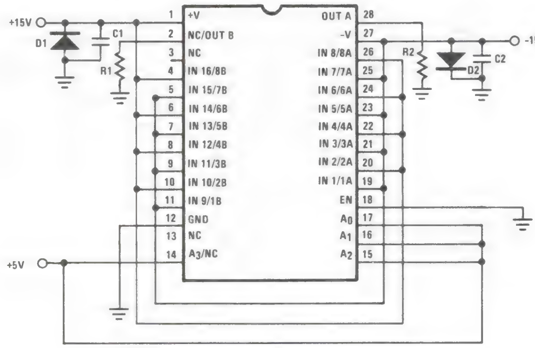
*SIMILAR CONNECTION FOR HI-507/883

ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$



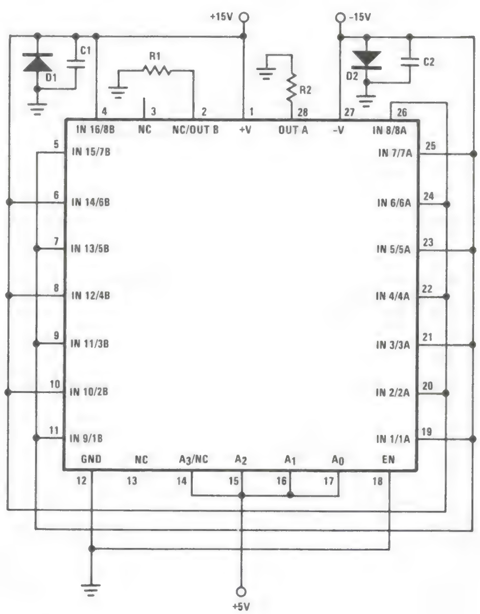
Burn-In Circuits

HI-506/883 HI-507/883 CERAMIC DIP



NOTES:
R1, R2 = 10kΩ ± 5% 1/2 or 1/4W (per socket)
C1, C2 = .01μF (per socket) or 0.1μF (per row)
D1, D2 = IN4002 (or equivalent) (per board)

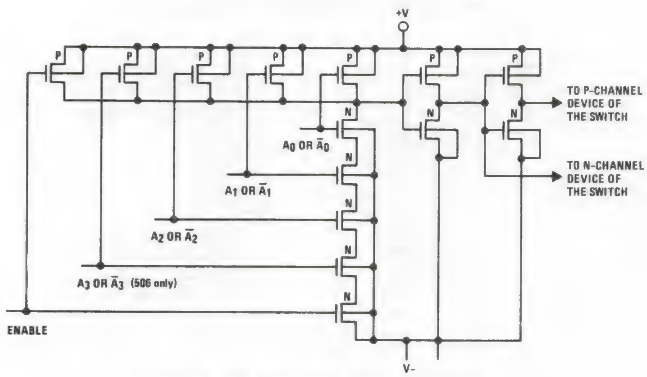
HI-506/883 HI-507/883 CERAMIC LCC



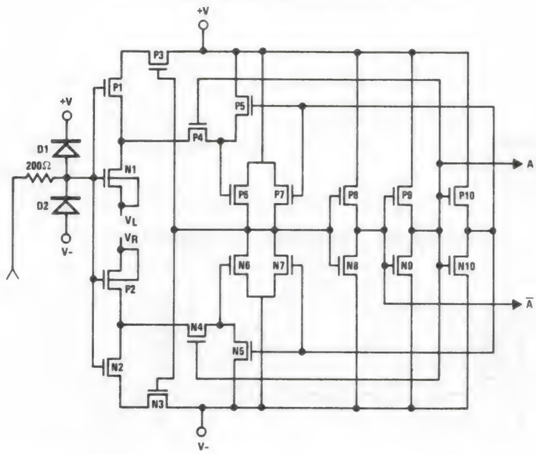
NOTES:
R1, R2 = 10kΩ ± 5% 1/2 or 1/4W (per socket)
C1, C2 = .01μF (per socket) or 0.1μF (per row)
D1, D2 = IN4002 (or equivalent) (per board)

Schematic Diagrams

ADDRESS DECODER

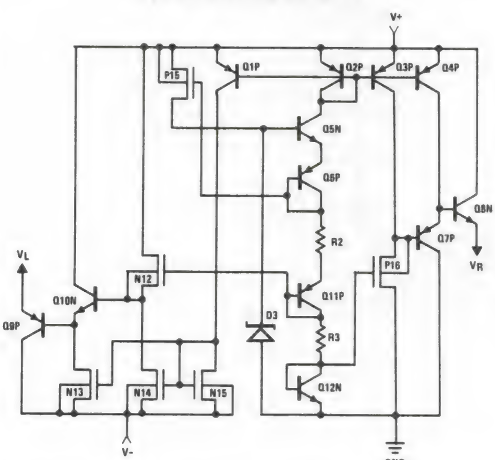


ADDRESS INPUT BUFFER LEVER SHIFTER

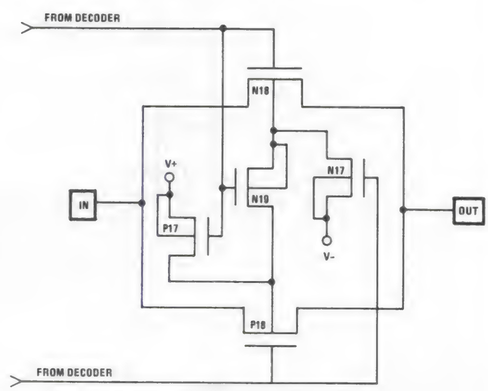


All N-Channel Bodies to V-
All P-Channel Bodies to V+
Unless Otherwise Indicated

TTL REFERENCE CIRCUIT



MULTIPLEX SWITCH



Die Characteristics

DIE DIMENSIONS: 82 x 129 x 19 mils

METALLIZATION

Type: Al

Thickness: 16kÅ ± 2kÅ

GLASSIVATION

Type: Nitride

Thickness: 7kÅ ± 0.7kÅ

WORST CASE CURRENT DENSITY: 1.4×10^5 A/cm^2

TRANSISTOR COUNT:

HI-506/883 421

HI-507/883 421

PROCESS: CMOS-DI

DIE ATTACH

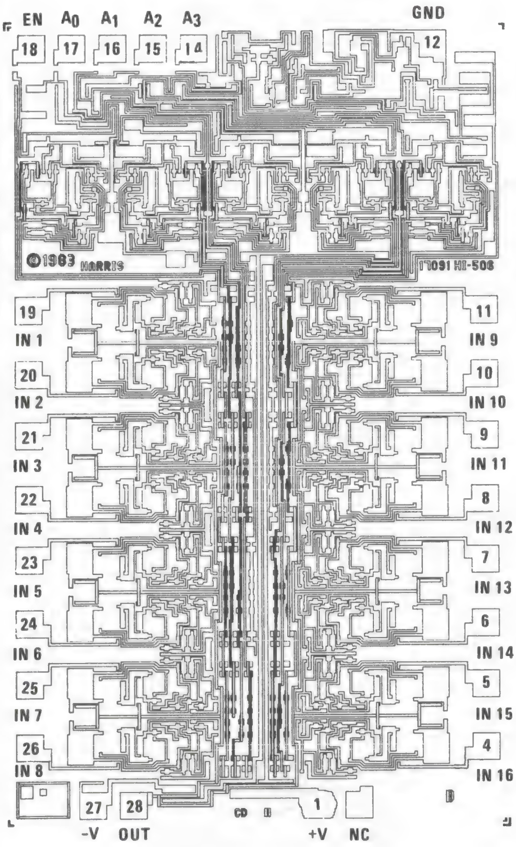
Material: Gold Silicon Eutectic Alloy

Temperature: Ceramic DIP — 460°C (Max)

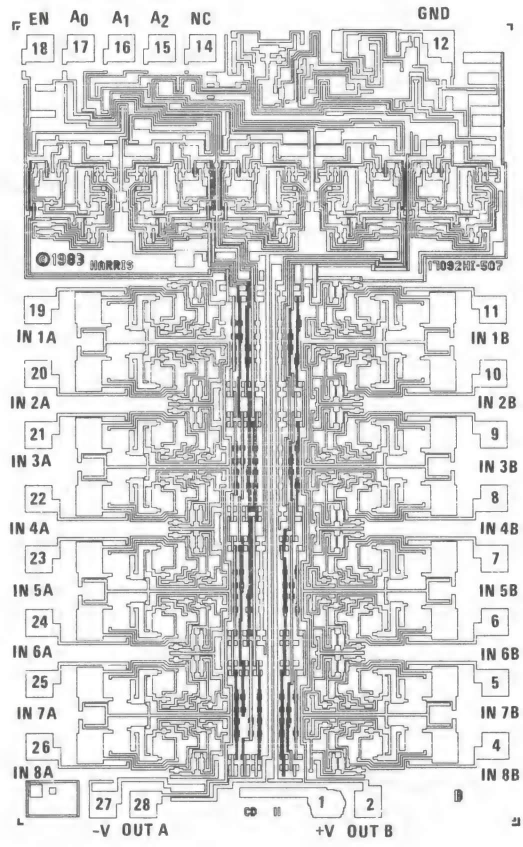
Ceramic LCC — 420°C (Max)

Metallization Mask Layout

HI-506/883



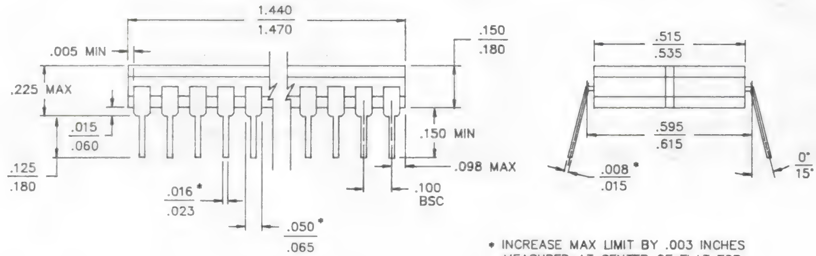
HI-507/883



NOTE: Pad Numbers Correspond to DIP Pin Numbers Only

Packaging†

28 PIN CERAMIC DIP

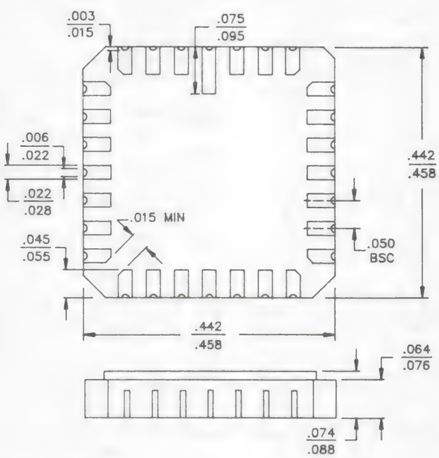


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-10

28 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-4

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

HI-506
HI-507

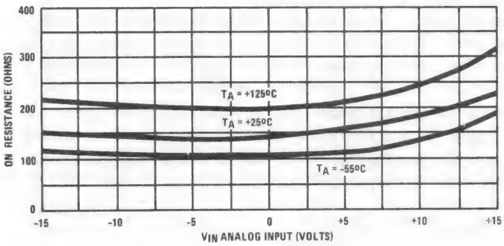
DESIGN INFORMATION

Single 16/Differential 8 Channel CMOS Analog Multiplexer

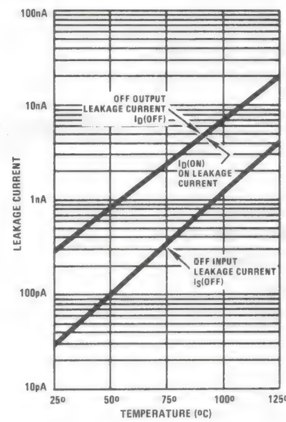
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics
Unless Otherwise Specified: $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = +2.4V$, $V_{AL} = 0.8V$.

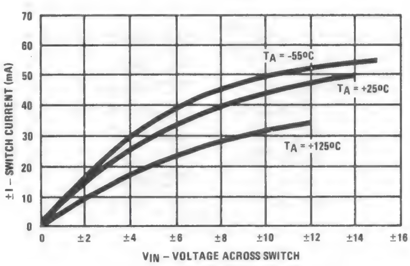
ON RESISTANCE vs. ANALOG INPUT VOLTAGE, TEMPERATURE



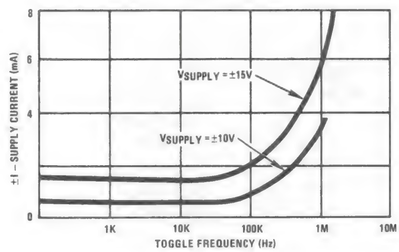
LEAKAGE CURRENT vs. TEMPERATURE



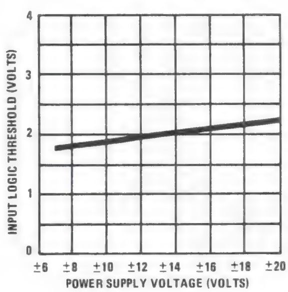
ON CHANNEL CURRENT vs. VOLTAGE



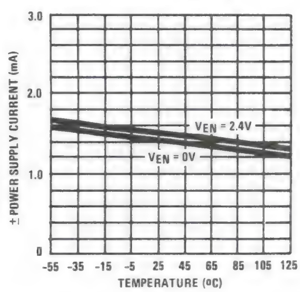
SUPPLY CURRENT vs. TOGGLE FREQUENCY



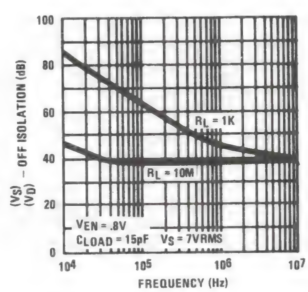
LOGIC THRESHOLD vs. POWER SUPPLY VOLTAGE



POWER SUPPLY CURRENT vs. TEMPERATURE



OFF ISOLATION vs. FREQUENCY



HARRIS

HI-508/883
HI-509/883

Single 8/Differential 4 Channel CMOS Analog Multiplexer

January 1989

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Low On Resistance (Max.) 400Ω**
- **Wide Analog Signal Range .... ±15V**
- **TTL/CMOS Compatible........................2.4V (Logic "1")**
- **Access Time (Max.) 1000ns**
- **44V Maximum Power Supply**
- **Break-Before-Make Switching**
- **No Latch-up**
- **Replaces DG508A/DG508AA and DG509A/DG509AA**

Applications

- **Data Acquisition Systems**
- **Precision Instrumentation**
- **Demultiplexing**
- **Selector Switch**

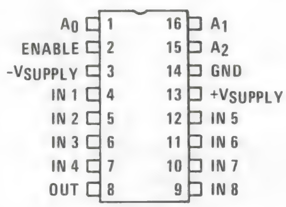
Description

These monolithic CMOS multiplexers each include an array of eight analog switches, a digital decode circuit for channel selection, a voltage reference for logic thresholds, and an ENABLE input for device selection when several multiplexers are present.

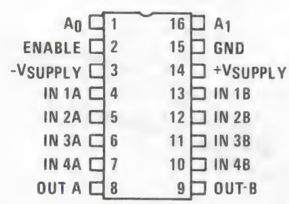
The Dielectric Isolation (DI) process used in fabrication of these devices eliminates the problem of latch-up. Also, DI offers much lower substrate leakage and parasitic capacitance than conventional junction-isolated CMOS. Switches are guaranteed to break-before-make, so that two channels are never shorted together. The switching threshold for each digital input is established by an internal +5V reference, providing a guaranteed minimum 2.4V for logic "1" and Maximum 0.8V for logic "0". This allows direct interface without pull-up resistors to signals from most logic families: CMOS, TTL, DTL and some PMOS. For protection against transient overvoltage, the digital inputs include a series 200Ω resistor and a diode clamp to each supply. The HI-508/883 is an eight channel single-ended multiplexer, and the HI-509/883 is a four channel differential version. If input overvoltage protection is needed, the HI-548/883 and HI-549/883 multiplexers are recommended. For further information, see Application Notes 520 and 521.

Pinouts

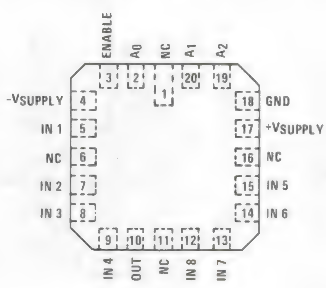
HI1-508/883 (CERAMIC DIP)
TOP VIEW



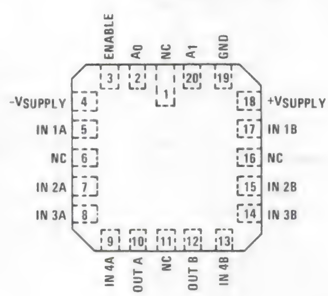
HI1-509/883 (CERAMIC DIP)
TOP VIEW



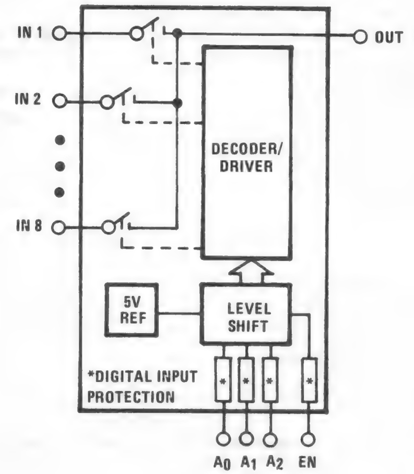
HI4-508/883 (CERAMIC LCC)
TOP VIEW



HI4-509/883 (CERAMIC LCC)
TOP VIEW



Functional Diagrams

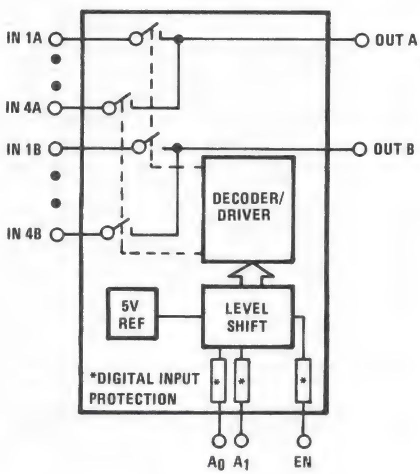


HI-508/883

TRUTH TABLES

HI-508/883

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8



HI-509/883

HI-509/883

A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

Absolute Maximum Ratings

Voltage Between Supply Pins 44V
$+V_{SUPPLY}$ to Ground 22V
$-V_{SUPPLY}$ to Ground 22V
Analog Input Voltage
- $+V_S$ .... $+V_{SUPPLY}$ +2V
- $-V_S$ .... $-V_{SUPPLY}$ -2V

Digital Input Voltage
- $+V_{EN}$, $+V_A$ .... $+V_{SUPPLY}$ +4V
- $-V_{EN}$, $-V_A$ .... $-V_{SUPPLY}$ -4V

or 20mA, whichever occurs first.

Continuous Current, S or D 20mA
Peak Current, S or D
(Pulsed at 1ms, 10% Duty Cycle Max.) 40mA
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering 10 Seconds) .... 275°C

Junction Temperature .... +175°C
Thermal Resistance, Junction-to-Case (θjc)
- Ceramic DIP Package .... 21°C/W
- Ceramic LCC Package .... 20°C/W

Thermal Resistance, Junction-to-Ambient (θja)
- Ceramic DIP Package .... 83°C/W
- Ceramic LCC Package .... 81°C/W

Power Dissipation (at 75°C)
- Ceramic DIP Package 1.20W
- Ceramic LCC Package 1.23W

Power Dissipation Derating Factor (Above +75°C)
- Ceramic DIP Package .... 12.0mW/°C
- Ceramic LCC Package .... 12.3mW/°C

ESD Classification .... ≤2000V

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) .... ±15V
Analog Input Voltage (V_S) .... $\pm V_{SUPPLY}$
Logic Low Level (V_{AL}) .... 0V to 0.8V
Logic High Level (V_{AH}) .... 2.4V to $+V_{SUPPLY}$
Max RMS Current, S or D 8mA

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 2.4V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current	I_{IH}	Measure Inputs Sequentially, Connect All Unused Inputs to GND	1, 2, 3	+25°C, +125°C -55°C	-1.0	1, 0	μA
	I_{IL}		1, 2, 3	+25°C, +125°C -55°C	-1.0	1, 0	μA
Leakage Current Into the Source Terminal of an"OFF" Switch	$+I_{S(OFF)}$	V_S = +10V, V_D = -10V, V_{EN} = 0.8V	1	+25°C	-10	+10	nA
		All Unused Inputs = -10V	2, 3	+125°C, -55°C	-50	+50	nA
	$-I_{S(OFF)}$	V_S = -10V, V_D = +10V, V_{EN} = 0.8V	1	+25°C	-10	+10	nA
		All Unused Inputs = +10V	2, 3	+125°C, -55°C	-50	+50	nA
Leakage Current Into the Drain Terminal of an "OFF" Switch	$+I_{D(OFF)}$	V_D = +10V, V_{EN} = 0.8V	1	+25°C	-10	+10	nA
		All Unused Inputs = -10V HI-508/883	2, 3	+125°C, -55°C	-200	+200	nA
		HI-509/883	2, 3	+125°C, -55°C	-100	+100	nA
	$-I_{D(OFF)}$	V_D = -10V, V_{EN} = 0.8V	1	+25°C	-10	+10	nA
		All Unused Inputs = +10V HI-508/883	2, 3	+125°C, -55°C	-200	+200	nA
		HI-509/883	2, 3	+125°C, -55°C	-100	+100	nA
Leakage Current From an "ON" Driver Into the Switch (Drain)	$+I_{D(ON)}$	V_S = V_D = +10V	1	+25°C	-10	+10	nA
		All Unused Inputs = -10V HI-508/883	2, 3	+125°C, -55°C	-200	+200	nA
		HI-509/883	2, 3	+125°C, -55°C	-100	+100	nA
	$-I_{D(ON)}$	V_S = V_D = -10V	1	+25°C	-10	+10	nA
		All Unused Inputs = +10V HI-508/883	2, 3	+125°C, -55°C	-200	+200	nA
		HI-509/883		+125°C, -55°C	-100	+100	nA
Positive Supply Current	I(+)	V_A = 0V, V_{EN} = 2.4V	1, 2, 3	+25°C, +125°C, -55°C		2.4	mA
Negative Supply Current	I(-)	V_A = 0V, V_{EN} = 2.4V	1, 2, 3	+25°C, +125°C, -55°C	-1.0		mA
Standby Positive Supply Current	$+I_{SBY}$	V_A = 0V, V_{EN} = 0V	1, 2, 3	+25°C, +125°C, -55°C		2.4	mA
Standby Negative Supply Current	$-I_{SBY}$	V_A = 0V, V_{EN} = 0V	1, 2, 3	+25°C, +125°C, -55°C	-1.0		mA
Switch "ON" Resistance	$+R_{DS1}$	V_S = 10V	1	+25°C		300	Ω
		I_D = 1mA	2, 3	+125°C, -55°C		400	Ω
	$-R_{DS1}$	V_S = -10V	1	+25°C		300	Ω
		I_D = -1mA	2, 3	+125°C, -55°C		400	Ω
Logic Level Voltage	V_{AL}	Note1	1, 2, 3	+25°C, +125°C,		0.8	V
	V_{AH}	Note 1	1, 2, 3	-55°C	2.4		V

NOTE 1. Used for forcing conditions for all DC tests unless otherwise specified.

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 2.4V, Unless Otherwise Specified.

A.C. PARAMETERS	SYMBOL	CONDITIONS	SUBGROUP	TEMP	LIMITS MIN	LIMITS MAX	UNITS
Break-Before-Make Time Delay	t_D	R_L = 200Ω, C_L = 12.5pF	9	+25°C	25		ns
Propagation Delay Times: Address Inputs to I/O Channel Times	t_A	R_L = 10MΩ, C_L = 14pF	9	+25°C		500	ns
			10, 11	+125°C, -55°C		1000	ns
Enable to I/O	$t_{ON(EN)}$	R_L = 200Ω, C_L = 12.5pF	9	+25°C		500	ns
			10, 11	+125°C, -55°C		1000	ns
	$t_{OFF(EN)}$	R_L = 200Ω, C_L = 12.5pF	9	+25°C		500	ns
			10, 11	+125°C, -55°C		1000	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Characterized at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 2.4V, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMP	LIMITS MIN	LIMITS MAX	UNITS
Capacitance: Address Input	C_A	V+ = V- = 0V f = 1MHz	2	+25°C		10	pF
Capacitance: Output Switch	C_{OS}	V+ = V- = 0V HI-508/883	2	+25°C		45	pF
		f = 1MHz HI-509/883	2	+25°C		25	pF
Capacitance Input Switch	C_{IS}	V+ = V- = 0V f = 1MHz	2	+25°C		12	pF
Charge Transfer Error	V_{CTE}	V_S = GND V_{GEN} = 0V to 5V	2	+25°C		10	mV
Off Channel Isolation	V_{ISO}	V_{EN} = 0.8V, R_L = 1kΩ C_L = 15pF, V_S = $7V_{RMS}$ f = 100kHz	2, 3	+25°C	-50		dB

NOTE 2. The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
3. Worst case isolation occurs on channel 4 due to proximity of the output pins.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

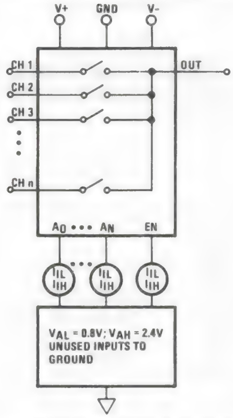
MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1, 2 & 3)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

*PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

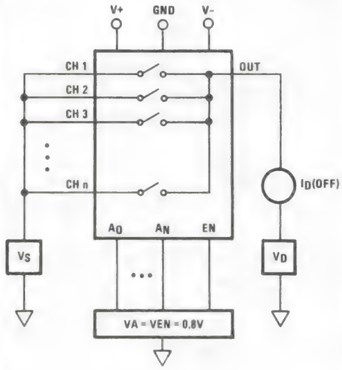
CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Test Circuits

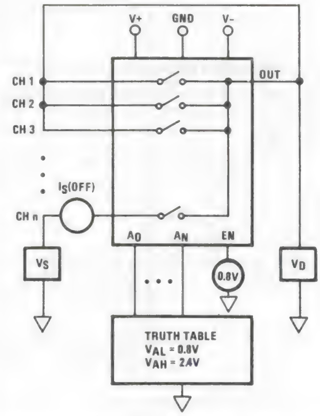
INPUT LEAKAGE CURRENT



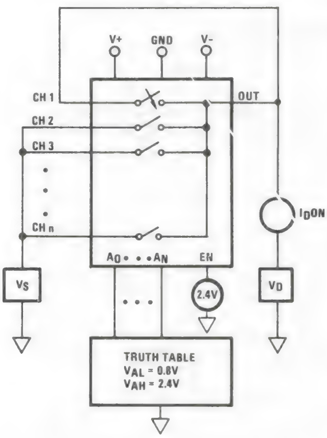
$I_{D(OFF)}$



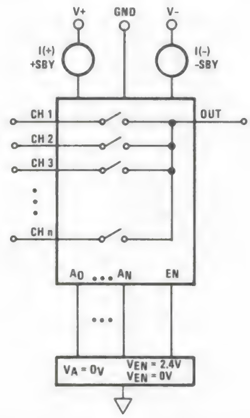
$I_{S(OFF)}$



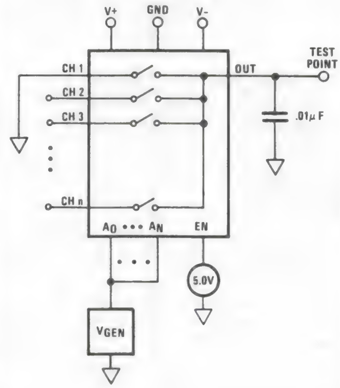
$I_{D(ON)}$



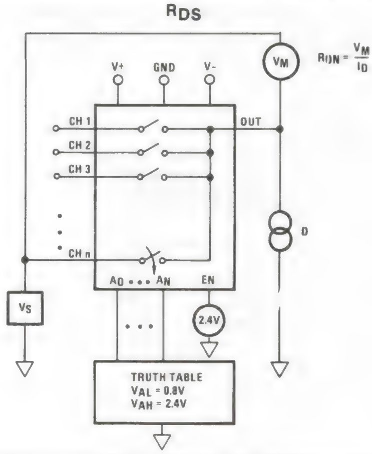
SUPPLY CURRENTS



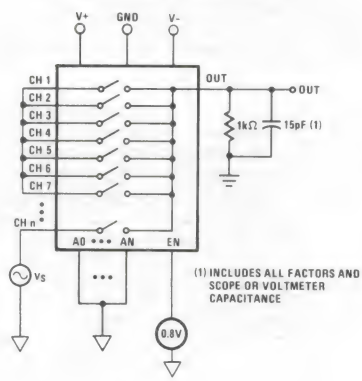
CHARGE TRANSFER ERROR



R_{DS}

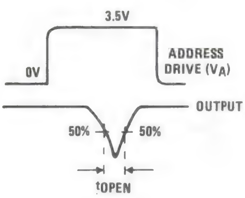


OFF CHANNEL ISOLATION

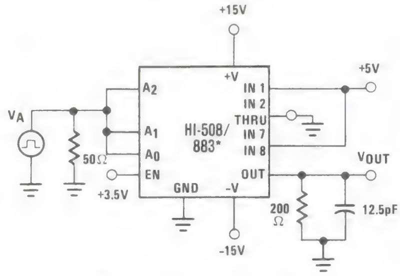


Switching Waveforms

ADDRESS DRIVE

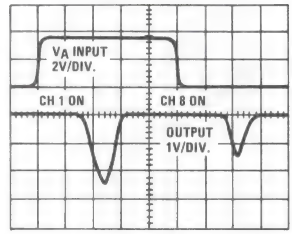


BREAK-BEFORE-MAKE DELAY (t_{OPEN})



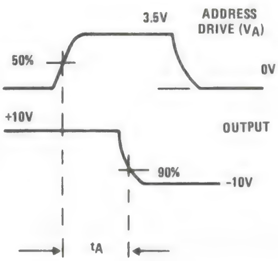
*SIMILAR CONNECTION FOR HI-509/883

BREAK-BEFORE-MAKE DELAY (t_{OPEN})

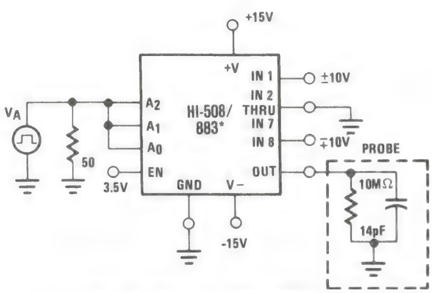


100ns/DIV

ACCESS TIME

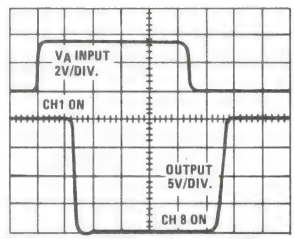


ACCESS TIME



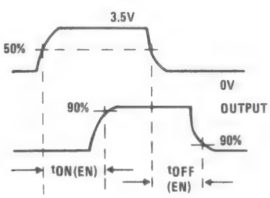
*SIMILAR CONNECTION FOR HI-509/883

ACCESS TIME

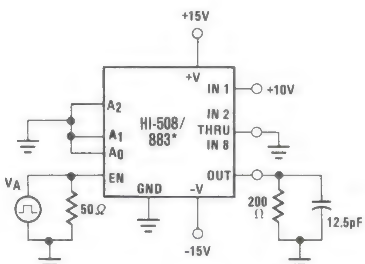


200ns/DIV

ENABLE DRIVE

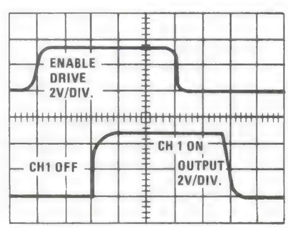


ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$



*SIMILAR CONNECTION FOR HI-509/883

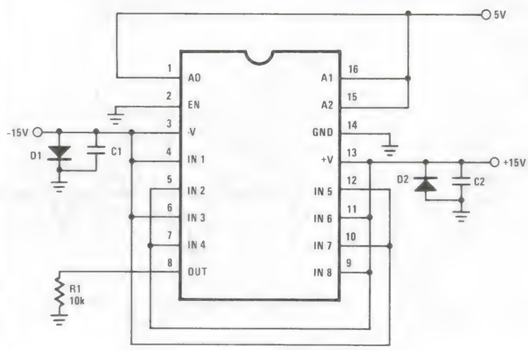
ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$



100ns/DIV

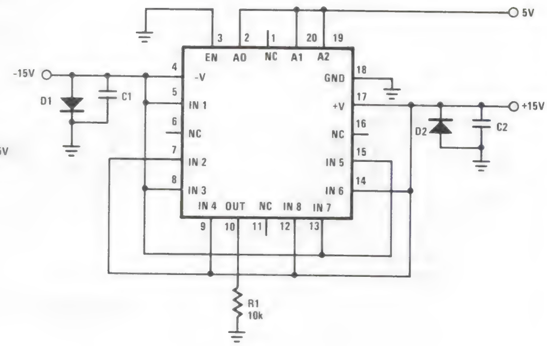
Burn-In Circuits

HI-508/883 CERAMIC DIP



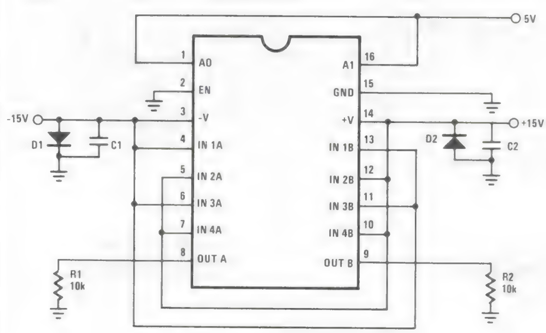
NOTES:
R1 = 10kΩ ± 5%, 1/2 or 1/4W (per socket)
C1, C2 = .01μF (per socket) or 0.1μF (per row)
D1, D2 = IN4002 (or equivalent) (per board)

HI-508/883 LCC



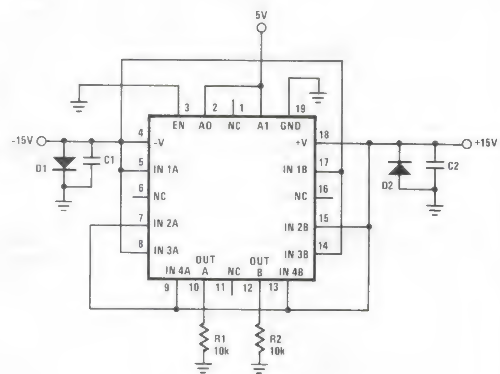
NOTES:
R1 = 10kΩ ± 5%, 1/2 or 1/4W (per socket)
C1, C2 = .01μF (per socket) or 0.1μF (per row)
D1, D2 = IN4002 (or equivalent) (per board)

HI-509/883 CERAMIC DIP



NOTES:
R1, R2 = 10kΩ ± 5%, 1/2 or 1/4W (per socket)
C1, C2 = .01μF (per socket) or 0.1μF (per row)
D1, D2 = IN4002 (or equivalent) (per board)

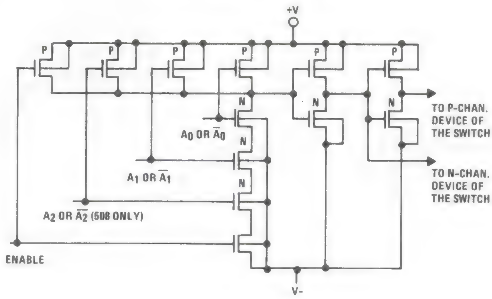
HI-509/883 LCC



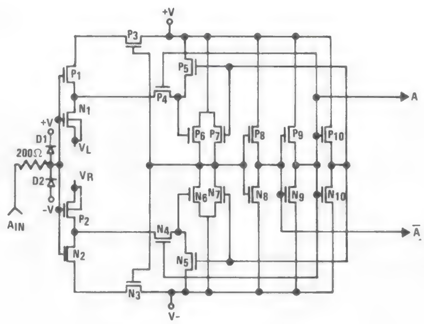
NOTES:
R1, R2 = 10kΩ ± 5%, 1/2 or 1/4W (per socket)
C1, C2 = .01μF (per socket) or 0.1μF (per row)
D1, D2 = IN4002 (or equivalent) (per board)

Schematic Diagrams

ADDRESS DECODER

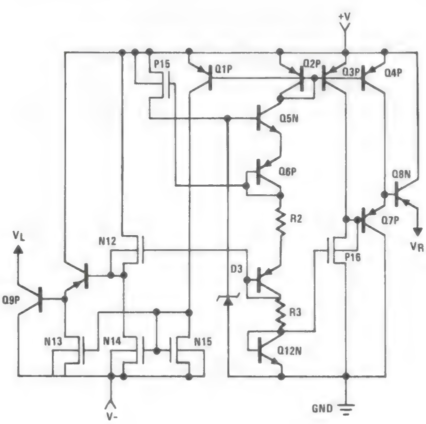


ADDRESS INPUT BUFFER LEVER SHIFTER

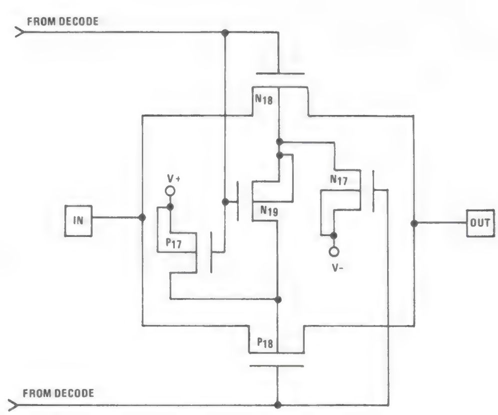


All N-Channel Bodies to V-
All P-Channel Bodies to V+
Unless Otherwise Indicated

TTL REFERENCE CIRCUIT



MULTIPLEX SWITCH



5
CMOS ANALOG MULTIPLEXERS

Die Characteristics

DIE DIMENSIONS: 81.9 x 90.2 x 19 mil

METALLIZATION

Type: Al

Thickness: 16kÅ ± 2kÅ

GLASSIVATION

Type: Nitride

Thickness: 7kÅ ± 0.7kÅ

WORST CASE CURRENT DENSITY: 1.4×10^5 A/cm^2

TRANSISTOR COUNT:

HI-508/883 243

HI-509/883 243

PROCESS: CMOS-DI

DIE ATTACH

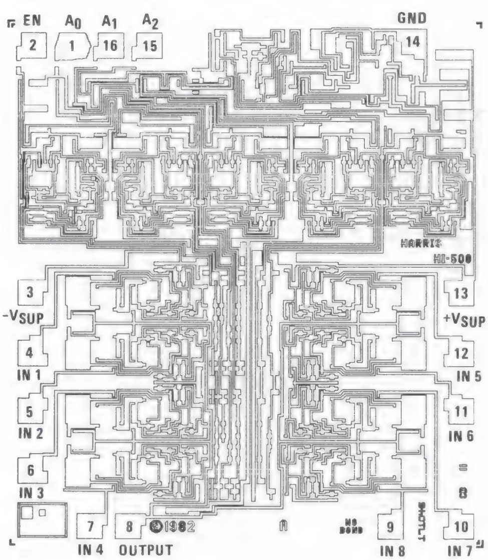
Material: Gold Silicon Eutectic Alloy

Temperature: Ceramic DIP — 460°C (Max)

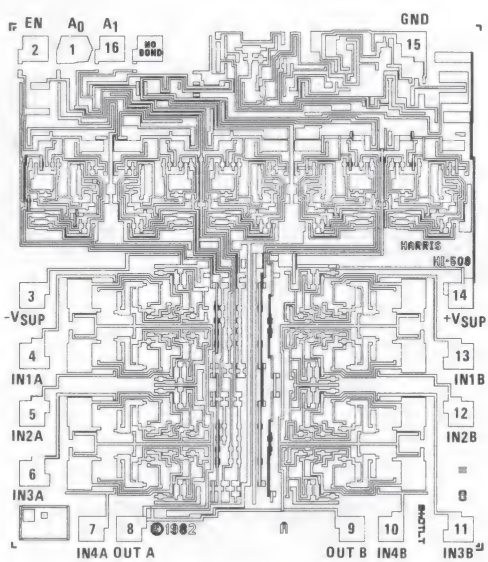
Ceramic LCC — 420°C (Max)

Metallization Mask Layout

HI-508/883



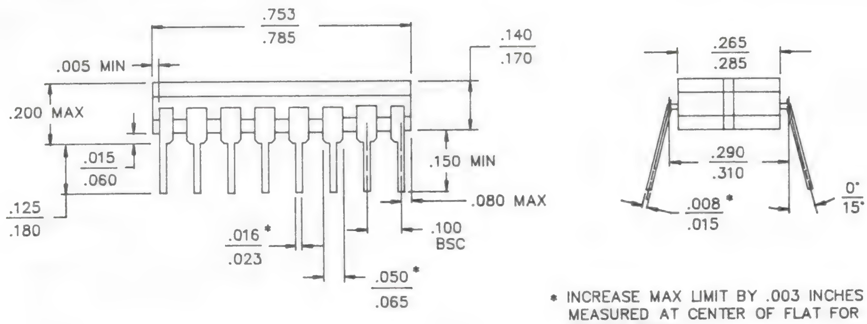
HI-509/883



NOTE: Pad Numbers Correspond to DIP Pin Numbers Only.

Packaging†

16 PIN CERAMIC DIP



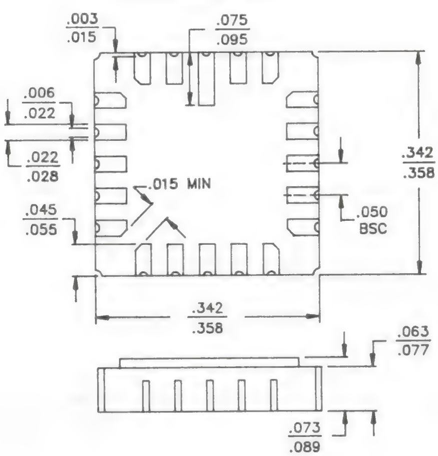
* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL
- Material: Glass Frit
- Temperature: 450°C ± 10°C
- Method: Furnace Seal

INTERNAL LEAD WIRE
- Material: Aluminum
- Diameter: 1.25 Mil
- Bonding Method: Ultrasonic

COMPLIANT OUTLINE: 38510 D-2

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL
- Material: Gold/Tin (80/20)
- Temperature: 320°C ± 10°C
- Method: Furnace Braze

INTERNAL LEAD WIRE
- Material: Aluminum
- Diameter: 1.25 Mil
- Bonding Method: Ultrasonic

COMPLIANT OUTLINE: 38510 C-2

4FEB88

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in inches.

† MIL-M-38510 Compliant Materials, Finishes & Dimensions.

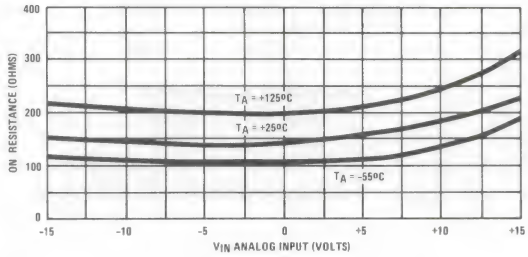
HI-508 HI-509

Single 8/Differential 4 Channel CMOS Analog Multiplexer

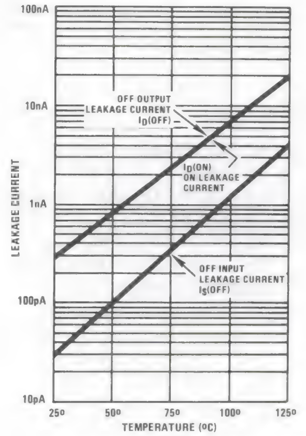
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics Unless Otherwise Specified: T_A = 25°C, V_{SUPPLY} = ±15V, V_{AH} = +2.4V, V_{AL} = 0.8V

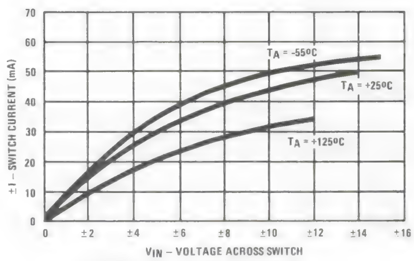
ON RESISTANCE vs. ANALOG INPUT VOLTAGE, TEMPERATURE



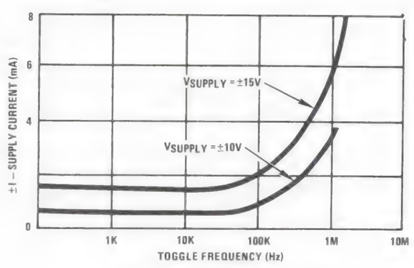
LEAKAGE CURRENT vs. TEMPERATURE



ON CHANNEL CURRENT vs. VOLTAGE



SUPPLY CURRENT vs. TOGGLE FREQUENCY



HARRIS

HI-516/883

16 Channel/Differential 8 Channel CMOS High Speed Analog Multiplexer

June 1988

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Access Time (Max. Over Temp.) 225ns
- Low Leakage (Max. Over Temp.) ..... $I_{D(OFF)}$ 100nA
- Single Ended to Differential Selectable (SDS)‡
- TTL/CMOS Compatible (LLS)†

Applications

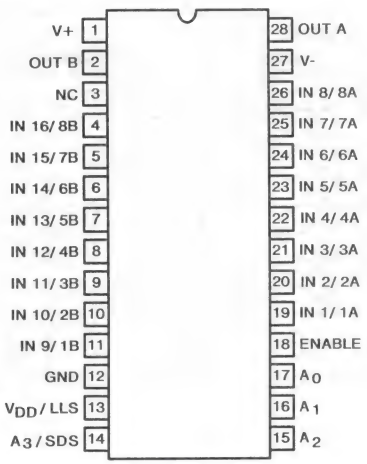
- Data Acquisition Systems
- Telemetry
- Industrial Control

Description

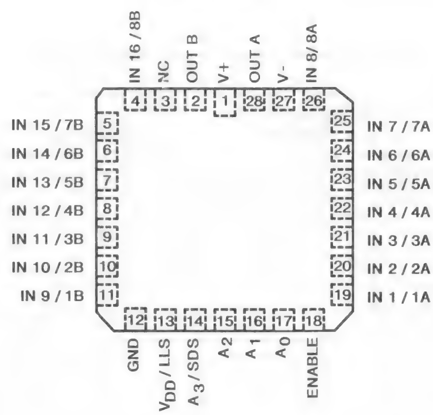
The HI-516/883 is a monolithic dielectrically isolated, high speed, high performance CMOS analog multiplexer. It offers unique built-in channel selection decoding plus an inhibit input for disabling all channels. The dual function of address input A_3 enables the HI-516/883 to be user programmed either as a single ended 16-channel multiplexer by connecting 'OUT A' to 'OUT B' and using A_3 as a digital address input, or as a 8-channel differential multiplexer by connecting A_3 to the $-V_{SUPPLY}$. The substrate leakages and parasitic capacitances are reduced substantially by using the Harris dielectric isolation process to achieve optimum performance in both high and low level signal applications. The low output leakage current ($I_{D(OFF)}$ < 100nA over temperature) of the device makes it an ideal choice for high speed data acquisition systems, precision instrumentation, and industrial process control.

Pinouts

HI1-516/883 (CERAMIC DIP)
TOP VIEW



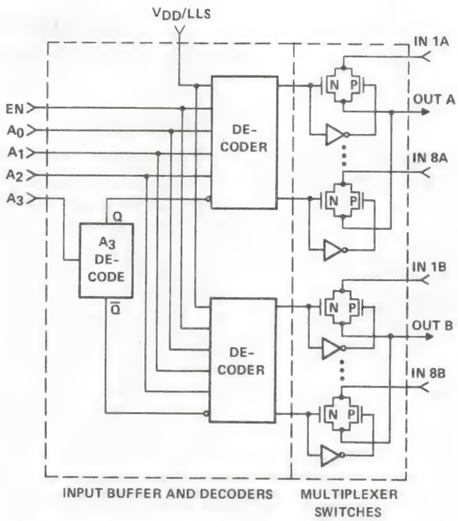
HI4-516/883 (CERAMIC LCC)
TOP VIEW



† LLS = Logic Level Select (TTL Compatible with V_{DD}/LLS Pin = Ground or Open, CMOS Compatible when V_{DD}/LLS Pin = V_{DD})

‡ SDS = Single Ended/Differential Select (Multiplexer is in Differential Mode when A_3/SDS Pin = $-V_{SUPPLY}$)

Functional Diagram



A_3 Decode		
A_3	Q	$\overline{Q}$
H	H	L
L	L	H
V-	L	L

Truth Tables

HI-516/883 USED AS 16-CHANNEL MULTIPLEXER*

USE A_3 AS DIGITAL ADDRESS INPUT					ON CHANNEL TO	
ENABLE	A_3	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	X	None	None
H	L	L	L	L	1A	None
H	L	L	L	H	2A	None
H	L	L	H	L	3A	None
H	L	L	H	H	4A	None
H	L	H	L	L	5A	None
H	L	H	L	H	6A	None
H	L	H	H	L	7A	None
H	L	H	H	H	8A	None
H	H	L	L	L	None	1B
H	H	L	L	H	None	2B
H	H	L	H	L	None	3B
H	H	L	H	H	None	4B
H	H	H	L	L	None	5B
H	H	H	L	H	None	6B
H	H	H	H	L	None	7B
H	H	H	H	H	None	8B

* For 16-Channel single-ended function, tie "Out A" to "Out B", for dual channel function use the A_3 address pin to select between MUX A and MUX B, where MUX A is selected with A_3 low.

HI-516/883 USED AS DIFFERENTIAL 8-CHANNEL MULTIPLEXER

A_3 CONNECTED TO $-V_{SUPPLY}$				ON CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	None	None
H	L	L	L	1A	1B
H	L	L	H	2A	2B
H	L	H	L	3A	3B
H	L	H	H	4A	4B
H	H	L	L	5A	5B
H	H	L	H	6A	6B
H	H	H	L	7A	7B
H	H	H	H	8A	8B

Absolute Maximum Ratings

Voltage Between Supply Pins 33V
$+V_{SUPPLY}$ to Ground 16.5V
$-V_{SUPPLY}$ to Ground 16.5V
Analog Input Voltage
- $+V_S$ .... $+V_{SUPPLY}$ +2V
- $-V_S$ .... $-V_{SUPPLY}$ -2V

Digital Input Voltage
- TTL Levels Selected (V_{DD}/LLS Pin = GND or Open)
  - $+V_A$ .... +6V
  - $-V_A$ .... -6V
  - $+A_3$/SDS .... $+V_{SUPPLY}$ +2V
  - $-A_3$/SDS .... $-V_{SUPPLY}$ -2V
- CMOS Levels Selected (V_{DD}/LLS Pin = V_{DD})
  - $+V_A$ .... $+V_{SUPPLY}$ +2V
  - $-V_A$ .... -2V

Storage Temperature Range .... -65°C to +150°C

Lead Temperature (Soldering 10 Seconds) .... 275°C
Junction Temperature .... +175°C
Thermal Resistance, Junction-to-Case (θjc)
- Ceramic DIP Package .... 18°C/W
- Ceramic LCC Package .... 40°C/W

Thermal Resistance, Junction-to-Ambient (θja)
- Ceramic DIP Package .... 50°C/W
- Ceramic LCC Package .... 81°C/W

Power Dissipation (at 75°C)
- Ceramic DIP Package 2.0W
- Ceramic LCC Package 1.23W

Power Dissipation Derating Factor (Above +75°C)
- Ceramic DIP Package .... 20.0mW/°C
- Ceramic LCC Package .... 12.3mW/°C

ESD Classification .... ≤2000V

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) .... ±15V
Analog Input Voltage (V_S) .... $\pm V_{SUPPLY}$
Logic Level Low (V_{AL}) .... 0V to 0.8V
Logic Level High (V_{AH}) .... 2.4V to $+V_{SUPPLY}$
Max RMS Current, S or D 8mA

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 2.4V, V_{DD}/LLS = GND, V_{AH} = 2.4V, V_{AL} = 0.8V Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current	I_{IH}	Measure Inputs Sequentially, Connect All Unused Inputs to GND	1, 2, 3	+25°C,+125°C,-55°C	-1.0	1.0	µA
	I_{IL}	Measure Inputs Sequentially, Connect All Unused Inputs to +5V	1, 2, 3	+25°C,+125°C,-55°C	-25	25	µA
Leakage Current Into the Source Terminal of an "OFF" Switch	$+I_{S(OFF)}$	V_S = +10V, V_D = -10V, V_{EN} = 0.8V All Unused Inputs = -10V	1, 2, 3	+25°C,+125°C,-55°C	-50	+50	nA
	$-I_{S(OFF)}$	V_S = -10V, V_D = +10V, V_{EN} = 0.8V All Unused Inputs = +10V	1, 2, 3	+25°C,+125°C,-55°C	-50	+50	nA
Leakage Current Into the Drain Terminal of an "OFF" Switch	$+I_{D(OFF)}$	V_D = +10V, V_{EN} = 0.8V, V_S = -10V All Unused Inputs = -10V	1, 2, 3	+25°C,+125°C,-55°C	-100	+100	nA
	$-I_{D(OFF)}$	V_D = -10V, V_{EN} = 0.8V, V_S = +10V All Unused Inputs = +10V	1, 2, 3	+25°C,+125°C,-55°C	-100	+100	nA
Leakage Current From an "ON" Driver Into the Switch (Drain)	$+I_{D(ON)}$	V_S = V_D = +10V All Unused Inputs = -10V	1, 2, 3	+25°C,+125°C,-55°C	-100	+100	nA
	$-I_{D(ON)}$	V_S = V_D = -10V All Unused Inputs = +10V	1, 2, 3	+25°C,+125°C,-55°C	-100	+100	nA
Positive Supply Current	I(+)	V_S = 0V, V_D = Open, V_{EN} = 2.4V Sequence All Address Combinations, Record Highest I+	1, 2, 3	+25°C,+125°C,-55°C	—	+25	mA
Negative Supply Current	I(-)	V_S = 0V, V_D = Open, V_{EN} = 2.4V Sequence All Address Combinations, Record Highest I-	1, 2, 3	+25°C,+125°C,-55°C	-25	—	mA
Standby Positive Supply Current	$+I_{SBY}$	V_A = 0.8V, V_{EN} = 0.8V, V_S = 0V, V_D = Open	1, 2, 3	+25°C,+125°C,-55°C	—	+25	mA
Standby Negative Supply Current	$-I_{SBY}$	V_A = 0.8V, V_{EN} = 0.8V, V_S = 0V, V_D = Open	1, 2, 3	+25°C,+125°C,-55°C	-25	—	mA
Switch "ON" Resistance	$+R_{DS1}$	V_S = +10V	1	+25°C	—	750	Ω
		I_D = 100µA	2, 3	+125°C,-55°C	—	1000	Ω
	$-R_{DS1}$	V_S = -10V	1	+25°C	—	750	Ω
		I_D = -100µA	2, 3	+125°C,-55°C	—	1000	Ω
Logic Level Voltage	V_{AL}(TTL)	V_{DD}/LLS = GND	1, 2, 3	+25°C,+125°C,-55°C	—	0.8	V
	V_{AH}(TTL)	V_{DD}/LLS = GND	1, 2, 3	+25°C,+125°C,-55°C	2.4	—	V
	V_{AL}(CMOS)	V_{DD}/LLS = +15V	1, 2, 3	+25°C,+125°C,-55°C	—	4.5	V
	V_{AH}(CMOS)	V_{DD}/LLS = +15V	1, 2, 3	+25°C,+125°C,-55°C	10.5	—	V

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 2.4V, V_{DD}/LLS = GND, V_{AH} = 2.4V, V_{AL} = 0.8V Unless Otherwise Specified.

A.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Break-Before-Make Time Delay	t_D	$R_L = 800\Omega$, C_L = 12.5pF	9	+25°C	10	-	ns
			10	+125°C	2	-	ns
Address Inputs to I/O Channel Delay	t_A	$R_L = 10M\Omega$, C_L = 12.5pF	9	+25°C	-	175	ns
			10, 11	+125°C, -55°C	-	225	ns
Enable to I/O Delay	$t_{ON(EN)}$	$R_L = 800\Omega$, C_L = 12.5pF	9	+25°C	-	175	ns
			10, 11	+125°C, -55°C	-	225	ns
	$t_{OFF(EN)}$	$R_L = 800\Omega$, C_L = 12.5pF	9	+25°C	-	175	ns
			10, 11	+125°C, -55°C	-	225	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 2.4V, V_{DD}/LLS = GND, V_{AH} = 2.4V, V_{AL} = 0.8V, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address Input Capacitance	C_A	V+ = V- = 0V f = 1MHz	1	+25°C	-	10	pF
Output Switch Capacitance	C_{OS}	V+ = V- = 0V f = 1MHz	1	+25°C	-	25	pF
Input Switch Capacitance	C_{IS}	V+ = V- = 0V f = 1MHz	1	+25°C	-	10	pF
Charge Transfer Error	V_{CTE}	V_S = GND, C_L = 100pF V_{GEN} = 0V to 5V, f = 500kHz	1	+25°C	-	20	mV
Off Channel Isolation	V_{ISO}	V_{EN} = 0.8V, $R_L = 1k\Omega$ C_L = 40pF, $V_S = 3V_{RMS}$ f = 500kHz	1	+25°C	-55	-	dB
Break-Before-Make Time Delay	t_D	$R_L = 800\Omega$, C_L = 12.5pF	1	-55°C	2	-	ns

NOTE: 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

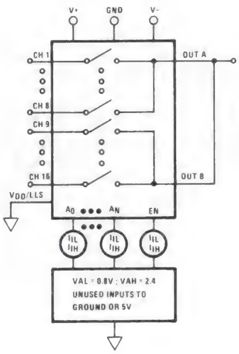
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1, 2 & 3)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

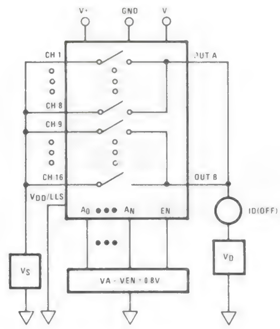
*PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

Test Circuits

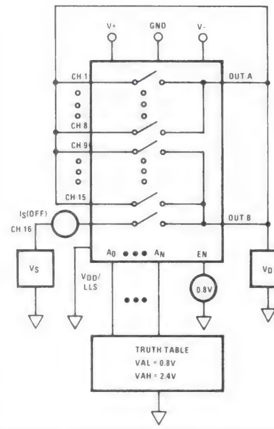
INPUT LEAKAGE CURRENT



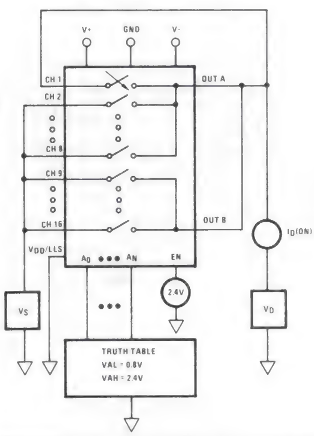
$I_{D(OFF)}$



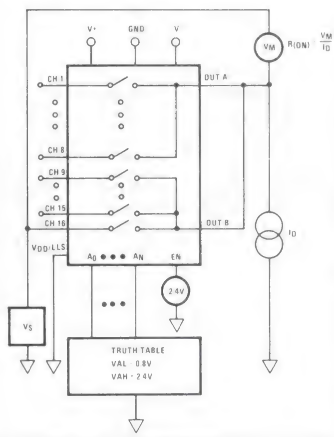
$I_{S(OFF)}$



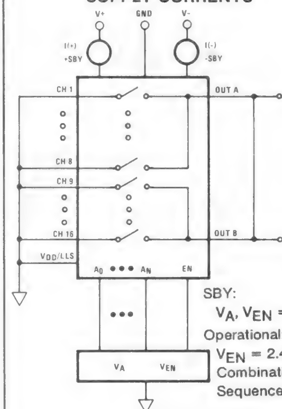
$I_{D(ON)}$



R_{DS}

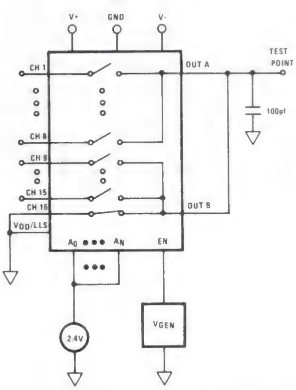


SUPPLY CURRENTS

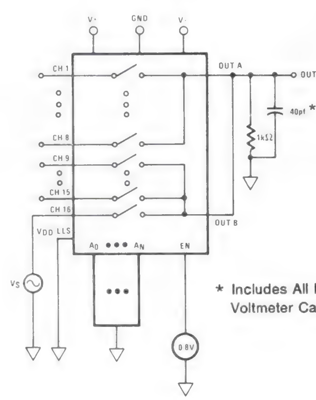


SBY:
V_A, V_{EN} = 0.8V
Operational:
V_{EN} = 2.4V, V_A = All Combinations are Sequenced

CHARGE TANSFER ERROR



OFF CHANNEL ISOLATION



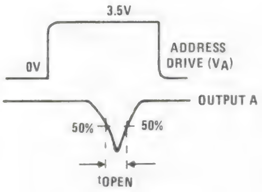
* Includes All Factors and Scope or Voltmeter Capacitance

5

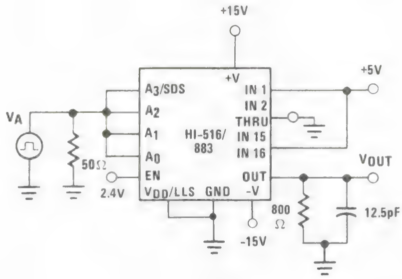
CMOS ANALOG MULTIPLEXERS

Switching Waveforms

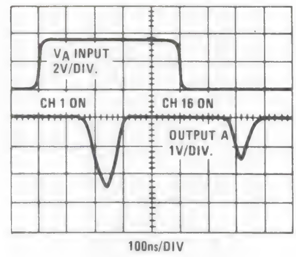
ADDRESS DRIVE



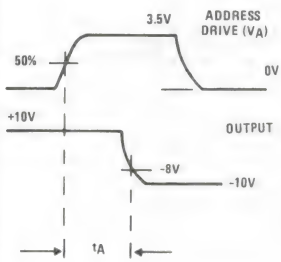
BREAK-BEFORE-MAKE DELAY (t_{OPEN})

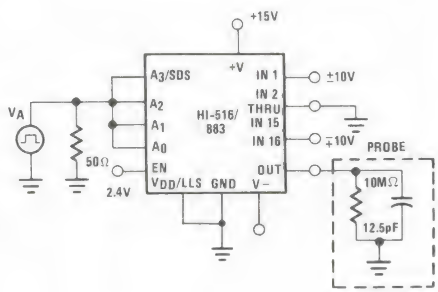


BREAK-BEFORE-MAKE DELAY (t_{OPEN})

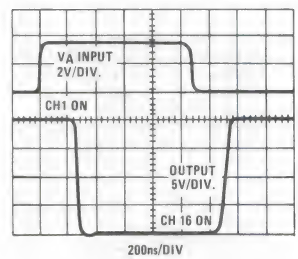


ACCESS TIME

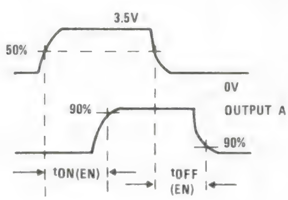




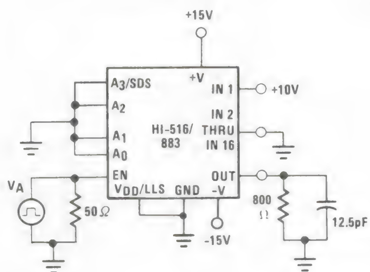
ACCESS TIME



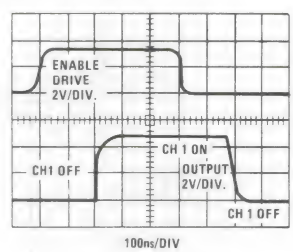
ENABLE DRIVE



ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$

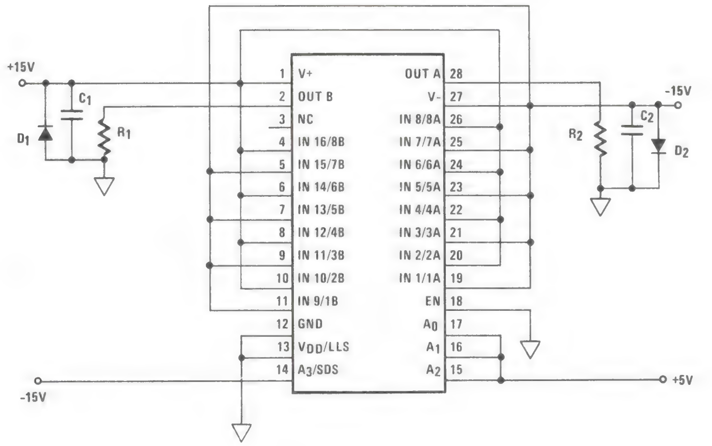


ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$



Burn-In Circuits

HI-516/883 CERAMIC DIP



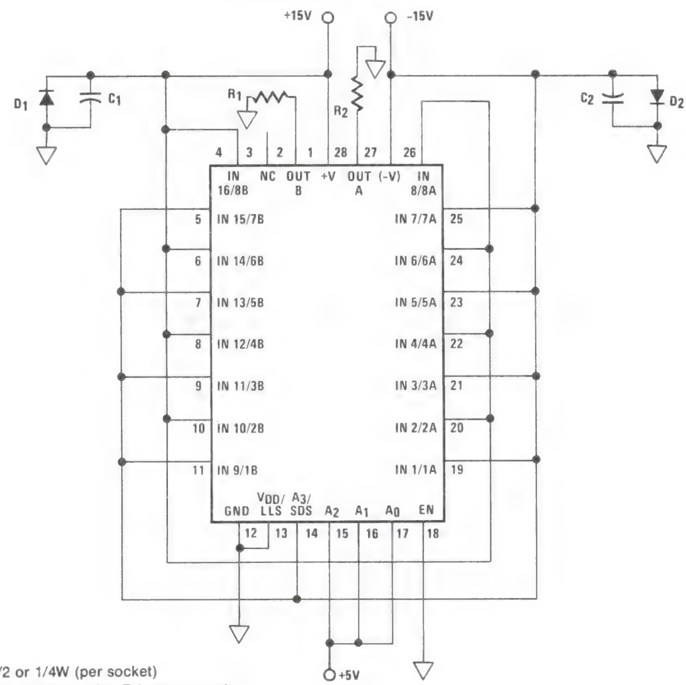
NOTES:

$R_1 = R_2 = 10k\Omega$, ±5%, 1/4 or 1/2W

$C_1 = C_2 = 0.01\mu F$ (one per socket) or $0.1\mu F$ (one per row)

$D_1 = D_2$ = IN4002 or equivalent (per board)

HI-516/883 CERAMIC LCC



NOTES:

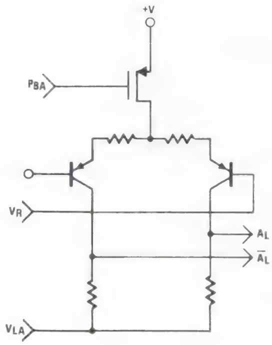
$R_1 = R_2 = 10k\Omega$, ±5%, 1/2 or 1/4W (per socket)

$C_1 = C_2 = 0.01\mu F$ (one per socket) or $0.1\mu F$ (one per row)

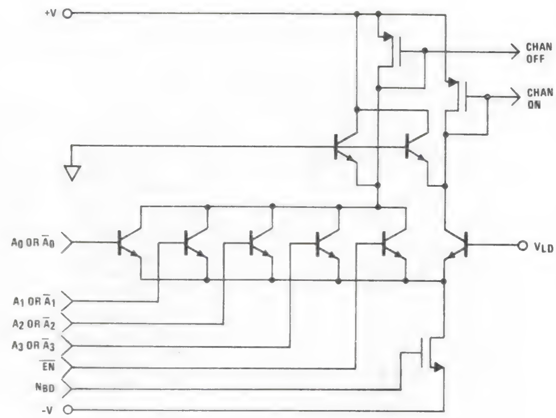
$D_1 = D_2$ = IN4002 or equivalent (per board)

Schematic Diagrams

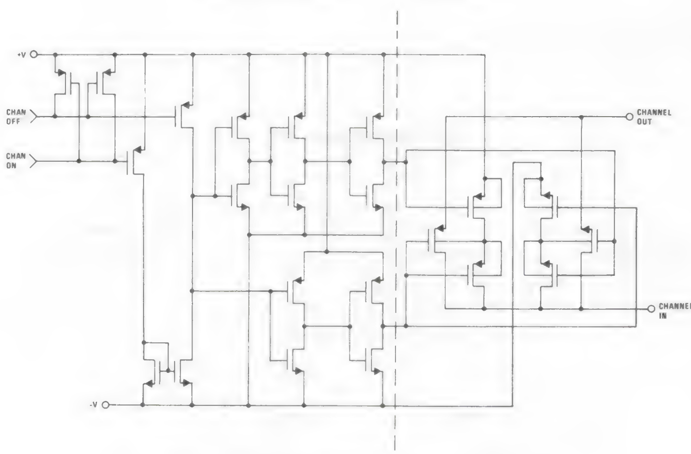
ADDRESS/ENABLE INPUT BUFFER



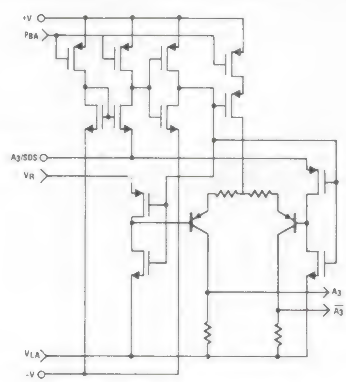
DECODE



LEVEL SHIFTER **SWITCH**

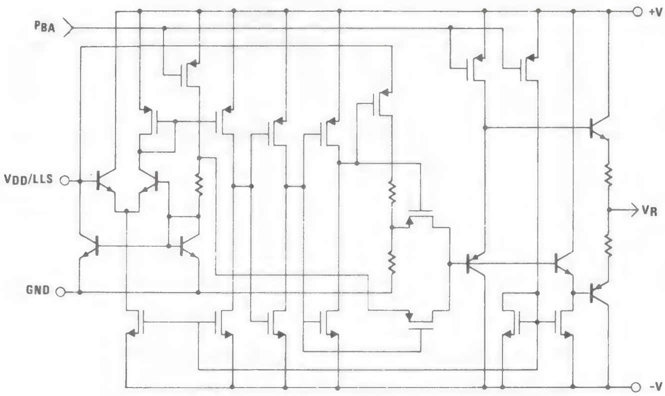


A_3-SINGLE ENDED/DIFFERENTIAL SELECT CIRCUIT

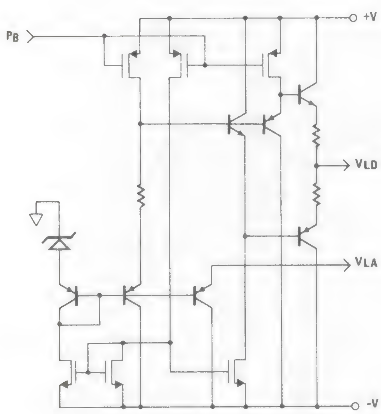


Schematic Diagrams (Continued)

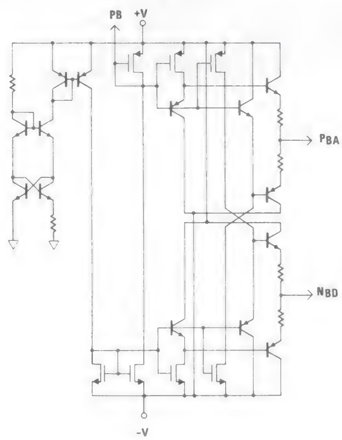
LOGIC LEVEL SELECT CIRCUIT



REFERENCE VOLTAGES



BIAS



Die Characteristics

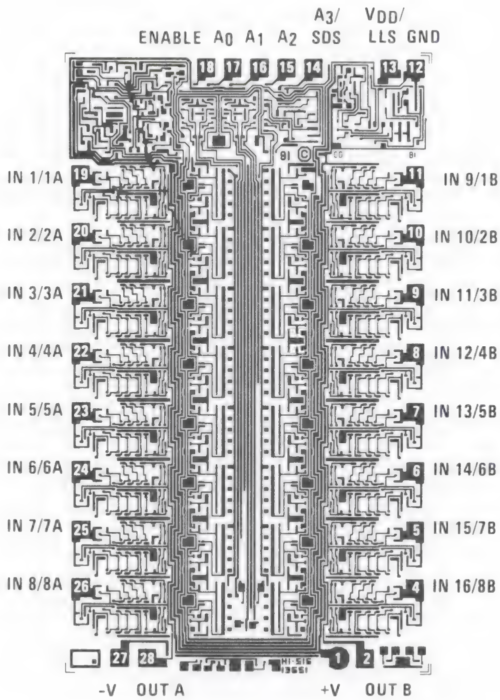
DIE DIMENSIONS: 146 x 89 x 19 mils
METALLIZATION:
Type: Al
Thickness: 16kÅ ± 2kÅ
GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 1kÅ

TRANSISTOR COUNT: 647
PROCESS: CMOS DI
DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY: 2×10^5 A/cm^2 when channel current remains below 8.4mA

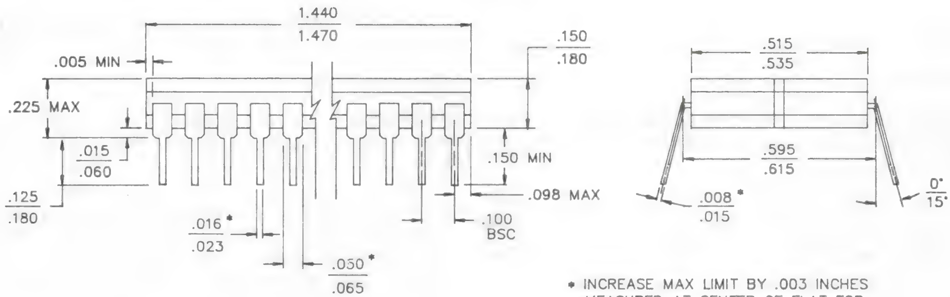
Metallization Mask Layout

HI-516/883



Packaging†

28 PIN CERAMIC DIP

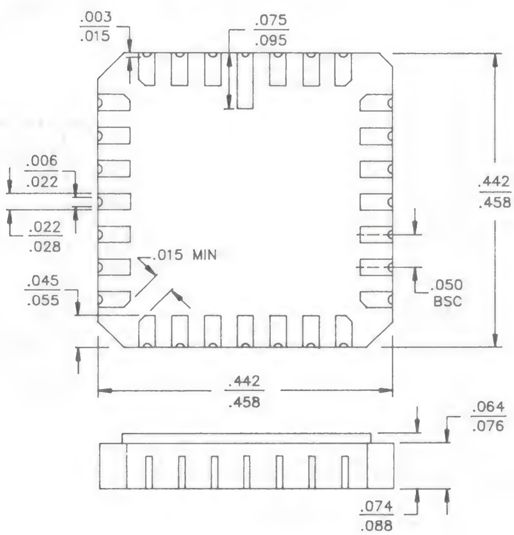


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-10

28 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-4

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

HI-518/883

8 Channel/Differential 4 Channel CMOS High Speed Analog Multiplexer

July 1987

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Access Time (Max. Over Temp.) 225ns**
- **Low Leakage (Max. Over Temp.) .... $I_{D(OFF)}$ 50nA**
- **Low Charge Transfer Error (100pF Load) 25mV**
- **Single Ended to Differential Selectable (SDS)**
- **TTL/CMOS Compatible**

Applications

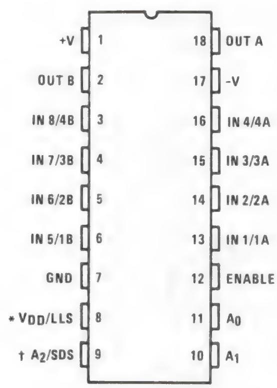
- **Data Acquisition Systems**
- **Telemetry**
- **Industrial Control**

Description

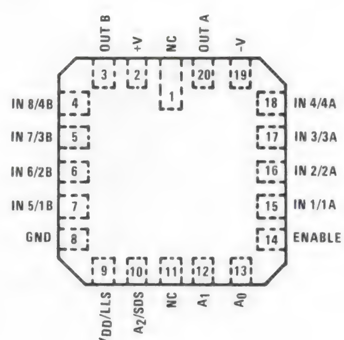
The HI-518/883 is a monolithic dielectrically isolated, high speed, high performance CMOS analog multiplexer. It offers unique built-in channel selection decoding plus an inhibit input for disabling all channels. The dual function of address input A_2 enables the HI-518/883 to be user programmed either as a single ended 8-channel multiplexer by connecting 'OUT A' to 'OUT B' and using A_2 as a digital address input, or as a 4-channel differential multiplexer by connecting A_2 to the $-V_{SUPPLY}$. The substrate leakages and parasitic capacitances are reduced substantially by using the Harris dielectric isolation process to achieve optimum performance in both high and low level signal applications. The low output leakage current ($I_{D(OFF)} < 50nA$ over temperature) of the device makes it an ideal choice for high speed data acquisition systems, precision instrumentation, and industrial process control.

Pinouts

HI1-518/883 (CERAMIC DIP)
TOP VIEW



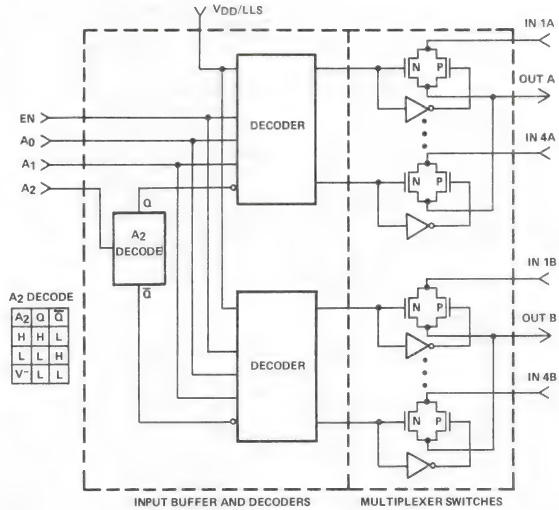
HI4-518/883 (CERAMIC LCC)
TOP VIEW



* LLS = Logic Level Select (TTL Compatible with V_{DD}/LLS Pin = Ground or Open, CMOS Compatible when V_{DD}/LLS Pin = V_{DD})

† SDS = Single Ended/Differential Select (Multiplexer is in Differential Mode when A_2/SDS Pin = $-V_{SUPPLY}$)

Functional Diagram



Truth Tables

HI-518/883 USED AS 8 CHANNEL MULTIPLEXER

USE A_2/SDS AS DIGITAL ADDRESS INPUT				ON CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	None	None
H	L	L	L	1A	None
H	L	L	H	2A	None
H	L	H	L	3A	None
H	L	H	H	4A	None
H	H	L	L	None	1B
H	H	L	H	None	2B
H	H	H	L	None	3B
H	H	H	H	None	4B

HI-518/883 USED AS DIFFERENTIAL 4 CHANNEL MULTIPLEXER

A_2/SDS CONNECTED TO $-V_{SUPPLY}$			ON CHANNEL TO	
ENABLE	A_1	A_0	OUT A	OUT B
L	X	X	None	None
H	L	L	1A	1B
H	L	H	2A	2B
H	H	L	3A	3B
H	H	H	4A	4B

5

CMOS ANALOG MULTIPLEXERS

Absolute Maximum Ratings

Voltage Between Supply Pins 33V
$+V_{SUPPLY}$ to Ground 16.5V
$-V_{SUPPLY}$ to Ground 16.5V
Analog Input Voltage
- $+V_S$ .... $+V_{SUPPLY}$ +2V
- $-V_S$ .... $-V_{SUPPLY}$ -2V

Digital Input Voltage
- TTL Levels Selected (V_{DD}/LLS Pin = GND or Open)
  - $+V_A$ .... +6V
  - $-V_A$ .... -6V
  - A_2/SDS .... $-V_{SUPPLY}$ -2V
  - A_2/SDS .... $+V_{SUPPLY}$ +2V
- CMOS Levels Selected (V_{DD}/LLS Pin = V_{DD})
  - $+V_A$ .... $+V_{SUPPLY}$ +2V
  - $-V_A$ .... -2V

Storage Temperature Range .... -65°C to +150°C

Lead Temperature (Soldering 10 Seconds) .... 275°C
Junction Temperature .... +175°C
Thermal Resistance, Junction-to-Case (θjc)
- Ceramic DIP Package .... 25°C/W
- Ceramic LCC Package .... 21°C/W

Thermal Resistance, Junction-to-Ambient (θja)
- Ceramic DIP Package .... 84°C/W
- Ceramic LCC Package .... 78°C/W

Power Dissipation (at 75°C)
- Ceramic DIP Package 1.19W
- Ceramic LCC Package 1.28W

Power Dissipation Derating Factor (Above +75°C)
- Ceramic DIP Package .... 11.9mW/°C
- Ceramic LCC Package .... 12.8mW/°C

ESD Classification .... ≤2000V

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) .... ±15V
Analog Input Voltage (V_S) .... ±14V
Logic Level Low (V_{AL}) .... 0V to 0.8V
Logic Level High (V_{AH}) .... 2.4V to $+V_{SUPPLY}$
Max RMS Current, S or D 8mA

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 2.4V, V_{DD}/LLS = GND, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current	I_{IH}	Measure Inputs Sequentially, Connect All Unused Inputs to GND	1, 2, 3	+25°C, +125°C -55°C	-1.0	1.0	μA
	I_{IL}	Measure Inputs Sequentially, Connect All Unused Inputs to +5V	1, 2, 3	+25°C, +125°C -55°C	-20	20	μA
Leakage Current Into the Source Terminal of an "OFF" Switch	$+I_{S(OFF)}$	V_S = 10V, V_D = -10V, V_{EN} = 0.8V All Unused Inputs = -10V	1, 2, 3	+25°C, +125°C, -55°C	-50	+50	nA
	$-I_{S(OFF)}$	V_S = -10V, V_D = 10V, V_{EN} = 0.8V All Unused Inputs = +10V	1, 2, 3	+25°C, +125°C, -55°C	-50	+50	nA
Leakage Current Into the Drain Terminal of an "OFF" Switch	$+I_{D(OFF)}$	V_S = -10V, V_D = +10V, V_{EN} = 0.8V All Unused Inputs = -10V	1, 2, 3	+25°C, +125°C, -55°C	-50	+50	nA
	$-I_{D(OFF)}$	V_S = +10V, V_D = -10V, V_{EN} = 0.8V All Unused Inputs = +10V	1, 2, 3	+25°C, +125°C, -55°C	-50	+50	nA
Leakage Current From an "ON" Driver Into the Switch (Drain)	$+I_{D(ON)}$	V_S = V_D = 10V All Unused Inputs = -10V	1, 2, 3	+25°C, +125°C, -55°C	-50	+50	nA
	$-I_{D(ON)}$	V_S = V_D = -10V All Unused Inputs = +10V	1, 2, 3	+25°C, +125°C -55°C	-50	+50	nA
Positive Supply Current	I(+)	V_S = 0V, V_D = Open, V_{EN} = 2.4V Sequence All Address Combinations, Record Highest I+	1, 2, 3	+25°C, +125°C, -55°C	—	+15	mA
Negative Supply Current	I(-)	V_S = 0V, V_D = Open, V_{EN} = 2.4V Sequence All Address Combinations, Record Highest I-	1, 2, 3	+25°C, +125°C, -55°C	—	+15	mA
Standby Positive Supply Current	$+I_{SBY}$	V_A = 0.8V, V_{EN} = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-15	—	mA
Standby Negative Supply Current	$-I_{SBY}$	V_A = 0.8V, V_{EN} = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-15	—	mA
Switch "ON" Resistance	$+R_{DS1}$	V_S = 10V	1	+25°C	—	750	Ω
		I_D = 100μA	2, 3	+125°C, -55°C	—	1000	Ω
	$-R_{DS1}$	V_S = -10V	1	+25°C	—	750	Ω
		I_D = -100μA	2, 3	+125°C, -55°C	—	1000	Ω
Logic Level Voltage	V_{AL} (TTL)	V_{DD}/LLS = GND	1, 2, 3	+25°C, +125°C, -55°C	—	0.8	V
	V_{AH} (TTL)	V_{DD}/LLS = GND	1, 2, 3	+25°C, +125°C -55°C	2.4	—	V
	V_{AL} (CMOS)	V_{DD}/LLS = +15V	1, 2, 3	+25°C, +125°C -55°C	—	4.5	V
	V_{AH} (CMOS)	V_{DD}/LLS = +15V	1, 2, 3	+25°C, +125°C, -55°C	10.5	—	V

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 2.4V, V_{DD}/LLS = GND, Unless Otherwise Specified.

A.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMP	LIMITS MIN	LIMITS MAX	UNITS
Break-Before-Make Time Delay	t_D	$R_L = 800\Omega$, C_L = 12.5pF	9	+25°C	10	—	ns
			10	+125°C	2	—	ns
Propagation Delay Times: Address Inputs to I/O Channel Times	t_A	$R_L = 10M\Omega$, C_L = 12.5pF	9	+25°C	—	175	ns
			10, 11	+125°C, -55°C	—	225	ns
Enable to I/O	$t_{ON(EN)}$	$R_L = 800\Omega$, C_L = 12.5pF	9	+25°C	—	175	ns
			10, 11	+125°C, -55°C	—	225	ns
	$t_{OFF(EN)}$	$R_L = 800\Omega$, C_L = 12.5pF	9	+25°C	—	175	ns
			10, 11	+125°C, -55°C	—	225	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Characterized at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 2.4V, V_{DD}/LLS = GND, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMP	LIMITS MIN	LIMITS MAX	UNITS
Capacitance: Address Input	C_A	V+ = V- = 0V f = 1MHz	1	+25°C	—	5.0	pF
Capacitance: Output Switch	C_{OS}	V+ = V- = 0V f = 1MHz	1	+25°C	—	10	pF
Capacitance: Input Switch	C_{IS}	V+ = V- = 0V f = 1MHz	1	+25°C	—	5.0	pF
Charge Transfer Error	V_{CTE}	V_S = GND, C_L = 100pF V_{GEN} = 0V to 5V	1	+25°C	—	25	mV
Off Channel Isolation	V_{ISO}	V_{EN} = 0.8V, $R_L = 1k\Omega$ C_L = 40pF, $V_S = 3V_{RMS}$ f = 500kHz	1	+25°C	-45	—	dB
Break-Before-Make Time Delay	t_D	$R_L = 800\Omega$, C_L = 12.5pF	1	-55°C	2	—	ns

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1, 2 & 3)
Interim Electrical Parameters (Pre-Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

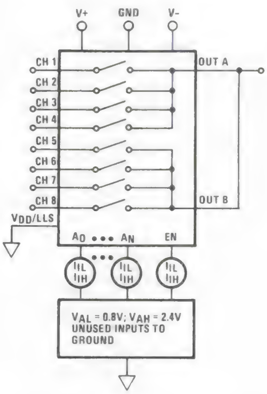
*PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

NOTE 1. The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

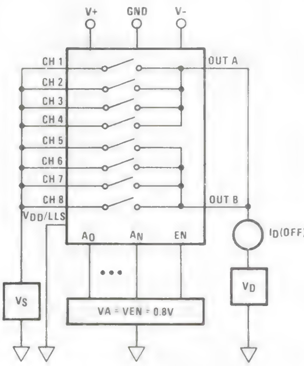
CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Test Circuits

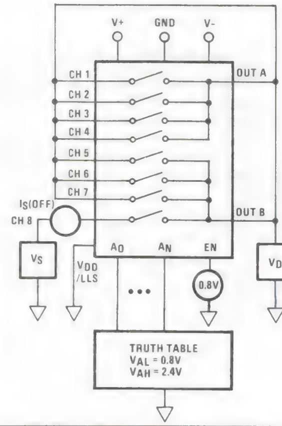
INPUT LEAKAGE CURRENT



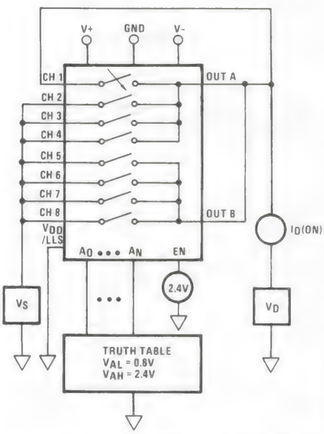
$I_{D(OFF)}$



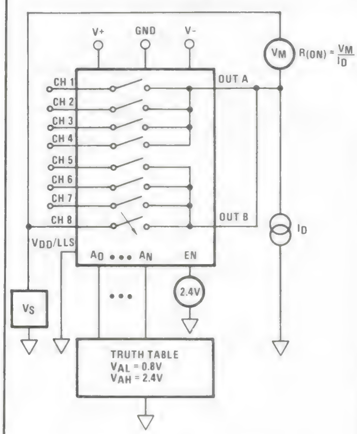
$I_{S(OFF)}$



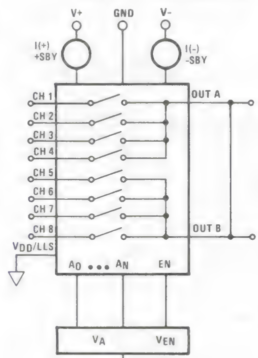
$I_{D(ON)}$



R_{DS}



SUPPLY CURRENTS

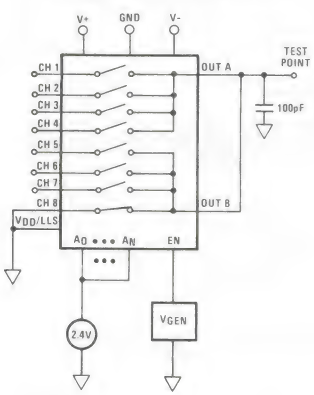


SBY: V_A, V_{EN} = 0.8V

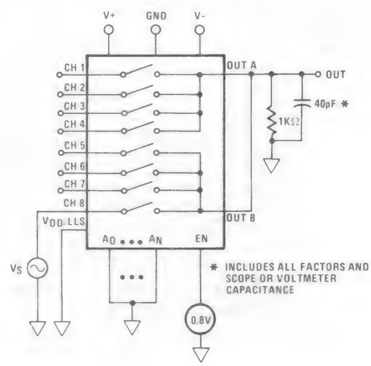
OPERATIONAL: V_{EN} = 2.4V,

V_A = All Combinations are Sequenced

CHARGE TRANSFER ERROR

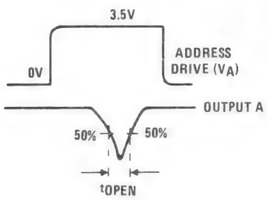


OFF CHANNEL ISOLATION

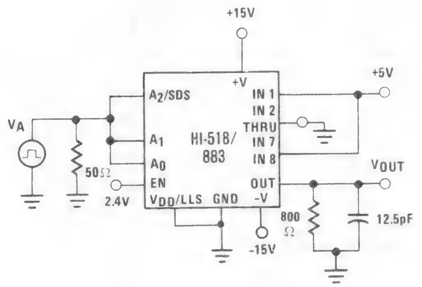


Switching Waveforms

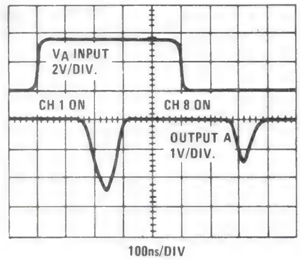
ADDRESS DRIVE



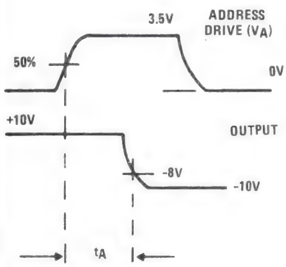
BREAK-BEFORE-MAKE DELAY (t_{OPEN})



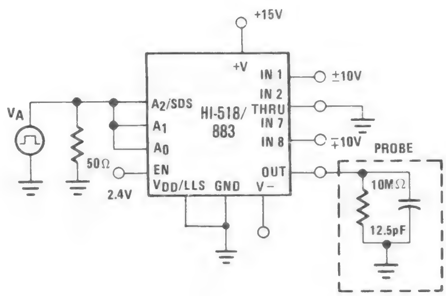
BREAK-BEFORE-MAKE DELAY (t_{OPEN})



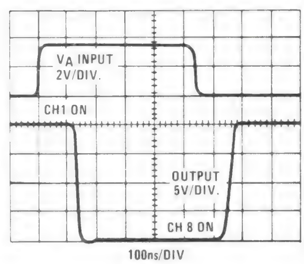
ACCESS TIME



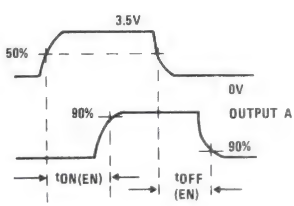
ACCESS TIME



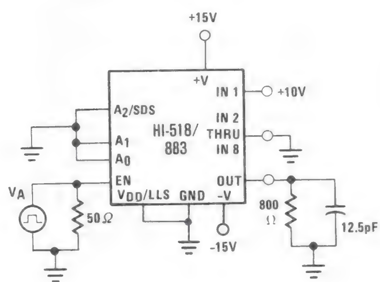
ACCESS TIME



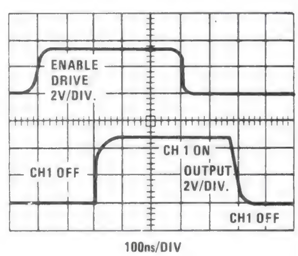
ENABLE DRIVE



ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$

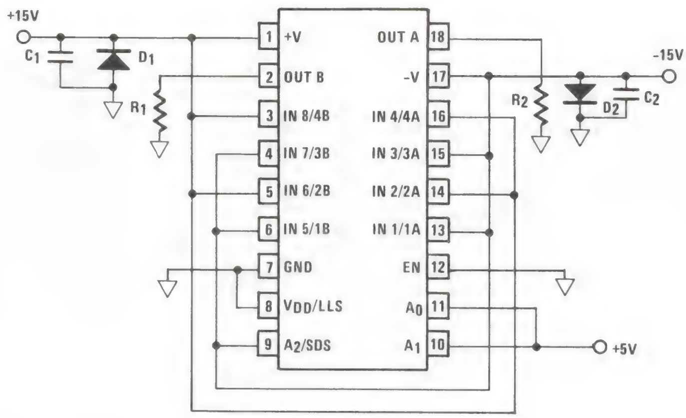


ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$



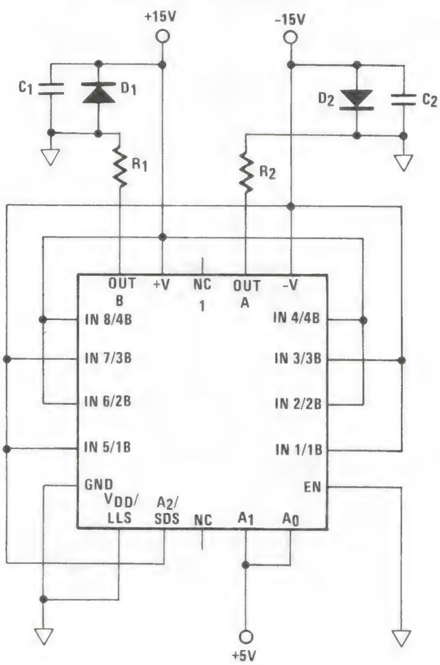
Burn-In Circuits

HI-518/883 CERAMIC DIP



NOTES:
$R_1 = R_2 = 10k\Omega$, ±5%, 1/4 or 1/2W
$C_1 = C_2 = 0.01\mu F$ (one per socket) or $0.1\mu F$ (one per row)
$D_1 = D_2$ = IN4002 or equivalent (per board)

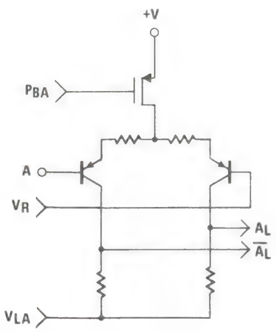
HI-518/883 CERAMIC LCC



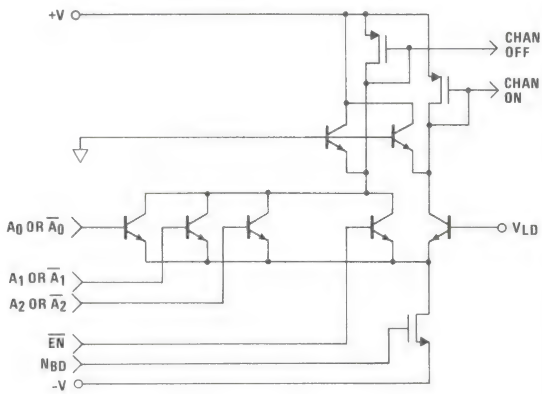
NOTES:
$R_1 = R_2 = 10k\Omega$, ±5%, 1/2 or 1/4W (per socket)
$C_1 = C_2 = 0.01\mu F$ (one per socket) or $0.1\mu F$ (one per row)
$D_1 = D_2$ = IN4002 or equivalent (per board)

Schematic Diagrams

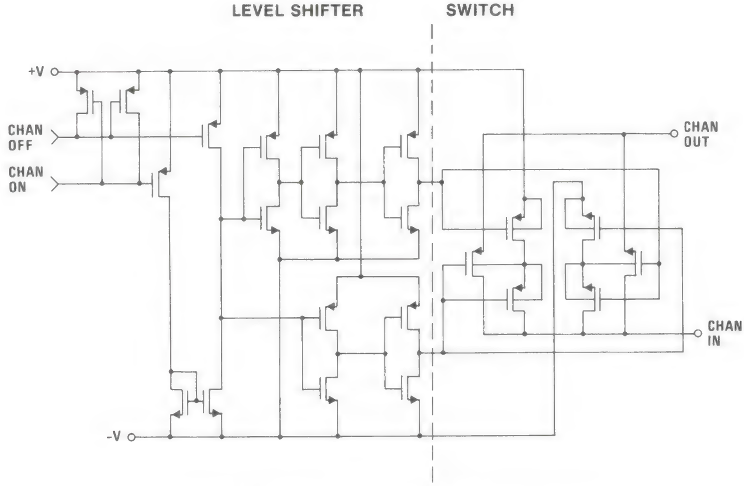
ADDRESS/ENABLE INPUT BUFFER



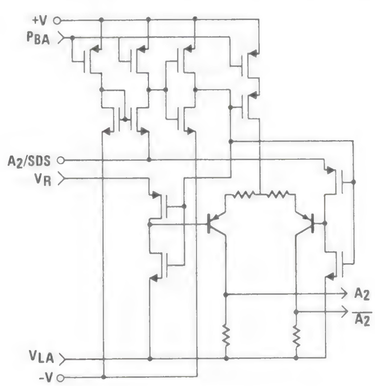
DECODE



LEVEL SHIFTER SWITCH

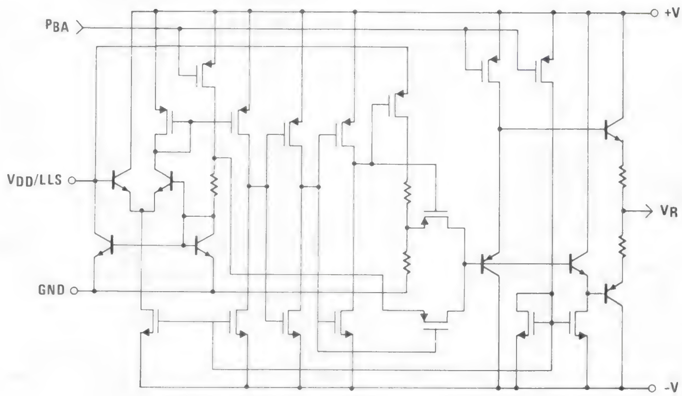


A_2-SINGLE ENDED/DIFFERENTIAL SELECT CIRCUIT

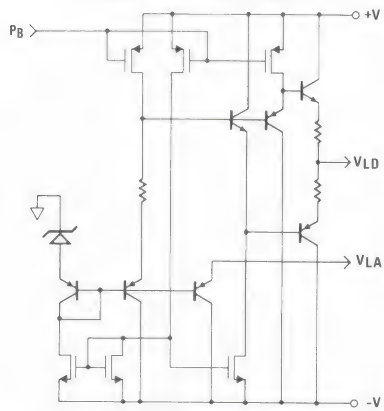


Schematic Diagrams (Continued)

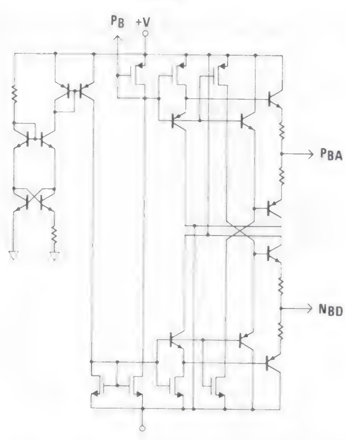
LOGIC LEVEL SELECT CIRCUIT



REFERENCE VOLTAGES



BIAS



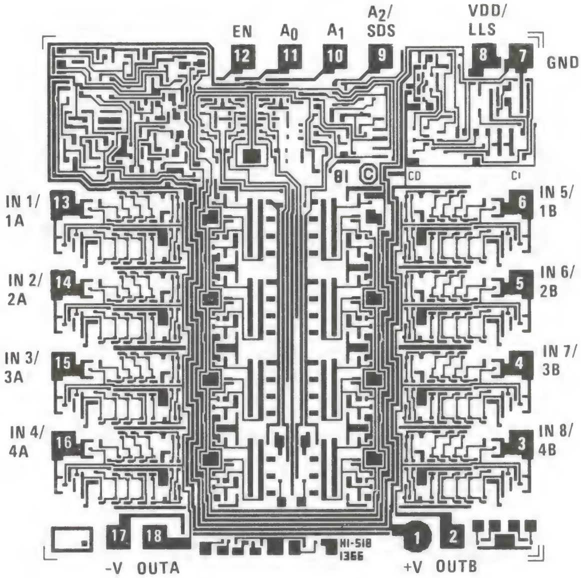
Die Characteristics

DIE DIMENSIONS: 89 x 93 x 19 mils
METALLIZATION:
Type: Al
Thickness: 16kÅ ± 2kÅ
GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 1.0kÅ
WORST CASE CURRENT DENSITY: 2 x 10^5A/cm^2

TRANSISTOR COUNT:
HI-518/883 356
PROCESS: CMOS DI
DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP - 460^o (Max)
Ceramic LCC - 420^o (Max)

Metallization Mask Layout

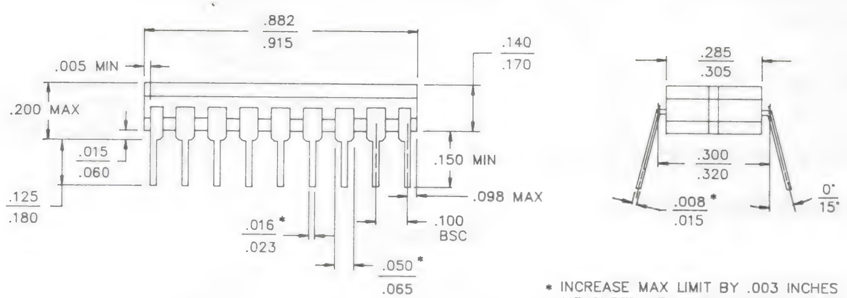
HI-518/883



NOTE: Pad Numbers Correspond to DIP Pin Numbers Only.

Packaging†

18 PIN CERAMIC DIP

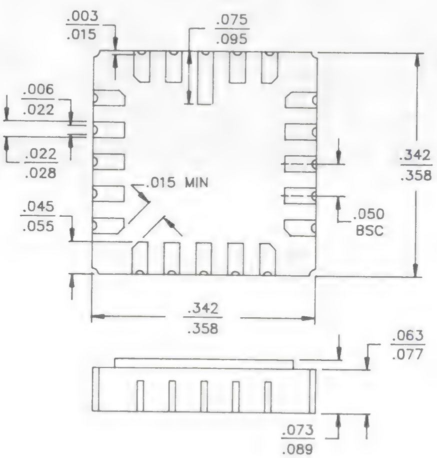


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ±10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-6

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ±10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$ Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

HI-524/883

4 Channel Wideband Multiplexer

August 1988

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Crosstalk (7.0MHz) .... <-56dB
- Fast access Time (Max. Over Temp.) 500ns
- TTL Compatible

Applications

- Wideband Switching
- Radar
- TV Video
- ECM

Description

The HI-524/883 is a four channel CMOS analog multiplexer designed to process single-ended signals with bandwidths up to 6.8MHz. The chip includes a 1 of 4 decoder for channel selection and an Enable input to inhibit all channels (chip select).

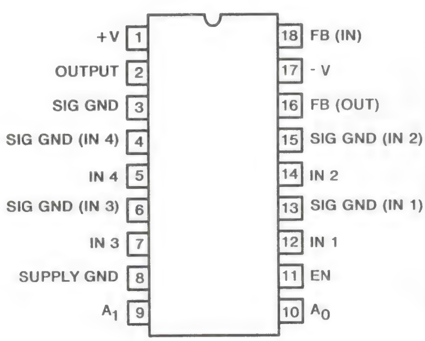
Three CMOS transmission gates are used in each channel, as compared to the single gate in more conventional CMOS multiplexers. This provides a double barrier to the unwanted coupling of signals from each input to the output. In addition, Dielectric Isolation (DI) processing helps to insure that Crosstalk is less than -56dB at 7MHz.

The HI-524/883 is designed to operate into a wideband buffer amplifer such as the Harris HA-2541/883. The multiplexer chip includes two "on" switches in series, for use as a feedback element with the amplifier. This feedback resistance matches and tracks the channel R_{ON} resistance, to minimize the amplifier V_{OS} and its variation with temperature.

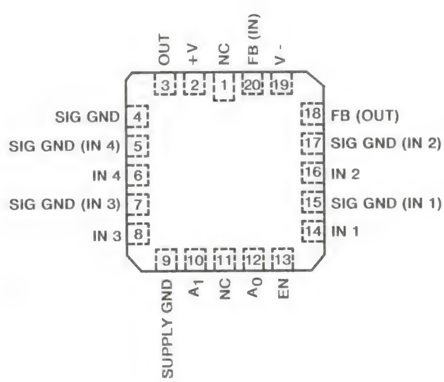
The HI-524/883 is well suited to the rapid switching of video and other wideband singals in telemetry, instrumentation, radar and video systems. It is packaged in an 18 pin Ceramic DIP or 20 pad LCC and operates on ±15V supplies.

Pinouts

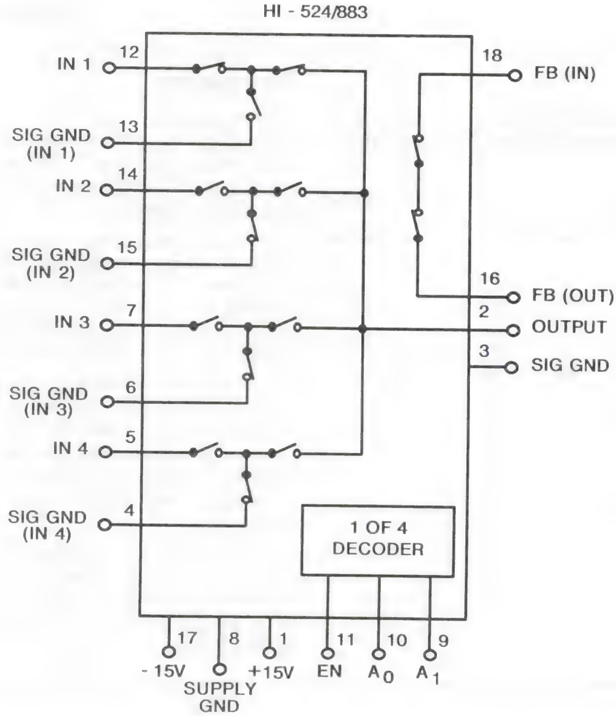
HI1-524/883 (CERAMIC DIP)
TOP VIEW



HI4-524/883 (CERAMIC LCC)
TOP VIEW



Functional Diagram



TRUTH TABLE

A1	A0	EN	ON CHANNEL
X	X	L	NONE
L	L	H	1*
L	H	H	2
H	L	H	3
H	H	H	4

*CHANNEL 1 IS SHOWN SELECTED IN THE DIAGRAM

NOTE: Pin Numbers Refer to DIP Package Only.

Absolute Maximum Ratings

Voltage Between Supply Pins 33V
$+V_{SUPPLY}$ to Ground .... +16.5V
$-V_{SUPPLY}$ to Ground .... -16.5V
Analog Input Voltage
$+V_S$ .... $+V_{SUPPLY}$ +2V
$-V_S$ .... $-V_{SUPPLY}$ -2V
Digital Input Voltage
$+V_{EN}$, $+V_A$ .... +6V
$-V_{EN}$, $-V_A$ .... -6V
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering 10 Seconds) .... +275°C
Junction Temperature .... +175°C

Thermal Information

Thermal Resistance, Junction-to-Case (θ_{jc})
Ceramic DIP Package .... 22°C/W
Ceramic LCC Package .... 19°C/W
Thermal Resistance, Junction-to-Ambient (θ_{ja})
Ceramic DIP Package .... 81°C/W
Ceramic LCC Package .... 76°C/W
Power Dissipation (at +75°C)
Ceramic DIP Package 1.23W
Ceramic LCC Package 1.32W
Power Dissipation Derating Factor (Above +75°C)
Ceramic DIP Package .... 12.3mW/°C
Ceramic LCC Package .... 13.2mW/°C
ESD Classification .... ≤2000V

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) .... ±15V
Analog Input Voltage (V_S) .... ±10V
Logic Level Low (V_{AL}) .... 0V to 0.8V
Logic Level High (V_{AH}) .... 2.4V to $+V_{SUPPLY}$
Max RMS Current, S or D 8mA

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V , V_{EN} = 2.4V, V_{AH} = 2.4V, V_{AL} = +0.8V, Unless Otherwise Specified

D.C.PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current	I_{IH}	Measure Inputs Sequentially, Connect all Unused Inputs to GND	1, 2, 3	+25°C, +125°C, -55°C	-1.0	1.0	µA
	I_{IL}	Measure Inputs Sequentially, Connect All Unused Inputs to +5V	1, 2, 3	+25°C, +125°C, -55°C	-20	20	µA
Leakage Current Into the Source Terminal of an "OFF" Switch	$+I_{S(OFF)}$	V_S = 10V, V_D = -10V, V_{EN} = 0.8V All Unused Inputs = -10V	1, 2, 3	+25°C, +125°C, -55°C	-50	+50	nA
	$-I_{S(OFF)}$	V_S = -10V, V_D = 10V, V_{EN} = 0.8V All Unused Inputs = +10V	1, 2, 3	+25°C, +125°C, -55°C	-50	+50	nA
Leakage Current Into the Drain Terminal of an "OFF" Switch	$+I_{D(OFF)}$	V_S = -10V, V_D = +10V, V_{EN} = 0.8V All Unused Inputs = -10V	1, 2, 3	+25°C, +125°C, -55°C	-50	+50	nA
	$-I_{D(OFF)}$	V_S = +10V, V_D = -10V, V_{EN} = 0.8V All Unused Inputs = +10V	1, 2, 3	+25°C, +125°C, -55°C	-50	+50	nA
Leakage Current From an "ON" Driver Into the Switch (Drain)	$+I_{D(ON)}$	V_S = V_D = 10V All Unused Inputs = -10V	1, 2, 3	+25°C, +125°C, -55°C	-50	+50	nA
	$-I_{D(ON)}$	V_S = V_D = -10V All Unused Inputs = +10V	1, 2, 3	+25°C, +125°C, -55°C	-50	+50	nA
Positive Supply Current	I(+)	V_S = 0V, V_D = Open, V_{EN} = 2.4V Sequence All Address Combinations, Record Highest I (+)	1, 2, 3	+25°C, +125°C, -55°C	-	25	mA
Negative Supply Current	I(-)	V_S = 0V, V_D = Open, V_{EN} = 2.4V Sequence All Address Combinations, Record Highest I (-)	1, 2, 3	+25°C, +125°C, -55°C	-23	-	mA
Standby Positive Supply Current	$+I_{SBY}$	V_A = 0.8V, V_{EN} = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	25	mA
Standby Negative Supply Current	$-I_{SBY}$	V_A = 0.8V, V_{EN} = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-23	-	mA
Switch "ON" Resistance	R_{DS}	V_S = 0V I_D = ±100µA	1, 2, 3	+25°C, +125°C, -55°C	-	1500	Ω
Digital Input Threshold Characteristics	V_{AL}		1, 2, 3	+25°C +125°C, -55°C	-	0.8	V
	V_{AH}		1, 2, 3	+25°C +125°C, -55°C	2.4	-	V

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PEFORMANCE CHARACTERISTICS

Devices Tested at $+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$, $V_{EN} = 2.4V$, $V_{AH} = 2.4$, $V_{AL} = 0.8V$, Unless Otherwise Specified.

A.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMP	LIMITS		UNITS
					MIN	MAX	
Break-Before-Make Time Delay	t_D	$R_L = 500\Omega$, $C_L = 12.5pF$	9	+25°C	10	-	ns
			10	+125°C	2	-	ns
Propagation Delay Times: Address Inputs to I/O Channel Times	t_A	$R_L = 10M\Omega$, $C_L = 12.5pF$	9	+25°C	-	300	ns
			10,11	+125°C, -55°C	-	500	ns
Enable to I/O	$t_{ON(EN)}$	$R_L = 500\Omega$, $C_L = 12.5pF$	9	+25°C	-	300	ns
			10, 11	+125°C, -55°C	-	500	ns
	$t_{OFF\ (EN)}$	$R_L = 500\Omega$, $C_L = 12.5pF$	9	+25°C	-	250	ns
			10, 11	+125°C, -55°C	-	500	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at $+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$, $V_{EN} = 2.4V$, $V_{AH} = 2.4$, $V_{AL} = 0.8V$, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMP	LIMITS		UNITS
					MIN	MAX	
Capacitance: Address Input	C_A	V+ = V- = 0V, f = 1MHz	1	+25°C	-	7	pF
Capacitance: Output Switch	C_{OS}	V+ = V- = 0V, f = 1MHz	1	+25°C	-	10	pF
Capacitance: Input Switch	C_{IS}	V+ = V- = 0V, f = 1MHz	1	+25°C	-	6	pF
Bandwidth (-3dB)	BW	$V_S = 3Vp\text{-}p$	1	+25°C	6.8	-	MHz
Crosstalk	C_t	$V_S = 7MHz$, 3Vp-p	1	+25°C	-56	-	dB
Break-Before-Make Time Delay	t_D	$R_L = 500\Omega$, $C_L = 12.5pF$	1	-55°C	2	-	ns

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1, 2, & 3)
Interim Electrical Parameters (Pre-Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

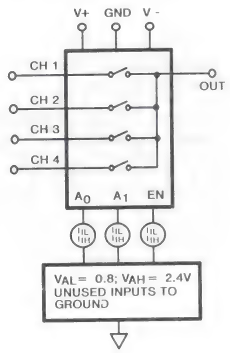
*PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

NOTE: 1. The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon intial design release and upon design changes which would affect these characteristics.

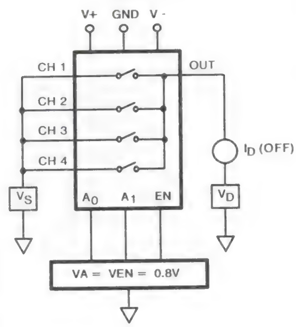
CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Test Circuits

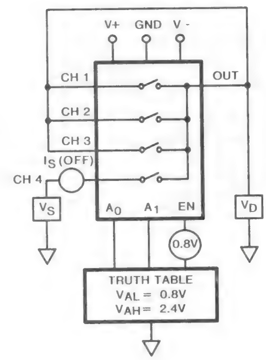
INPUT LEAKAGE CURRENT



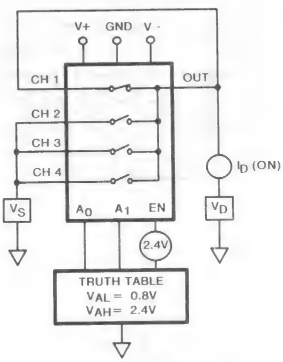
$I_{D(OFF)}$



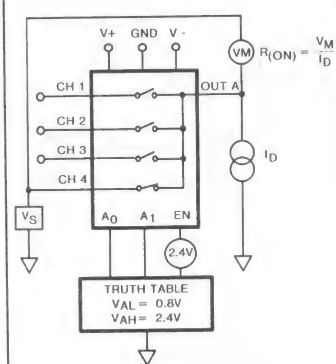
$I_{S(OFF)}$



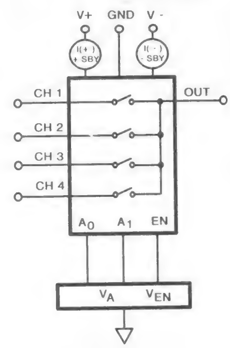
$I_{D(ON)}$



R_{DS}

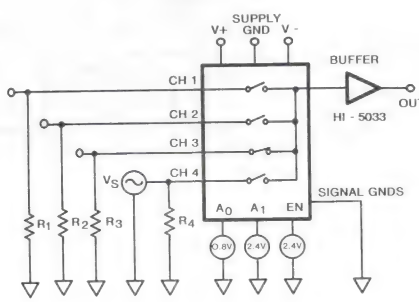


SUPPLY CURRENTS



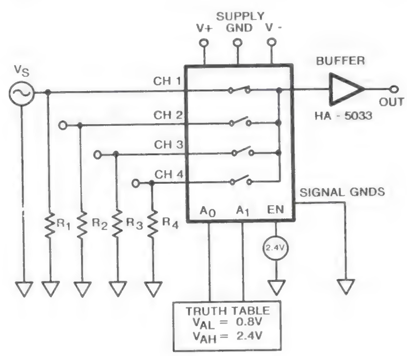
SBY: V_A = 0.8V, V_{EN} = 0.8V
OPERATIONAL: V_{EN} = 2.4V, V_A = All Combinations are Sequenced

CROSSTALK



NOTE: R_1 thru R_4 = 75Ω
Worst Case is Channel Selected with Input On Channel 4

BANDWIDTH

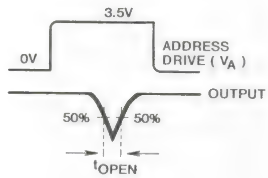


NOTES: R_1 thru R_4 = 75Ω
V_S Applied to Each Channel Separately, Worst Case is Recorded

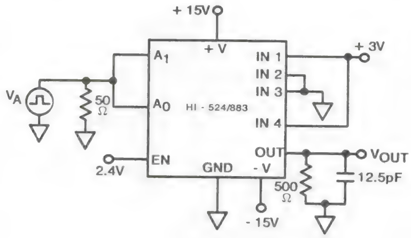
5
CMOS ANALOG MULTIPLEXERS

Switching Waveforms

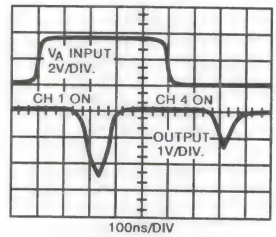
ADDRESS DRIVE



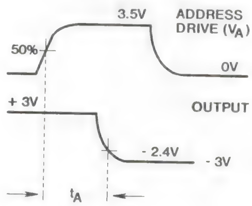
BREAK-BEFORE-MAKE DELAY (t_{OPEN})



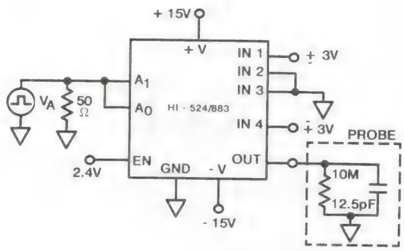
BREAK-BEFORE-MAKE DELAY (t_{OPEN})



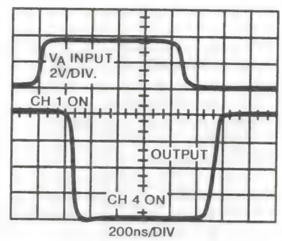
ADDRESS DRIVE



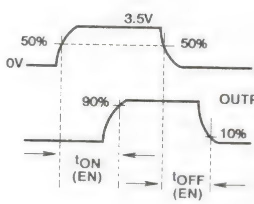
ACCESS TIME



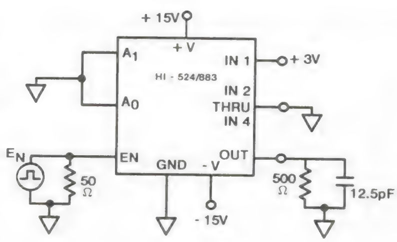
ACCESS TIME



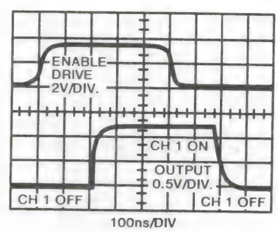
ENABLE DRIVE



ENABLE DELAY
$t_{ON(EN)}$, $t_{OFF\ (EN)}$

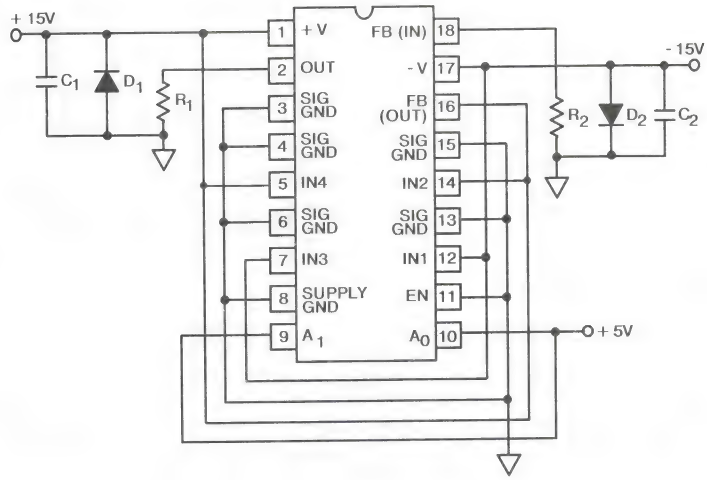


ENABLE DELAY
$t_{ON(EN)}$, $t_{OFF\ (EN)}$

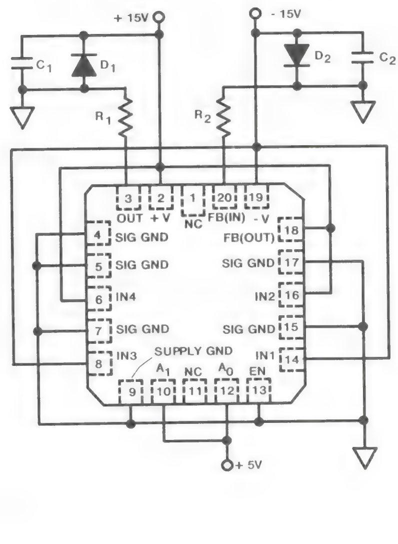


Burn-In Circuits

HA-524/883 CERAMIC DIP



HA-524/883 CERAMIC LCC



NOTES:

R_1 = 10kΩ, ±5%, 1/4 or1/2W (Per Socket)

R_2 = 10kΩ, ±5%, 1/4 or 1/2W (Per Socket)

C_1 = 0.01μF/Socket or 0.1μF/Row, (min.)

C_2 = 0.01μF/Socket or 0.1μF/Row, (min.)

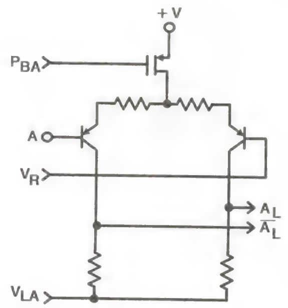
D_1 = D_2 = 1N4002 or Equivalent/Board

5

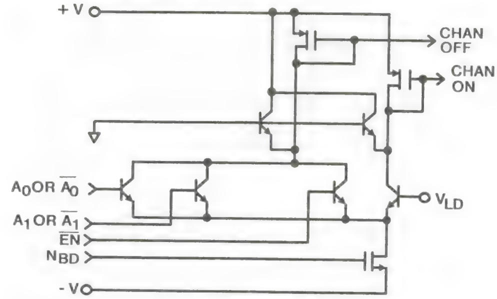
CMOS ANALOG MULTIPLEXERS

Schematic Diagrams

ADDRESS/ENABLE INPUT BUFFER

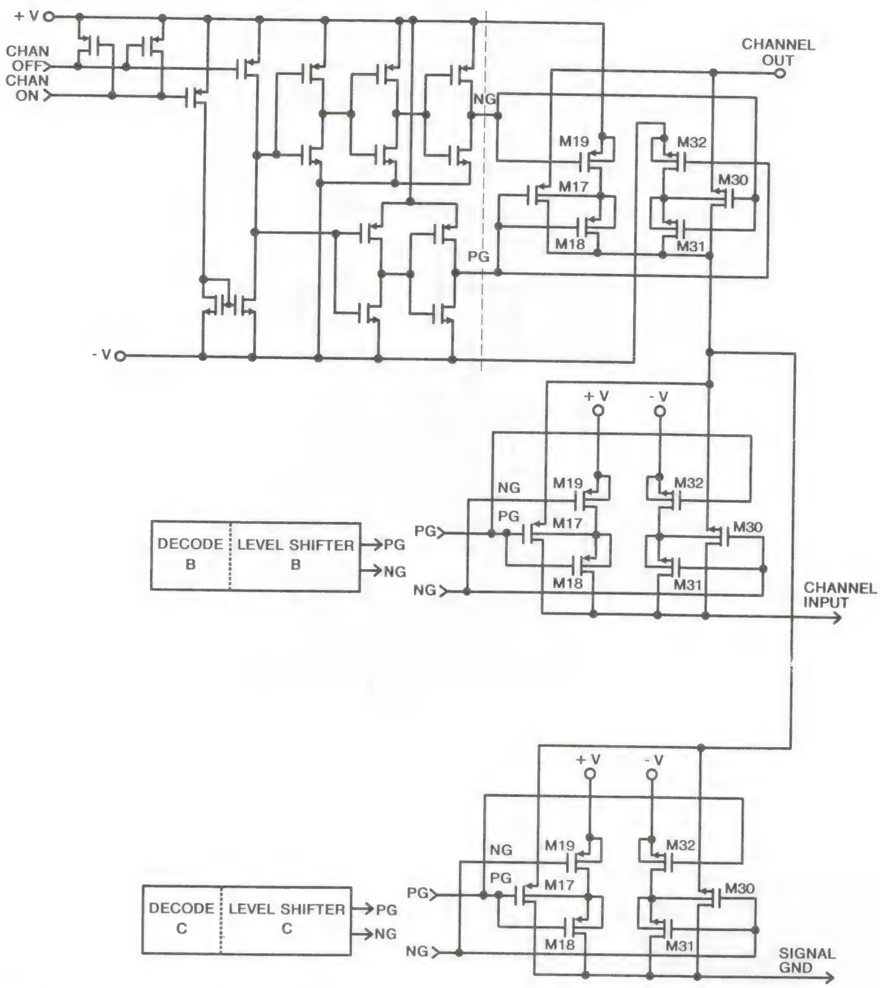


A-DECODE



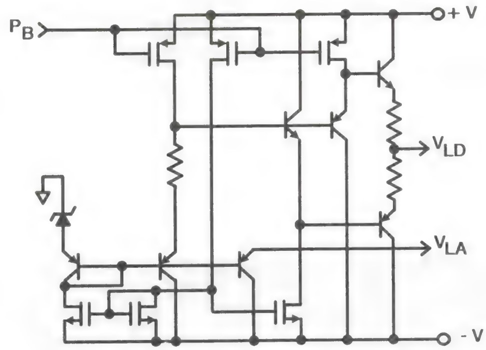
A-LEVEL SHIFTER

A-SWITCH CELL

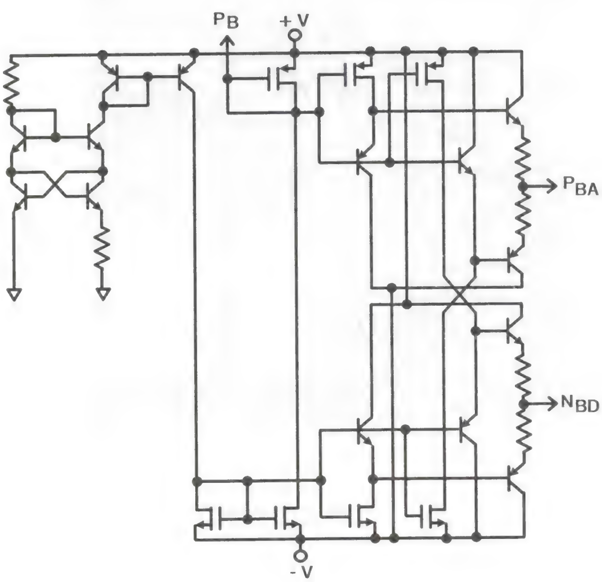


Schematic Diagrams (Continued)

REFERENCE VOLTAGES



BIAS



Die Characteristics

DIE DIMENSIONS:
146 x 89 x 19 mils
(3710 x 2260 x 483 μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$2 \times 10^5 A/cm^2$

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

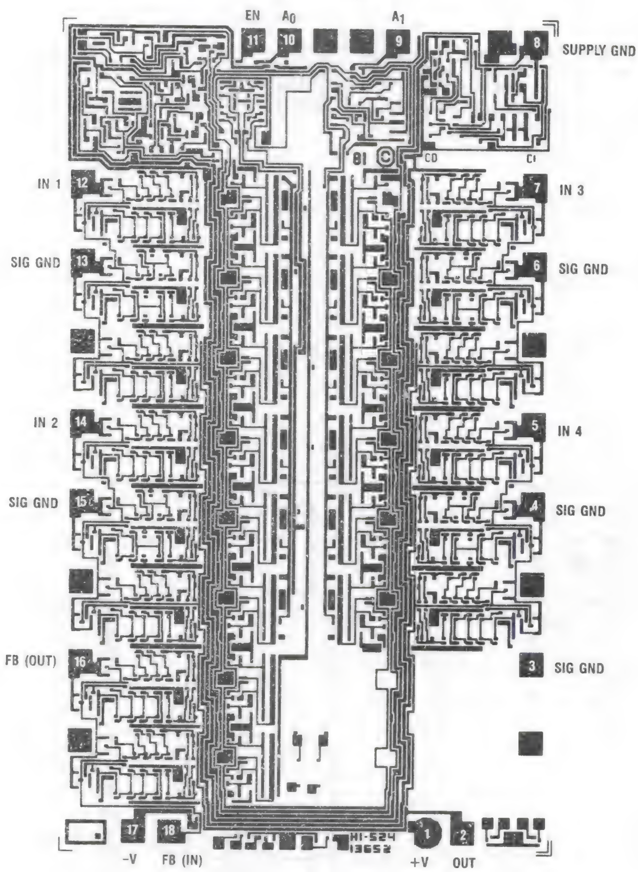
TRANSISTOR COUNT: 599

PROCESS: CMOS-DI

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

Metallization Mask Layout

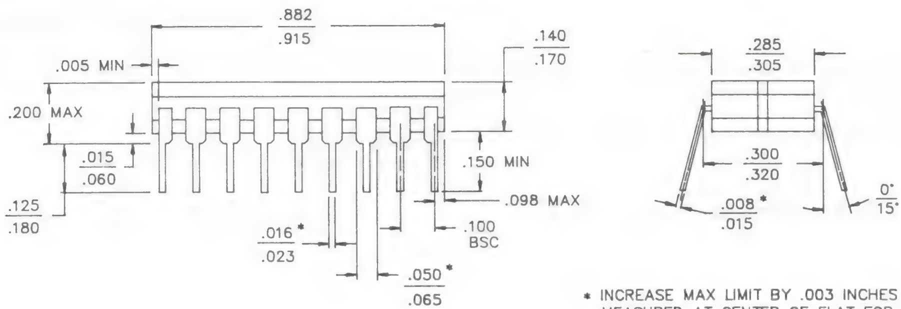
HI-524/883



NOTE: Pin Numbers Correspond to DIP Package Only.

Packaging†

18 PIN CERAMIC DIP

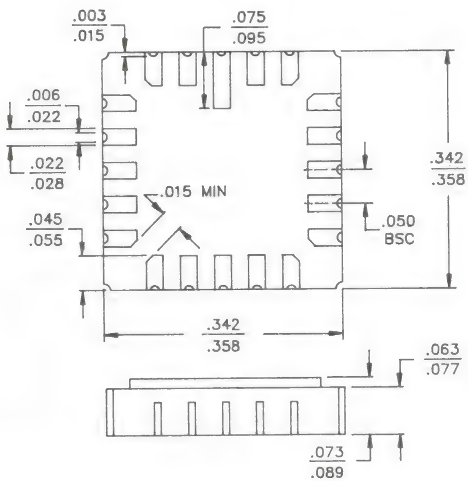


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-6

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

DESIGN INFORMATION

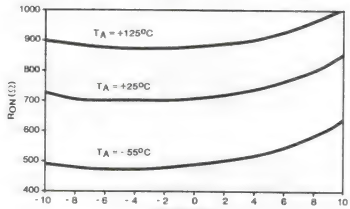
4 Channel Wideband Multiplexer

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

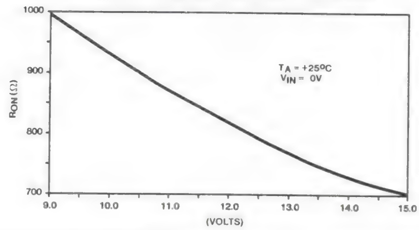
Typical Performance Characteristics

Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = +2.4V$, $V_{AL} = 0.8V$, Pin Numbers Refer to DIP.

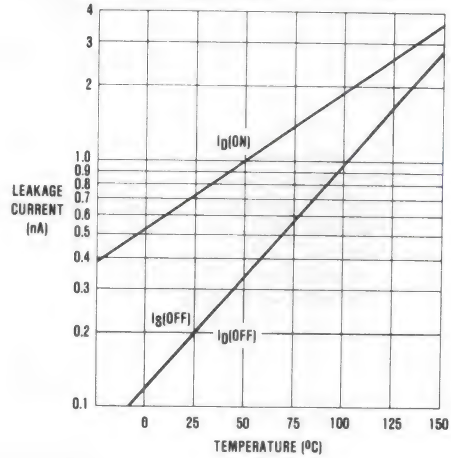
ON RESISTANCE vs. ANALOG INPUT VOLTAGE, TEMPERATURE



ON RESISTANCE vs. SUPPLY VOLTAGE

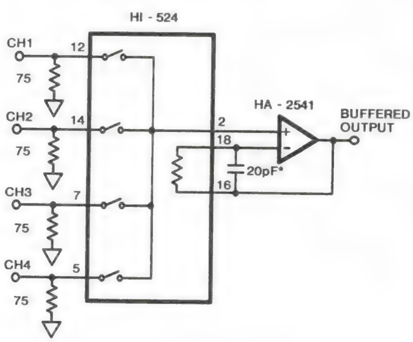


LEAKAGE CURRENT vs. TEMPERATURE



Applications

Often it is desirable to buffer the HI-524 output, to avoid loading errors due to the channel "ON" resistance:



*Capacitor value may be selected to optimize AC performance.

The buffer amplifier should offer sufficient bandwidth and slew rate to avoid degradation of the anticipated signals. For video switching, the HA-5033 and HA-2542 offer good performance plus ± 100mA output current for driving coaxial cables. For general wideband applications, the HA-2541 offers the convenience of unity gain stability plus 90ns settling (to ±0.1%) and ±10V output swing. Also, the HI-524 includes a feedback resistance for use with the HA-2541. This resistance matches and tracks the channel "ON" resistance, to minimize offset voltage due to the buffer's bias currents.

Note that the on-chip feedback element between pins 16 and 18 includes two switches in series, to simulate a channel resistance. These swiches open for V_{EN} = Low. This allows two or more HI-524's to operate into one HA-2541, with their feedback elements connected in parallel. Thus, only the selected multiplexer provides feedback and the amplifier remains stable.

All HI-524 package pins labeled 'SIG GND' (pins 3, 4, 6, 13, 15) should be externally connected to signal ground for best crosstalk performance.

Bypass capacitors (0.1 to 1.0μF) are recommended from each HI-524 supply pin to power ground (pins 1 and 17 to pin 8). Locate the buffer amplifier near the HI-524 so the two capacitors may bypass both devices.

If an analog input 1V or greater is present when supplies are off, a low resistance is seen from that input to a supply line. (For example, the resistance is approximately 160Ω for an input of -3V.) Current flow may be blocked by a diode in each supply line, or limited by a resistor in series with each channel. The best solution, of course, is to arrange that no digital or analog inputs are present when the power supplies are off.

HARRIS

HI-546/883
HI-547/883

Single 16/Differential 8 Channel CMOS Analog Multiplexers With Active Overvoltage Protection

January 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- No Channel Interaction During Overvoltage
- Guaranteed R_{ON} Matching
- 44V Maximum Power Supply
- Break-Before-Make Switching
- Analog Signal Range .... ±15V
- Access Time (Max.) 1.0μs
- Power Dissipation (Max.) 45mW

Applications

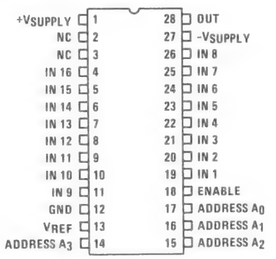
- Data Acquisition Systems
- Control Systems
- Telemetry

Description

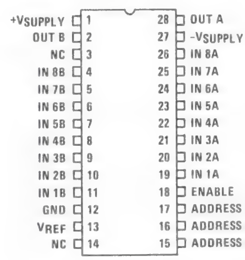
The HI-546/883 and HI-547/883 are analog multiplexers with Active Overvoltage Protection and guaranteed R_{ON} matching. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant 70 volt peak-to-peak levels with ±15V supplies and digital inputs will sustain continuous faults up to 4 volts greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur; each input presents 1kΩ of resistance under this condition. These features make the HI-546/883 and HI-547/883 ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. Both devices are fabricated with 44 volt dielectrically isolated CMOS technology. The HI-546/883 is a 16 channel device and the HI-547/883 is an 8 channel differential version. If input overvoltage protection is not needed, the HI-506/883 and HI-507/883 multiplexers are recommended. For further information see Application Notes 520 and 521.

Pinouts

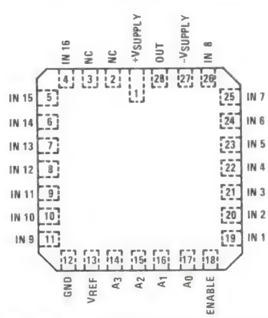
HI1-546/883 (CERAMIC DIP)
TOP VIEW



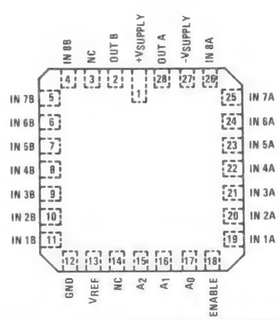
HI1-547/883 (CERAMIC DIP)
TOP VIEW



HI4-546/883 (CERAMIC LCC)
TOP VIEW

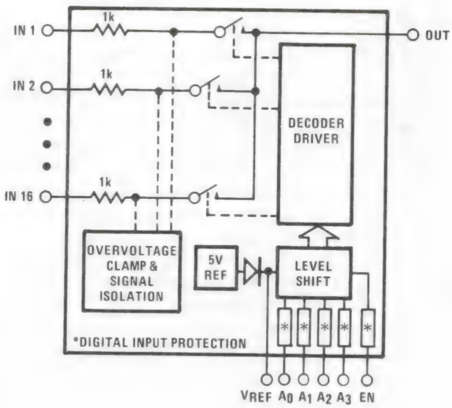


HI4-547/883 (CERAMIC LCC)
TOP VIEW



Functional Diagrams

HI-546/883

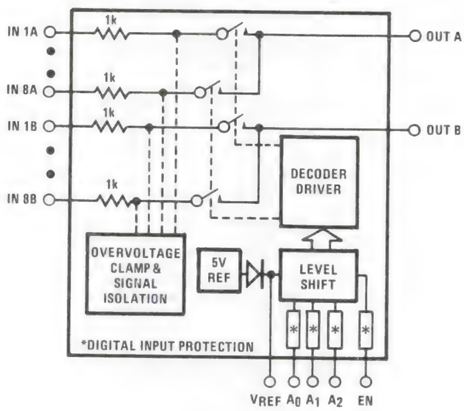


TRUTH TABLES

HI-546/883

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	None
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-547/883



HI-547/883

A_2	A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

Absolute Maximum Ratings

Voltage Between Supply Pins 44V
$+V_{SUPPLY}$ to Ground 22V
$-V_{SUPPLY}$ to Ground 25V
Analog Input Voltage
  $+V_S$ .... $+V_{SUPPLY}$ +20V
  $-V_S$ .... $-V_{SUPPLY}$ -20V
Digital Input Voltage
  $+V_{EN}$, $+V_A$ .... $+V_{SUPPLY}$ +4V
  $-V_{EN}$, $-V_A$ .... $-V_{SUPPLY}$ -4V
  or 20mA, whichever occurs first.
Continuous Current, S or D 20mA
Peak Current, S or D
  (Pulsed at 1ms, 10% Duty Cycle Max.) 40mA
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering 10 Seconds) .... 275°C

Junction Temperature .... +175°C
Thermal Resistance, Junction-to-Case (θjc)
  Ceramic DIP Package .... 18°C/W
  Ceramic LCC Package .... 40°C/W
Thermal Resistance, Junction-to-Ambient (θja)
  Ceramic DIP Package .... 50°C/W
  Ceramic LCC Package .... 81°C/W
Power Dissipation
  Ceramic DIP Package 2.0W
  Ceramic LCC Package 1.23W
Power Dissipation Derating Factor (Above +75°C)
  Ceramic DIP Package .... 20.0mW/°C
  Ceramic LCC Package .... 12.3mW/°C
ESD Classification .... ≤2000V

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) .... ±15V
Analog Input Voltage (V_S) .... $\pm V_{SUPPLY}$

Logic Low Level (V_{AL}) .... 0V to 0.8V
Logic High Level (V_{AH}) .... +4V to $+V_{SUPPLY}$
Max RMS Current, S or D 8mA

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 4.0V, V_{REF} (Pin 13) = OPEN, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current	I_{IH}	Measure Inputs Sequentially,	1, 2, 3	+25°C, +125°C, -55°C	-1.0	1.0	μA
	I_{IL}	Connect All Unused Inputs to GND	1, 2, 3	+25°C, +125°C, -55°C	-1.0	1.0	μA
Leakage Current Into the Source Terminal of an "OFF" Switch	$+I_{S(OFF)}$	V_S = +10V, V_D = -10V, V_{EN} = 0.8V	1	+25°C	-10	+10	nA
		All Unused Inputs = -10V	2, 3	+125°C, -55°C	-50	+50	nA
	$-I_{S(OFF)}$	V_S = -10V, V_D = +10V, V_{EN} = 0.8V	1	+25°C	-10	+10	nA
		All Unused Inputs = +10V	2, 3	+125°C, -55°C	-50	+50	nA
Leakage Current Into the Drain Terminal of an "OFF" Switch	$+I_{D(OFF)}$	V_D = +10V, V_{EN} = 0.8V	1	+25°C	-10	+10	nA
		All Unused Inputs = -10V HI-546/883	2, 3	+125°C, -55°C	-300	+300	nA
		HI-547/883	2, 3	+25°C, -55°C	-200	+200	nA
	$-I_{D(OFF)}$	V_D = -10V, V_{EN} = 0.8V	1	+25°C	-10	+10	nA
		All Unused Inputs = +10V HI-546/883	2, 3	+25°C, -55°C	-300	+300	nA
		HI-547/883	2, 3	+125°C, -55°C	-200	+200	nA
Leakage Current From an "ON" Driver Into the Switch (Drain)	$+I_{D(ON)}$	V_{IN} (Selected Chan.) = V_D = +10V	1	+25°C	-10	+10	nA
		V_S = Unused Inputs = -10V HI-546/883	2, 3	+125°C, -55°C	-300	+300	nA
		HI-547/883	2, 3	+125°C, -55°C	-200	+200	nA
	$-I_{D(ON)}$	V_{IN} (Selected Chan.) = V_D = -10V	1	+25°C	-10	+10	nA
		V_S = Unused Inputs = +10V HI-546/883	2, 3	+125°C, -55°C	-300	+300	nA
		HI-547/883	2, 3	+125°C, -55°C	-200	+200	nA
Overvoltage Protected, Leakage Current Into the Drain Terminal of an "OFF" Switch	$I_{D(OFF)}$ Overvoltage	V_S = 33V, V_D = 0V, V_{EN} = 0.8V V_S applied at ≤ 25% duty cycle	1, 2, 3	+25°C, +125°C, -55°C	-2.0	+2.0	μA
		V_S = -33V, V_D = 0V, V_{EN} = 0.8V V_S applied at ≤ 25% duty cycle	1, 2, 3	+25°C, +125°C, -55°C	-2.0	+2.0	μA
Positive Supply Current	I(+)	V_A = 0V, V_{EN} = 4.0V	1, 2, 3	+25°C, +125°C, -55°C		2.0	mA
Negative Supply Current	I(-)	V_A = 0V, V_{EN} = 4.0V	1, 2, 3	+25°C, +125°C, -55°C	-1.0		mA
Standby Positive Supply Current	$+I_{SBY}$	V_A = 0V, V_{EN} = 0V	1, 2, 3	+25°C, +125°C, -55°C		2.0	mA
Standby Negative Supply Current	$-I_{SBY}$	V_A = 0V, V_{EN} = 0V	1, 2, 3	+25°C, +125°C, -55°C	-1.0		mA
Switch "ON" Resistance	$+R_{DS1}$	V_S = 10V	1	+25°C		1500	Ω
		I_D = 100μA	2, 3	+125°C, -55°C		1800	Ω
	$-R_{DS1}$	V_S = -10V	1	+25°C		1500	Ω
		I_D = -100μA	2, 3	+125°C, -55°C		1800	Ω
Logic Level Voltage	V_{AL1}	Notes 1, 2	1, 2, 3	+25°C, +125°C, -55°C		0.8	V
	V_{AH1}	Notes 1, 2	1, 2, 3	+25°C, +125°C, -55°C	4.0		V
	V_{AL2}	Note 3	1, 2, 3	+25°C, +125°C, -55°C		0.8	V
	V_{AH2}	Note 3	1, 2, 3	+25°C, +125°C, -55°C	6.0		V
Difference in switch "ON" Resistance Between Channels	$+\Delta R_{DS1}$	$\frac{(+R_{DS1}MAX) - (+R_{DS1}MIN) \times 100}{+R_{DS1}AVE}$	1	+25°C		7	%
	$-\Delta R_{DS1}$	$\frac{(-R_{DS1}MAX) - (-R_{DS1}MIN) \times 100}{-R_{DS1}AVE}$	1	+25°C		7	%

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 4.0V, V_{REF} (Pin 13) = OPEN, Unless Otherwise Specified.

A.C. PARAMETER	SYMBOL	CONDITIONS	SUBGROUP	TEMP	LIMITS		UNITS
					MIN	MAX	
Break-Before-Make Time Delay	t_D	R_L = 1kΩ, C_L = 12.5pF	9	+25°C	25		ns
Propagation Delay Times: Address Inputs to I/O Channel Times	t_A	R_L = 10MΩ, C_L = 14pF	9	+25°C		500	ns
			10, 11	+125°C, -55°C		1000	ns
Enable to I/O	$t_{ON(EN)}$	R_L = 1kΩ, C_L = 12.5pF	9	+25°C		500	ns
			10, 11	+125°C, -55°C		1000	ns
	$t_{OFF(EN)}$	R_L = 1kΩ, C_L = 12.5pF	9	+25°C		500	ns
			10, 11	+125°C, -55°C		1000	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Characterized at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 4.0V, V_{REF} (Pin 13) = OPEN, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMP	LIMITS		UNITS
					MIN	MAX	
Capacitance: Address Input	C_A	V+ = V- = 0V f = 1MHz	4	+25°C		12	pF
Capacitance: Output Switch	C_{OS}	V+ = V- = 0V HI-546/883	4	+25°C		85	pF
		f = 1MHz HI-547/883	4	+25°C		50	pF
Capacitance Input Switch	C_{IS}	V+ = V- + 0V f = 1MHz	4	+25°C		15	pF
Charge Transfer Error	V_{CTE}	V_S = GND V_{GEN} = 0V to 5V	4	+25°C		10	mV
Off Isolation	V_{ISO}	V_{EN} = 0.8V, R_L = 1kΩ C_L = 15pF, V_S = 7VRMS f = 100kHz	4, 5	+25°C	-50		dB

NOTES: 1. Used for forcing conditions for all DC Tests, unless otherwise specified.
2. To drive from DTL/TTL circuits, 1kΩ pull-up resistors to +5.0V supply are recommended.
3. V_{REF} = +10V.
4. The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
5. Worst case isolation occurs on channel 8B due to proximity of the output pins.

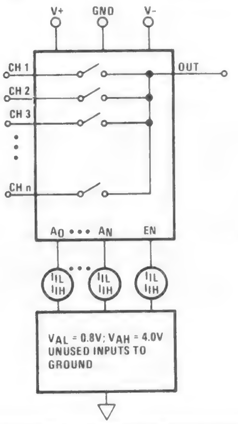
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1, 2 & 3)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

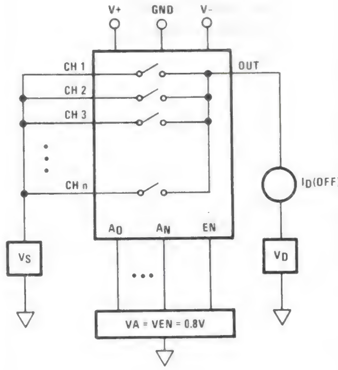
*PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

Test Circuits

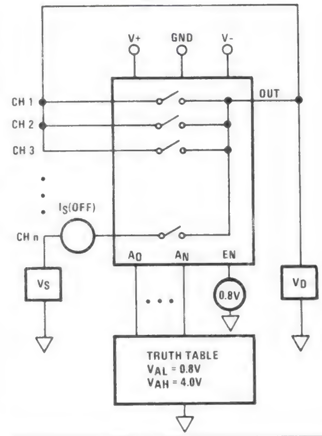
INPUT LEAKAGE CURRENT



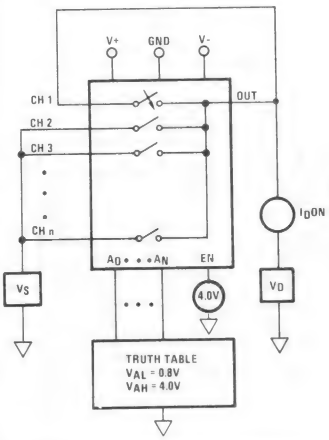
I_D(OFF)



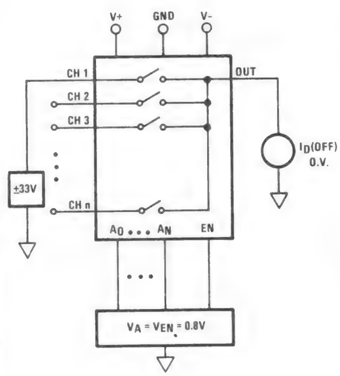
I_S(OFF)



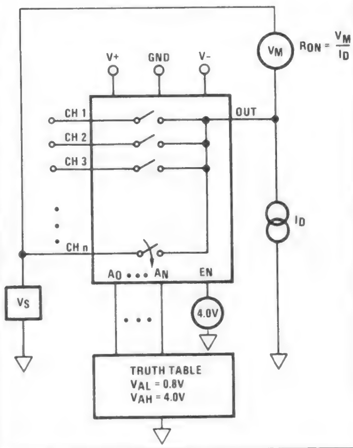
I_D(ON)



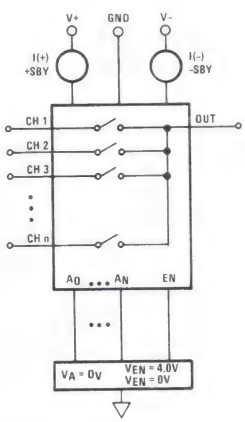
I_D(OFF) OVERVOLTAGE



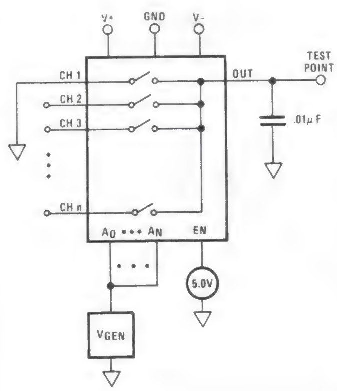
R_{DS}



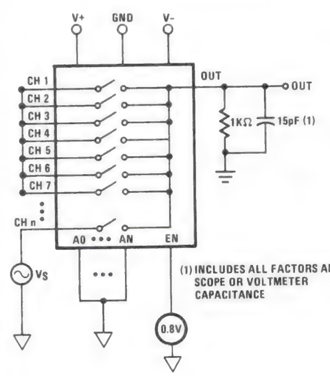
SUPPLY CURRENTS



CHARGE TRANSFER ERROR

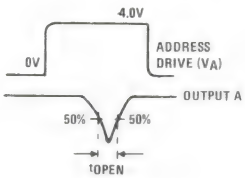


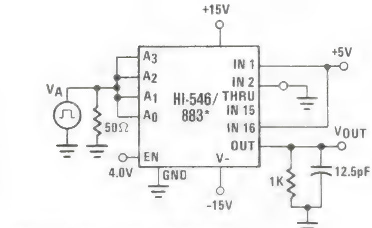
OFF CHANNEL ISOLATION



Switching Waveforms

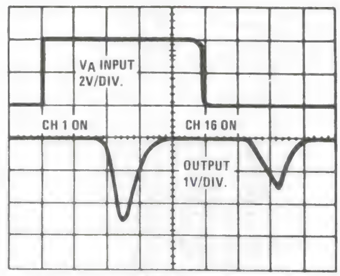
BREAK-BEFORE-MAKE DELAY (t_{OPEN})





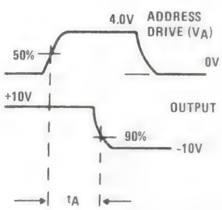
*SIMILAR CONNECTION FOR HI-547/883

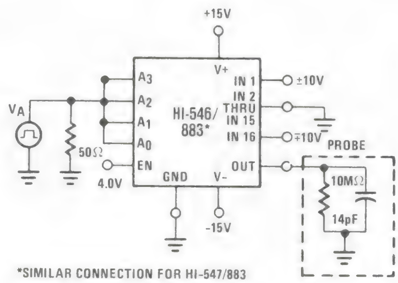
BREAK-BEFORE-MAKE DELAY (t_{OPEN})



100ns/Div.

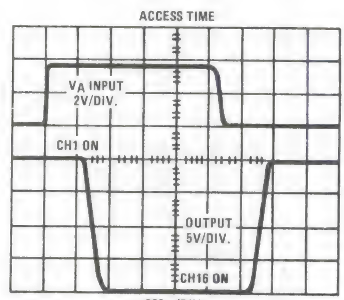
ACCESS TIME vs. LOGIC LEVEL (HIGH)





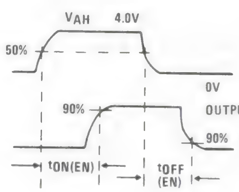
*SIMILAR CONNECTION FOR HI-547/883

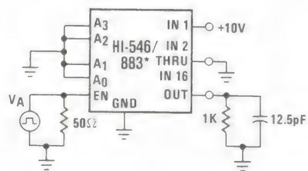
ACCESS TIME



200ns/DIV.

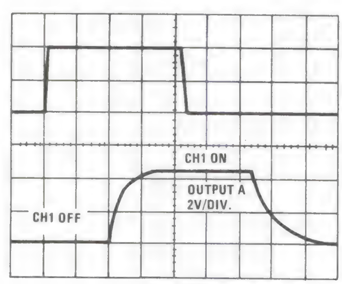
ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$





*SIMILAR CONNECTION FOR HI-547/883

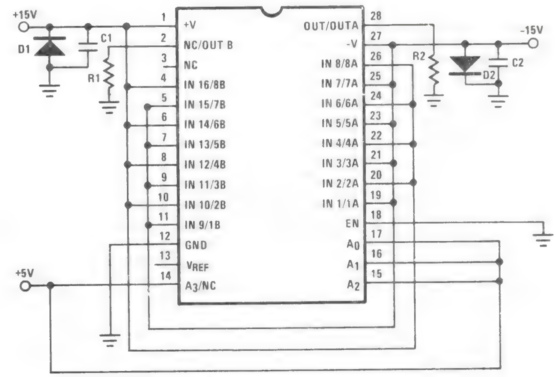
ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$



100ns/DIV.

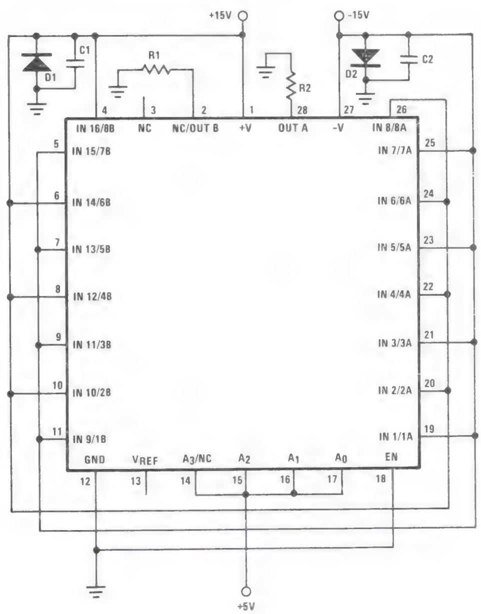
Burn-In Circuits

HI-546/883 HI-547/883 CERAMIC DIP



NOTES:
R1, R2 = 10kΩ ± 5% 1/2 or 1/4W (per socket)
C1, C2 = 0.01μF (per socket) or 0.1μF (per row)
D1, D2 = IN4002 (or equivalent) (per board)

HI-546/883 HI-547/883 CERAMIC LCC

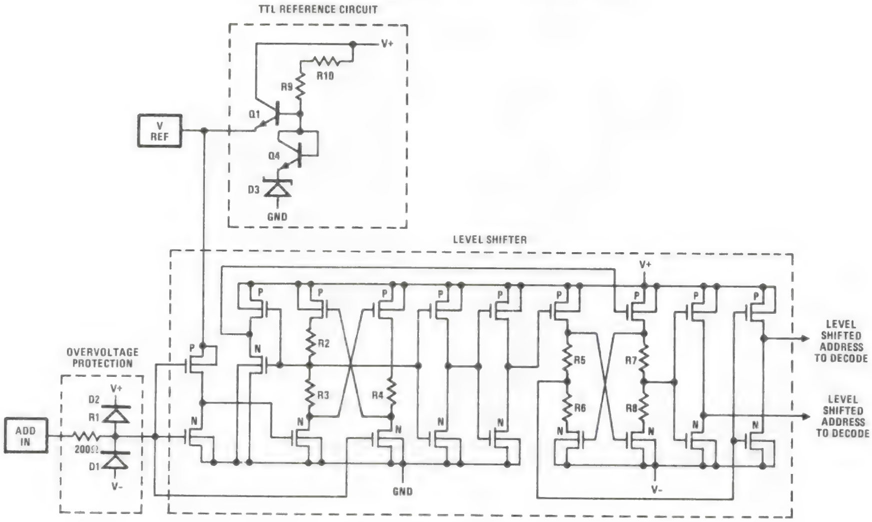


NOTES:
R1, R2 = 10kΩ ± 5% 1/2 or 1/4W (per socket)
C1, C2 = 0.01μF (per socket) or 0.1μF (per row)
D1, D2 = IN4002 (or equivalent) (per board)

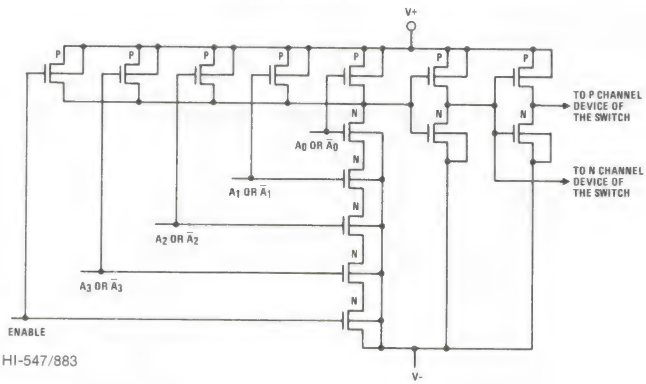
5 CMOS ANALOG MULTIPLEXERS

Schematic Diagrams

ADDRESS INPUT BUFFER AND LEVER SHIFTER

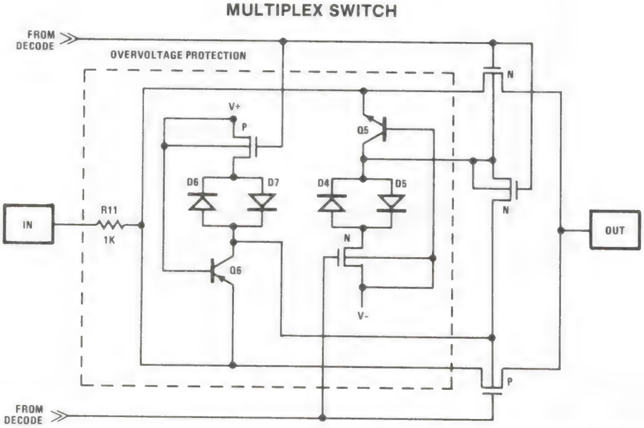


ADDRESS DECODER



Delete A_3 or $\bar{A}_3$ Inputs for HI-547/883

MULTIPLEX SWITCH



Die Characteristics

DIE DIMENSIONS: 83.9 x 159 x 19 mils

METALLIZATION

Type: Al

Thickness: 16kÅ ± 2kÅ

GLASSIVATION

Type: Nitride

Thickness: 7kÅ ± 0.7kÅ

WORST CASE CURRENT DENSITY: 1.4×10^5 A/cm^2

TRANSISTOR COUNT:

HI-546/883 485

HI-547/883 485

PROCESS: CMOS-DI

DIE ATTACH

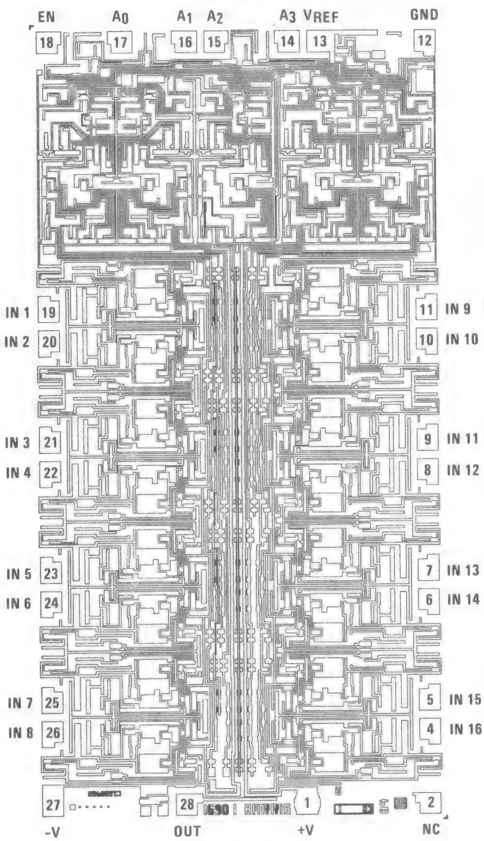
Material: Gold Silicon Eutectic Alloy

Temperature: Ceramic DIP — 460°C (Max)

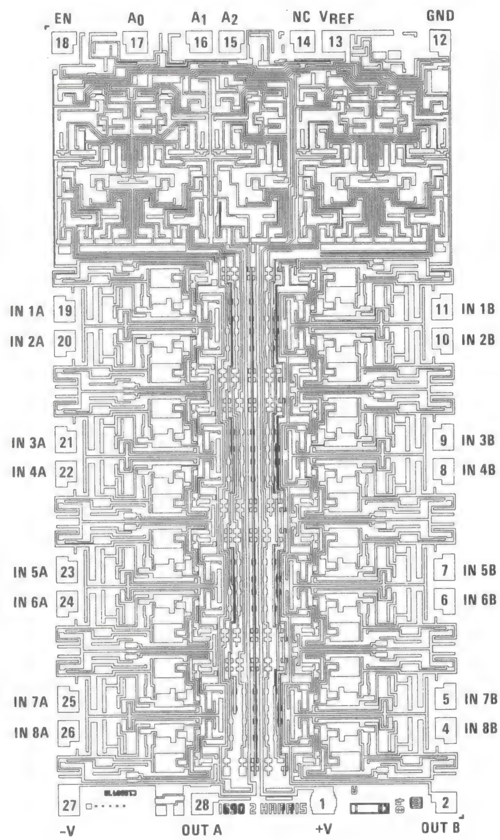
Ceramic LCC — 420°C (Max)

Metallization Mask Layout

HI-546/883

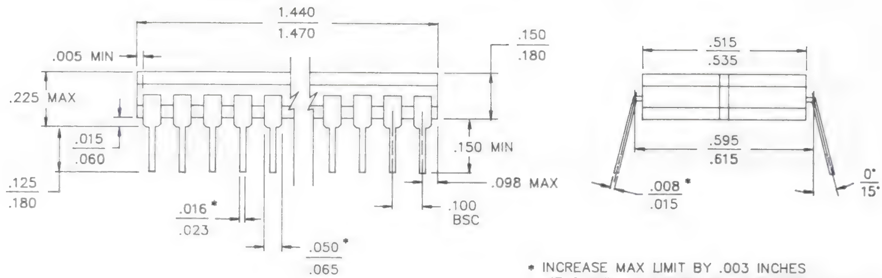


HI-547/883



Packaging†

28 PIN CERAMIC DIP

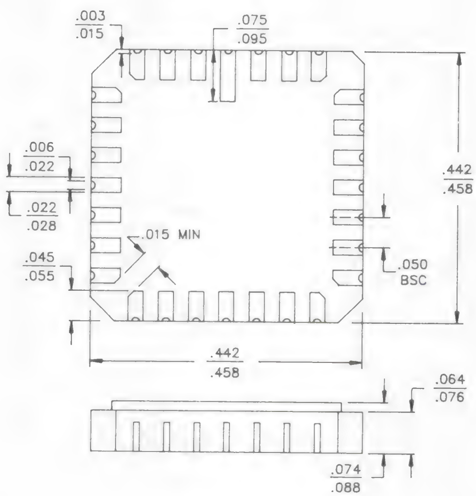


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-10

28 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-4

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HI-546
HI-547

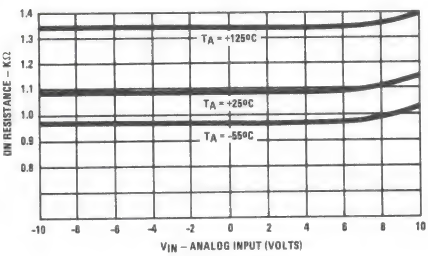
DESIGN INFORMATION

Single 16/Differential 8 Channel CMOS Analog Multiplexers With Active Overvoltage Protection

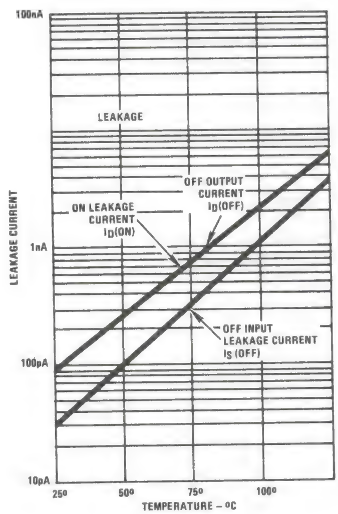
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics
Unless Otherwise Specified: T_A = 25°C, V_{SUPPLY} = ±15V, V_{AH} = +4V, V_{AL} = 0.8V, V_{REF} = Open

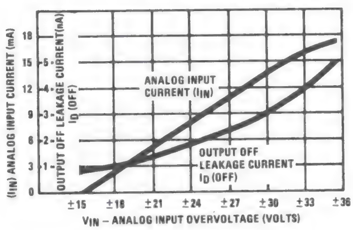
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



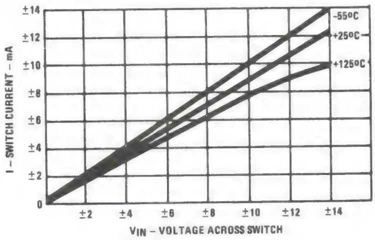
LEAKAGE CURRENT vs. TEMPERATURE



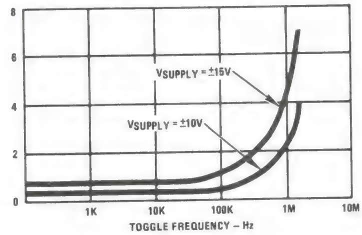
ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



ON CHANNEL CURRENT vs. VOLTAGE



SUPPLY CURRENT vs. TOGGLE FREQUENCY



HARRIS

HI-548/883
HI-549/883

Single 8/Differential 4 Channel CMOS Analog Multiplexers With Active Overvoltage Protection

January 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- No Channel Interaction During Overvoltage
- Guaranteed R_{ON} Matching
- 44V Maximum Power Supply
- Break-Before-Make Switch'
- Analog Signal Range .... ±15V
- Access Time (Max.) 1.0μs
- Power Dissipation (Max.) 45mW

Applications

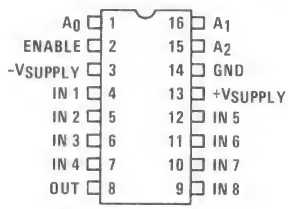
- Data Acquisition Systems
- Control Systems
- Telemetry

Description

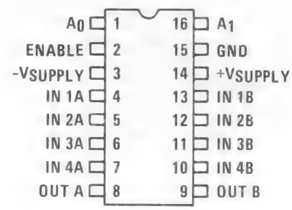
The HI-548/883 and HI-549/883 are analog multiplexers with Active Overvoltage Protection and guaranteed R_{ON} matching. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant 70 volt peak-to-peak levels with ±15V supplies and digital inputs will sustain continuous faults up to 4 volts greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur; each input presents 1kΩ of resistance under this condition. These features make the HI-548/883 and HI-549/883 ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. Both devices are fabricated with 44 volt dielectrically isolated CMOS technology. The HI-548/883 is a 8 channel device and the HI-549/883 is a 4 channel differential version. If input overvoltage protection is not needed, the HI-508/883 and HI-509/883 multiplexers are recommended. For further information see Application Notes 520 and 521.

Pinouts

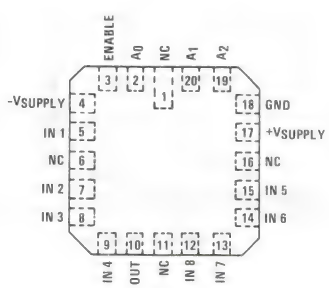
HI1-548/883 (CERAMIC DIP)
TOP VIEW



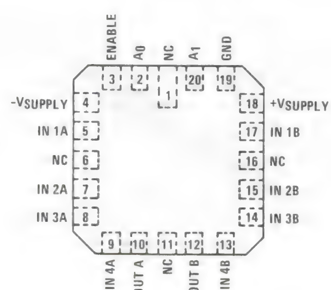
HI1-549/883 (CERAMIC DIP)
TOP VIEW



HI4-548/883 (CERAMIC LCC)
TOP VIEW

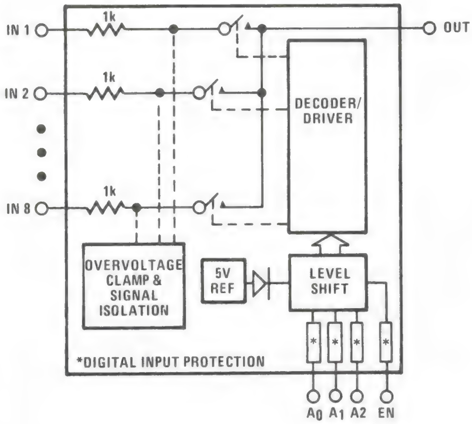


HI4-549/883 (CERAMIC LCC)
TOP VIEW



Functional Diagrams

HI-548/883

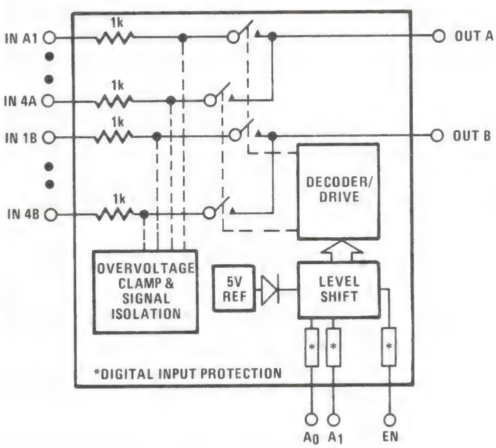


TRUTH TABLES

HI-548/883

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-549/883



HI-549/883

A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

Absolute Maximum Ratings

Voltage Between Supply Pins 44V
$+V_{SUPPLY}$ to Ground 22V
$-V_{SUPPLY}$ to Ground 25V
Analog Input Voltage
$+V_S$ .... $+V_{SUPPLY}$ +20V
$-V_S$ .... $-V_{SUPPLY}$ -20V
Digital Input Voltage
$+V_{EN}$, $+V_A$ .... $+V_{SUPPLY}$ +4V
$-V_{EN}$, $-V_A$ .... $-V_{SUPPLY}$ -4V
or 20mA, whichever occurs first.
Continuous Current, S or D 20mA
Peak Current, S or D
(Pulsed at 1ms, 10% Duty Cycle Max.) 40mA
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering 10 Seconds) .... 275°C

Junction Temperature .... +175°C
Thermal Resistance, Junction-to-Case (θjc)
Ceramic DIP Package .... 26°C/W
Ceramic LCC Package .... 19°C/W
Thermal Resistance, Junction-to-Ambient (θja)
Ceramic DIP Package .... 80°C/W
Ceramic LCC Package .... 76°C/W
Power Dissipation (at 75°C)
Ceramic DIP Package 1.25W
Ceramic LCC Package 1.32W
Power Dissipation Derating Factor (Above +75°C)
Ceramic DIP Package .... 12.5mW/°C
Ceramic LCC Package .... 13.2mW/°C
ESD Classification .... ≤2000V

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) .... ±15V
Analog Input Voltage (V_S) .... $\pm V_{SUPPLY}$

Logic Low Level (V_{AL}) .... 0V to 0.8V
Logic High Level (V_{AH}) .... +4V to $+V_{SUPPLY}$
Max RMS Current, S or D 8mA

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 4.0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current	I_{IH}	Measure Inputs Sequentially,	1, 2, 3	+25°C, +125°C, -55°C	-1.0	1.0	μA
	I_{IL}	Connect All Unused Inputs to GND	1, 2, 3	+25°C, +125°C, -55°C	-1.0	1.0	μA
Leakage Current Into the Source Terminal of an "OFF" Switch	$+I_{S(OFF)}$	V_S = +10V, V_D = -10V, V_{EN} = 0.8V	1	+25°C	-10	+10	nA
		All Unused Inputs = -10V	2, 3	+125°C, -55°C	-50	+50	nA
	$-I_{S(OFF)}$	V_S = -10V, V_D = +10V, V_{EN} = 0.8V	1	+25°C	-10	+10	nA
		All Unused Inputs = +10V	2, 3	+125°C, -55°C	-50	+50	nA
Leakage Current Into the Drain Terminal of an "OFF" Switch	$+I_{D(OFF)}$	V_D = +10V, V_{EN} = 0.8V	1	+25°C	-10	+10	nA
		All Unused Inputs = -10V HI-548/883	2, 3	+125°C, -55°C	-200	+200	nA
		HI-549/883	2, 3	+125°C, -55°C	-100	+100	nA
	$-I_{D(OFF)}$	V_D = -10V, V_{EN} = 0.8V	1	+25°C	-10	+10	nA
		All Unused Inputs = +10V HI-548/883	2, 3	+125°C, -55°C	-200	+200	nA
		HI-549/883	2, 3	+125°C, -55°C	-100	+100	nA
Leakage Current From an "ON" Driver Into the Switch (Drain)	$+I_{D(ON)}$	$V_S = V_D$ = +10V	1	+25°C	-10	+10	nA
		All Unused Inputs = -10V HI-548/883	2, 3	+125°C, -55°C	-200	+200	nA
		HI-549/883	2, 3	+125°C, -55°C	-100	+100	nA
	$-I_{D(ON)}$	$V_S = V_D$ = -10V	1	+25°C	-10	+10	nA
		All Unused Inputs = +10V HI-548/883	2, 3	+125°C, -55°C	-200	+200	nA
		HI-549/883	2, 3	+125°C, -55°C	-100	+100	nA
Overvoltage Protected, Leakage Current Into the Drain Terminal of an "OFF" Switch	I_D(OFF) Overvoltage	V_S = 33V, V_D = 0V, V_{EN} = 0.8V, V_S applied at ≤25% duty cycle	1, 2, 3	+25°C, +125°C, -55°C	-2.0	+2.0	μA
		V_S = -33V, V_D = 0V, V_{EN} = 0.8V, V_S applied at ≤25% duty cycle	1, 2, 3	+25°C, +125°C, -55°C	-2.0	+2.0	μA
Positive Supply Current	I(+)	V_A = 0V, V_{EN} = 4.0V	1, 2, 3	+25°C, +125°C, -55°C		2.0	mA
Negative Supply Current	I(-)	V_A = 0V, V_{EN} = 4.0V	1, 2, 3	+25°C, +125°C, -55°C	-1.0		mA
Standby Positive Supply Current	$+I_{SBY}$	V_A = 0V, V_{EN} = 0V	1, 2, 3	+25°C, +125°C, -55°C		2.0	mA
Standby Negative Supply Current	$-I_{SBY}$	V_A = 0V, V_{EN} = 0V	1, 2, 3	+25°C, +125°C, -55°C	-1.0		mA
Switch "ON" Resistance	$+R_{DS1}$	V_S = 10V	1	+25°C		1500	Ω
		I_D = 100μA	2, 3	+125°C, -55°C		1800	Ω
	$-R_{DS1}$	V_S = -10V	1	+25°C		1500	Ω
		I_D = -100μA	2, 3	+125°C, -55°C		1800	Ω
Logic Level Voltage	V_{AL}	Note 1, 2	1, 2, 3	+25°C, +125°C, -55°C		0.8	V
	V_{AH}	Note 1, 2	1, 2, 3	+25°C, +125°C, -55°C	4.0		V
Difference in switch "ON" Resistance Between Channels	$+\Delta R_{DS1}$	$\frac{(+R_{DS1}MAX) - (+R_{DS1}MIN) \times 100}{+R_{DS1}AVE}$	1	+25°C		7	%
	$-\Delta R_{DS1}$	$\frac{(-R_{DS1}MAX) - (-R_{DS1}MIN) \times 100}{-R_{DS1}AVE}$	1	+25°C		7	%

NOTES:
1. Used for forcing conditions for all DC tests unless otherwise specified.
2. To drive from DTL/TTL circuits, 1kΩ pull-up resistors to +5.0V supply are recommended.

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 4.0V, Unless Otherwise Specified.

A.C. PARAMETERS	SYMBOL	CONDITIONS	SUBGROUP	TEMP	LIMITS		UNITS
					MIN	MAX	
Break-Before-Make Time Delay	t_D	R_L = 1kΩ, C_L = 12.5pF	9	+25°C	25		ns
Propagation Delay Times: Address Inputs to I/O Channel Times	t_A	R_L = 10MΩ, C_L = 14pF	9	+25°C		500	ns
			10, 11	+125°C, -55°C		1000	ns
Enable to I/O	$t_{ON(EN)}$	R_L = 1kΩ, C_L = 12.5pF	9	+25°C		500	ns
			10, 11	+125°C, -55°C		1000	ns
	$t_{OFF(EN)}$	R_L = 1kΩ, C_L = 12.5pF	9	+25°C		500	ns
			10, 11	+125°C, -55°C		1000	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Characterized at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 4.0V, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMP	LIMITS		UNITS
					MIN	MAX	
Capacitance: Address Input	C_A	V+ = V- = 0V, f = 1MHz	3	+25°C		10	pF
Capacitance: Output Switch	C_{OS}	V+ = V- = 0V, f = 1MHz, HI-548/883	3	+25°C		45	pF
		HI-549/883	3	+25°C		25	pF
Capacitance Input Switch	C_{IS}	V+ = V- = 0V, f = 1MHz	3	+25°C		15	pF
Charge Transfer Error	V_{CTE}	V_S = GND, V_{GEN} = 0V to 5V, f = 200kHz	3	+25°C		10	mV
Off Isolation	V_{ISO}	V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF, V_S = $7V_{RMS}$, f = 100kHz	3, 4	+25°C	-50		dB

NOTES: 3. The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
4. Worst case isolation occurs on channel 4 due to proximity of the output pins.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

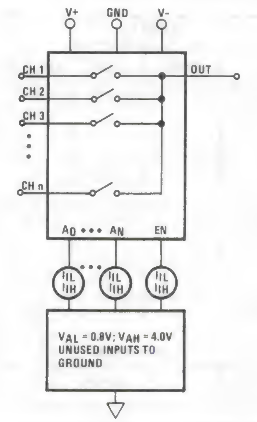
MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1, 2 & 3)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

*PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

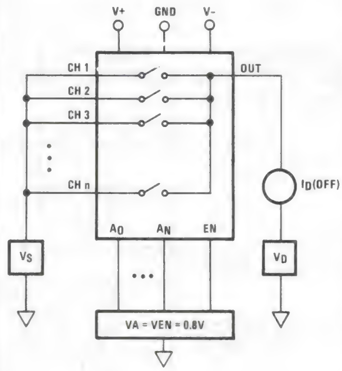
CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Test Circuits

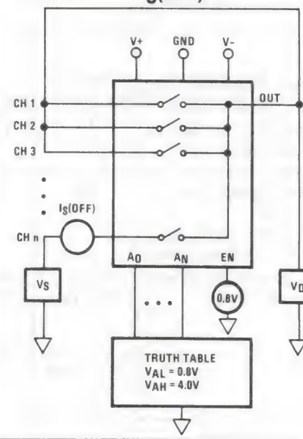
INPUT LEAKAGE CURRENT



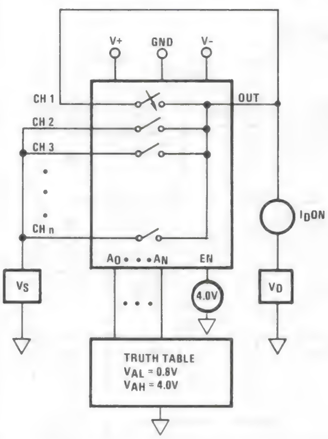
I_D(OFF)



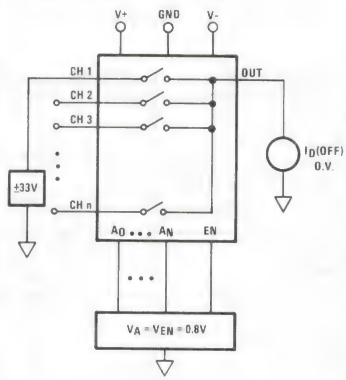
I_S(OFF)



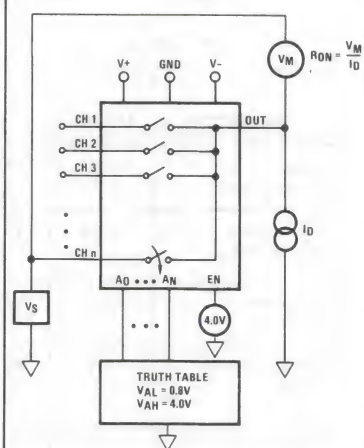
I_D(ON)



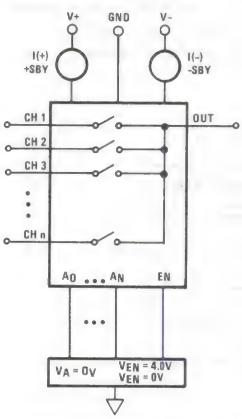
I_D(OFF) OVERVOLTAGE



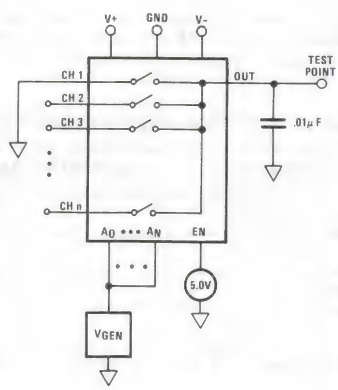
R_{DS}



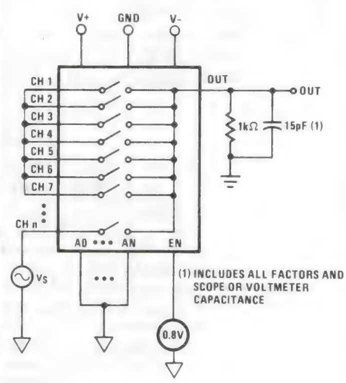
SUPPLY CURRENTS



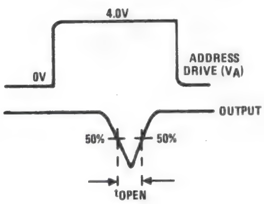
CHARGE TRANSFER ERROR



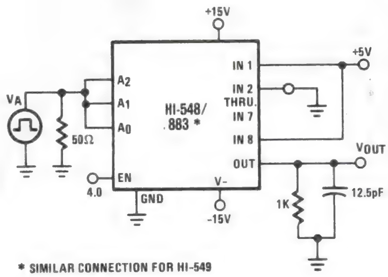
OFF CHANNEL ISOLATION



Switching Waveforms

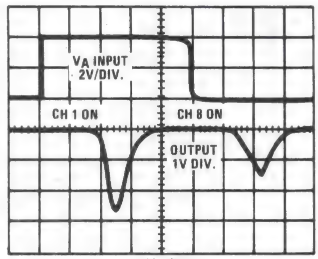


BREAK-BEFORE-MAKE DELAY (t_{OPEN})

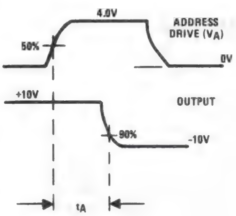


* SIMILAR CONNECTION FOR HI-549

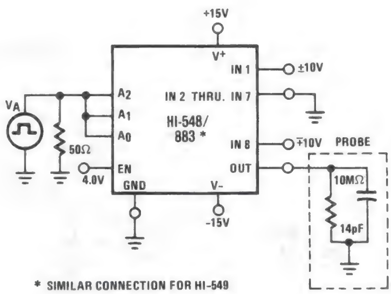
BREAK-BEFORE-MAKE DELAY (t_{OPEN})



100ns/DIV.

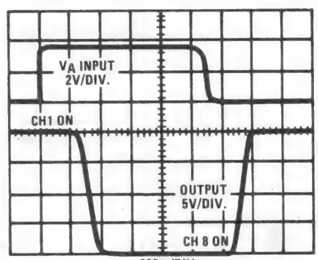


ACCESS TIME



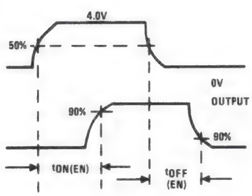
* SIMILAR CONNECTION FOR HI-549

ACCESS TIME

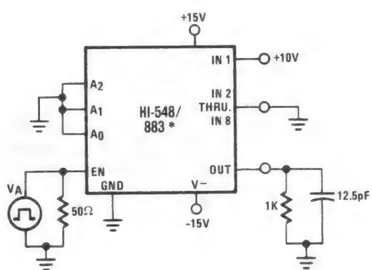


200ns/DIV.

ENABLE DRIVE

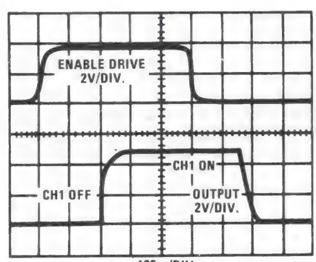


ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$



*SIMILAR CONNECTION FOR HI-549

ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$

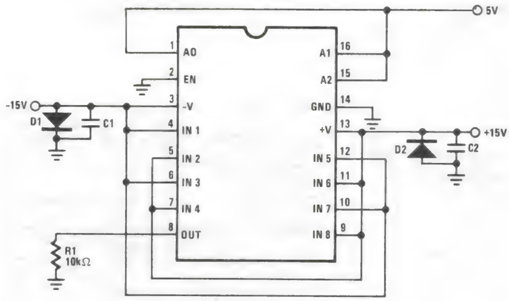


100ns/DIV.

5
CMOS ANALOG MULTIPLEXERS

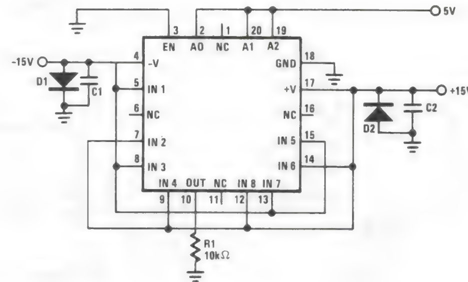
Burn-In Circuits

HI-548/883 CERAMIC DIP



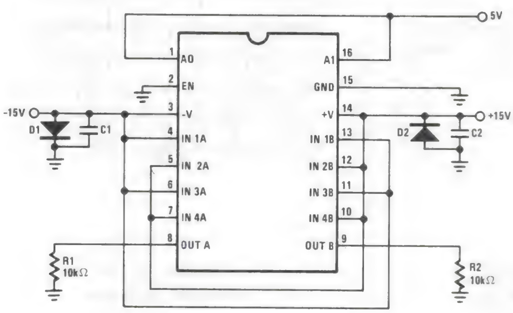
NOTES:
R1 = 10kΩ ± 5% 1/2 or 1/4W (per socket)
C1, C2 = 0.01μF (per socket) or 0.1μF (per row)
D1, D2 = IN4002 (or equivalent) (per board)

HI-548/883 CERAMIC LCC



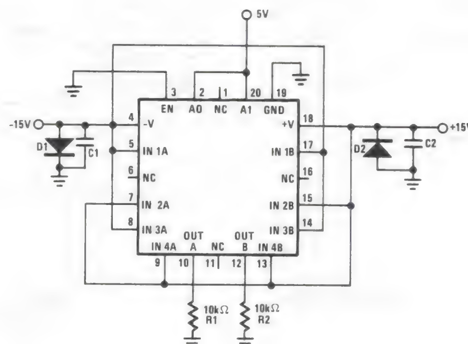
NOTES:
R1 = 10kΩ ± 5% 1/2 or 1/4W (per socket)
C1, C2 = .01μF (per socket) or 0.1μF (per row)
D1, D2 = IN4002 (or equivalent) (per board)

HI-549/883 CERAMIC DIP



NOTES:
R1, R2 = 10kΩ ± 5% 1/2 or 1/4W (per socket)
C1, C2 = 0.01μF (per socket) or 0.1μF (per row)
D1, D2 = IN4002 (or equivalent) (per board)

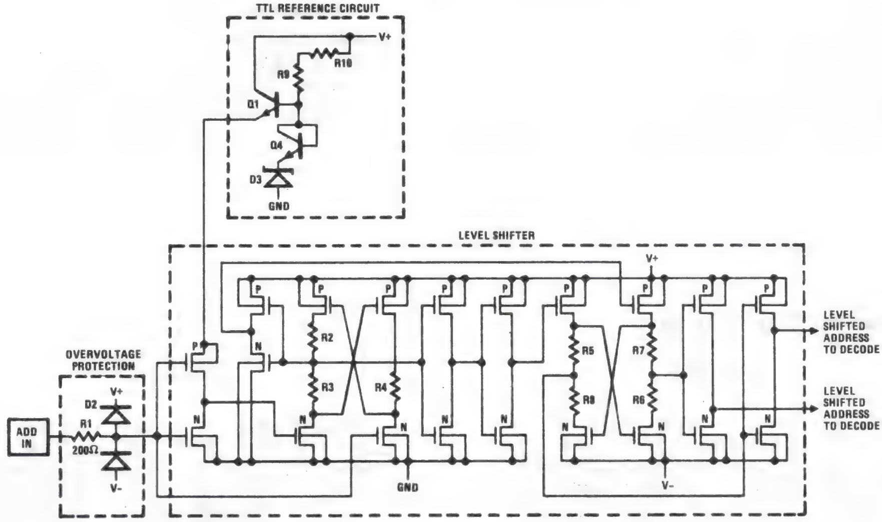
HI-549/883 CERAMIC LCC



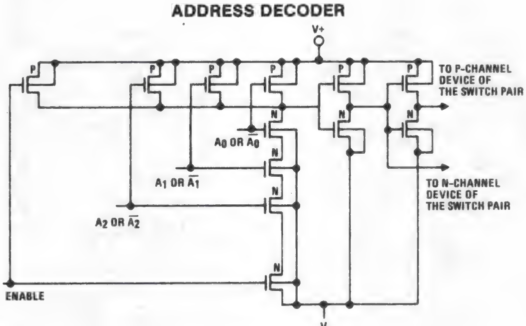
NOTES:
R1, R2 = 10kΩ ± 5% 1/2 or 1/4W (per socket)
C1, C2 = 0.01μF (per socket) or 0.1μF (per row)
D1, D2 = IN4002 (or equivalent) (per board)

Schematic Diagrams

ADDRESS INPUT BUFFER AND LEVER SHIFTER

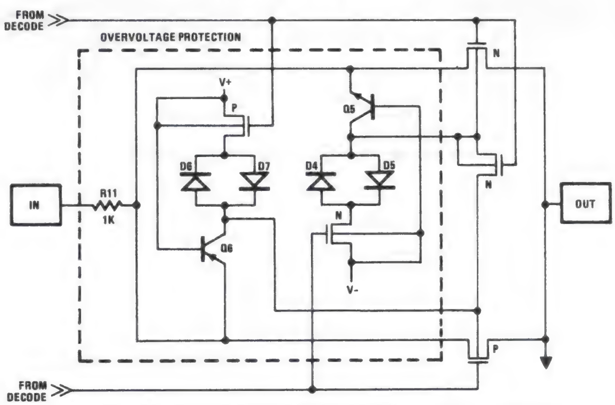


ADDRESS DECODER



Delete A_2 or $\overline{A_2}$ input for HI-549/883

MULTIPLEX SWITCH



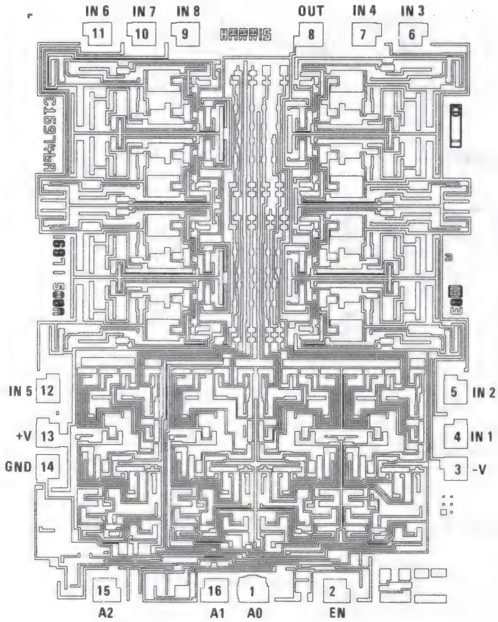
Die Characteristics

DIE DIMENSIONS: 83 x 108 x 19 mils
METALLIZATION
Type: Al
Thickness: 16kÅ ± 2kÅ
GLASSIVATION
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ
WORST CASE CURRENT DENSITY: 1.4×10^5 A/cm^2

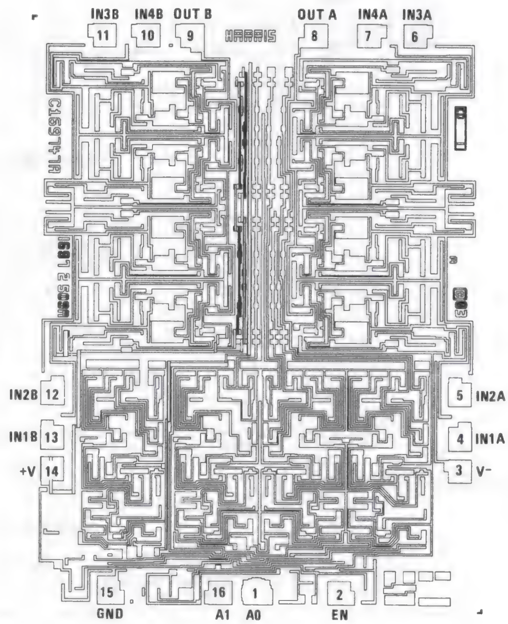
TRANSISTOR COUNT:
HI-548/883 253
HI-549/883 253
PROCESS: CMOS-DI
DIE ATTACH
Material: Gold Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

Metallization Mask Layout

HI-548/883



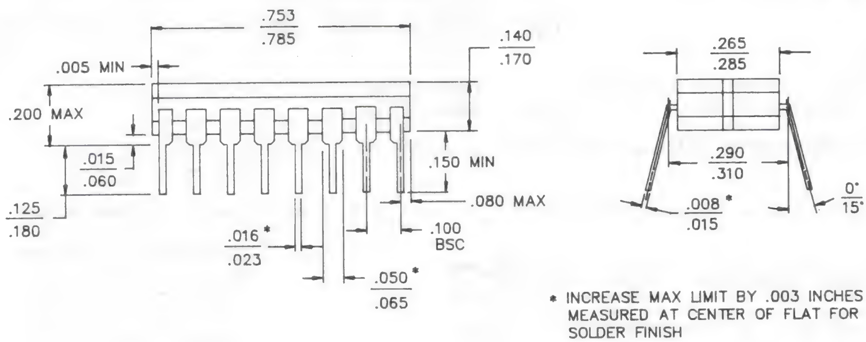
HI-549/883



NOTE: Pad Numbers Correspond to DIP Pin Numbers Only

Packaging†

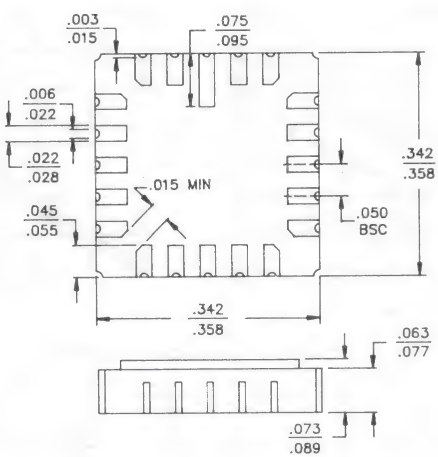
16 PIN CERAMIC DIP



LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-2

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

5
CMOS ANALOG MULTIPLEXERS

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in inches.

† MIL-M-38510 Compliant Materials, Finishes & Dimensions.

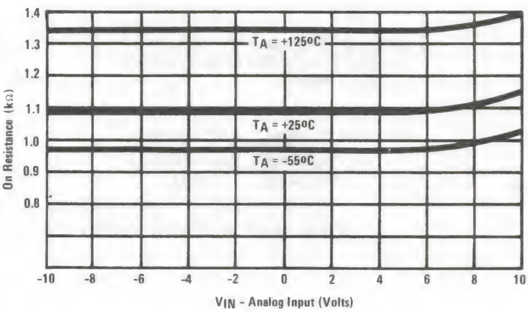
HI-548
HI-549

Single 8/Differential 4 Channel CMOS Analog Multiplexers With Active Overvoltage Protection

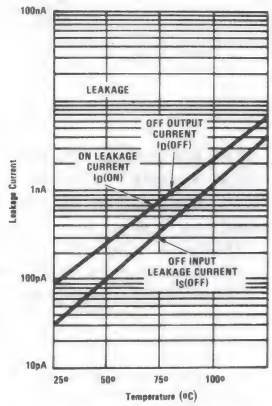
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics Unless Otherwise Specified: T_A = 25°C, V_{SUPPLY} = ±15V, V_{AH} = +4V, V_{AL} = 0.8V

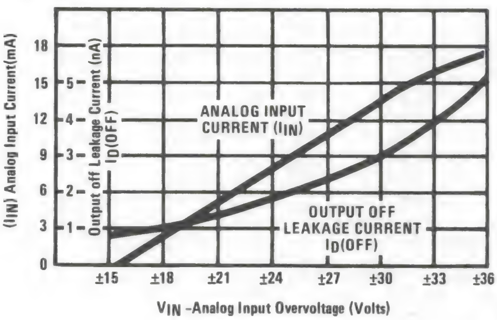
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



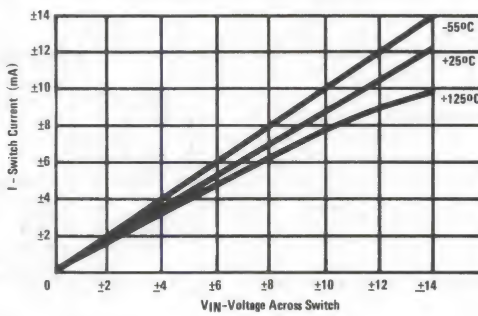
LEAKAGE CURRENT vs. TEMPERATURE



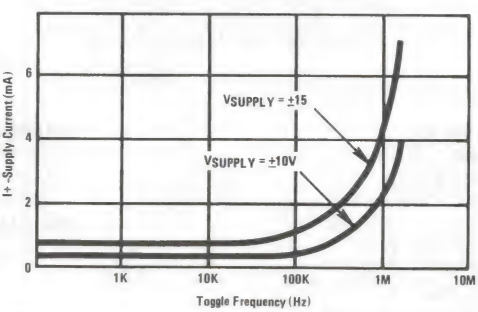
ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



ON CHANNEL CURRENT vs. VOLTAGE



SUPPLY CURRENT vs. TOGGLE FREQUENCY



HARRIS

HI-1818A/883
HI-1828A/883

Low Resistance Single 8/Differential 4 Channel CMOS Analog Multiplexers

July 1987

Features

- **This Circuit Is Processed In Accordance to Mil-Std-883 and Is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Low On Resistance (Max. Over Temp.)................500Ω**
- **Wide Analog Signal Range .... ±15V**
- **Very Low Power Consumption........................< 30mW**
- **Access Time (Max. Over Temp.).........................1000ns**
- **Break-Before-Make Switching**

Applications

- **Data Acquisition Systems**
- **Precision Instrumentation**
- **Demultiplexing**
- **Selector Switch**

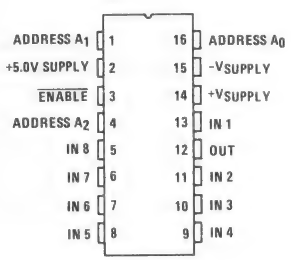
Description

The HI-1818A/883 and HI-1828/883 are monolithic high performance CMOS analog multiplexers offering built-in channel selection decoding plus an inhibit (enable) input for disabling all channels. Dielectric Isolation (DI) processing is used for enhanced reliability and performance (see Application Note 521). Substrate leakage and parasitic capacitance are much lower, resulting in extremely low static errors and high throughput rates. Low output leakage (250nA max.) and low channel ON resistance (500Ω max.) assure optimum performance in low level or current mode applications.

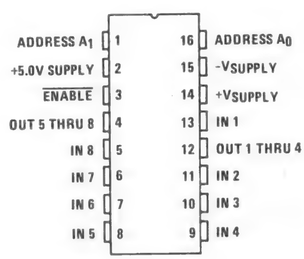
The HI-1818A/883 is a single-ended 8 channel multiplexer, while the HI-1828A/883 is a differential 4 channel version. Either device is ideally suited for medical instrumentation, telemetry systems, and microprocessor based data acquisition systems.

Pinouts

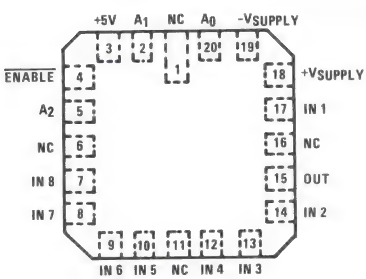
HI1-1818A/883 (CERAMIC DIP)
TOP VIEW



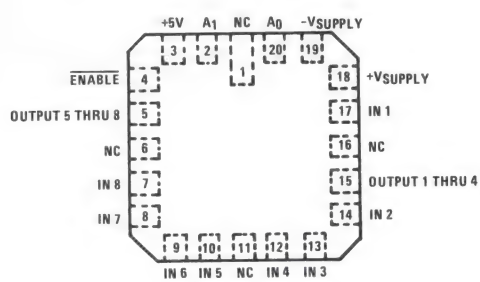
HI1-1828A/883 (CERAMIC DIP)
TOP VIEW



HI4-1818A/883 (CERAMIC LCC)
TOP VIEW

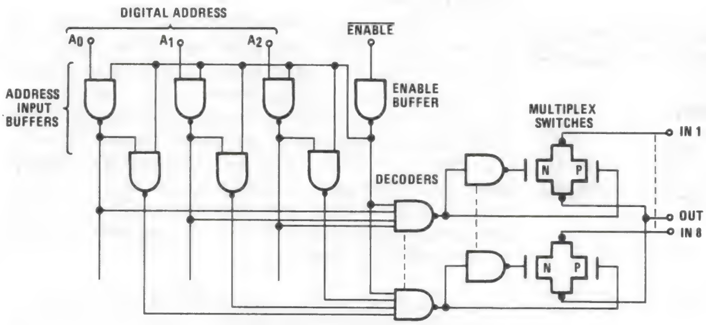


HI4-1828A/883 (CERAMIC LCC)
TOP VIEW



Functional Diagrams

HI-1818A/883

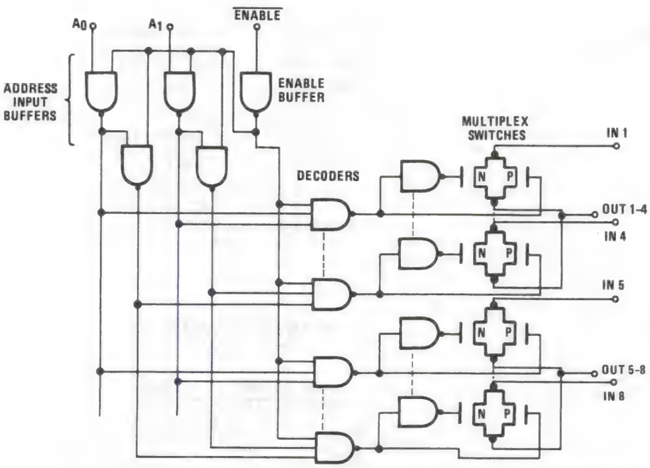


TRUTH TABLES

HI-1818A/883

ADDRESS				"ON"
A_2	A_1	A_0	$\overline{EN}$	CHANNEL
L	L	L	L	1
L	L	H	L	2
L	H	L	L	3
L	H	H	L	4
H	L	L	L	5
H	L	H	L	6
H	H	L	L	7
H	H	H	L	8
X	X	X	H	None

HI-1828A/883



HI-1828A/883

ADDRESS			"ON"
A_1	A_0	$\overline{EN}$	CHANNELS
L	L	L	1 and 5
L	H	L	2 and 6
H	L	L	3 and 7
H	H	L	4 and 8
X	X	H	None

Absolute Maximum Ratings

Voltage Between Supply Pins 40V
$+V_{SUPPLY}$ to Ground 20V
$-V_{SUPPLY}$ to Ground 20V
V_L to GND 30V
Analog Input Voltage
$+V_S$ .... $+V_{SUPPLY}$ +2V
$-V_S$ .... $-V_{SUPPLY}$ -2V
Digital Input Voltage
$+V_{\overline{EN}}$, $+V_A$ .... $+V_{SUPPLY}$
$-V_{\overline{EN}}$, $-V_A$ .... $-V_{SUPPLY}$
Continuous Current, S or D 20mA
Peak Current, S or D (Pulsed at 1ms, 10% Duty Cycle Max.) 40mA
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering 10 Seconds) .... 275°C

Junction Temperature .... +175°C
Thermal Resistance, Junction-to-Case (θjc)
Ceramic DIP Package .... 35°C/W
Ceramic LCC Package .... 25°C/W
Thermal Resistance, Junction-to-Ambient (θja)
Ceramic DIP Package .... 90°C/W
Ceramic LCC Package .... 83°C/W
Power Dissipation (@ 75°C)
Ceramic DIP Package 1.11W
Ceramic LCC Package 1.20W
Power Dissipation Derating Factor (Above +75°C)
Ceramic DIP Package .... 11.1mW/°C
Ceramic LCC Package .... 12.0mW/°C
ESD Classification .... ≤ 2000V

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) .... ±15V
Analog Input Voltage (V_S) .... $\pm V_{SUPPLY}$
Logic Low Level (V_{AL}) .... 0V to 0.4V
Logic High Level (V_{AH}) .... 4.0V to $+V_{SUPPLY}$
+5.0V Supply (V_L) .... +5.0V
Max RMS Current, S or D 11mA

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, $V_{\overline{EN}}$ = 0.4V, V_L = +5V Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current	I_{IH}	Measure Inputs Sequentially, Connect all Unused Inputs to GND	1, 2, 3	+25°C, +125°C, -55°C	-1.0	1.0	µA
	I_{IL}	Measure Inputs Sequentially, Connect all Unused Inputs to 5V	1, 2, 3	+25°C, +125°C, -55°C	-1.0	1.0	µA
Leakage Current Into the Source Terminal of an "OFF" Switch	$+I_{S(OFF)}$	V_S = +10V, V_D = -10V, $V_{\overline{EN}}$ = 4.0V	1	+25°C	-10	+10	nA
		All Unused Inputs = -10V	2, 3	+125°C, -55°C	-50	+50	nA
	$-I_{S(OFF)}$	V_S = -10V, V_D = +10V, $V_{\overline{EN}}$ = 4.0V	1	+25°C	-10	+10	nA
		All Unused Inputs = +10V	2, 3	+125°C, -55°C	-50	+50	nA
Leakage Current Into the Drain Terminal of an "OFF" Switch	$+I_{D(OFF)}$	V_D = +10V, $V_{\overline{EN}}$ = 4.0V	1	+25°C	-10	+10	nA
		All Unused Inputs = -10V HI-1818A/883	2, 3	+125°C, -55°C	-250	+250	nA
		HI-1828A/883	2, 3	+125°C, -55°C	-125	+125	nA
	$-I_{D(OFF)}$	V_D = -10V, $V_{\overline{EN}}$ = 4.0V	1	+25°C	-10	+10	nA
		All Unused Inputs = +10V HI-1818A/883	2, 3	+125°C, -55°C	-250	+250	nA
		HI-1828A/883	2, 3	+125°C, -55°C	-125	+125	nA
Leakage Current From an "ON" Driver Into the Switch (Drain)	$+I_{D(ON)}$	$V_S = V_D$ = +10V, $V_{\overline{EN}}$ = 0.4V	1	+25°C	-10	+10	nA
		All Unused Inputs = -10V HI-1818A/883	2, 3	+125°C, -55°C	-250	+250	nA
		HI-1828A/883	2, 3	+125°C, -55°C	-125	+125	nA
	$-I_{D(ON)}$	$V_S = V_D$ = -10V, $V_{\overline{EN}}$ = 0.4V	1	+25°C	-10	+10	nA
		All Unused Inputs = +10V HI-1818A/883	2, 3	+125°C, -55°C	-250	+250	nA
		HI-1828A/883	2, 3	+125°C, -55°C	-125	+125	nA
Positive Supply Current	I(+)	$V_{\overline{EN}}$ = 0.4V, V_{AL} = 0.4V, V_{AH} = 4.0V	1, 2, 3	+25°C, +125°C, -55°C	—	0.5	mA
Negative Supply Current	I(-)	$V_{\overline{EN}}$ = 0.4V V_{AL} = 0.4V, V_{AH} = 4.0V	1, 2, 3	+25°C, +125°C, -55°C	-1.0	—	mA
Logic Supply Current	I_L	$V_{\overline{EN}}$ = 0.4V V_{AL} = 0.4V, V_{AH} = 4.0V	1, 2, 3	+25°C, +125°C, -55°C	—	1.0	mA
Switch "ON" Resistance	$+R_{DS1}$	V_S = 10V	1	+25°C	—	400	Ω
		I_D = 1mA	2, 3	+125°C, -55°C	—	500	Ω
	$-R_{DS1}$	V_S = -10V	1	+25°C	—	400	Ω
		I_D = -1mA	2, 3	+125°C, -55°C	—	500	Ω
Logic Level Voltage	V_{AL}	Applied to all Digital Inputs for all DC Tests	1, 2, 3	+25°C, +125°C, -55°C	—	0.4	V
	V_{AH}	Applied to all Digital Inputs for all DC Tests	1, 2, 3	+25°C, +125°C, -55°C	4.0	—	V

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, $V_{\overline{EN}}$ = 0.4V, V_L = +5V Unless Otherwise Specified.

A.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMP	LIMITS MIN	LIMITS MAX	UNITS
Break-Before-Make Time Delay	t_D	R_L = 200Ω, C_L = 12.5pF	9	+25°C	5	—	ns
Propagation Delay Times: Address Inputs to I/O Channel Times	t_A	R_L = 10MΩ, C_L = 12.5pF	9	+25°C	—	500	ns
			10, 11	+125°C, -55°C	—	1000	ns
Enable to I/O	$t_{ON(EN)}$	R_L = 200Ω, C_L = 12.5pF	9	+25°C	—	500	ns
	$t_{OFF(EN)}$	R_L = 200Ω, C_L = 12.5pF	10, 11	+125°C, -55°C	—	1000	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Characterized at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, $V_{\overline{EN}}$ = 0.4V, V_L = +5V Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMP	LIMITS MIN	LIMITS MAX	UNITS
Capacitance: Address	C_A	V+ = V- = 0V, f = 1MHz	1	+25°C	—	10	pF
Capacitance: Output Switch	C_{OS}	V+ = V- = 0V, f = 1MHz HI-1818A/883	1	+25°C	—	50	pF
		HI-1828A/883	1	+25°C	—	25	pF
Capacitance: Input Switch	C_{IS}	V+ = V- = 0V, f = 1MHz	1	+25°C	—	10	pF
Charge Transfer Error	V_{CTE}	V_S = GND, V_{GEN} = 0V to 5V	1	+25°C	—	10	mV
Off Isolation	V_{ISO}	$V_{\overline{EN}}$ = 4.0V, R_L = 1k, C_L = 15pF, V_S = $7V_{RMS}$, f = 100kHz	1	+25°C	-50	—	dB

NOTE: 1. The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

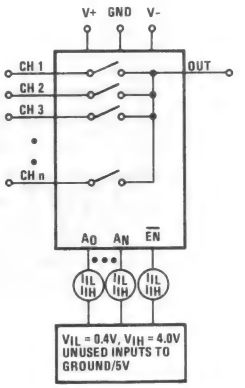
MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1, 2 & 3)
Interim Electrical Parameters (Pre-Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

*PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

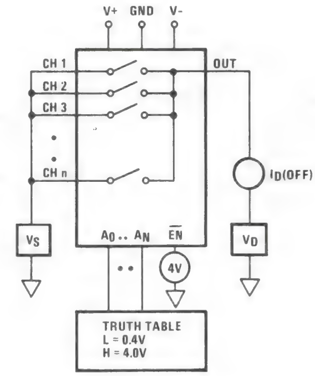
CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Test Circuits

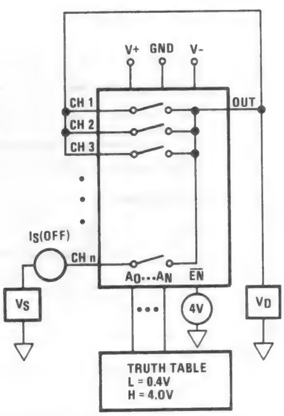
INPUT LEAKAGE CURRENT



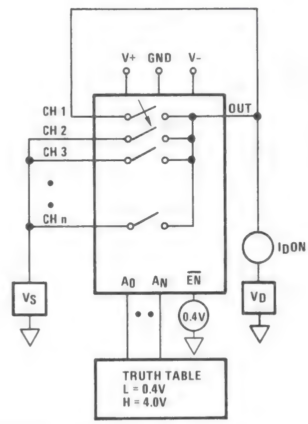
ID(OFF)



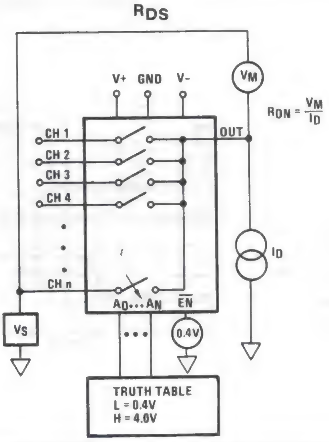
IS(OFF)



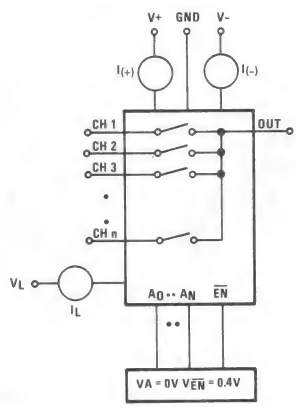
ID(ON)



RDS

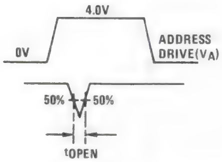


SUPPLY CURRENTS

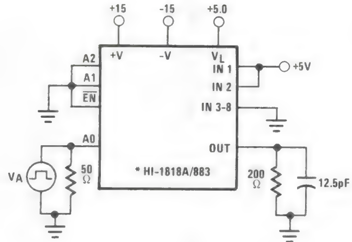


Switching Waveforms

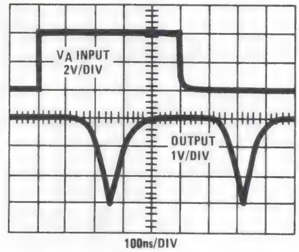
ADDRESS DRIVE



BREAK-BEFORE-MAKE DELAY (t_{OPEN})

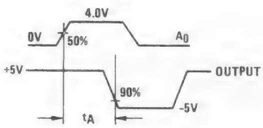


BREAK-BEFORE-MAKE DELAY (t_{OPEN})

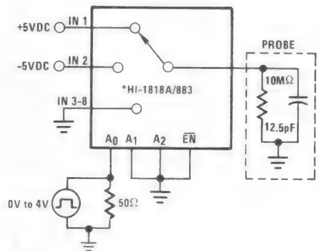


*Similar Connection for HI-1828A/883

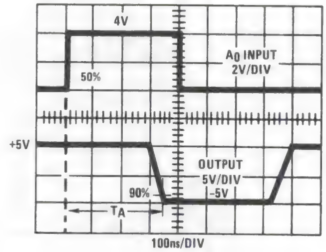
ADDRESS DRIVE



ACCESS TIME

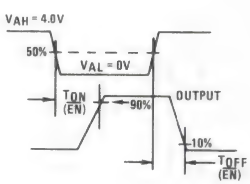


ACCESS TIME

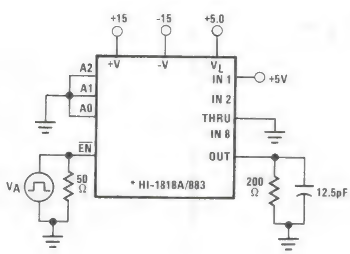


*Similar Connection for HI-1828A/883

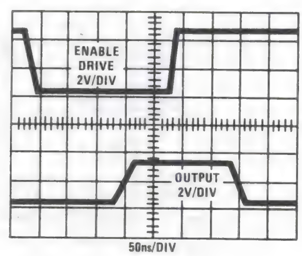
ENABLE DRIVE



ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$



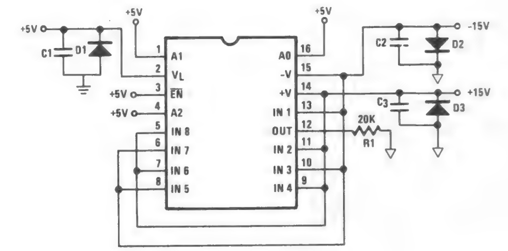
ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$



*Similar Connection for HI-1828A/883

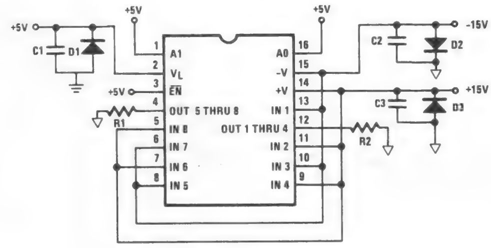
Burn-In Circuits

HI-1818A/883 CERAMIC DIP



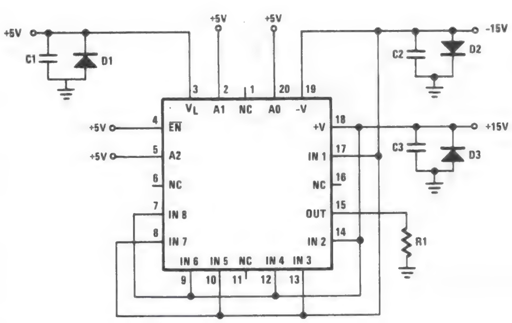
NOTES:
R_1 = 20kΩ ± 5%, 1/2 or 1/4W (per socket)
C_1, C_2, C_3 = 0.01μF (per socket) or 0.1μF (per row)
D_1, D_2, D_3 = IN4002 (or equivalent) (per board)

HI-1828A/883 CERAMIC DIP



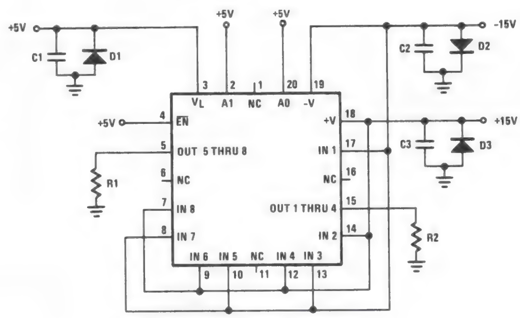
NOTES:
R_1, R_2 = 20kΩ ± 5%, 1/2 or 1/4W (per socket)
C_1, C_2, C_3 = 0.01μF (per socket) or 0.1μF (per row)
D_1, D_2, D_3 = IN4002 (or equivalent) (per board)

HI-1818A/883 CERAMIC LCC



NOTES:
R_1 = 20kΩ ± 5%, 1/4 or 1/2W (per socket)
C_1, C_2, C_3 = 0.01μF (per socket) or 0.1μF (per row)
D_1, D_2, D_3 = IN4002 (or equivalent) (per board)

HI-1828A/883 CERAMIC LCC

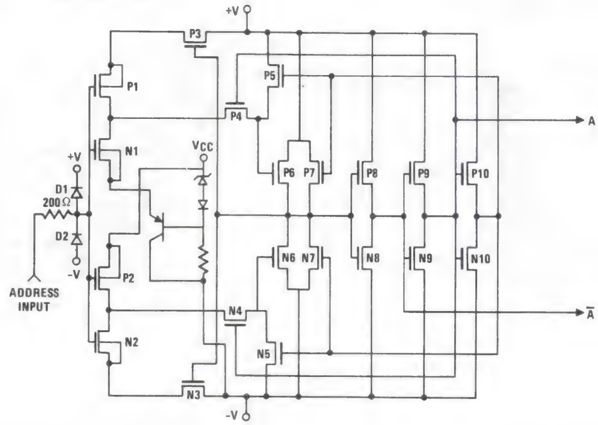


NOTES:
R_1, R_2 = 20kΩ ± 5%, 1/4 or 1/2W (per socket)
C_1, C_2, C_3 = 0.01μF (per socket) or 0.1μF (per row)
D_1, D_2, D_3 = IN4002 (or equivalent) (per board)

Schematic Diagrams

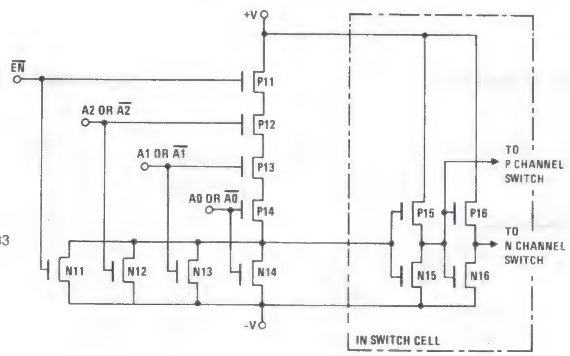
ADDRESS INPUT BUFFER

All N-Channel Bodies to V-
All P-Channel Bodies to V+
Unless Otherwise Indicated



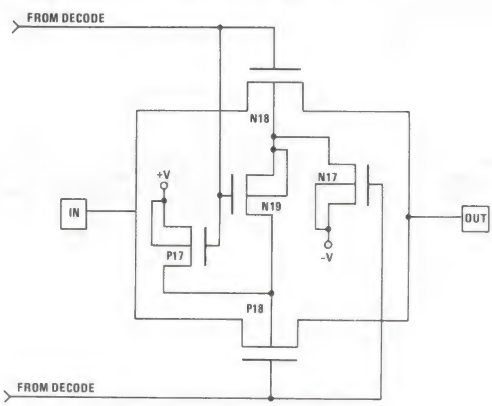
ADDRESS DECODER

All N-Channel Bodies to V-
All P-Channel Bodies to V+
A_2 or $\overline{A_2}$ not used for HI-1828A/883



MULTIPLEX SWITCH

All N- Channel Bodies to V-
All P- Channel Bodies to V+
Unless Otherwise Indicated



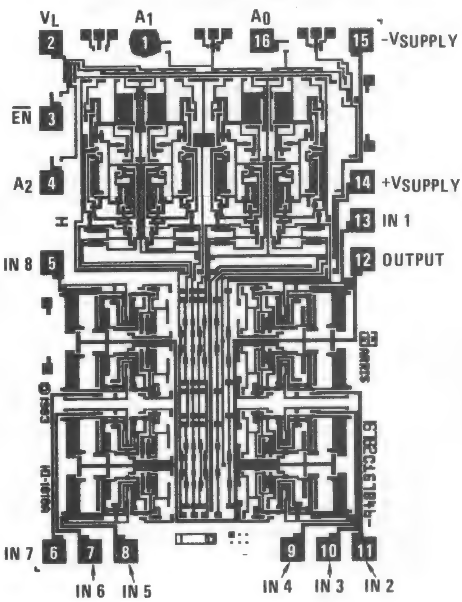
Die Characteristics

DIE DIMENSIONS: 67.7 x 103.5 x 19 mil
METALLIZATION
Type: Al
Thickness: 16kÅ ± 2kÅ
GLASSIVATION
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ
WORST CASE CURRENT DENSITY: 1.43×10^5 A/cm^2

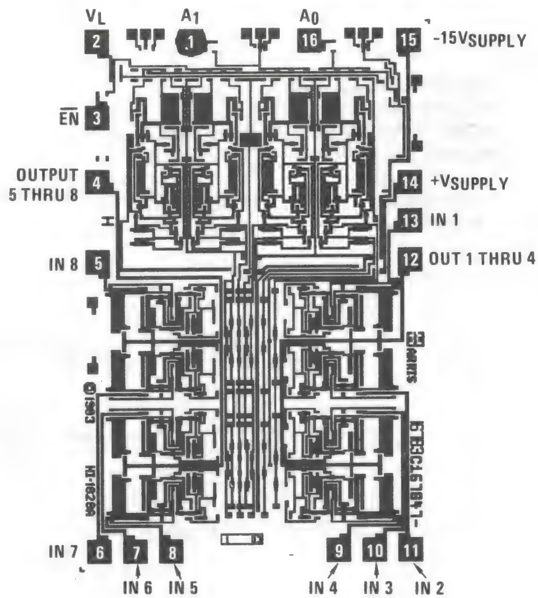
TRANSISTOR COUNT:
HI-1818A/883 210
HI-1828A/883 210
PROCESS: CMOS-DI
DIE ATTACH
Material: Gold Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

Metallization Mask Layout

HI-1818A/883



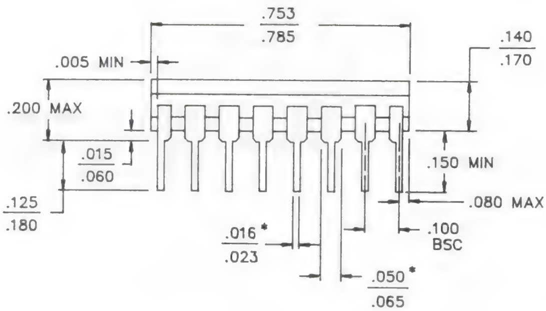
HI-1828A/883

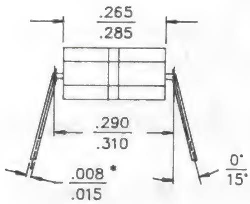


NOTE: Pad Numbers Correspond to DIP Pin Numbers Only

Packaging†

16 PIN CERAMIC DIP



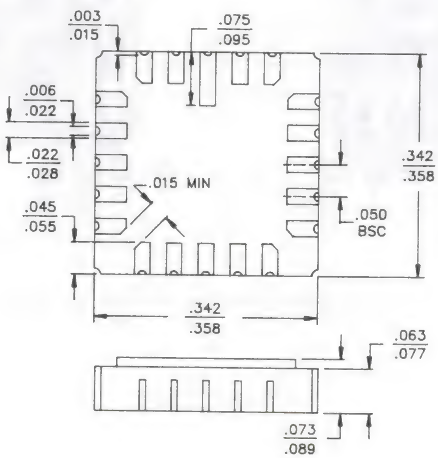


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-2

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in inches.

† MIL-M-38510 Compliant Materials, Finishes & Dimensions.

HARRIS

HI-1818A
HI-1828A

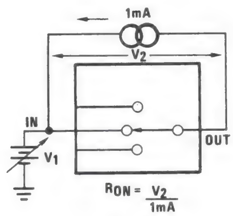
DESIGN INFORMATION

Low Resistance Single 8/Differential 4 Channel CMOS Analog Multiplexers

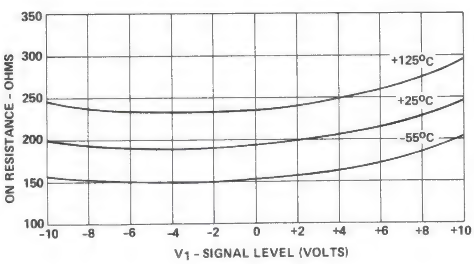
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics

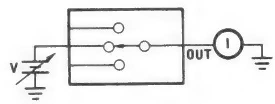
ON RESISTANCE vs. ANALOG SIGNAL LEVEL



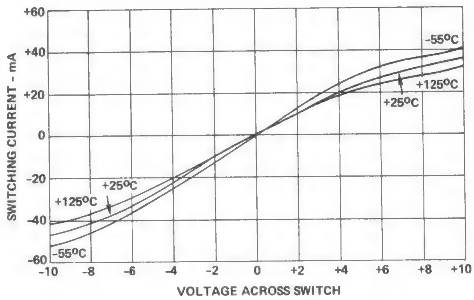
Test Circuit



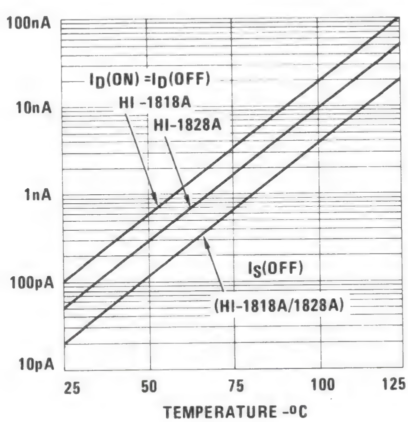
ON CHANNEL CURRENT vs. VOLTAGE



Test Circuit



LEAKAGE CURRENT vs. TEMPERATURE



5

CMOS ANALOG MULTIPLEXERS

ANALOG

Data Conversion Products

6

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

HARRIS

HI-562A/883

12-Bit High Speed Monolithic Digital-to-Analog Converter

July 1988

Features

- **This Circuit Is Processed In Accordance to Mil-Std-883 and Is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- Output Current ....2mA, F.S.
- Monolithic Construction
- Extremely Fast Settling ....600ns to 0.01% (Max)
- Low Gain Drift ....±10ppm/°C (Max)
- Linearity, +25°C Maximum ....±1/4 LSB
- Designed for Minimum Glitches
- Monotonic Over Temperature

Applications

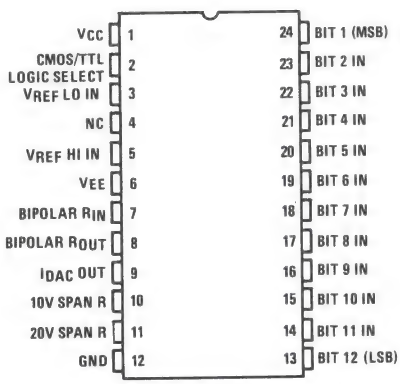
- CRT Display Generation
- High Speed A/D Converters
- Video Signal Reconstruction
- Waveform Synthesizers
- High Speed Data Acquisition
- High Reliability Applications
- Precision Instruments

Description

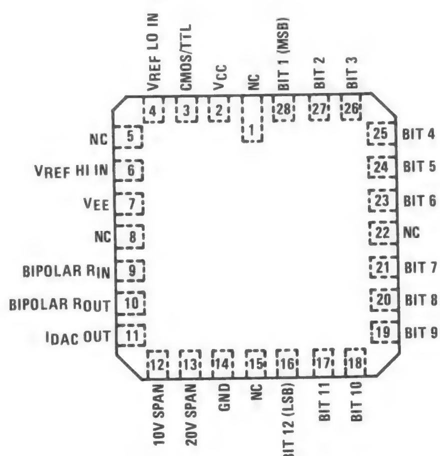
The Harris HI-562A/883 is the first monolithic digital-to-analog converter to combine both high speed performance and 12-bit accuracy on the same chip. The HI-562A/883's fast output current settling of 600ns (Max) to ±0.01% is achieved using dielectric isolation processing to reduce internal parasitics for fast rise and fall times during switching. Output glitches are minimized in the HI-562A/883 by incorporating equally weighted current sources switched into an R-2R ladder network for symmetrical turn-ON and turn-OFF switching times. This creates, within the chip, a very uniform and constant thermal distribution for excellent linearity and also completely eliminates thermal transients during switching. High stability thin film resistor processing together with laser trimming provide the HI-562A/883 with guaranteed 12-bit linearity to within ±1/4 LSB maximum at +25°C. The HI-562A/883 is recommended as a replacement for higher cost hybrid and modular units for increased reliability and accuracy in applications such as CRT displays, precision instruments and data acquisition systems requiring throughput rates as high as 2.86MHz for full range transitions. Its small size makes it an ideal choice as the heart of high speed A/D converter designs or as a building block in high speed or high resolution industrial process control systems. The HI-562A/883 is also ideally suited for aircraft and space instrumentation where operation over a wide temperature range (-55°C to +125°C) is required.

Pinouts

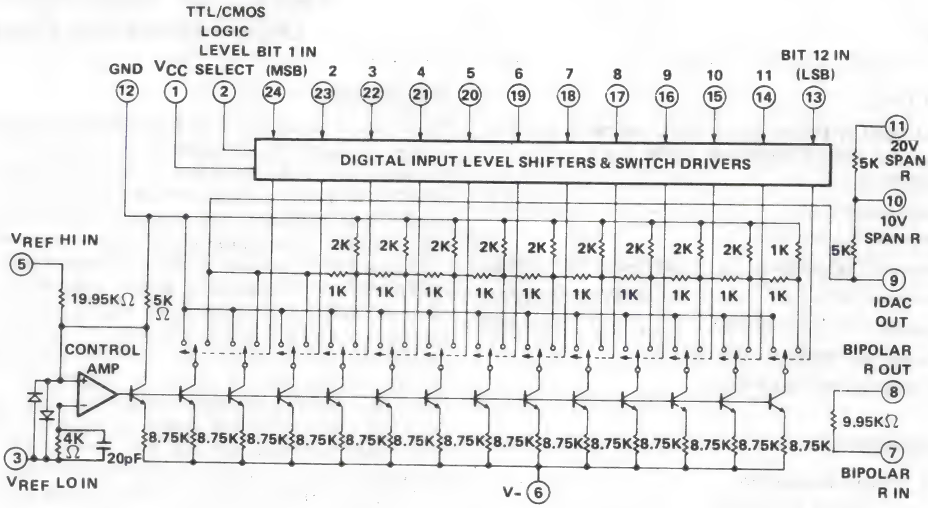
HI1-562A/883 (CERAMIC SIDEBRAZE DIP)
TOP VIEW



HI4-562A/883 (CERAMIC LCC)
TOP VIEW



Functional Diagram



Pin Numbers Correspond to DIP Package Only.

Absolute Maximum Ratings (NOTE 1)

Voltages Referred to Ground
Power Supply Inputs
V_{CC} .... +20V
V_{EE} .... -20V
Reference Inputs
V_{REF} (High) .... ±16.5V
Digital Inputs
Bits 1-12 (TTL) .... -1V to +7.5V
Bits 1-12 (CMOS) .... -1V to V_{CC}
CMOS/TTL Logic Select .... -1V to +16.5V
Pins 7, 8, 10, 11 (DIP Package) .... V_{EE} to V_{CC}
I_{DAC} Out .... -5V to V_{CC}
Lead Temperature (Soldering 10sec) .... +275°C
Storage Temperature Range .... -65°C to +150°C
Junction Temperature .... +175°C

Thermal Information

Thermal Resistance, Junction-to-Case (θ_{jc})
Ceramic DIP Package .... 15°C/W
Ceramic LCC Package .... 40°CW
Thermal Resistance Junction-to-Ambient (θ_{ja})
Ceramic DIP Package .... 50°C/W
Ceramic LCC Package .... 81°C/W
Power Dissipation (@ +75°C)
Ceramic DIP Package 2000mW
Ceramic LCC Package 1235mW
Power Dissipation Derating Factor (Above +75°C)
Ceramic DIP Package .... 20mW/°C
Ceramic LCC Package .... 12.35mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltages
V_{CC} .... +5V to +15V
V_{EE} .... -15V
Reference Input Voltage .... +10.0V
Digital Inputs (TTL)
V_{IL}, Logic Low .... 0V to 0.8V
V_{IH}, Logic High .... 2.0V to 5V

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at $+V_{CC}$ = +5V, $-V_{EE}$ = -15V, V_{REF} HI IN = +10.0V, V_{REF} LO IN = GND, CMOS/TTL = GND, Unless Otherwise Specified

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current From V_{CC}	I_{CC}	For all Bits ON, and all Bits OFF V_{IH} = 2.0V, V_{IL} = 0.8V (Note 4)	1	+25°C		15.0	mA
			2, 3	+125°C, -55°C		17.0	mA
Supply Current From V_{EE}	I_{EE}	For all Bits ON, and all Bits OFF V_{IH} = 2.0V, V_{IL} = 0.8V (Note 4)	1	+25°C		-23.0	mA
			2, 3	+125°C, -55°C		-25.0	mA
Power Dissipation	P_d	All Bits ON V_{IH} = 2.0V (Note 4)	1	+25°C	—	420	mW
			2, 3	+125°C, -55°C	—	500	mW
Digital Input High Current	I_{IH}	Each Bit Tested Separately, Bit Under Test, V_{IH} = 5V, all other Bits V_{IL} = 0.8V	1	+25°C	-100	100	nA
			2, 3	+125°C, -55°C	-500	500	nA
Digital Input Low Current	I_{IL}	Each Bit Tested Separately, Bit Under Test, V_{IH} = 0V, all other Bits V_{IL} = 0.8V	1	+25°C	-50	1.0	μA
			2, 3	+125°C, -55°C	-100	1.0	μA
Unipolar Offset Error	V_{OS}	All Bits OFF V_{IL} = 0.8V (Note 5)	1	+25°C	-0.05	0.05	% FSR
			2, 3	+125°C, -55°C	-0.7	0.07	% FSR
Unipolar Gain Error	A_E	All Bits ON V_{IH} = 2.0V (Note 5)	1	+25°C	-0.25	0.25	% FSR
			2, 3	+125°C, -55°C	-0.35	0.35	% FSR
Power Supply Sensitivity From V_{CC}	$+P_{SSI}$	Unipolar Mode, all Bits ON, V_{IH} = 2.0V V_{CC} from 4.5 to 5.5V	1	+25°C	-3.5	3.5	ppm of FSR / % V_{PS}
			2, 3	+125°C, -55°C	-14.0	14.0	
Power Supply Sensitivity From V_{EE}	$-P_{SSI}$	Unipolar Mode, all Bits ON, V_{IH} = 2.0V V_{EE} from -13.5 to-16.5V	1	+25°C	-7.5	7.5	ppm of FSR / % V_{PS}
			2, 3	+125°C, -55°C	-30	30	
Output Current Unipolar	$I_{OUT\ 1}$	All Bits ON V_{IH} = 2.0V, Pin 9 to Ground	1	+25°C	-2.4	-1.6	mA
Output Current Bipolar	$I_{OUT\ 2}$	All Bits ON, V_{IH} = 2V Pin 7 @ 10V, Pin 8 to Pin 9, Pin 9 to Ground	1	+25°C	-1.2	-0.8	mA
Bipolar Offset Error	BP_{OE}	All Bits OFF, V_{IL} = 0.8V ±10V Range (Note 5)	1	+25°C	-.25	.25	%FSR
			2, 3	+125°C, -55°C	-0.29	0.29	%FSR
Bipolar Zero Error	BP_{ZE}	MSB on V_{IH} = 2.0V, all other Bits OFF V_{IL} = 0.8V, ±10V Range	1	+25°C	-0.25	0.25	% FSR
			2, 3	+125°C, -55°C	-0.29	0.29	% FSR
Bipolar Gain Error	BP_{AE}	All Bits ON V_{IH} = 2.0V ±10V Range (Note 5)	1	+25°C	-0.25	0.25	% FSR
			2, 3	+125°C, -55°C	-0.35	0.35	% FSR

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Devices Tested at $+V_{CC}$ = +5V, $-V_{EE}$ = -15V, V_{REF} HI IN = +10.0V, V_{REF} LO IN = GND, CMOS/TTL = GND, Unless Otherwise Specified

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Integral Linearity Error	L_E	Unipolar 10V Range Reference Chart C for Codes Tested (Note 6)	1	+25°C	-0.25	0.25	LSB
			2, 3	+125°C, -55°C	-1.0	1.0	LSB
Differential Linearity Error	DL_E	Unipolar 10V Range Reference Chart D for Codes Tested (Notes 6, 10)	1	+25°C	-0.25	0.25	LSB
			2, 3	+125°C, -55°C	-1.0	1.0	LSB
Unipolar Offset Drift	$\frac{dV_{OS}}{dT}$	(Note 2)	1, 2	+25°C, +125°C	-2.0	2.0	ppm of FSR/°C
			1, 3	+25°C, -55°C	-2.0	2.0	ppm of FSR/°C
Unipolar Gain Drift	$\frac{dA_E}{dT}$	(Note 2)	1, 2	+25°C, +125°C	-10	10	ppm of FSR/°C
			1, 3	+25°C, -55°C	-10	10	
Bipolar Offset Drift	$\frac{dBP_{OE}}{dT}$	(Note 2)	1, 2	+25°C, +125°C	-4	4	ppm of FSR/°C
			1, 3	+25°C, -55°C	-4	4	
Bipolar Gain Drift	$\frac{dBP_{AE}}{dT}$	(Note 2)	1, 2	+25°C, +125°C	-10	10	ppm of FSR/°C
			1, 3	+25°C, -55°C	-10	10	

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Characterized at $+V_{CC}$ = +5V, $-V_{EE}$ = -15V, V_{REF} HI IN = +10.0V, V_{REF} LO IN = GND, CMOS/TTL = GND, Unless Otherwise Specified.

A.C. PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Settling Time	t_S	All Bits OFF to ON and all Bits ON to OFF, 10V Unipolar Mode to 0.01% Figures 2 and 3, (Note 2) V_{IL} = 0.8V, V_{IH} = 3.5V, RL = 50Ω	11	+25°C	—	600	ns

NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. See Definitions.
3. FSR is "Full Scale Range" and is 20V for ±10V range, 10V for ±5V range, etc., or 2mA (±20%) for current output.
4. After 30 seconds warm-up.
5. Errors are adjustable to zero using R_1 and R_2 potentiometers. (See Application Information Figure 5).
6. For accuracy measurements, the reference DAC shall be full scale adjusted to match the full scale gain less the zero scale offset of the device under test. All switches are in position 2. The 16-bit reference DAC will supply the ideal voltage for the code under test to pin 10 (10V span) of the DUT. V_O will represent the difference between the ideal current for the code under test (provided by the 16-bit reference DAC through the 10V span resistor) and the actual DUT current for that code. The reference DAC is used to determine the output voltage value for a 12-bit LSB (measured at V_O) with the DUT at zero scale. This value is the scaling factor used for accuracy error calculations.
7. **For unipolar full scale and offset measurements, all switches are in position 2. The ideal voltages (9.99758 for full scale, and 0V for offset) are applied to pin 10 (10V span) of the DUT via the 16-bit reference DAC. The transresistance amplifier is scaled such that 1V measured at V_O corresponds to 0.1% of the full scale range.**

   For Full Scale V_O = Scaling Factor x $\left[\frac{10 \times 4095/4096}{R_{10V}\ \text{Span}} - I_{FULL}\ \text{Scale (OUT)}\right]$
8. For bipolar full scale, zero, and offset measurements, switch S_1 is in position 2, switches S_2 and S_3 are in position 1. The ideal voltages 9.99512, 0, and -10 are applied to pin 11 (20V span) of the DUT via the 16-bit reference DAC. **The transresistance amplifier is scaled such** that 1V measured at V_O corresponds to 0.1% of the full scale range.
9. For power supply rejection ratio tests, all switches are in position 2. An ideal voltage of 9.99756V is applied to pin 10 of the DUT via the 16-bit reference DAC. Voltages at the output of the error amplifier are measured under the conditions noted in Chart A.
10. Differential nonlinearity tests are performed twice, the first sequence is performed by applying the "From Code" immediately prior to its associatied "To Code". The second sequence is performed by applying the "To Code" immediately prior to its associated "From Code".
11. **The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.**

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLE 1)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3
Group A Test Rquirements	1, 2, 3
Group C & D Endpoints	1

*PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

Test Circuits

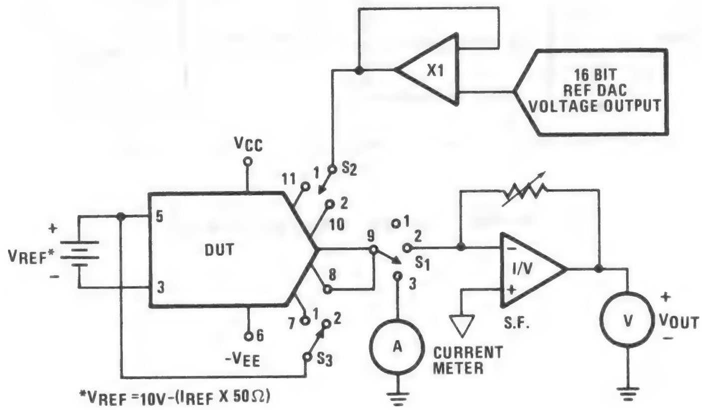


FIGURE 1. TEST CIRCUIT

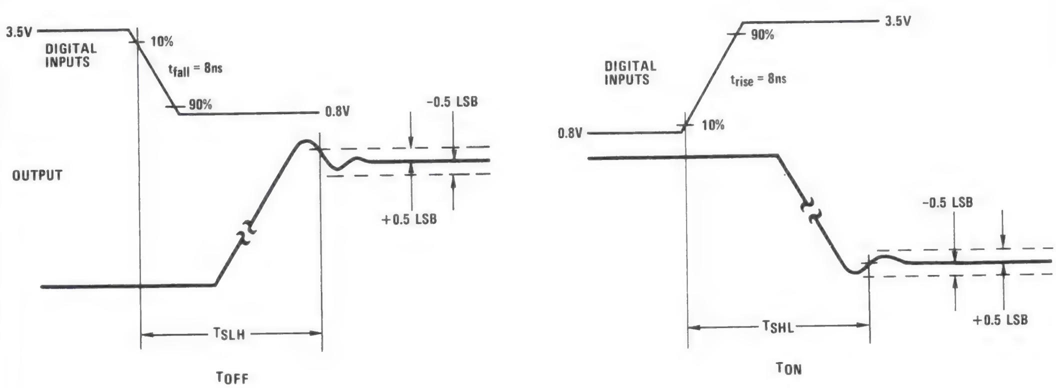


FIGURE 2. SETTLING TIME WAVEFORMS

Settling Time Circuit

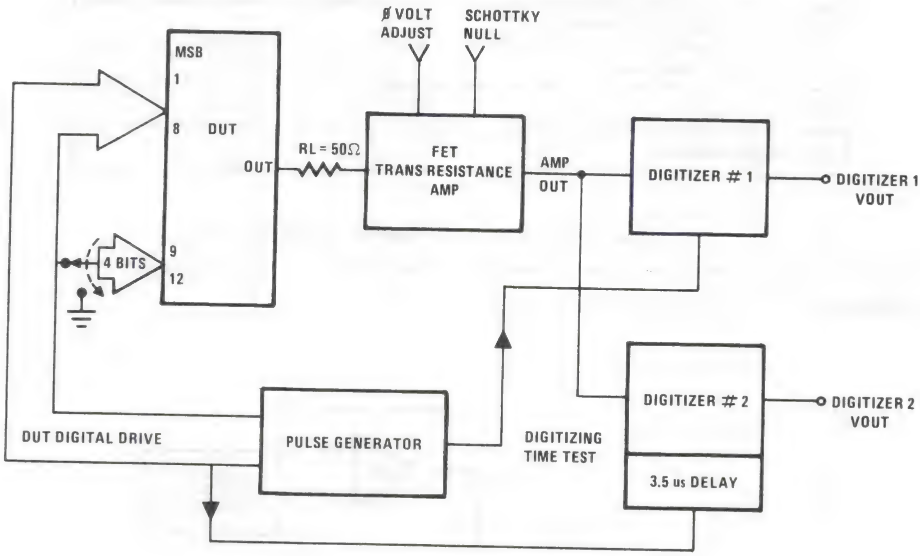


FIGURE 3. DAC SETTLING TIME FIXTURE

Test Conditions V_{REF} HI = +10.0V, TTL/CMOS = GND, Unless Otherwise Specified, All Pin Numbers Refer to DIP Package

CHART A. TEST CONDITIONS

TEST	SYMBOL	CONDITIONS	PIN 1	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	PIN 11	SWITCH POSITIONS			MEASURE		TEMP	CALCULATIONS
			V_{CC}	V_{EE}	B.P. R_{IN}	B.P. R_{OUT}	I_{OUT}	10V SPAN	20V SPAN	S_1	S_2	S_3	VALUE	UNITS		
Supply Current From V_{CC}	I_{CC}	Two Tests Performed All Bits ON, V_{IH} = 2.0V All Bits OFF, V_{IL} = 0.8V	5V	-15V	O.C.	Pin 9	O.C.	0V	O.C.	1	2	2	—	mA	+25°C +125°C -55°C	
Supply Current From V_{EE}	I_{EE}	Two Tests Performed All Bits ON, V_{IH} = 2.0V All Bits OFF, V_{IL} = 0.8V	5V	-15V	O.C.	Pin 9	O.C.	0V	O.C.	1	2	2	—	mA	+25°C +125°C -55°C	
Digital Input High Current (TTL)	I_{IH}	Each Bit Tested Separately Bit Under Test, V_{IH} = 5.0V All Other Bits, V_{IL} = 0.8V	5V	-15V	O.C.	Pin 9	O.C.	0V	O.C.	1	2	2	—	nA	+25°C +125°C -55°C	
Digital Input Low Current (TTL)	I_{IL}	Each Bit Tested Separately Bit Under Test, V_{IH} = 0V All Other Bits, V_{IL} = 0.8V	5V	-15V	O.C.	Pin 9	O.C.	0V	O.C.	1	2	2	—	μA	+25°C +125°C -55°C	
Unipolar Offset	V_{OS}	All Bits OFF, V_{IL} = 0.8V (Note 7) G = 0.1% FSR/V	5V	-15V	O.C.	Pin 9	—	—	O.C.	2	2	2	E_{1R} E_{1H} E_{1L}	V	+25°C +125°C -55°C	$E_1 \cdot G = \%\,FSR$
Unipolar Gain Error	A_E	All Bits ON, V_{IH} = 2.0V (Note 7) G = 0.1% FSR/V	5V	-15V	O.C.	Pin 9	—	—	O.C.	2	2	2	E_{2R} E_{2H} E_{2L}	V	+25°C +125°C -55°C	$[E_2 - E_1] \cdot G = \%\,FSR$
Power Supply Sensitivity From V_{CC}	$+P_{SS}$	All Bits ON, V_{IH} = 2.0V Unipolar, 10V Range (Note 9) G = 0.1% FSR/V	4.5V	-15V	O.C.	Pin 9	—	—	O.C.	2	2	2	E_{3AR} E_{3AH} E_{3AL}	V	+25°C +125°C -55°C	$\left[\frac{E_{3A} - E_{3B}}{20\% \cdot 100}\right] \cdot G10^6 = \frac{ppm\ FSR}{\%\ V_{CC}}$
			5.5V	-15V	O.C.	Pin 9	—	—	O.C.	2	2	2	E_{3BR} E_{3BH} E_{3BL}	V	+25°C +125°C -55°C	
Power Supply Sensitivity From V_{EE}	$-P_{SS}$	All Bits ON, V_{IH} = 2.0V Unipolar, 10V Range (Note 9) G = 0.1% FSR/V	5V	-13.5V	O.C.	Pin 9	—	—	O.C.	2	2	2	E_{4AR} E_{4AH} E_{4AL}	V	+25°C +125°C -55°C	$\left[\frac{E_{4A} - E_{4B}}{20\% \cdot 100}\right] \cdot G10^6 = \frac{ppm\ FSR}{\%\ V_{EE}}$
			5V	-16.5V	O.C.	Pin 9	—	—	O.C.	2	2	2	E_{4BR} E_{4BH} E_{4BL}	V	+25°C +125°C -55°C	
Output Current Unipolar Mode	I_{OUT1}	All Bits ON, V_{IH} = 2.0V Unipolar Mode	5V	-15V	O.C.	Pin 9	0V	0V	O.C.	3	2	2	—	mA	+25°C +125°C -55°C	
Output Current Bipolar Mode	I_{OUT2}	All Bits ON, V_{IL} = 2.0V Bipolar Mode	5V	-15V	10V	Pin 9	0V	O.C.	0V	3	1	1	—	mA	+25°C +125°C -55°C	
Bipolar Offset Error	BP_{OE}	All Bits OFF, V_{IL} = 0.8V Bipolar ±10V Range (Note 8) G = 0.1% FSR/V	5V	-15V	10V	Pin 9	—	O.C.	—	2	1	1	E_{5R} E_{5H} E_{5L}	V	+25°C +125°C -55°C	$E_5 \cdot G = \%\,FSR$
Bipolar Zero Error	BP_{ZE}	MSB ON, V_{IH} = 2.0V All Other Bits OFF, V_{IL} = 0.8V (Note 8) G = 0.1% FSR/V	5V	-15V	10V	Pin 9	—	O.C.	—	2	1	1	E_{6R} E_{6H} E_{6L}	V	+25°C +125°C -55°C	$E_6 \cdot G = \%\,FSR$
Bipolar Gain Error	BP_{AE}	All Bits ON, V_{IH} = 2.0V Bipolar ±10V Range (Note 8) G = 0.1% FSR/V	5V	-15V	10V	Pin 9	—	O.C.	—	2	1	1	E_{7R} E_{7H} E_{7L}	V	+25°C +125°C -55°C	$[E_7 - E_5] \cdot G = \%\,FSR$
Integral Linearity Error	L_E	Unipolar 10V Range V_{IL} = 0.8V, V_{IH} = 2.0V Chart C (Note 6) G = 1LSB/V	5V	-15V	O.C.	Pin 9	—	—	O.C.	2	2	2	L_{ER} L_{EH} L_{EL}	V	+25°C +125°C -55°C	$L_E \cdot G = LSB$
Differential Linearity Error	DL_E	Unipolar 10V Range V_{IL} = 0.8V, V_{IH} = 2.0V Chart D (Notes 6, 10) G = 1LSB/V	5V	-15V	O.C.	Pin 9	—	—	O.C.	2	2	2	D_{LER} D_{LEH} D_{LEL}	V	+25°C +125°C -55°C	$D_{LE} \cdot G = LSB$

CHART B.

TEST	SYMBOL	CONDITIONS	TEMPERATURE	CALCULATIONS
Unipolar Offset Drift	$\frac{dV_{OS}}{dT}$	Calculations Made From Tests Previously Defined in this Table	+25°C +125°C	$\left[\frac{E_{1H} - E_{1R}}{10^4}\right] \cdot G \cdot 10^6 = \frac{\text{ppm of FSR}}{^oC}$
			+25°C -55°C	$\left[\frac{E_{1R} - E_{1L}}{0.8 \times 10^4}\right] \cdot G \cdot 10^6 = \frac{\text{ppm of FSR}}{^oC}$
Unipolar Gain Drift	$\frac{dA_E}{dT}$	Calculations Made From Tests Previously Defined in this Table	+25°C +125°C	$\left[\frac{(E_{2H} - E_{1H}) - (E_{2R} - E_{1R})}{10^4}\right] \cdot G \cdot 10^6 = \frac{\text{ppm of FSR}}{^oC}$
			+25°C -55°C	$\left[\frac{(E_{2R} - E_{1R}) - (E_{2L} - E_{1L})}{0.8 \cdot 10^4}\right] \cdot G \cdot 10^6 = \frac{\text{ppm of FSR}}{^oC}$
Bipolar Offset Drift	$\frac{dBP_{OE}}{dT}$	Calculations Made From Tests Previously Defined in this Table	+25°C +125°C	$\left[\frac{E_{5H} - E_{5R}}{10^4}\right] \cdot G \cdot 10^6 = \frac{\text{ppm of FSR}}{^oC}$
			+25°C -55°C	$\left[\frac{E_{5R} - E_{5L}}{0.8 \times 10^4}\right] \cdot G \cdot 10^6 = \frac{\text{ppm of FSR}}{^oC}$
Bipolar Gain Drift	$\frac{dBP_{AE}}{dT}$	Calculations Made From Tests Previously Defined in this Table	+25°C +125°C	$\left[\frac{(E_{7H} - E_{5H}) - (E_{7R} - E_{5R})}{10^4}\right] \cdot G \cdot 10^6 = \frac{\text{ppm of FSR}}{^oC}$
			+25°C -55°C	$\left[\frac{(E_{7R} - E_{5R}) - (E_{7L} - E_{5L})}{0.8 \times 10^4}\right] \cdot G \cdot 10^6 = \frac{\text{ppm of FSR}}{^oC}$

CHART C.

DIGITAL CODE MSB — LSB	NOTES
0 0 0 0 0 0 0 0 0 0 0 1	
0 0 0 0 0 0 0 0 0 0 1 0	
0 0 0 0 0 0 0 0 0 1 0 0	
0 0 0 0 0 0 0 0 1 0 0 0	
0 0 0 0 0 0 0 1 0 0 0 0	
0 0 0 0 0 0 1 0 0 0 0 0	
0 0 0 0 0 1 0 0 0 0 0 0	
0 0 0 0 1 0 0 0 0 0 0 0	
0 0 0 1 0 0 0 0 0 0 0 0	
0 0 1 0 0 0 0 0 0 0 0 0	
0 1 0 0 0 0 0 0 0 0 0 0	
1 0 0 0 0 0 0 0 0 0 0 0	
0 1 1 0 0 0 0 0 0 0 0 0	
1 0 1 0 0 0 0 0 0 0 0 0	
1 1 0 0 0 0 0 0 0 0 0 0	
1 1 1 0 0 0 0 0 0 0 0 0	
X X X X X X X X X X X X	1
X X X X X X X X X X X X	2

CHART D.

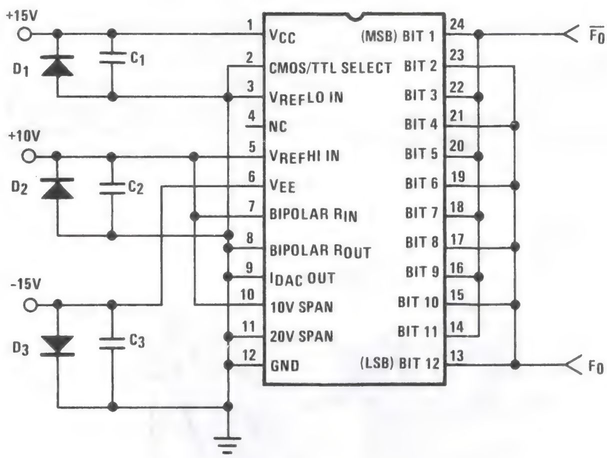
DIGITAL CODE FROM CODE	DIGITAL CODE TO CODE
0 0 0 0 0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 0 0 0 1 0
0 0 0 0 0 0 0 0 0 0 1 1	0 0 0 0 0 0 0 0 0 1 0 0
0 0 0 0 0 0 0 0 0 1 1 1	0 0 0 0 0 0 0 0 1 0 0 0
0 0 0 0 0 0 0 0 1 1 1 1	0 0 0 0 0 0 0 1 0 0 0 0
0 0 0 0 0 0 0 1 1 1 1 1	0 0 0 0 0 0 1 0 0 0 0 0
0 0 0 0 0 0 1 1 1 1 1 1	0 0 0 0 0 1 0 0 0 0 0 0
0 0 0 0 0 1 1 1 1 1 1 1	0 0 0 0 1 0 0 0 0 0 0 0
0 0 0 0 1 1 1 1 1 1 1 1	0 0 0 1 0 0 0 0 0 0 0 0
0 0 0 1 1 1 1 1 1 1 1 1	0 0 1 0 0 0 0 0 0 0 0 0
0 0 1 1 1 1 1 1 1 1 1 1	0 1 0 0 0 0 0 0 0 0 0 0
0 1 1 1 1 1 1 1 1 1 1 1	1 0 0 0 0 0 0 0 0 0 0 0

NOTES:

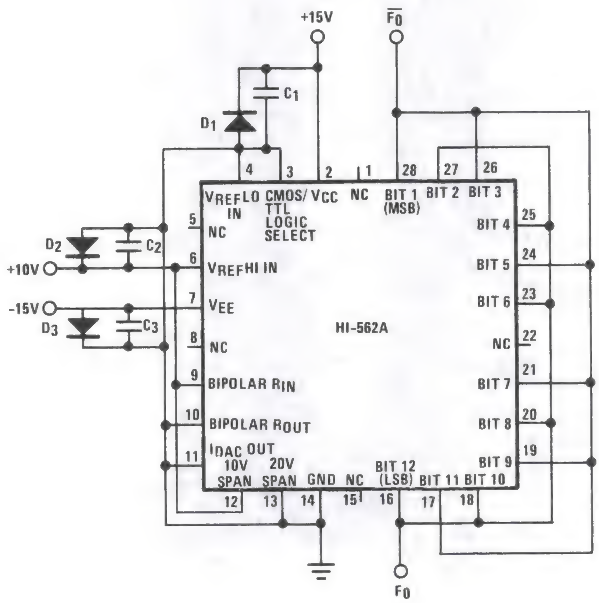
1. X is a logic 1 (V_{IH} = 2.0V) if the linearity error for that bit was measured as a positive error. X is a logic 0 (V_{IL} = 0.8V) if the linearity error for that bit was measured as a negative error.
2. X is a logic 1 (V_{IH} = 2.0V) if the linearity error for that bit was measured as a negative error. X is a logic 0 (V_{IL} = 0.8V) if the linearity error for that bit was measured as a positive error.

Burn-In Circuits

HI-562A/883 CERAMIC SIDEBRAZED DIP



HI-562A/883 CERAMIC LCC



NOTES:

$C_1 = C_2 = C_3 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row)

$D_1 = D_2 = D_3$ = IN4002 or equivalent (per board)

F_0 = 100KHz; TTL Levels 50% Duty Cycle

Die Characteristics

DIE DIMENSIONS:
103 x 209 x 19 mils

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$4.59 \times 10^5 A/cm^2$
This device meets Glassivation Integrity Test requirement per Mil-Std-883 Method 2021 and Mil-M-38510 paragraph 3.5.5.4.

GLASSIVATION:
Type: Silox
Thickness: 14kÅ ± 2kÅ

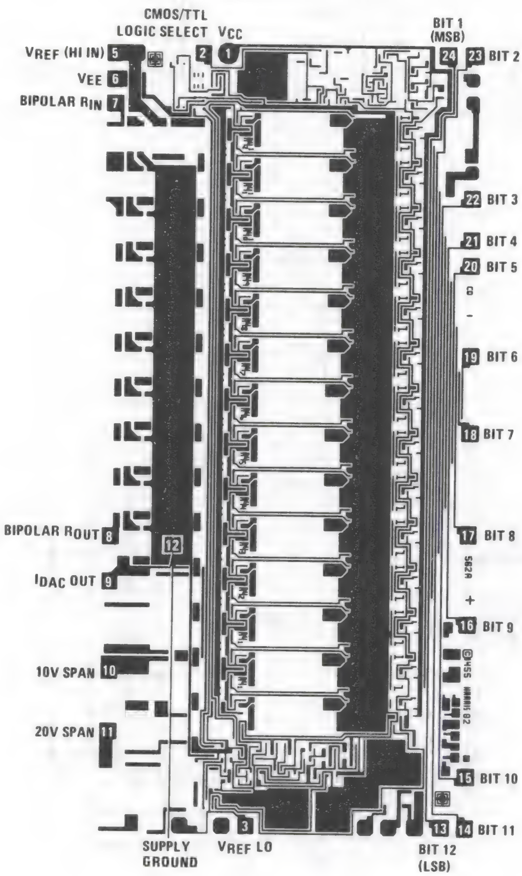
TRANSISTOR COUNT: 150

PROCESS: BIPOLAR-DI

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Sidebrazed Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

Metallization Mask Layout

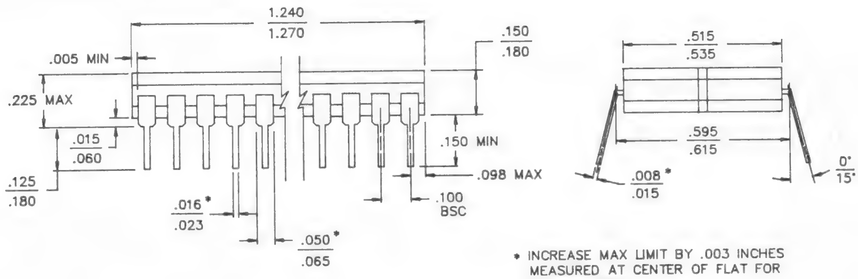
HI-562A/883



NOTE: Pin Numbers Correspond to DIP Package Only.

Packaging†

24 PIN CERAMIC DIP

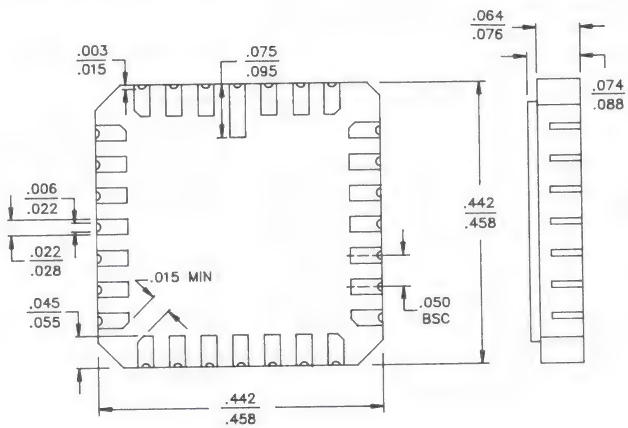


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type C
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-3

28 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type C
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-4

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HI-562A

12-Bit High Speed Monolithic Digital-to-Analog Converter

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Definitions of Specifications

Digital Inputs

The HI-562A/883 accepts digital input codes in binary format and may be user connected for any one of three binary codes: Straight Binary, Two's Complement, or Offset Binary (see Operating Instructions).

DIGITAL INPUT	ANALOG OUTPUT		
	STRAIGHT BINARY	OFFSET BINARY	TWO'S COMPLEMENT*
MSB LSB			
000 . . . 000	Zero	-FS (Full Scale)	Zero
100 . . . 000	1/2 FS	Zero	-FS
111 . . . 111	+FS - 1 LSB	+FS - 1 LSB	1/2 FS - 1 LSB
011 . . . 111	1/2 FS - 1 LSB	Zero - 1 LSB	+FS - 1 LSB

*Invert MSB with external inverter to obtain Two's Complement Coding

Accuracy

INTEGRAL NONLINEARITY—The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to "end-point linearity" for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00 . . . 0 and 11 . . . 1).

DIFFERENTIAL NONLINEARITY—The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY—The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

Settling Time

That interval between application of a digital step input, and final entry of the analog output within a specified window about the settled value. Harris Semiconductor usually specifies a unipolar 10V full scale step, to be measured from 50% of the input digital transition, and a window of ±1/2 LSB about the final value. The device output is then rated according to the worst (longest settling) case: low to high, or high to low.

Drift

GAIN DRIFT—The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per ^{o}C (ppm of FSR/^{o}C). Gain error is measured with respect to +25^{o}C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25^{o}C) and low (+25^{o}C -T_L) ranges by dividing the gain error by the respective change in temperature. The specification is the larger of the two, representing worst case drift.

OFFSET DRIFT—The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per ^{o}C (ppm of FSR/^{o}C). Offset error is measured with respect to +25^{o}C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25^{o}C) and low (+25^{o}C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

Power Supply Sensitivity

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V, +5V or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

Compliance

Compliance voltage is the maximum output range for which specified accuracy limits are guaranteed. Compliance limit implies functional operation only and makes no claims to accuracy.

Glitch

A glitch on the output of a D/A converter is a large transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011 . . . 1 to 100 . . . 0 or vice versa. For example, if turn ON is greater than turn OFF for 011 . . . 1 to 100 . . . 0, an intermediate state of 000 . . . 0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Operating Instructions

Decoupling and Grounding

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in Figure 4 should be used. Decoupling capacitors should be connected close to the HI-562A/883 (preferably to the device pins) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

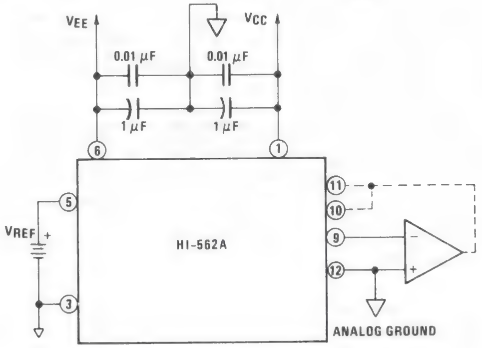


FIGURE 4.

Unipolar and Bipolar Voltage Output Connections

CONNECTIONS—Using an external resistive load, the output compliance should not exceed ±1V to maintain specified accuracy. For higher output voltages, accuracy can be maintained by using an external op amp and the internal span resistors as shown in Figure 5 and defined in Chart F for unipolar and bipolar modes.

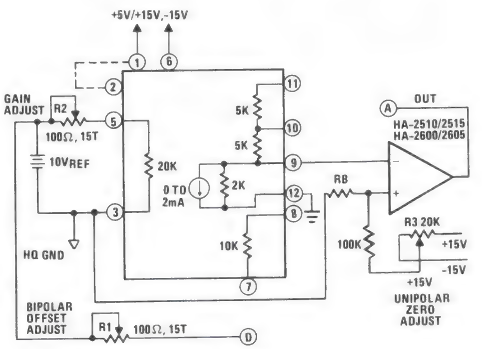


FIGURE 5.

* For TTL and DTL compatibility, connect +5V to pin 1 and tie pin 2 to pin 12.

** Bias resistor, RB, should be chosen to equalize op amp offset voltage due to bias current. Its value is calculated from the parallel combination of the current source output resistance (2K) and the op amp feedback resistor. See Chart A for values of RB.

CHART F. Pin Numbers Correspond to DIP Package Only

	OUTPUT RANGE	CONNECTIONS PIN 7 TO	PIN 8 TO	PIN 10 TO	PIN 11 TO	BIAS (R_B) RESISTOR
Unipolar Mode	0 to +10V	N.C.	N.C.	A	N.C.	1.43K
	0 to +5V	N.C.	N.C.	A	9	1.11K
Bipolar Mode	±10V	D	9	N.C.	A	760Ω
	±5V	D	9	A	N.C.	840Ω
	±2.5V	D	9	A	9	766Ω

External Gain and Zero Calibration (See Figure 5)

The input reference resistor (20K nominal) and bipolar offset resistors shown in Figure 5 are both intentionally set low by 50Ω to allow the user to externally trim-out initial errors to a very high degree of precision. The adjustments are made in the voltage output mode using an external op amp as current-to-voltage converter and the HI-562A/883 internal scaling resistors as feedback elements for optimum accuracy and temperature coefficient. For best accuracy over temperature, select an op amp that has good front-end temperature coefficients such as the HA-2600/883 with offset voltage and offset current tempco's of 5 µV/°C in 1nA/°C, respectively. For high speed voltage mode applications where fast settling is required, the HA-2510/883 is recommended for better than 1.5µs settling to 0.01%. Using either one, potentiometer R_3 conveniently nulls unipolar offset plus op amp offset in one operation (for HA-2510/883 and HA-2600/883 use R_3 = 20K and 100K, respectively). For bipolar mode operation, R_3 should be used to null op amp offset to optimize its tempco (i.e., short 9 to A and adjust R_3 for zero before calibration in bipolar mode). The gain and bipolar offset adjustment range using 100Ω potentiometers is ±0.25% FSR. If desired, the potentiometers can be relpaced with fixed 50µ (1%) resistors resulting in an initial gain and bipolar offset accuracy of typically ±1/2 LBS.

UNIPOLAR CALIBRATION

Step 1: Unipolar Offset
- Turn all bits OFF
- Adjut R3 for zero volts output

Step 2: Gain
- Turn all bits ON
- Adjut R2 for an output of FS - 1 LSB

  That is, adjust for:

  9.9976V for 0V to +10V range

  4.9988V for 0V to +5V range

BIPOLAR CALIBRATION

Step 1: Bipolar Offset
- Turn all bits OFF
- Adjust R1 for an output of:

  -10V for ±10V range

  -5V for ±5V range

  -2.5V for ±2.5V range

Step 2: Gain
- Turn bit 1 (MSB) ON; all other bits OFF
- Adjust R2 for zero volts output

HARRIS

HI-565A/883

High Speed, Monolithic Digital-to-Analog Converter With Reference

January 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- DAC and Reference on a Single Chip
- Pin Compatible With AD565A
- Very High Speed: Settles to 1/2 LSB in 500ns Max
- Monotonicity Guaranteed Over Temperature
- 1/2 LSB Max Nonlinearity Guaranteed Over Temp
- Low Gain Drift (Max, DAC Plus Reference) .. 25ppm/°C
- Low Power Dissipation (Max Over Temp) 425mW

Applications

- High Speed A/D Converters
- Precision Instrumentation
- CRT Display Generation
- Signal Reconstruction

Description

The HI-565A/883 is a fast, 12 bit current output, digital to analog converter. The monolithic chip includes a precision voltage reference, thin-film R-2R ladder, reference control amplifier and twelve high-speed bipolar current switches.

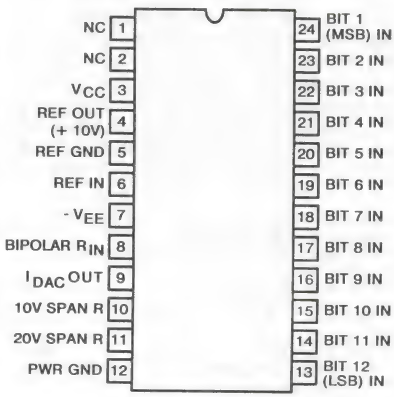
The Harris Semiconductor Dielectric Isolation process provides latch-free operation while minimizing stray capacitance and leakage currents, to produce an excellent combination of speed and accuracy. Also, ground currents are minimized to produce a low and constant current through the ground terminal, which reduces error due to code-dependent ground currents.

HI-565A/883 dice are laser trimmed for a maximum integral nonlinearity error of ±1/4 LSB at +25°C. In addition, the low noise buried zener reference is trimmed both for absolute value and minimum temperature coefficient.

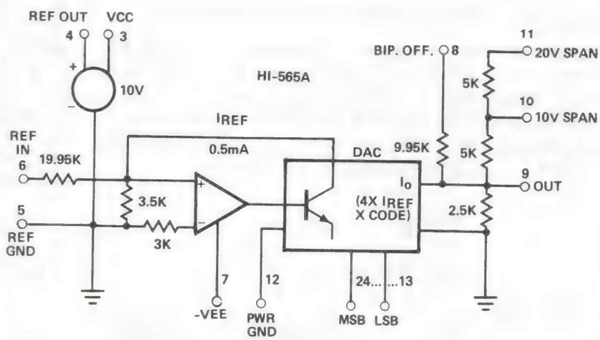
The HI-565A/883 is packaged in a 24 pin Ceramic Sidebrazed DIP.

Pinout

HA1-565A/883 (CERAMIC SIDEBRAZED DIP)
TOP VIEW



Functional Diagram



Absolute Maximum Ratings (Note 1)

Power Supply Inputs (Referred to Power GND)
- V_{CC} .... +18V
- $-V_{EE}$ .... -18V

Reference (Referred to Ref. GND)
- Input .... ±12V
- Output .... Indefinite Short to Power GND

Analog Output .... -3V to +12V
Bipolar Offset (Referred to Ref. GND) .... ±12V
Digital Inputs
- Bits 1 to 12 .... -1V to +7V

Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering 10s) .... 275°C
Junction Temperature .... 175°C

Thermal Information

Thermal Resistance, Junction-to-Case (θ_{jc})
- Ceramic DIP Package .... 19°C/W

Thermal Resistance Junction-to-Ambient (θ_{ja})
- Ceramic DIP Package .... 79°C/W

Power Dissipation at 75°C
- Ceramic DIP Package 1270mW

Power Dissipation Derating Factor (Above +75°C)
- Ceramic DIP Package .... 12.7mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltages
- $+V_{CC}$ .... +12V to +15V
- $-V_{EE}$ .... -12V to -15V

Reference Input Voltage 10V
Logic Low Level .... 0V to 0.8V
Logic High Level .... 2.0V to +5.5V

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at $+V_{CC}$ = +15V, $-V_{EE}$ = -15V, Reference In Connected to Reference Out, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	HI-565AS/883 MIN	HI-565AS/883 MAX	HI-565AT/883 MIN	HI-565AT/883 MAX	UNITS
Supply Current From V_{CC}	I_{CC}	All Bits = 2.0V	1	+25°C	-	11.8	-	11.8	mA
			2, 3	+125°C, -55°C	-	12.8	-	12.8	mA
Supply Current From V_{EE}	I_{EE}	All Bits = 2.0V	1	+25°C	-	-14.5	-	-14.5	mA
			2, 3	+125°C, -55°C	-	-15.5	-	-15.5	mA
Power Dissipation	PD	Calculated	1	+25°C	-	375	-	375	mW
			2, 3	+125°C, -55°C	-	425	-	425	mW
Digital Input High Current	I_{IH}	Bit Under Test = 5.5V, Others = 0.8V	1	+25°C	-400	400	-400	400	nA
			2, 3	+125°C, -55°C	-1	1	-1	1	µA
Digital Input Low Current	I_{IL}	Bit Under Test = 0V, Others = 0.8V	1	+25°C	-10	-	-10	-	µA
			2, 3	+125°C, -55°C	-20	-	-20	-	µA
Unipolar Offset Error	V_{OS}	All Bits = 0.8V Note 2	1	+25°C	-0.05	0.05	-0.05	0.05	% of FSR
			2, 3	+125°C, -55°C	-0.07	0.07	-0.07	0.07	% of FSR
Unipolar Gain Error	A_E	All Bits = 2.0V Note 2	1	+25°C	-0.25	0.25	-0.25	0.25	% of FSR
			2, 3	+125°C, -55°C	-0.55	0.55	-0.5	0.5	% of FSR
Power Supply Sensitivity to V_{CC}	$+P_{SS1}$	V_{CC} = 11.4V to 16.5V All Bits = 2.0V, Unipolar	1	+25°C	10	10	10	10	ppm of FSR / $\%\Delta V_{CC}$
			2, 3	+125°C, -55°C	20	20	20	20	
Power Supply Sensitivity to to V_{EE}	$-P_{SS1}$	V_{EE} = -11.4V to -16.5V. All Bits = 2.0V Unipolar	1	+25°C	25	25	25	25	ppm of FSR / $\%\Delta V_{EE}$
			2, 3	+125°C, -55°C	50	50	50	50	
Output Current Unipolar	I_{OUT1}	I_{DAC} Out = 0V, All Bits = 2.0V	1	+25°C	-2.4	-1.6	-2.4	-1.6	mA
Output Current Bipolar	I_{OUT2}	$BIPR_{IN}$ Tied to V_{REF} All Bits = 2V, I_{DAC} = 0	1	+25°C	±0.8	±1.2	±0.8	±1.2	mA
Bipolar Offset Error	BPO_E	B.P.±10V Range All Bits = 0.8V, Notes 2, 3	1	+25°C	-0.15	0.15	-0.1	0.1	% FSR
			2, 3	+125°C, -55°C	-0.25	0.25	-0.2	0.2	% FSR
Bipolar Zero Error	BPZ_E	B.P.±10V Range, Note 2, MSB = 2V, Bit 1 thru 11 = 0.8V	1	+25°C	-0.15	0.15	-0.1	0.1	% FSR
			2, 3	+125°C, -55°C	-0.25	0.25	-0.2	-0.2	% FSR

6 DATA CONVERSION PRODUCTS

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Devices Tested at $+V_{CC} = +15V$, $-V_{EE} = -15V$, Reference In Connected to Reference Out, Unless Otherwise Specified

D.C. PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	HI-565AS/883		HI-565AT/883		UNITS
					MIN	MAX	MIN	MAX	
Bipolar Gain Error	BPA_E	B.P.±10V Range All Bits = 2.0V, Note 2	1	+25°C	-0.25	0.25	-0.25	0.25	% FSR
			2, 3	+125°C, -55°C	-0.55	0.55	-0.5	0.5	% FSR
Integral Linearity Error	L_E	Note 2	1	+25°C	-0.5	0.5	-0.25	0.25	LSB
			2, 3	+125°C, -55°C	-0.75	0.75	-0.5	0.5	LSB
Differential Linearity Error	DL_E	Note 2	1	+25°C	-0.5	0.5	-0.5	0.5	LSB
			2, 3	+125°C, -55°C	-1	1	-1	1	LSB
Ref. Voltage (Unipolar)	$V_{REF(U)}$	No Load on V_{REF}, $V_{REF(OUT)}$ not tied to $V_{REF(IN)}$, All Bits = 0.8V	1	+25°C	9.95	10.05	9.95	10.05	V
			2, 3	+125°C, -55°C	9.95	10.05	9.95	10.05	V
Ref. Voltage (Bipolar)	$V_{REF(B)}$	No Load on V_{REF}, $V_{REF(OUT)}$ Not Tied To $V_{REF(IN)}$, All Bits = 0.8V	1	+25°C	9.95	10.05	9.95	10.05	V
			2, 3	+125°C, -55°C	9.95	10.05	9.95	10.05	V
Ref. Voltage (Loaded)	$V_{REF(L)}$	Pull Additional 1.5mA Out of V_{REF}. $V_{REF(OUT)}$ Tied to $V_{REF(IN)}$ and $BIPR_{IN}$. All Bits = 0.8V	1	+25°C	9.95	10.05	9.95	10.05	V
			2, 3	+125°C, -55°C	9.95	10.05	9.95	10.05	V
Unipolar Offset Drift	$\frac{d_{VOS}}{dT}$	Note 4	1, 2	+25°C to +125°C	-2.0	2.0	-2.0	2.0	ppm of FSR per °C
			1, 3	+25°C to -55°C	-2.0	2.0	-2.0	2.0	
Unipolar Gain Drift	$\frac{d_{AE}}{dT}$	Note 4	1, 2	+25°C to +125°C	-40	40	-25	25	
			1, 3	+25°C to -55°C	-40	40	-25	25	
Bipolar Zero Drift	$\frac{dBP_Z}{dT}$	Note 4	1, 2	+25°C to +125°C	-10	10	-10	10	
			1, 3	+25°C to -55°C	-10	10	-10	10	
Bipolar Gain Drift	$\frac{dBP_{AE}}{dT}$	Note 4	1, 2	+25°C to +125°C	-40	40	-25	25	
			1, 3	+25°C to -55°C	-40	40	-25	25	

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

This Table Intentionally Left Blank. See A.C. Parameters on Table 3.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Characterized at $V_{CC} = +15V$, $V_{EE} = -15V$, $V_{REF(OUT)}$ Tied to $V_{REF(IN)}$, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	HI-565AS/883		HI-565AT/883		UNITS
					MIN	MAX	MIN	MAX	
Settling Time	t_S	All Bits OFF to ON, and ON to OFF. 10V Unipolar Mode to 0.01%. $V_{IL} = 0.8V$ $V_{IH} = 3.5V$, $R_L = 50\Omega$	5	+25°C	-	500	-	500	ns

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLE 1)
Interim Electrical Parameters (Pre-Burn-In)	-
Final Electrical Test Parameters	1*, 2, 3
Group A Test Requirements	1, 2, 3
Groups C & D Endpoints	1

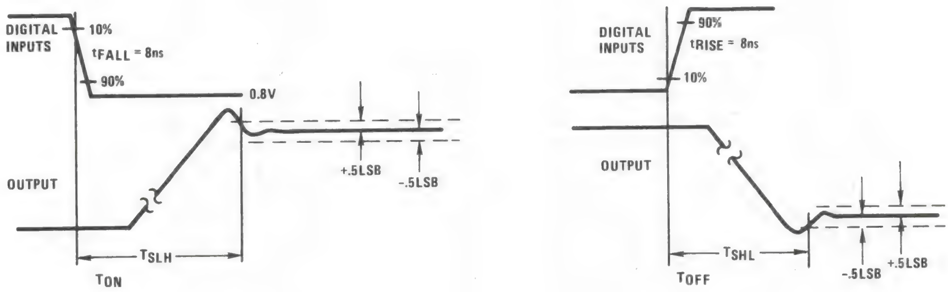
*PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

ELECTRICAL CHARACTERISTICS (Continued)

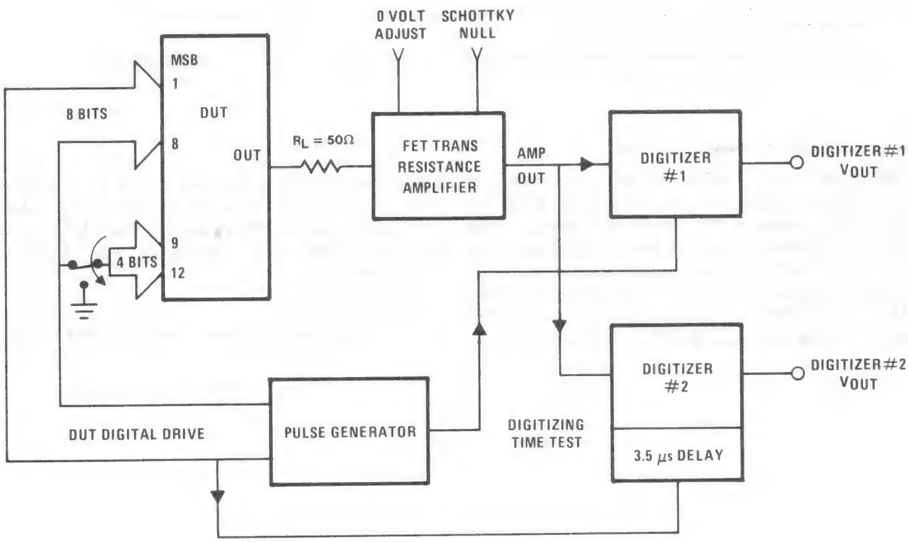
NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. An external reference voltage is set to the measured internal reference value - I_{REF} (50Ω)
3. Adjustable to zero using external potentiometers.
4. See Definitions.
5. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

Waveforms

SETTLING TIME



Test Circuit



SETTLING TIME TEST FIXTURE

6 DATA CONVERSION PRODUCTS

CHART A.

DIGITAL CODE	NOTE	DIGITAL CODE	NOTE
MSB —————— LSB		MSB —————— LSB	
0 0 0 0 0 0 0 0 0 0 0 1		0 1 1 0 X X X X X X X X	7
0 0 0 0 0 0 0 0 0 0 1 0		0 1 1 1 X X X X X X X X	6
0 0 0 0 0 0 0 0 0 1 0 0		0 1 1 1 X X X X X X X X	7
0 0 0 0 0 0 0 0 1 0 0 0		1 0 0 0 X X X X X X X X	6
0 0 0 0 0 0 0 1 0 0 0 0		1 0 0 0 X X X X X X X X	7
0 0 0 0 0 0 1 0 0 0 0 0		1 0 0 1 X X X X X X X X	6
0 0 0 0 0 1 0 0 0 0 0 0		1 0 0 1 X X X X X X X X	7
0 0 0 0 1 0 0 0 0 0 0 0		1 0 1 0 X X X X X X X X	6
0 0 0 1 0 0 0 0 0 0 0 0		1 0 1 0 X X X X X X X X	7
0 0 1 0 0 0 0 0 0 0 0 0		1 0 1 1 X X X X X X X X	6
0 1 0 0 0 0 0 0 0 0 0 0		1 0 1 1 X X X X X X X X	7
1 0 0 0 0 0 0 0 0 0 0 0		1 1 0 0 X X X X X X X X	6
0 0 0 1 X X X X X X X X	6	1 1 0 0 X X X X X X X X	7
0 0 0 1 X X X X X X X X	7	1 1 0 1 X X X X X X X X	6
0 0 1 0 X X X X X X X X	6	1 1 0 1 X X X X X X X X	7
0 0 1 0 X X X X X X X X	7	1 1 1 0 X X X X X X X X	6
0 0 1 1 X X X X X X X X	6	1 1 1 0 X X X X X X X X	7
0 0 1 1 X X X X X X X X	7	1 1 1 1 X X X X X X X X	6
0 1 0 0 X X X X X X X X	6	1 1 1 1 X X X X X X X X	7
0 1 0 0 X X X X X X X X	7	X X X X X X X X X X X X	6
0 1 0 1 X X X X X X X X	6	X X X X X X X X X X X X	7
0 1 0 1 X X X X X X X X	7		
0 1 1 0 X X X X X X X X	6		

NOTES:
6. X = 0 (V_{IL} = 0.8V) if the linearity error for that bit was measured as a positive error. X = 1 (V_{IH} = 2.0V) if the linearity error for that bit was measured as a negative error.
7. X = 0 (V_{IL} = 0.8V) if the linearity error for that bit was measured as a negative error. X = 1 (V_{IH} = 2.0V) if the linearity error error for that bit was measured as a positive error.

Integral Linearity Error Measurements

The transfer characteristics of the DUT are first determined by measuring its end points (all bits OFF, all bits ON). The end points of the reference DAC are then matched to the DUTs through software and hardware adjustments, to establish an ideal transfer characteristic for the DUT. The reference DAC then supplies one 12-bit LSB of current (DUT, all Bits OFF) to the input of the error amplifier and R_T* is adjusted to obtain an output of 1V. The integral linearity error, measured at the output of the error amplifier is a scaled voltage conversion of the difference between the ideal current supplied by the reference DAC through the DUT span resistor and the output current of the DUT for the code under test

$$\text{LSB's of Error} = (\text{Ideal voltage} - \text{measured voltage}) \times \frac{\text{LSBs}}{\text{Volt}}$$

*R_T = Trim resistor in error amplifier

CHART B.

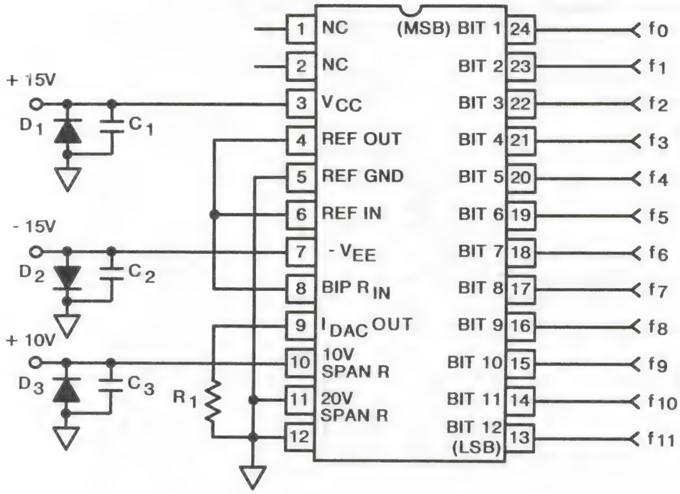
TO CODE	FROM CODE
MSB ———————— LSB	MSB ———————— LSB
0 0 0 0 0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 1 0	0 0 0 0 0 0 0 0 0 0 0 1
0 0 0 0 0 0 0 0 0 1 0 0	0 0 0 0 0 0 0 0 0 0 1 1
0 0 0 0 0 0 0 0 1 0 0 0	0 0 0 0 0 0 0 0 0 1 1 1
0 0 0 0 0 0 0 1 0 0 0 0	0 0 0 0 0 0 0 0 1 1 1 1
0 0 0 0 0 0 1 0 0 0 0 0	0 0 0 0 0 0 0 1 1 1 1 1
0 0 0 0 0 1 0 0 0 0 0 0	0 0 0 0 0 0 1 1 1 1 1 1
0 0 0 0 1 0 0 0 0 0 0 0	0 0 0 0 0 1 1 1 1 1 1 1
0 0 0 1 0 0 0 0 0 0 0 0	0 0 0 0 1 1 1 1 1 1 1 1
0 0 1 0 0 0 0 0 0 0 0 0	0 0 0 1 1 1 1 1 1 1 1 1
0 1 0 0 0 0 0 0 0 0 0 0	0 0 1 1 1 1 1 1 1 1 1 1
1 0 0 0 0 0 0 0 0 0 0 0	0 1 1 1 1 1 1 1 1 1 1 1
0 0 0 1 0 0 0 0 0 0 0 0	0 0 0 0 1 1 1 1 1 1 1 1
0 0 1 0 0 0 0 0 0 0 0 0	0 0 0 1 1 1 1 1 1 1 1 1
0 0 1 1 0 0 0 0 0 0 0 0	0 0 1 0 1 1 1 1 1 1 1 1
0 1 0 0 0 0 0 0 0 0 0 0	0 0 1 1 1 1 1 1 1 1 1 1
0 1 0 1 0 0 0 0 0 0 0 0	0 1 0 0 1 1 1 1 1 1 1 1
0 1 1 0 0 0 0 0 0 0 0 0	0 1 0 1 1 1 1 1 1 1 1 1
0 1 1 1 0 0 0 0 0 0 0 0	0 1 1 0 1 1 1 1 1 1 1 1
1 0 0 0 0 0 0 0 0 0 0 0	0 1 1 1 1 1 1 1 1 1 1 1
1 0 0 1 0 0 0 0 0 0 0 0	1 0 0 0 1 1 1 1 1 1 1 1
1 0 1 0 0 0 0 0 0 0 0 0	1 0 0 1 1 1 1 1 1 1 1 1
1 0 1 1 0 0 0 0 0 0 0 0	1 0 1 0 1 1 1 1 1 1 1 1
1 1 0 0 0 0 0 0 0 0 0 0	1 0 1 1 1 1 1 1 1 1 1 1
1 1 0 1 0 0 0 0 0 0 0 0	1 1 0 0 1 1 1 1 1 1 1 1
1 1 1 0 0 0 0 0 0 0 0 0	1 1 0 1 1 1 1 1 1 1 1 1
1 1 1 1 0 0 0 0 0 0 0 0	1 1 1 0 1 1 1 1 1 1 1 1

Differential Linearity Error Measurements

The DUT and the reference DAC supply the code under test (less 1 LSB) to the input of the error amplifier, and the resulting output error is measured (E_1). The digital code of the DUT is then increased by 1 LSB and the output error is measured a second time (E_2). The differential linearity error is calculated as, $\frac{(E_2 - E_1)}{\text{Volts/LSB}} - 1\ \text{LSB} = \text{LSBs of error.}$

Burn-In Circuit

HI-565A/883 CERAMIC SIDEBRAZE DIP



PARTS:

$R_1 = 0\Omega$ or Jumper Wire

$C_1 = C_2 = C_3 = 0.01\mu F$ (per socket) or $0.1\mu F$ (per row) minimum

$D_1 = D_2 = D_3$ = IN4002 or equivalent (per board)

NOTES: TTL Levels 50% Duty Cycle

f_0 = 100kHz	$f_6 = f_0/64$
$f_1 = f_0/2$	$f_7 = f_0/128$
$f_2 = f_0/4$	$f_8 = f_0/256$
$f_3 = f_0/8$	$f_9 = f_0/512$
$f_4 = f_0/16$	$f_{10} = f_0/1024$
$f_5 = f_0/32$	$f_{11} = f_0/2048$

Die Characteristics

DIE DIMENSIONS:
107 x 180 x 19 mils

METALLIZATION:
Type: Aluminum
Thickness: 20kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
0.75 x 10^5A/cm^2

GLASSIVATION:
Type: Silox
Thickness: 14kÅ ± 2.0kÅ

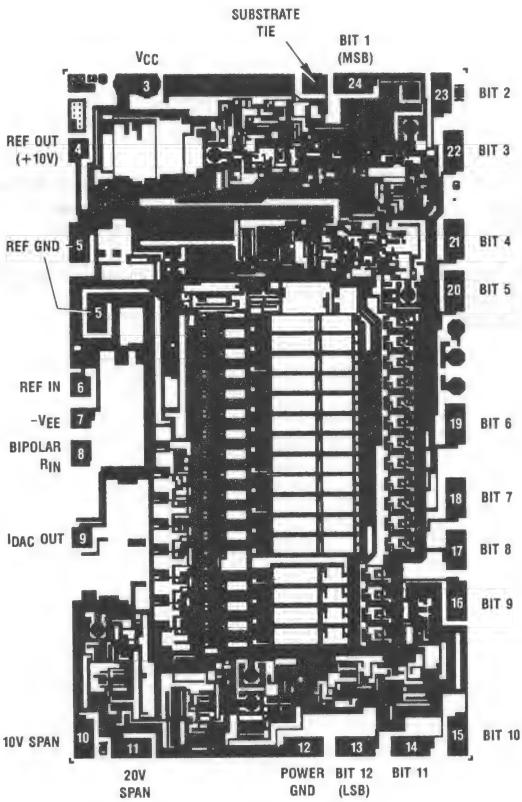
TRANSISTOR COUNT: 200

PROCESS: Bipolar-DI

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Sidebraze Ceramic DIP — 460°C (Max)

Metallization Mask Layout

HI-565A/883

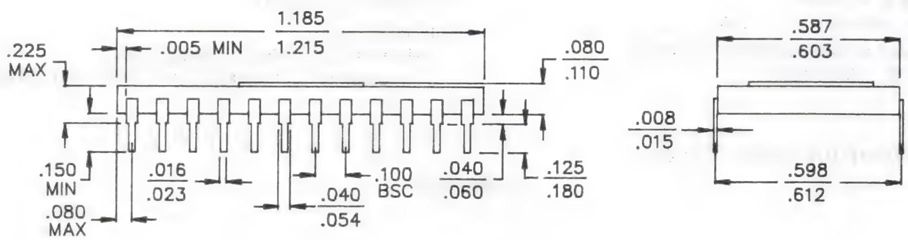


DATA CONVERSION PRODUCTS

6

Packaging†

24 PIN CERAMIC SIDEBRAZE DIP



LEAD MATERIAL: Type B
LEAD FINISH: Type C
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-3

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

High Speed, Monolithic Digital-to-Analog Converter With Reference

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Definitions of Specifications

Digital Inputs

The HI-565A accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight Binary, Two's Complement*, or Offset Binary, (see Operating Instructions).

DIGITAL INPUT	ANALOG OUTPUT		
	STRAIGHT BINARY	OFFSET BINARY	TWO'S COMPLEMENT*
MSB...LSB			
000...000	Zero	-FS (Full Scale)	Zero
100...000	1/2 FS	Zero	-FS
111...111	+FS - 1 LSB	+FS - 1 LSB	Zero - 1 LSB
011...111	½FS - 1 LSB	Zero - 1 LSB	+FS - 1 LSB

* Invert MSB with external inverter to obtain Two's Complementing Coding

Accuracy

NONLINEARITY - Nonlinearity of a D/A converter is an important measure of its accuracy. It describes the deviation from an ideal straight line transfer curve drawn between zero (all bits OFF) and full scale (all bits ON).

DIFFERENTIAL NONLINEARITY - For a D/A converter, it is the difference between the actual output voltage change and the ideal (1 LSB) voltage change for a one bit change in code. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity; i.e., the output always increases and never decreases for an increasing input.

Settling Time

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale or major carry transition, settling to within 1/2 LSB of final value.

Drift

GAIN DRIFT - The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per ^{o}C (ppm of FSR/^{o}C). Gain error is measured with respect to +25^{o}C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25^{o}C) and low ranges (+25^{o}C, -T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT - The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per ^{o}C (ppm of FSR/^{o}C). Offset error is measured with respect to +25^{o}C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25^{o}C) and low (+25^{o}C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

Power Supply Sensitivity

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

Compliance

Compliance Voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance Limit implies functional operation only and makes no claims to accuracy.

Glitch

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably.

Applying the HI-565A

Op Amp Selection

The HI-565A's current output may be converted to voltage using the standard connections shown in Figures 1 and 2. The choice of operational amplifier should be reviewed for each application, since a significant trade-off may be made between speed and accuracy.

For highest precision, use an HA-5177. This amplifier contributes negligible error, but requires about 11μs to settle within ±0.1% following a 10V step.

The Harris Semiconductor HA-2600 is the best all-around choice for this application, and it settles in 1.5μs (also to ±0.1% following a 10V step). Remember, settling time for the DAC-amplifier combination is $\sqrt{t_D2 + t_A2}$, where t_D, t_A are settling times for the DAC and amplifier.

No-Trim Operation

The HI-565A will perform as specified without calibration adjustments. To operate without calibration, substitute 50Ω

resistors for the 100Ω trimming potentiometers: In Figure 1 replace R2 with 50Ω; also remove the network on pin 8 and connect 50Ω to ground. For bipolar operation in Figure 2, replace R3 and R4 with 50Ω resistors.

Typical unipolar zero will be ±1/2 LSB plus the op amp offset.

The Feedback capacitor C must be selected to minimize settling time.

Calibration

Calibration provides the maximum accuracy from a converter by adjusting its gain and offset errors to zero. For the HI-565A, these adjustments are similar whether the current output is used or whether an external op amp is added to convert this current to a voltage. Refer to Table 5 for the voltage output case, along with Figure 1 or 2.

Calibration is a two step process for each of the five output ranges shown in Table 1. First adjust the negative full scale (zero for unipolar ranges). This is an offset adjust which translates the output characteristic, i.e. affects each code by the same amount.

Next adjust positive FS. This is a gain error adjustment, which rotates the output characteristic about the negative FS value.

For the bipolar ranges, this approach leaves an error at the zero code, whose maximum value is the same as for integral nonlinearity error. In general, only two values of output may be calibrated exactly; all others must tolerate some error. Choosing the extreme end points (plus and minus full scale) minimizes this distributed error for all other codes.

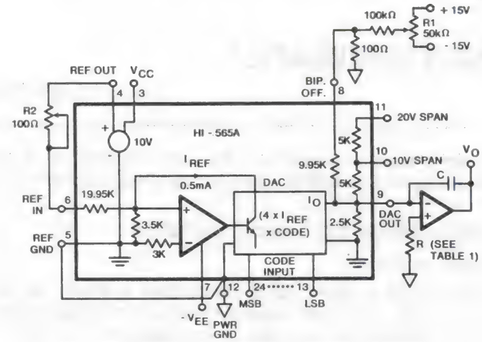


FIGURE 1. UNIPOLAR VOLTAGE OUTPUT

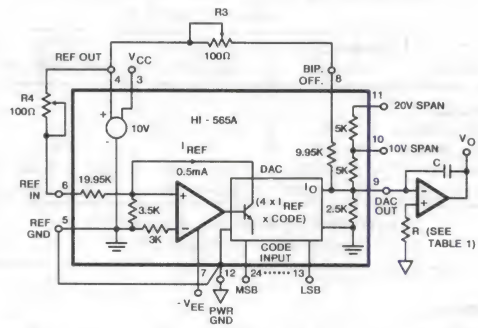


FIGURE 2. BIPOLAR VOLTAGE OUTPUT

TABLE 5. OPERATING MODES AND CALIBRATION

MODE	CIRCUIT CONNECTIONS				CALIBRATION		
	OUTPUT RANGE	PIN 10 TO	PIN 11 TO	RESISTOR (R)	APPLY INPUT CODE	ADJUST	TO SET V_O
Unipolar (See Fig. 1)	0 to +10V	V_O	Pin 10	1.43K	All 0's All 1's	R1 R2	0V +9.99756V
	0 to +5V	V_O	Pin 9	1.1K	All 0's All 1's	R1 R2	0V +4.99878V
Bipolar (See Figure 2)	±10V	NC	V_O	1.69K	All 0's All 1's	R3 R4	-10V +9.99512V
	±5V	V_O	Pin 10	1.43K	All 0's All 1's	R3 R4	-5V +4.99756V
	±2.5V	V_O	Pin 9	1.1K	All 0's All 1's	R3 R4	-2.5V +2.49878V

Other Considerations

Grounds

The HI-565A has two ground terminals, pin 5 (REF GND) and pin 12 (PWR GND). These should not be tied together near the package unless that point is also the system signal ground to which all returns are connected. (If such a point exists, then separate paths are required to pins 5 and 12).

The current through pin 5 is near-zero DC*; but pin 12 carries up to 1.75mA of code — dependent current from bits 1, 2 and 3. The general rule is to connect pin 5 directly to the system "quiet" point, usually called signal or analog ground. Then, of course, a single path must connect the analog/signal and digital/power grounds.

Layout

Connections to pin 9 (I_{OUT}) on the HI-565A are most critical for high speed performance. Output capacitance of the DAC is only 20pF, so a small change or additional capacitance may alter the op amp's stability and affect settling time. Connections to pin 9 should be short and few. Component leads should short on the side connecting to pin 9 (as for feedback capacitor C).

Bypass Capacitors

Power supply bypass capacitors on the op amp will serve the HI-565A also. If no op amp is used, a 0.01μF ceramic capacitor from each supply terminal to pin 12 is sufficient, since supply current variations are small.

*Current cancellation is a two-step process within the HI-565A in which code-dependent variations are eliminated, then the resulting DC current is supplied internally. First an auxilliary 9 bit R-2R ladder is driven by the complement of the DACs input code. Together, the main and auxilliary ladders draw a continuous 2.25mA from the internal ground node, regardless of input code. Part of this DC current is supplied by the zener voltage reference, and the remainder is sourced from the positive supply via a current mirror which is laser trimmed for zero current through the external terminal (pin 5).

HARRIS HI-5687V/883

Wide Temperature Range Monolithic 12-Bit Digital-to-Analog Converter

May 1988

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- DAC 87 Alternate Source
- Monolithic Construction (Single Chip)
- Fast Settling
- Guaranteed Specifications
- Wafer Laser Trimmed
- Applications Resistors On-Chip
- On-Chip Reference
- Dielectric Isolation (DI) Processing
- ±12V Power Supply Operation

Applications

- High Speed A/D Converters
- Precision Instrumentation
- CRT Display Generation

Description

The HI-5687V/883 is a monolithic direct replacement for the popular DAC 87-CBI wide temperature range digital-to-analog converter. Single chip construction, along with several design innovations make the HI-5687/883 the optimum choice for low cost, high reliability applications.

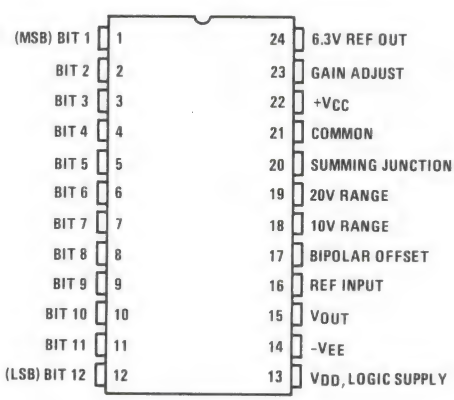
The Harris unique Dielectric Isolation (DI) processing reduces internal parasitics, resulting in fast switching times and minimum glitch. On-board span resistors are provided for good tracking over temperature, and are laser trimmed to high accuracy. These may be used with the on-chip op amp.

Internally, the HI-5687V/883 eliminates code dependent ground currents by routing current from the positive supply to the internal ground node, as determined by an auxiliary R-2R ladder. This results in a cancellation of code dependent ground currents, allowing virtually zero variation in current through the package common, pin 21, (25).

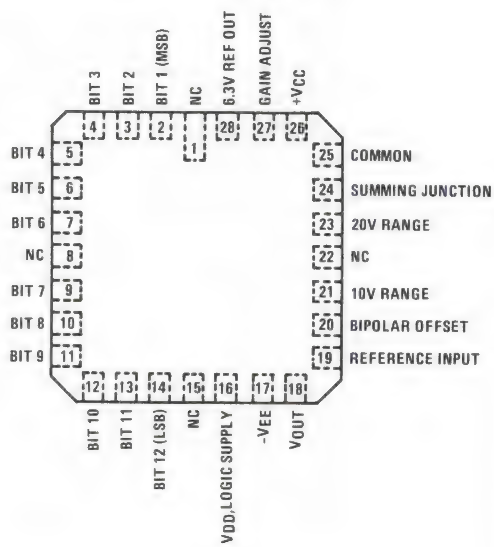
The HI-5687V/883 includes an on-chip output amplifier, a buried zener voltage reference featuring low temperature coefficient, and operates with a +5V logic supply and a $+V_{CC}$, $-V_{EE}$ in the range of ±11.4V to ±16.5V.

Pinouts

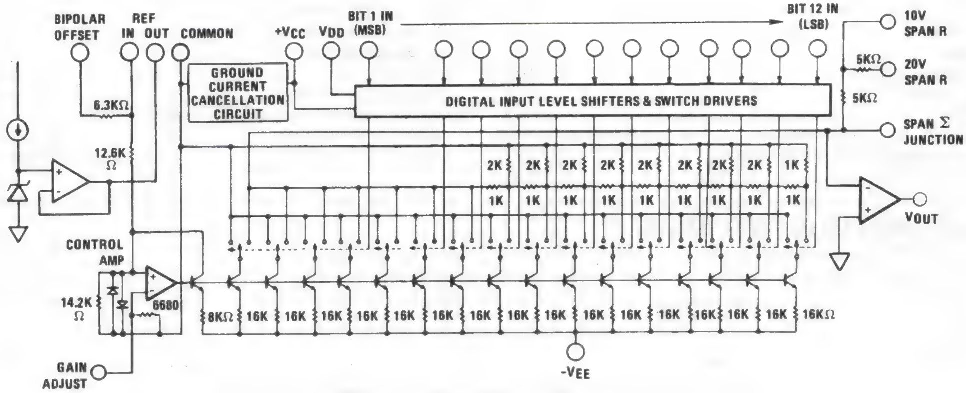
HI1-5687V/883 (CERAMIC SIDEBRAZE DIP)
TOP VIEW



HI4-5687V/883 (CERAMIC LCC)
TOP VIEW



Functional Block Diagram



Absolute Maximum Ratings (Note 1)

All Voltages Referred to Common

Power Supply Inputs
- $+V_{CC}$ .... +20V
- $-V_{EE}$ .... -20V
- V_{DD} .... +20V

Reference
- Input .... $+V_{CC}$ to $-V_{EE}$
- Output Current 6mA

Digital Inputs
- Bits 1 to 12 .... -1V to +12V

Storage Temperature Range .... -65°C to +150°C

Lead Temperature (Soldering 10sec) .... 275°C

Junction Temperature .... 175°C

Thermal Information

Thermal Resistance, Junction-to-Case (θ_{jc})
- Ceramic DIP Package .... 12°C/W
- Ceramic LCC Package .... 40°C/W

Thermal Resistance Junction-to-Ambient (θ_{ja})
- Ceramic DIP Package .... 49°C/W
- Ceramic LCC Package .... 81°C/W

Power Dissipation at 75°C
- Ceramic DIP Package 2040mW
- Ceramic LCC Package 1235mW

Power Dissipation Derating Factor (Above +75°C)
- Ceramic DIP Package .... 20.4mW/°C
- Ceramic LCC Package .... 12.35mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C

Operating Supply Voltage (Note 5);
- $+V_{CC}$ .... +12V to +15V
- $-V_{EE}$ .... -12V to -15V
- $+V_{DD}$ .... +5V

Reference Input Voltage 6.3V

Logic Low Level .... 0V to 0.8V

Logic High Level .... 2.0V to 5.5V

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at $+V_{CC}$ = +15V, $-V_{EE}$ = −15V, V_{DD} = +5V, Reference Out Connected to Reference In, Pin numbers correspond to DIP package only; Unless Otherwise Specified.

D.C PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	MAX	UNITS
Supply Current From V_{CC}	I_{CC}	All Bits OFF, V_{IH} = 2.0V	1	+25°C	—	11.0	mA
			2, 3	-55°C, +125°C	—	13.5	mA
Supply Current From V_{EE}	I_{EE}	All Bits OFF, V_{IH} = 2.0V	1	+25°C	-20.0	—	mA
			2, 3	-55°C, +125°C	-22.5	—	mA
Supply Current From V_{DD}	I_{DD}	All Bits OFF, V_{IH} = 2.0V	1	+25°C	—	8.0	mA
			2, 3	-55°C, +125°C	—	9.50	mA
Digital Input Low Current	I_{IL}	Each Bit Tested Separately Input Under Test, V_{IL} = 0V, all other Bits, V_{IL} = 0.8V	1	+25°C	-50	—	μA
			2, 3	-55°C, +125°C	-100	—	μA
Digital Input High Current	I_{IH}	Each Bit Tested Separately Input Under Test, V_{IH} = 5.5V all other Bits, V_{IL} = 0.8V	1	+25°C	-0.25	0.25	μA
			2, 3	-55°C, +125°C	-1.0	1.0	μA
Reference Voltage Unipolar Bipolar Loaded	$V_{REF(U)}$ $V_{REF(B)}$ $V_{REF(L)}$	All Bits OFF, V_{IH} = 2.0V Unipolar 10V Range Bipolar 20V Range Bipolar 20V Range 2.5mA Current Source from Pin 24 to Ground	1	+25°C	6.20	6.40	V
			2, 3	-55°C, +125°C	6.20	6.40	V
Unipolar Offset Error	V_{OS}	All Bits OFF, V_{IH} = 2.0V (Note 2)	1	+25°C	-0.10	0.10	% FSR
			2, 3	-55°C, +125°C	-0.13	0.13	% FSR
Unipolar Gain Error	A_E	All Bits OFF to all Bits ON V_{IH} = 2.0V, V_{IL} = 0.8V (Note 2)	1	+25°C	-0.20	0.20	% FSR
			2, 3	-55°C, +125°C	-0.45	0.45	% FSR
Unipolar Gain Error, ±5mA Load Current	$A_{EL\pm}$	All Bits OFF to all Bits ON ±5mA Load Current from V_O (Pin 15) to Ground	1	+25°C	-0.20	0.20	% FSR
			2, 3	-55°C, +125°C	-0.45	0.45	% FSR
Power Supply Sensitivity From V_{CC}	$+P_{SS1}$	All Bits ON, V_{IL} = 0.8V V_{CC} from 16.5V to 11.4V Bipolar Mode, ±5V Range	1	+25°C	-0.002	0.002	$\frac{\Delta \% FSR}{\% \Delta V_{CC}}$
Power Supply Sensitivity From V_{DD}	$+P_{SS2}$	All Bits ON, V_{IL} = 0.8V V_{DD} from 4.5V to 5.5V Bipolar Mode ±5V Range	1	+25°C	-0.002	0.002	$\frac{\Delta \% FSR}{\% \Delta V_{DD}}$
Power Supply Sensitivity From V_{EE}	$-P_{SS1}$	All Bits ON. V_{IN} = 0.8V V_{EE} from -16.5V to −11.4V Bipolar Mode ±5V Range	1	+25°C	-0.002	0.002	$\frac{\Delta \% FSR}{\% \Delta V_{EE}}$

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Devices Tested at $+V_{CC} = +15V$, $-V_{EE} = -15V$, $V_{DD} = +5V$, Reference Out connected to Reference In, Pin numbers correspond to DIP package only, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Bipolar Offset Error	BPO_E	All Bits OFF, $V_{IH} = 2.0V$ Bipolar ±10V Range (Note 2)	1	+25°C	-0.10	0.10	% FSR
			2, 3	-55°C, +125°C	-0.20	0.20	% FSR
Bipolar Zero Error	BPZ_E	MSB ON, $V_{IL} = 0.8V$; all other Bits OFF, $V_{IH} = 2.0V$ Bipolar ±10V Range	1	+25°C	-0.10	0.10	% FSR
			2, 3	-55°C, +125°C	-0.20	0.20	% FSR
Bipolar Gain Error	BPA_E	All Bits OFF, to all Bits ON, $V_{IH} = 2V$, $V_{IL} = 0.8V$ Bipolar ±10V Range (Note 2)	1	+25°C	-0.20	0.20	% FSR
			2, 3	-55°C, +125°C	-0.45	0.45	% FSR
Integral Linearity Error	L_E	Unipolar Mode 10V Range, Reference Chart B for Codes Tested	1	+25°C	-0.375	0.375	LSB
			2, 3	-55°C, +125°C	-0.75	0.75	LSB
Differential Linearity Error	DL_E	Unipolar Mode 10V Range Reference Chart C for Codes Tested	1	+25°C	-0.50	0.50	LSB
			2, 3	-55°C, +125°C	-1.0	1.0	LSB
Gain Adjust	A_A	Unipolar Mode All Bits ON, $V_{IL} = 0.8V$ (Note 6)	1	+25°C	±0.20	—	% FSR
Reference Voltage Drift Unipolar	$\frac{dV_{REF(U)}}{dT}$	(Note 3)	1, 2	+25°C, +125°C	-20	20	$\frac{\text{ppm of } V_{REF}}{^oC}$
			1, 3	+25°C, -55°C	-20	20	
Reference Voltage Drift Bipolar	$\frac{dV_{REF(B)}}{dT}$	(Note 3)	1, 2	+25°C, +125°C	-20	20	$\frac{\text{ppm of } V_{REF}}{^oC}$
			1, 3	+25°C, -55°C	-20	20	
Unipolar Offset Drift	$\frac{dV_{OS}}{dT}$	(Note 3)	1, 2	+25°C, +125°C	+3.0	-3.0	$\frac{\text{ppm of FSR}}{^oC}$
			1, 3	+25°C, -55°C	+3.0	-3.0	
Unipolar Gain Drift	$\frac{dA_{E1}}{dT}$	(Note 3)	1, 2	+25°C, +125°C	-25	+25	$\frac{\text{ppm of FSR}}{^oC}$
			1, 3	+25°C, -55°C	-25	+25	
Unipolar Gain Drift Exclusive of the Internal Reference	$\frac{dA_{E2}}{dT}$	(Note 3)	1, 2	+25°C, +125°C	-10	+10	$\frac{\text{ppm of FSR}}{^oC}$
			1, 3	+25°C, -55°C	-10	+10	
Total Unipolar Error	U_{ET}	(Note 3)	1, 2	+25°C, +125°C	-0.3	0.3	% FSR
			1, 3	+25°C, -55°C	-0.3	0.3	% FSR
Bipolar Offset Drift	$\frac{dBP_{OE}}{dT}$	(Note 3)	1, 2	+25°C, +125°C	-10	+10	$\frac{\text{ppm of FSR}}{^oC}$
			1, 3	+25°C, -55°C	-10	+10	
Bipolar Gain Drift	$\frac{dBP_{AE1}}{dT}$	(Note 3)	1, 2	+25°C, +125°C	-25	25	$\frac{\text{ppm of FSR}}{^oC}$
			1, 3	+25°C, -55°C	-25	25	
Bipolar Gain Drift Exclusive of the Internal Reference	$\frac{dBP_{AE2}}{dT}$	(Note 3)	1, 2	+25°C, +125°C	-10	10	$\frac{\text{ppm of FSR}}{^oC}$
			1, 3	+25°C, -55°C	-10	10	
Total Bipolar Error	B_{ET}	(Note 3)	1, 2	+25°C, +125°C	-0.24	0.24	% FSR
			1, 3	+25°C, -55°C	-0.24	0.24	% FSR
Total Bipolar Drift	$\frac{dBP_T}{dT}$	(Note 3)	1, 2	+25°C, +125°C	-30	30	$\frac{\text{ppm of FSR}}{^oC}$
			1, 3	+25°C, -55°C	-30	30	

NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Adjustable to zero using external potentiometers.
3. See Definitions.
4. FSR is a "Full Scale Range" and is 20V for ±10V range, 10V for ±5V range, etc.
5. The HI-5687/883 will operate with supply voltage as low as ±11.4V. It is recommended that output voltage ranges -10V to +10V not be used if the supply voltages are less than ±12.5V.
6. Gain Adjust capability is tested by first measuring the full scale output voltage with pin 23 (DIP package) open, positive and negative adjustability are checked by applying ±15V to pin 23 (DIP package) through a 2.8MΩ resistor and measuring the full scale voltage for each condition. A minimum delta of ±20mV with respect to the initial reading guarantees ideal full scale adjustment as the gain error specification at +25°C is ±20mV (0.2% FSR).

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at $+V_{CC}$ = +15V, $-V_{EE}$ = -15V, V_{DD} = +5V, Reference Out Connected to Reference In, Unless Otherwise Specified

A.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMP	LIMITS MIN	LIMITS MAX	UNITS
Positive Slew Rate	S_{R+}	All Bits OFF (V_{IH} = 2V) to all Bits ON (V_{IL} = 0.8V). Bipolar ±10V Range. Measurement Points at -6V and +6V. Figure 2.	4	+25°C	11.0	—	V/μs
Negative Slew Rate	S_{R-}	All Bits ON (V_{IL} = 0.8V) to all Bits OFF (V_{IH} = 2.0V). Bipolar ±10V Range. Measurement Points at +6V and -6V. Figure 2.	4	+25°C	11.0	—	V/μs

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Characterized at $+V_{CC}$ = +15V, $-V_{EE}$ = -15V, V_{DD} = +5V, Reference Out Connected to Reference In, Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMP	LIMITS MIN	LIMITS MAX	UNITS
Settling Time	t_S	To ±0.5LSB for Full Scale Transition Unipolar 10V Range, R_L = 5kΩ Figures 3 & 4	3, 7	+25°C	—	2.0	μs

NOTES: 7. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1, 2 & 3)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 4
Group A Test Requirements	1, 2, 3, 4
Groups C & D Endpoints	1

*PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

Test Circuit & Test Conditions

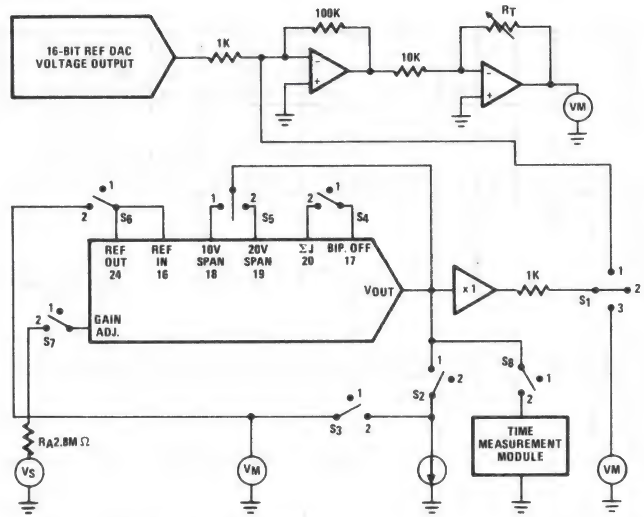


FIGURE 1. TEST CIRCUIT

CHART A. GROUP A TEST CONDITIONS

Pin 24 Tied to Pin 16, and Pin 23 Open Unless Otherwise Noted, All Pin Number's Listed Refer to the 24 Lead DIP Package.

			PIN13	PIN14	PIN15	PIN17	PIN18	PIN19	PIN20	PIN22	SWITCH POSITION								MEASURE		
TEST	SYMBOL	CONDITIONS	V_{DD}	V_{EE}	V_{OUT}	B.P. ROUT	10V SPAN	20V SPAN	Σ_J	V_{CC}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	VALUE	UNIT	EQUATIONS
Supply Current From V_{CC}	I_{CC}	All Bits OFF, V_{IH} = 2.0V	5V	-15V	Pin 18	O.C.	Pin 15	O.C.	O.C.	15V	2	2	1	1	1	1	1	1	—	mA	
Supply Current From V_{EE}	I_{EE}	All Bits OFF, V_{IH} = 2.0V	5V	-15V	Pin 18	O.C.	Pin 15	O.C	O.C.	15V	2	2	1	1	1	1	1	1	—	mA	
Supply Current From V_{DD}	I_{DD}	All Bits OFF, V_{IH} = 2.0V	5V	-15V	Pin 18	O.C	Pin 15	O.C.	O.C.	15V	2	2	1	1	1	1	1	1	—	mA	
Digital Input Low Current	I_{IL}	Each Bit Test Separately Bit Input Under Test, V_{IL} = 0V, All Other Bits, V_{IL} = 0.8V	5V	-15V	Pin 18	O.C.	Pin 15	O.C.	O.C.	15V	2	2	1	1	1	1	1	1	—	μA	
Digital Input High Current	I_{IH}	Each Bit Test Separately Bit Input Under Test, V_{IH} = 5.5V, All Other Bits, V_{IL} = 0.8V	5V	-15V	Pin 18	O.C.	Pin 15	O.C.	O.C.	15V	2	2	1	1	1	1	1	1	—	μA	

DATA CONVERSION PRODUCTS 6

Test Conditions

CHART A. GROUP A TEST CONDITIONS (Continued)

Pin 24 Tied to Pin 16, and Pin 23 Open Unless Otherwise Noted, All Pin Number's Listed Refer to the 24 Lead DIP Package.

TEST	SYMBOL	CONDITIONS	PIN13	PIN14	PIN15	PIN17	PIN18	PIN19	PIN20	PIN22	SWITCH POSITION								MEASURE		EQUATIONS
			V_{DD}	V_{EE}	V_{OUT}	B.P. R_{OUT}	10V SPAN	20V SPAN	Σ_J	V_{CC}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	VALUE	UNIT	
Reference Voltage Loaded	$V_{REF(L)}$	All Bits OFF (V_{IH} = 2V) 2.5mA Current Source From Pin 24 to GND. Bipolar Mode ±10V Range	5V	-15V	Pin 19	Pin 20	O.C	Pin 15	Pin 17	15V	2	2	2	2	2	2	1	1	E_{1R} E_{1H} E_{1L}	V	
Reference Voltage Unipolar Mode	$V_{REF(U)}$	All Bits OFF (V_{IH} = 2V)	5V	-15V	Pin 18	O.C.	Pin 15	O.C	O.C.	15V	2	2	1	1	1	2	1	1	E_{2R} E_{2H} E_{2L}	V	
Reference Voltage Bipolar Mode	$V_{REF(B)}$	All Bits OFF (V_{IH} = 2V) Bipolar Mode ±10V Range	5V	-15V	Pin 19	Pin 20	O.C	Pin 15	Pin 17	15V	2	2	1	2	2	2	1	1	E_{3R} E_{3H} E_{3L}	V	
Unipolar Offset	V_{OS}	All Bits OFF (V_{IH} = 2V)	5V	-15V	Pin 18	O.C.	Pin 15	O.C	O.C.	15V	3	2	1	1	1	1	1	1	E_{4R} E_{4H} E_{4L}	V	$\frac{E_4}{10} \times 100 = \%$ FSR
Unipolar Gain Error	A_{E1}	All Bits OFF to All Bits ON, (V_{IH} = 2V, V_{IL} = 0.8V)	5V	-15V	Pin 18	O.C.	Pin 15	O.C	O.C.	15V	3	2	1	1	1	1	1	1	E_{5R} E_{5H} E_{5L}	V	$\frac{[(E_5 - E_4) - 9.99756]}{10} \times 100 = \%$ FSR
Unipolar Gain Error Output Loaded	A_{E2}	All Bits OFF to All Bits ON, (V_{IH} = 2V, V_{IL} = 0.8V) +5mA Current Source From V_{OUT} to GND	5V	-15V	Pin 18	O.C.	Pin 15	O.C	O.C.	15V	3	1	1	1	1	1	1	1	E_{6R} E_{6H} E_{6L}	V	Calculation Same as Above
Unipolar Gain Error Output Loaded	A_{E3}	All Bits OFF to All Bits ON, V_{IL} = 0.8V -5mA Current Source From V_{OUT} to GND	5V	-15V	Pin 18	O.C.	Pin 15	O.C.	O.C.	15V	3	1	1	1	1	1	1	1	E_{7R} E_{7H} E_{7L}	V	Calculation Same as Above
Power Supply Sensitivity From V_{CC}	$+P_{SS1}$	All Bits ON, V_{IL} = 0.8V V_{CC} = 16.5/11.4V Bipolar ±5V Range	5V	-15V	Pin 18	Pin 20	Pin 15	O.C.	Pin 17	16.5V 11.4V	3	2	1	2	1	1	1	1	E_{8A} E_{8B}	V	$\frac{E_{8A} - E_{8B}}{(10)(34\%)} \times 100 = \frac{\Delta\ \%\ FSR}{\%\ \Delta\ V_{CC}}$
Power Supply Sensitivity From V_{DD}	$+P_{SS2}$	All Bits ON, V_{IL} = 0.8V V_{DD} = 5.5V/4.5V Bipolar ±5V Range	5.5V 4.5V	-15V	Pin 18	Pin 20	Pin 15	O.C.	Pin 17	15V	3	2	1	2	1	1	1	1	E_{9A} E_{9B}	V	$\frac{E_{9A} - E_{9B}}{(10)(34\%)} \times 100 = \frac{\Delta\ \%\ FSR}{\%\ \Delta\ V_{CC}}$
Power Supply Sensitivity From V_{EE}	$-P_{SS1}$	All Bits ON, V_{IL} = 0.8V V_{EE} = -16.5/-11.4V Bipolar ±5V Range	5V	-16.5V -11.4V	Pin 18	Pin 20	Pin 15	O.C.	Pin 17	15V	3	2	1	2	1	1	1	1	E_{10A} E_{10B}	V	$\frac{E_{10A} - E_{10B}}{(10)(34\%)} \times 100 = \frac{\Delta\ \%\ FSR}{\%\ \Delta\ V_{EE}}$
Bipolar Offset Error	BP_{OE}	All Bits OFF, V_{IH} = 2V ±10V Range	5V	-15V	Pin 19	Pin 20	O.C.	Pin 15	Pin 17	15V	3	2	1	2	2	1	1	1	E_{11R} E_{11H} E_{11L}	V	$\frac{E_{11} + 10}{20} \times 100 = \%$ FSR

Test Conditions

CHART A. GROUP A TEST CONDITIONS (Continued)

Pin 24 Tied to Pin 16, and Pin 23 Open Unless Otherwise Noted, All Pin Number's Listed Refer to the 24 Lead DIP Package.

			PIN13	PIN14	PIN15	PIN17	PIN18	PIN19	PIN20	PIN22	SWITCH POSITION								MEASURE		
TEST	SYMBOL	CONDITIONS	V_{DD}	V_{EE}	V_{OUT}	B.P. ROUT	10V SPAN	20V SPAN	Σ_J	V_{CC}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	VALUE	UNIT	EQUATIONS
Bipolar Zero Error	BP_{ZE}	MSB ON, $V_{IL} = 0.8V$ All Other Bits OFF, $V_{IH} = 2.0V$ ±10V Range	5V	-15V	Pin 19	Pin 20	O.C.	Pin 15	Pin 17	15V	3	2	1	2	2	1	1	1	E_{12R} E_{12H} E_{12L}	V	$\frac{E_{12}}{20} \times 100 = \%\ FSR$
Bipolar Gain Error	BP_{AE}	All Bits OFF ($V_{IH} = 2V$) to All Bits ON ($V_{IL} = 0.8V$) ±10V Range	5V	-15V	Pin 19	Pin 20	O.C.	Pin 15	Pin 17	15V	3	2	1	2	2	1	1	1	E_{13R} E_{13H} E_{13L}	V	$\left[\frac{(E_{13}-E_{11})-19.995}{20}\right] \times 100 = \%\ FSR$
Integral Linearity Error	L_E	Unipolar Mode 0 to 10V Range $V_{IL} = 0.8V$, $V_{IH} = 2.0V$	5V	-15V	Pin 18	O.C.	Pin 15	O.C.	O.C.	15V	1	2	1	1	1	1	1	1	E_{LR} E_{LH} E_{LL}	V	E_L(1LSB) = LSBs of Error
Differential Linearity Error	D_{LE}	Unipolar Mode 0 to 10V Range $V_{IL} = 0.8V$, $V_{IH} = 2.0V$	5V	-15V	Pin 18	O.C.	Pin 15	O.C.	O.C.	15V	1	2	1	1	1	1	1	1	E_{DLR} E_{DLH} E_{DLL}	V	E_{DL}(1LSB) = LSBs of Error
Gain Adjust	A_A	$V_S = 15V$, RA = 2.8MΩ $V_S = -15V$, RA = 2.8MΩ	5V	-15V	Pin 18	O.C.	Pin 15	O.C.	O.C.	15V	3	2	1	1	1	1	2	1	E_{14} E_{15}	V	$\frac{E_{14}-E_{5R}}{10} \times 100 = \%FSR$ $\frac{E_{5R}-E_{15}}{10} \times 100 = \%FSR$
Positive Slew Rate	+SR	All Bits OFF ($V_{IH} = 2V$) to All Bits ON ($V_{IL} = 0.8V$) Bipolar ±10V Range	5V	-15V	Pin 19	Pin 20	O.C.	Pin 15	Pin 17	15V	2	2	1	2	2	1	1	2	T_1 T_2	μs	$\frac{12V}{T_2-T_1} = \frac{V}{\mu s}$
Negative Slew Rate	-SR	All Bits ON ($V_{IL} = 0.8V$) to All Bits OFF ($V_{IH} = 2V$) Bipolar ±10V Range	5V	-15V	Pin 19	Pin 20	O.C.	Pin 15	Pin 17	15V	2	2	1	2	2	1	1	2	T_3 T_4	μs	$\frac{12V}{T_3-T_4} = \frac{V}{\mu s}$

TEST	SYMBOL	CONDITIONS	TEMPERATURE	EQUATIONS
Reference Voltage Drift Unipolar Mode	$\frac{dV_{REF(U)}}{dT}$	Calculations Made From Tests Previously Defined in this Chart	+25°C to +125°C	$\frac{(E_{2H}-E_{2R})10^6}{E_{2R}\ (100^oC)} = \frac{PPM\ of\ V_{REF}}{^oC}$
			-55°C to +25°C	$\frac{(E_{2R}-E_{2L})10^6}{E_{2R}\ (80^oC)} = \frac{PPM\ of\ V_{REF}}{^oC}$
Reference Voltage Drift Bipolar Mode	$\frac{dV_{REF(B)}}{dT}$	Calculations Made From Tests Previously Defined in this Chart	+25°C to +125°C	$\frac{(E_{3H}-E_{3R})10^6}{E_{3R}\ (100^oC)} = \frac{PPM\ of\ V_{REF}}{^oC}$
			-55°C to +25°C	$\frac{(E_{3R}-E_{3L})10^6}{E_{3R}\ (80^oC)} = \frac{PPM\ of\ V_{REF}}{^oC}$
Unipolar Offset Drift	$\frac{dV_{OS}}{dT}$	Calculations Made From Tests Previously Defined in this Chart	+25°C to +125°C	$\frac{(E_{4H}-E_{4R})10^6}{10\ (100^oC)} = \frac{PPM\ of\ FSR}{^oC}$
			-55°C to +25°C	$\frac{(E_{4R}-E_{4L})10^6}{10\ (80^oC)} = \frac{PPM\ of\ FSR}{^oC}$

Test Conditions

CHART A. GROUP A TEST CONDITIONS (Continued)

Pin 24 Tied to Pin 16, and Pin 23 Open Unless Otherwise Noted, All Pin Number's Listed Refer to the 24 Lead DIP Package.

TEST	SYMBOL	CONDITIONS	TEMPERATURE	EQUATIONS
Unipolar Gain Drift	$\frac{dA_{E1}}{dT}$	Calculations Made From Tests Previously Defined in this Chart	$+25^oC$ to $+125^oC$	$\left[\frac{(E_{5H}-E_{4H}) - (E_{5R}-E_{4R})}{10\ (100^oC)}\right] 10^6 = \frac{\text{PPM of FSR}}{^oC}$
			-55^oC to $+25^oC$	$\left[\frac{(E_{5R}-E_{4R}) - (E_{5L}-E_{4L})}{10\ (80^oC)}\right] 10^6 = \frac{\text{PPM of FSR}}{^oC}$
Unipolar Gain Drift Exclusive of the Internal Reference	$\frac{dA_{E2}}{dT}$	Calculations Made From Tests Previously Defined in this Chart	$+25^oC$ to $+125^oC$	$\left[\frac{(E_{5H}-E_{4H}) - (E_{5R}-E_{4R})}{10} - \frac{(E_{2H}-E_{2R})}{6.3}\right] \frac{10^6}{100^oC} = \frac{\text{PPM of FSR}}{^oC}$
			-55^oC to $+25^oC$	$\left[\frac{(E_{5R}-E_{4R}) - (E_{5L}-E_{4L})}{10} - \frac{(E_{2R}-E_{2L})}{6.3}\right] \frac{10^6}{80^oC} = \frac{\text{PPM of FSR}}{^oC}$
Total Unipolar Error	U_{ET}	Calculations Made From Tests Previously Defined in This Chart	$+25^oC$ to $+125^oC$	$\frac{(E_{5H}-E_{5R})}{10}\ (100) = \%\ \text{FSR}$
			-55^oC to $+25^oC$	$\frac{(E_{5R}-E_{5L})}{10}\ (100) = \%\ \text{FSR}$
Bipolar Offset Drift	$\frac{dBP_{OE}}{dT}$	Calculations Made From Tests Previously Defined in This Chart	$+25^oC$ to $+125^oC$	$\frac{(E_{11H}-E_{11R})\ 10^6}{20\ (100^oC)} = \frac{\text{PPM of FSR}}{^oC}$
			-55^oC to $+25^oC$	$\frac{(E_{11R}-E_{11L})\ 10^6}{20\ (80^oC)} = \frac{\text{PPM of FSR}}{^oC}$
Bipolar Gain Drift	$\frac{dBP_{AE1}}{dT}$	Calculations Made From Tests Previously Defined in This Chart	$+25^oC$ to $+125^oC$	$\left[\frac{(E_{13H}-E_{11H}) - (E_{13R}-E_{11R})}{20\ (100^oC)}\right] 10^6 = \frac{\text{PPM of FSR}}{^oC}$
			-55^oC to $+25^oC$	$\left[\frac{(E_{13R}-E_{11R})-(E_{13L}-E_{11L})}{20\ (80^oC)}\right] 10^6 = \frac{\text{PPM of FSR}}{^oC}$
Bipolar Gain Drift Exclusive of the Internal Reference	$\frac{dBA_{E2}}{dT}$	Calculations Made From Tests Previously Defined in This Chart	$+25^oC$ to $+125^oC$	$\left[\frac{(E_{13H}-E_{11H})-(E_{13R}-E_{11R})}{20} - \frac{(E_{3H}-E_{3R})}{6.3}\right] \frac{10^6}{100^oC} = \frac{\text{PPM of FSR}}{^oC}$
			-55^oC to $+25^oC$	$\left[\frac{(E_{13R}-E_{11R})-(E_{13L}-E_{11L})}{20} - \frac{(E_{3R}-E_{3L})}{6.3}\right] \frac{10^6}{80^oC} = \frac{\text{PPM of FSR}}{^oC}$
Total Bipolar Error	B_{ET}	Calculations Made From Tests Previously Defined in This Chart	$+25^oC$ to $+125^oC$	$\frac{(E_{13H} - E_{13R})}{20}\ (100) = \%\ \text{FSR}$
			-55^oC to $+25^oC$	$\frac{(E_{13R} - E_{13L})}{20}\ (100) = \%\ \text{FSR}$
Total Bipolar Drift	$\frac{dBp}{dT}$	Calculations Made From Tests Previously Defined in This Chart	$+25^oC$ to $+125^oC$	$\frac{(E_{13H} - E_{13R})\ 10^6}{20\ (100^oC)} = \frac{\text{PPM of FSR}}{^oC}$
		Includes Gain, Offset and Linearity Drift	-55^oC to $+25^oC$	$\frac{(E_{13R} - E_{13L})\ 10^6}{20\ (80^oC)} = \frac{\text{PPM of FSR}}{^oC}$

Waveforms

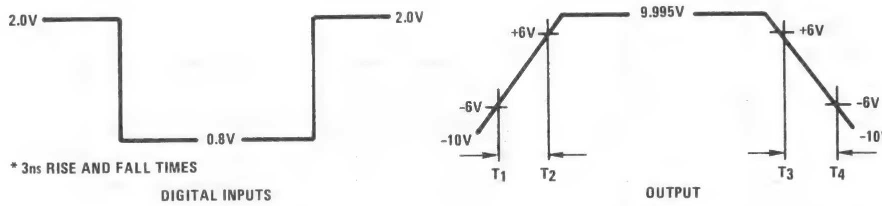


FIGURE 2. SLEW RATE WAVEFORMS

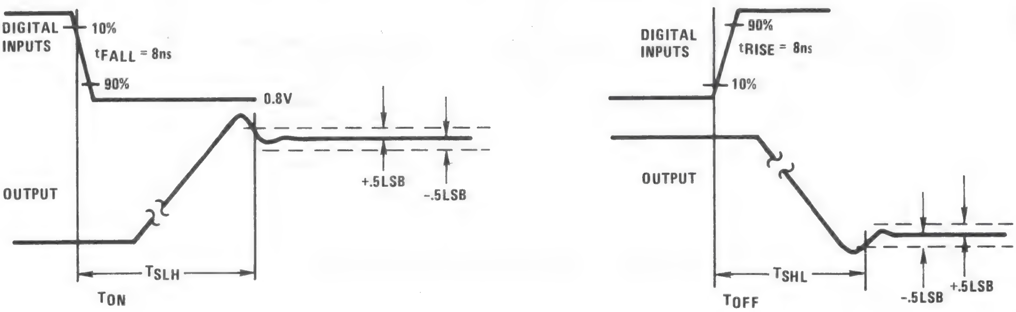


FIGURE 3. SETTLING TIME WAVEFORMS

Test Circuit

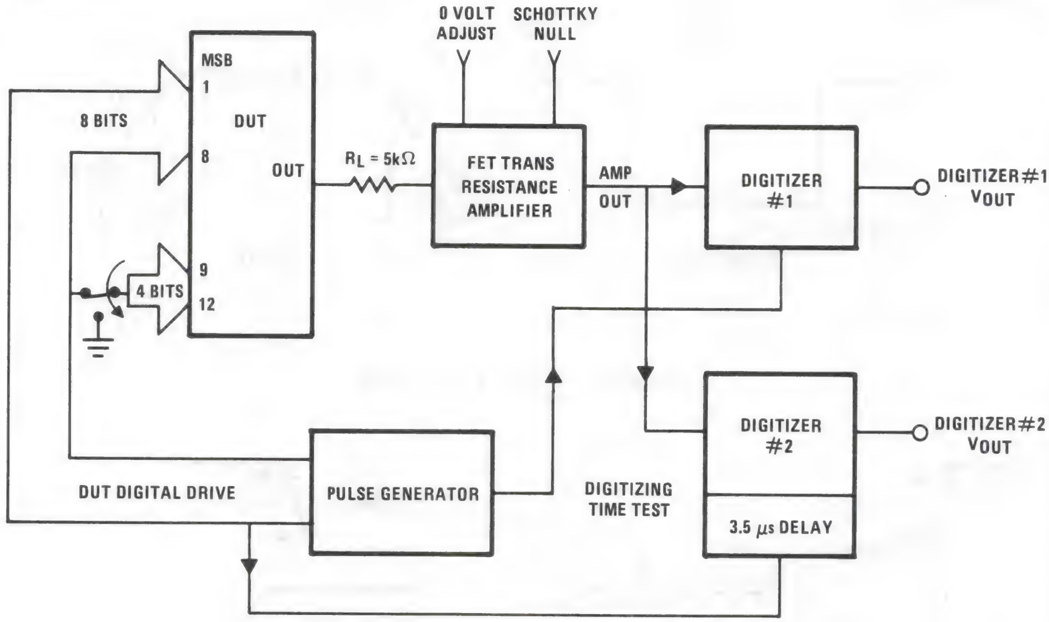


FIGURE 4. SETTLING TIME TEST FIXTURE

CHART B.

DIGITAL CODE	NOTE	DIGITAL CODE	NOTE
MSB ———— LSB		MSB ———— LSB	
1 1 1 1 1 1 1 1 1 1 1 0		1 0 0 1 X X X X X X X X	9
1 1 1 1 1 1 1 1 1 1 0 1		1 0 0 0 X X X X X X X X	8
1 1 1 1 1 1 1 1 1 0 1 1		1 0 0 0 X X X X X X X X	9
1 1 1 1 1 1 1 1 0 1 1 1		0 1 1 1 X X X X X X X X	8
1 1 1 1 1 1 1 0 1 1 1 1		0 1 1 1 X X X X X X X X	9
1 1 1 1 1 1 0 1 1 1 1 1		0 1 1 0 X X X X X X X X	8
1 1 1 1 1 0 1 1 1 1 1 1		0 1 1 0 X X X X X X X X	9
1 1 1 1 0 1 1 1 1 1 1 1		0 1 0 1 X X X X X X X X	8
1 1 1 0 1 1 1 1 1 1 1 1		0 1 0 1 X X X X X X X X	9
1 1 0 1 1 1 1 1 1 1 1 1		0 1 0 0 X X X X X X X X	8
1 0 1 1 1 1 1 1 1 1 1 1		0 1 0 0 X X X X X X X X	9
0 1 1 1 1 1 1 1 1 1 1 1		0 0 1 1 X X X X X X X X	8
1 1 1 0 X X X X X X X X	8	0 0 1 1 X X X X X X X X	9
1 1 1 0 X X X X X X X X	9	0 0 1 0 X X X X X X X X	8
1 1 0 1 X X X X X X X X	8	0 0 1 0 X X X X X X X X	9
1 1 0 1 X X X X X X X X	9	0 0 0 1 X X X X X X X X	8
1 1 0 0 X X X X X X X X	8	0 0 0 1 X X X X X X X X	9
1 1 0 0 X X X X X X X X	9	0 0 0 0 X X X X X X X X	8
1 0 1 1 X X X X X X X X	8	0 0 0 0 X X X X X X X X	9
1 0 1 1 X X X X X X X X	9	X X X X X X X X X X X X	8
1 0 1 0 X X X X X X X X	8	X X X X X X X X X X X X	9
1 0 1 0 X X X X X X X X	9		
1 0 0 1 X X X X X X X X	8		

NOTES: 8. X = 0 (V_{IL} = 0.8V) if the linearity error for that bit was measured as a positive error. X = 1 (V_{IH} = 2.0V) if the linearity error for that bit was measured as a negative error.

9. X = 0 (V_{IL} = 0.8V) if the linearity error for that bit was measured as a negative error. X = 1 (V_{IH} = 2.0V) if the linearity error for that bit was measured as a positive error.

Integral Linearity Error Measurements

The transfer characteristics of the DUT are first determined by measuring its end points (all bits OFF, all bits ON). The end points of the reference DAC are then matched to the DUTs through software and hardware adjustments, to establish an ideal transfer characteristic for the DUT. The reference DAC then supplies one 12-bit LSB (DUT, all Bits OFF) to the input of the error amplifier and R_T is adjusted to obtain an output of 1V. The integral linearity error, measured at the output of the error amplifier is the difference between the ideal voltage supplied by the reference DAC and the output voltage of the DUT for the code under test

$$\text{LSB's of Error} = \left(\text{Ideal voltage - measured voltage}\right) \times \frac{\text{LSB's}}{\text{Volt}}$$

6

DATA CONVERSION PRODUCTS

CHART C.

TO CODE	FROM CODE
MSB ——— LSB	MSB ——— LSB
1 1 1 1 1 1 1 1 1 1 1 0	1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 0 1	1 1 1 1 1 1 1 1 1 1 1 0
1 1 1 1 1 1 1 1 1 0 1 1	1 1 1 1 1 1 1 1 1 1 0 0
1 1 1 1 1 1 1 1 0 1 1 1	1 1 1 1 1 1 1 1 1 0 0 0
1 1 1 1 1 1 1 0 1 1 1 1	1 1 1 1 1 1 1 1 0 0 0 0
1 1 1 1 1 1 0 1 1 1 1 1	1 1 1 1 1 1 1 0 0 0 0 0
1 1 1 1 1 0 1 1 1 1 1 1	1 1 1 1 1 1 0 0 0 0 0 0
1 1 1 1 0 1 1 1 1 1 1 1	1 1 1 1 1 0 0 0 0 0 0 0
1 1 1 0 1 1 1 1 1 1 1 1	1 1 1 1 0 0 0 0 0 0 0 0
1 1 0 1 1 1 1 1 1 1 1 1	1 1 1 0 0 0 0 0 0 0 0 0
1 0 1 1 1 1 1 1 1 1 1 1	1 1 0 0 0 0 0 0 0 0 0 0
0 1 1 1 1 1 1 1 1 1 1 1	1 0 0 0 0 0 0 0 0 0 0 0
1 1 1 0 1 1 1 1 1 1 1 1	1 1 1 1 0 0 0 0 0 0 0 0
1 1 0 1 1 1 1 1 1 1 1 1	1 1 1 0 0 0 0 0 0 0 0 0
1 1 0 0 1 1 1 1 1 1 1 1	1 1 0 1 0 0 0 0 0 0 0 0
1 0 1 1 1 1 1 1 1 1 1 1	1 1 0 0 0 0 0 0 0 0 0 0
1 0 1 0 1 1 1 1 1 1 1 1	1 0 1 1 0 0 0 0 0 0 0 0
1 0 0 1 1 1 1 1 1 1 1 1	1 0 1 0 0 0 0 0 0 0 0 0
1 0 0 0 1 1 1 1 1 1 1 1	1 0 0 1 0 0 0 0 0 0 0 0
0 1 1 1 1 1 1 1 1 1 1 1	1 0 0 0 0 0 0 0 0 0 0 0
0 1 1 0 1 1 1 1 1 1 1 1	0 1 1 1 0 0 0 0 0 0 0 0
0 1 0 1 1 1 1 1 1 1 1 1	0 1 1 0 0 0 0 0 0 0 0 0
0 1 0 0 1 1 1 1 1 1 1 1	0 1 0 1 0 0 0 0 0 0 0 0
0 0 1 1 1 1 1 1 1 1 1 1	0 1 0 0 0 0 0 0 0 0 0 0
0 0 1 0 1 1 1 1 1 1 1 1	0 0 1 1 0 0 0 0 0 0 0 0
0 0 0 1 1 1 1 1 1 1 1 1	0 0 1 0 0 0 0 0 0 0 0 0
0 0 0 0 1 1 1 1 1 1 1 1	0 0 0 1 0 0 0 0 0 0 0 0

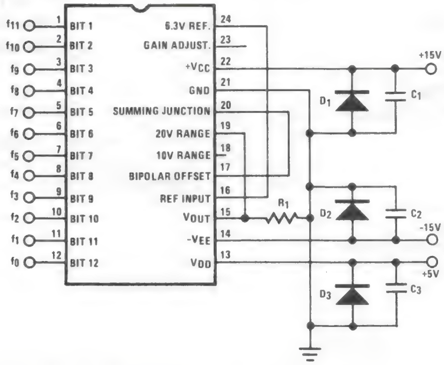
Differential Linearity Error Measurements

The DUT and the reference DAC supply the code under test to the input of the error amplifier, and the resulting output error is measured (E_1). The digital code of the DUT is then increased by 1LSB and the output error is measured a second time (E_2). The differential linearity error is calculated as,

$$\frac{(E_2 - E_1)}{\text{Volts/LSB}} - 1\text{LSB} = \text{LSB's of error.}$$

Burn-In Circuits

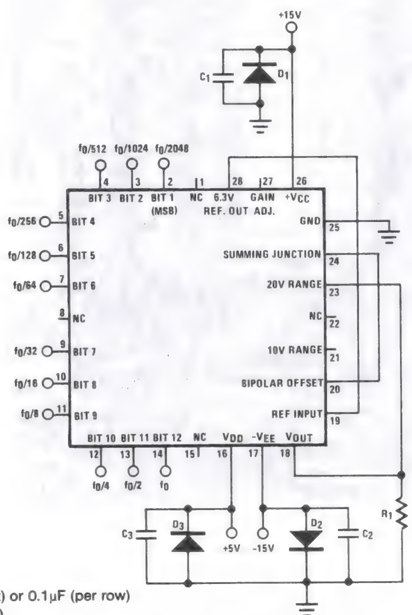
HI-5687V/883 (CERAMIC SIDEBRAZE DIP)



NOTES:
R_1 = 2.0kΩ, ± 5%, 1/2 or 1/4 Watt
C_1 - C_3 = 0.01μF (one each per socket) or 0.1μF (per row)
D_1 - D_3 = 1N4003 (one each per board)

f_0 = 100kHz	TTL Logic Levels	$f_6 = f_0/64$	TTL Logic Levels
$f_1 = f_0/2$	50% Duty Cycle	$f_7 = f_0/128$	50% Duty Cycle
$f_2 = f_0/4$		$f_8 = f_0/256$	
$f_3 = f_0/8$		$f_9 = f_0/512$	
$f_4 = f_0/16$		$f_{10} = f_0/1024$	
$f_5 = f_0/32$		$f_{11} = f_0/2048$	

HI-5687V/883 (CERAMIC LCC)



NOTES:
R_1 = 2.0kΩ, ± 5%, 1/2 or 1/4 Watt
C_1 - C_3 = 0.01μF (one each per socket) or 0.1μF (per row)
D_1 - D_3 = IN4002 (one each per board)
F_0 = 100kHz (TTL Logic Level), 50% Duty Cycle

Die Characteristics

DIE DIMENSIONS: 125 x 210 x 19 mils

METALLIZATION:

Type: Al

Thickness: 16kÅ ± 2kÅ

GLASSIVATION:

Type: Silox

Thickness: 14kÅ ± 2.0kÅ

WORST CASE CURRENT DENSITY: $2.26 \times 10^5 A/cm^2$

This device meets Glassivation Integrity Test requirement per Mil-Std-883 Method 2021 and Mil-M-38510 paragraph 3.5.5.4.

TRANSISTOR COUNT: 259

PROCESS: Bipolar-DI

DIE ATTACH:

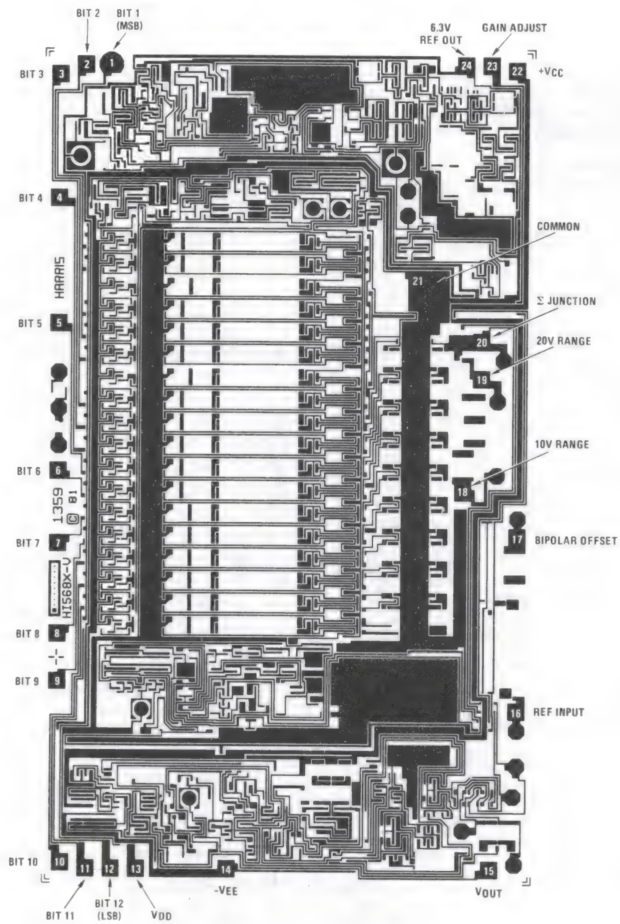
Material: Gold/Silicon Eutectic Alloy

Temperature: Ceramic DIP - 460°C (Max)

Ceramic LCC - 420°C (Max)

Metallization Mask Layout

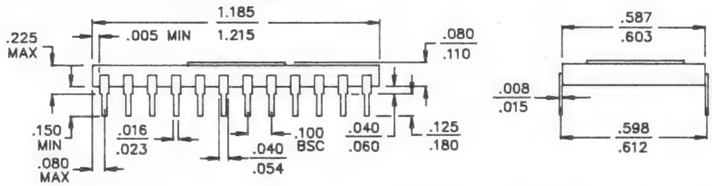
HI-5687V/883



NOTE: Pad Numbers Correspond to DIP Package Only.

Packaging†

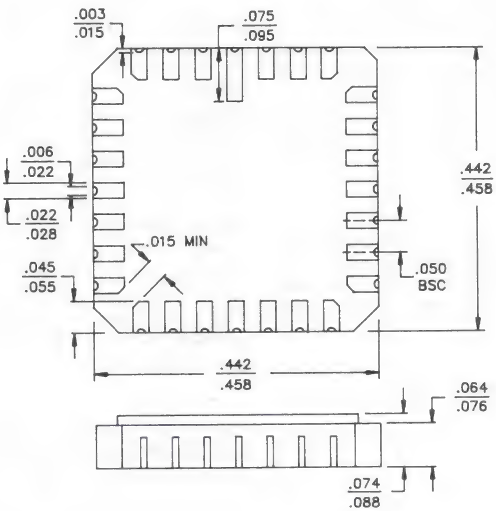
24 PIN CERAMIC SIDEBRAZE DIP



LEAD MATERIAL: Type B
LEAD FINISH: Type C
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 450°C ±10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-3

28 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ±10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-4

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$ Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

HI-5687V

DESIGN INFORMATION

Wide Temperature Range Monolithic 12-Bit Digital-to-Analog Converter

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Definitions of Specifications

Digital Inputs

The HI-5687V accepts digital input codes in complementary binary, complementary offset binary, and complementary two's complement binary.

DIGITAL INPUT	ANALOG OUTPUT		
	COMPLEMENTARY BINARY	COMPLEMENTARY OFFSET BINARY	COMPLEMENTARY TWO's COMPLEMENT*
MSB LSB			
000 . . . 000	+Full Scale	+Full Scale	-LSB
100 . . . 000	Mid Scale -1 LSB	-1 LSB	+Full Scale
111 . . . 111	Zero	-Full Scale	Zero
011 . . . 111	+1/2 Full Scale	Zero	-Full Scale

*Invert MSB with external inverter to obtain CTC Coding

Settling Time

That interval between application of a digital step input, and final entry of the analog output within a specified window about the settled value. Harris Semiconductor usually specifies a unipolar 10V full scale step, to be measured from 10% of the input digital transition, and a window of ±1/2 LSB about the final value. The device output is then rated according to the worst (longest settling) case: low to high, or high to low. In a 12 bit system ±1/2 LSB = ±0.012% of FSR.

Thermal Drift

Thermal drift is based on measurements at +25°C, +125°C (T_H) and -55°C (T_L). Drift calculations are made for the high (+125°C, +25°C) and low (+25°C, -55°C) ranges, and the larger of the two values is given as a specification representing worstcase drift.

Gain Drift, Offset Drift, Reference Drift and Total Bipolar Drift are calculated in parts per million per °C as follows:

$$\text{Gain Drift} = \frac{\Delta\ FSR/\Delta^{o}C}{FSR} \times 10^6$$

$$\text{Offset Drift} = \frac{\Delta\ Offset/\Delta^{o}C}{FSR} \times 10^6$$

$$\text{Reference Drift} = \frac{\Delta\ V_{REF}/\Delta^{o}C}{V_{REF}} \times 10^6$$

$$\text{Total Bipolar Drift} = \frac{\Delta V_O/\Delta^{o}C}{FSR} \times 10^6$$

NOTE: FSR = Full Scale Output Voltage - Zero Scale Output Voltage

Δ FSR = FSR (+125°C) - FSR (+25°C)

or FSR (+25°C) - FSR (-55°C)

V_O = Steady-state response to any input code.

Total Bipolar Drift is the variation of output voltage with temperature, in the bipolar mode of operation. It represents the net effect of drift in Gain, Offset, Linearity and Reference Voltage. Total Bipolar Drift values are calculated, based on measurements as explained above. Gain and Offset need not be calibrated to zero at +25°C. The specified limits for TBD apply for any input code.

Accuracy

LINEARITY ERROR—(Short for "Integral Linearity Error." Also, sometimes called "Integral Nonlinearity" and "Nonlinearity".)- The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to end-point linearity for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00...0 and 11...1).

DIFFERENTIAL LINEARITY ERROR—The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY—The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

TOTAL ERROR—The net output error resulting from all internal effects (primarily non-ideal Gain, Offset, Linearity and Reference Voltage). Gain and offset errors must be calibrated to zero at +25°C. Then the specified limits for Total Error apply for any input code and for any temperature within the specified operating range.

Power Supply Sensitivity

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in $+V_{CC}$, V_{DD} or $-V_{EE}$ supplies. It is specified under DC conditions and expressed as full scale range percent of change divided by power supply percent change.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied. Pin numbers correspond to DIP package only.

$$\text{P.S.S.} = \frac{\dfrac{\Delta \text{ Full Scale Range x } 100}{\text{Full Scale Range (Nominal)}}}{\dfrac{\Delta \text{ V x } 100}{\text{V (Nominal)}}}$$

Glitch

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale, i.e. the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably. (Measured as one half the product of duration and amplitude.)

Decoupling and Grounding

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in Figure 5 should be used. Decoupling capacitors should be connected close to the HI-5687V (preferably to the device pins) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

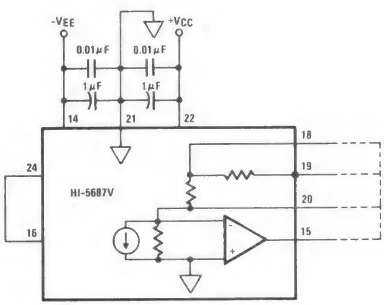


FIGURE 5.

Reference Supply

An internal 6.3 Volt reference is provided on board the HI-5687V models. This voltage reference (pin 24) must be connected to the reference input (pin 16) for specified operation. This reference may be used externally, provided current drain is limited to 2.5mA. An external buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven by the reference will result in gain variations of the HI-5687V. All gain adjustments should be made under constant load conditions.

Output Voltage Ranges

HI-5687V

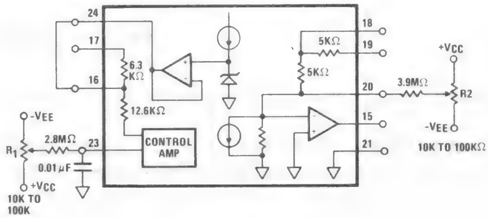


FIGURE 6.

RANGE CONNECTIONS

	RANGE	CONNECT PIN 15	PIN 17	PIN 19
Unipolar	0 to +5V	18	N.C.	20
	0 to +10V	18	N.C.	N.C.
Bipolar	±2.5V	18	20	20
	±5.0V	18	20	N.C.
	±10V	19	20	15

Gain and Offset Calibration

UNIPOLAR CALIBRATION

Step 1: Offset
- Turn all bits OFF (11...1)
- Adjust R_2 for zero volts out

Step 2: Gain
- Turn all bits ON (00...0)
- Adjust R_1 for FS-1LSB

  That is:
  4.9988 for 0 to +5V range
  9.9976 for 0 to +10V range

BIPOLAR CALIBRATION

Step 1: Offset
- Turn all bits OFF (11...1)
- Adjust R2 for Negative FS

  That Is:
  -10V for ±10V range
  -5V for ±5V range
  -2.5V for ±2.5 range

Step 2: Gain
- Turn all bits ON (00...0)
- Adjust R1 for positive FS-1LSB

  That is:
  +9.9951V for ±10V range
  +4.9976V for ±5V range
  +2.4988V for ±2.5V range

This Bipolar procedure adjusts the output range end points. The maximum error at zero (half scale) will not exceed the Linearity error. See the "Accuracy" specifications.

DESIGN INFORMATION (Continued)

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TYPICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMP	LIMITS			UNITS
					MIN	TYP	MAX	
Output Impedance	Z_O	Closed Loop, DC	10	+25°C	—	0.05	—	Ω
Internal Reference Output Impedance	REF_{OUT}	DC	10	+25°C	—	1.5	—	Ω
Output Short Circuit to GND	I_{SC}	Pin 15 to GND, Unipolar 10V Range, All Bits ON	10, 11	+25°C	—	40	—	mA

NOTES: 10. The parameters listed in this Table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

11. Under short circuit conditions, the amplifier will current limit. The duty cycle must not exceed 2.7% to maintain an acceptable current density level.

HARRIS HI-574A/883

Fast, Complete 12-Bit A/D Converter With Microprocessor Interface

July 1988

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Complete 12-Bit A/D Converter with Reference and Clock**
- **Full 8-, 12-, or 16-Bit Microprocessor Bus Interface**
- **250ns Bus Access Time (Max. Over Temp.)**
- **No Missing Codes Over Temperature**
- **Minimal Setup Time For Control Signals**
- **25μs Maximum Conversion Time**
- **Low Noise, Via Current-Mode Signal Transmission Between Chips**
- **Byte Enable/Short Cycle (A_0 Input)**
  - **Guarantees Break-Before-Make Action, Eliminating Bus Contention During Read Operation. Latched by the Start Convert Input (To Set the Conversion Length)**
- **Improved Second Source For AD574A And HS574**
- **±12V to ±15V Operation**

Applications

- **Military and Industrial Data Acquisition Systems**
- **Electronic Test And Scientific Instrumentation**
- **Process Control Systems**

Description

The HI-574A/883 is a complete 12-bit Analog-to-Digital Converter, including a +10V reference, clock, three-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice housed in a single package. The bipolar analog die features the Harris Dielectric Isolation process, which provides enhanced AC performance and freedom from latch-up.

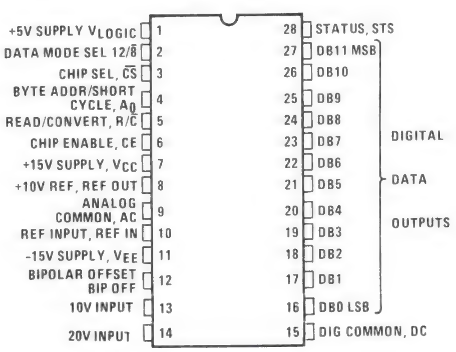
Custom design of each IC (bipolar analog and CMOS digital) has yielded improved performance over existing versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1 LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital ICs. Also, the clock oscillator is current-controlled for excellent stability over temperature. The oscillator is trimmed for a nominal conversion time of 20 ± 1μs.

The HI-574A/883 offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity, gain and offset accuracy. The buried zener reference circuit is trimmed for minimum temperature coefficient.

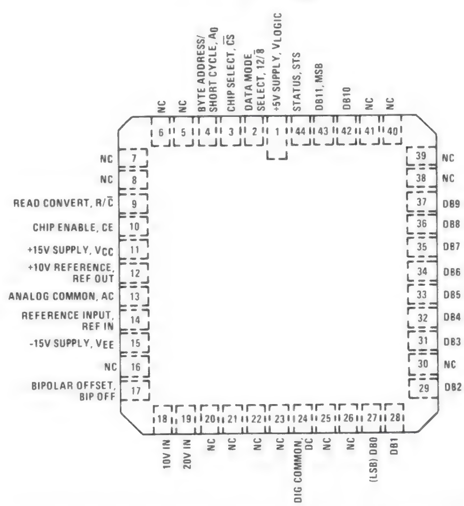
Power requirements are +5V and ±12V to ±15V, with typical dissipation of 385mW at ±12V. Two electrical grades are offered over the -55°C to +125°C temperature range. Both models are available in a 28 pin Sidebrazed DIP, or a 44 pad Ceramic LCC package.

Pinouts

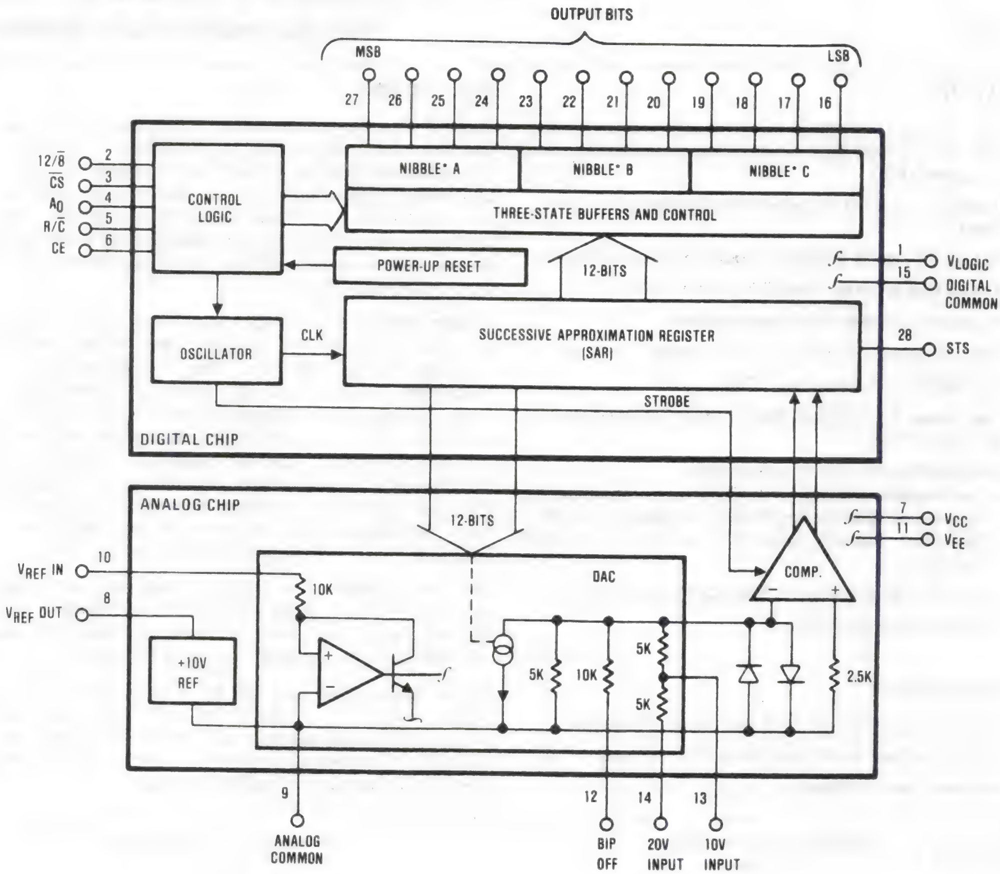
HI1-574A/883 (SIDEBRAZED DIP)
TOP VIEW



HI4-574A/883 (CERAMIC LCC)
TOP VIEW



Functional Diagram



*("NIBBLE" IS A 4-BIT DIGITAL WORD.)

Absolute Maximum Ratings

V_{CC} to Digital Ground .... 0 to +16.5V
V_{EE} to Digital Ground .... 0 to −16.5V
V_{LOGIC} to Digital Ground .... 0 to 7V
Analog Common to Digital Common .... ±1V
Control Inputs (CE, $\overline{CS}$, A0, 12/$\overline{8}$, R/$\overline{C}$) to
Digital Common .... −0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$) to
Analog Common .... ±16.5V
20 V_{IN} to Analog Common .... ±24V
REF OUT .... Indefinite Short to Common
10ms Short to V_{CC}
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering 10 Seconds) .... 275°C
Junction Temperature .... +175°C

Thermal Information

Thermal Resistance, Junction-to-Case (θ_{jc})
Sidebrazed DIP Package .... 12°C/W
Ceramic LCC Package .... 11°C/W
Thermal Resistance, Junction-to-Ambient (θ_{ja})
Sidebrazed DIP Package .... 70°C/W
Ceramic LCC Package .... 38°C/W
Power Dissipation (at +75°C)
Sidebrazed DIP Package 2.08W
Ceramic LCC Package 2.27W
Power Dissipation Derating Factor (Above +75°C)
Sidebrazed DIP Package .... 20.8mW/°C
Ceramic LCC Package .... 22.7mW/°C

Recommended Operating Conditions

Operating Temperature Range .... −55°C +125°C
$+V_{SUPPLY}$ .... +15V
$-V_{SUPPLY}$ .... −15V
$-V_{LOGIC}$ .... +5V
V_{REF} .... +10V
Analog Input Voltage, $10V_{IN}$ .... ±5V or 0 to +10V
Analog Input Voltage, $20V_{IN}$ .... ±10V or 0 to +20V
Logic Level Low (V_{IL}) .... 0V to 0.8V
Logic Level High (V_{IH}) .... 2.4V to+ 5V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested At V_{CC} = +15V, V_{EE} = -15V, V_{LOG} = 5.0V, Unless Otherwise Specified.

(Note 1) DC PARAMETER	SYMBOL	(Fig. 1, 2 & Note 1, Chart A Apply Unless Otherwise Noted) CONDITIONS	GROUP A SUBGROUPS	TEMP	LIMITS HI-574AS MIN	HI-574AS MAX	HI-574AT MIN	HI-574AT MAX	UNITS
Power Supply Current From V_{CC}	I_{CC}	Output Code = 000000000000 and 111111111111 (Note 2)	1	+25°C		15		15	mA
			2, 3	+125°C, -55°C		16		15	mA
Power Supply Current From V_{EE}	I_{EE}	Output Code = 000000000000 and 111111111111 (Note 2)	1	+25°C		28		28	mA
			2, 3	+125°C, -55°C		32		30	mA
Power Supply Current From V_{LOGIC}	I_{LOG}	Output Code = 000000000000 and 111111111111 (Note 2)	1	+25°C		15		15	mA
			2, 3	+125°C, -55°C		17		17	mA
Power Dissipation	P_d	Calculated Worst Case of 2 Conditions (Note 3)	1	+25°C		720		720	mW
			2, 3	+125°C, -55°C		805		760	mW
Input Low Current	I_{IL}	V_{LOG} = 5.5V V_{IN}(LOGIC) = 0.0V	1	+25°C	-5	5	-5	5	μA
			2, 3	+125°C, -55°C	-5	5	-5	5	μA
Input High Current	I_{IH}	V_{LOG} = 5.5V V_{IN}(LOGIC) = 2.4V	1	+25°C	-5	5	-5	5	μA
			2, 3	+125°C, -55°C	-5	5	-5	5	μA
		V_{IN}(LOGIC) = 5.5V	1	+25°C	-5	5	-5	5	μA
			2, 3	+125°C, -55°C	-5	5	-5	5	μA
High Impedance State Output Current	I_{ZL}	V_{LOG} = 5.5V V_{IN} = 11.0V Min Output Code = 111111111111 Set R/$\overline{C}$ = Logic "0" Output Bits 1 thru 12 Measured Separately V_O = 0.0V all Bits (Note 2)	1	+25°C	-5	5	-5	5	μA
			2, 3	+125°C, -55°C	-5	5	-5	5	μA

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Devices Tested At V_{CC} = +15V, V_{EE} = -15V, V_{LOG} = 5.0V, Unless Otherwise Specified.

(Note 1) DC PARAMETER	SYMBOL	(Fig. 1, 2 & Note 1 Apply Unless Otherwise Noted) CONDITIONS	GROUP A SUBGROUPS	TEMP	LIMITS HI-574AS MIN	LIMITS HI-574AS MAX	LIMITS HI-574AT MIN	LIMITS HI-574AT MAX	UNITS
High Impedance State Output Current	I_{ZH}	V_{LOG} = 5.5V V_{IN} = -1.0V Max Output Code = 000000000000 Set $R/\overline{C}$ = Logic "0" Output Bits 1 thru 12 Measured Separately V_O = 5.5V All Bits (Note 2)	1	+25°C	-5	5	-5	5	μA
			2, 3	+125°C, -55°C	-5	5	-5	5	μA
Output Logic Voltage Levels	V_{OL}	V_{LOG} = 5.0V Output Code = 000000000000 Measure Output Bits 1 thru 12 & STS I_L = 1.6mA (Note 2)	1	+25°C	-0.5	0.4	-0.5	0.4	V
			2, 3	+125°C, -55°C	-0.5	0.4	-0.5	0.4	V
	V_{OH}	V_{LOG} = 4.5 Output Code = 111111111111 Measure Bits 1 thru 12 I_L = -0.5mA (Note 2)	1	+25°C	2.4	5.5	2.4	5.5	V
			2, 3	+125°C, -55°C	2.4	5.5	2.4	5.5	V
Reference Voltage	V_{REF}	Output Code = 000000000000 Bipolar, VFSR = 20V I_L = 2.0mA (Notes 2, 4)	1	+25°C	9.970	10.030	9.970	10.030	V
			2, 3	+125°C, -55°C	9.950	10.050	9.950	10.050	V
Power Supply Sensitivity To V_{CC}	$+PSS_1$	13.5V ≤ V_{CC} ≤ 16.5V Output Transition = 11111111111X-00000000000X (Note 5)	1	+25°C	-2	2	-1	1	LSB
			2, 3	+125°C, -55°C	-2.5	2.5	-1.5	1.5	LSB
	$+PSS_2$	11.4V ≤ V_{CC} ≤ 12.6V Output Transition = 11111111111X-00000000000X (Note 5)	1	+25°C	-2	2	-1	1	LSB
Power Supply Sensitivity To V_{LOG}	$+PSS_3$	4.5V ≤ V_{LOG} ≤ 5.5V Output Transition = 11111111111X-00000000000X (Note 5)	1	+25°C	-0.5	0.5	-0.5	0.5	LSB
			2, 3	+125°C, -55°C	-0.5	0.5	-0.5	0.5	LSB
Power Supply Sensitivity To V_{EE}	$-PSS_1$	-16.5 ≤ V_{EE} ≤ -13.5V Output Transition = 11111111111X-00000000000X (Note 5)	1	+25°C	-2	2	-1	1	LSB
			2, 3	+125°C, -55°C	-2.5	2.5	-2	2	LSB
	$-PSS_2$	-12.6V ≤ V_{EE} ≤ -11.4V Output Transition = 11111111111X-00000000000X (Note 5)	1	+25°C	-2	2	-1	1	LSB
Unipolar Offset Voltage	V_{IO}	Output Transition = 00000000000X (Note 5)	1	+25°C	-2	2	-2	2	LSB
			2, 3	+125°C, -55°C	-4	4	-3	3	LSB
Bipolar Zero	BZ	Output Transition = XXXXXXXXXXXX Bipolar, VFSR = 20V (Note 5)	1	+25°C	-10	10	-4	4	LSB
			2, 3	+125°C, -55°C	-14	14	-6	6	LSB

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Devices Tested At V_{CC} = +15V, V_{EE} = -15V, V_{LOG} = 5.0V, Unless Otherwise Specified.

(Note 1) DC PARAMETER	SYMBOL	(Figure 1, 2 & Note 1 Apply Unless Otherwise Noted) CONDITIONS	GROUP A SUBGROUPS	TEMP	LIMITS HI-574AS MIN	HI-574AS MAX	HI-574AT MIN	HI-574AT MAX	UNITS
Gain Error	A_E	Output Transition = 00000000000X to 11111111111X (Note 5)	1	+25°C	-0.3	0.3	-0.3	0.3	% of FSR
			2, 3	+125°C, -55°C	-0.8	0.8	-0.55	0.55	
	BPA_E	Bipolar, VFSR = 20V (Note 5)	1	+25°C	-0.3	0.3	-0.3	0.3	% of
			2, 3	+125°C, -55°C	-0.8	0.8	-0.55	0.55	FSR
Integral Linearity Error	L_E	Abbreviated Test (Note 5)	1	+25°C	-1	1	-1/2	1/2	LSB
			2, 3	+125°C, -55°C	-1	1	-1	1	LSB
Differential Linearity Error	DL_E	Abbreviated Test (Note 5)	1	+25°C	-2	2	-1	1	LSB
			2, 3	+125°C, -55°C	-2	2	-1	1	LSB
Input Resistance	R_i10V	10V Span Input (Note 11)	1	+25°C	3.75	6.25	3.75	6.25	KΩ
			2, 3	+125°C, -55°C	3	7	3	7	KΩ
	R_i20V	20V Span Input (Note 11)	1	+25°C	7.50	12.50	7.50	12.50	KΩ
			2, 3	+125°C, -55°C	6	14	6	14	KΩ
Unipolar Offset Voltage Drift	$\frac{dV_{IO}}{dT}$	Output Transition = 00000000000X (Note 5)	2, 3	+125°C, -55°C	-2	2	-1	1	LSB
Bipolar Zero Drift	$\frac{dB_Z}{dT}$	Output Transition = XXXXXXXXXXXX Bipolar, VFSR = 20V (Note 5)	2, 3	+125°C, -55°C	-4	4	-2	2	LSB
Gain Error Drift	$\frac{dA_E}{dT}$	Output Transition = 00000000000X to 11111111111X (Note 5)	2, 3	+125°C, -55°C	-20	20	-10	10	LSB
	$\frac{dBPA_E}{dT}$	Bipolar, VFSR = 20V (Note 5)	2, 3	+125°C, -55°C	-20	20	-10	10	LSB

6

DATA CONVERSION PRODUCTS

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested At V_{CC} = +15V, V_{EE} = -15V, V_{LOG} = 5.0V, Unless Otherwise Specified.

(Note 1) AC PARAMETER	SYMBOL	(Figure 1, 2 & Note 1 Apply Unless Otherwise Noted) CONDITIONS	GROUP A SUBGROUPS	TEMP	LIMITS HI-574AS MIN	LIMITS HI-574AS MAX	LIMITS HI-574AT MIN	LIMITS HI-574AT MAX	UNITS
Conversion Time	t_C	V_{IN} = -1V Max Output Code = 000000000000 8 Bit Cycle (Note 5)	9	+25°C	10	17	10	17	μs
			10, 11	+125°C, -55°C	10	17	10	17	μs
		V_{IN} = 11V Max Output Code = 111111111111 12 Bit Cycle (Note 5)	9	+25°C	15	25	15	25	μs
			10, 11	+125°C, -55°C	15	25	15	25	μs

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Characterized at V_{CC} = +15V, V_{EE} = -15V, V_{LOG} = 5.0V Unless Otherwise Specified. Load is 3kΩ, 50pF where applicable. Figures 3, 4, 5, & 6 apply Unless Otherwise Noted.

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMP	HI-574AS/883 HI-574AT/883 MIN	HI-574AS/883 HI-574AT/883 MAX	UNITS
STS Delay From R/$\overline{C}$	t_{DS}	Low to High Transition Referenced to High to Low R/$\overline{C}$ Transition. Output Code = 000000000000	1, 5, 10	+25°C		200	ns
				+125°C, -55°C		600	ns
Low R/$\overline{C}$ Pulse Width	t_{HRL}	Minimum R/$\overline{C}$ Pulse Width Required to Start a Conversion	1, 10	+25°C	50		ns
				+125°C, -55°C	350		ns
Data Valid After R/$\overline{C}$ Low	t_{HDR}	Output Data Valid, Referenced to High to Low R/$\overline{C}$ Transition Output Code = 000000000000 & 111111111111	1, 2, 10	+25°C	25		ns
				+125°C, -55°C	15		ns
STS Delay After Data Valid	t_{HS}	STS High to Low Transition Referenced to Valid Output Data Output Code = 000000000000 & 111111111111	1, 2, 10	+25°C	300	1200	ns
High R/$\overline{C}$ Pulse Width	t_{HRH}	Minimum R/$\overline{C}$ Pulse Width Required to Enable Output Bits Output Code = 000000000000 & 111111111111	1, 2, 10	+25°C	150		ns
				+125°C, -55°C	300		ns
Data Access Time	t_{DDR}	Output Data Valid, Referenced to Low to High R/$\overline{C}$ Transition Output Code = 000000000000 & 111111111111	1, 2, 10	+25°C		150	ns
				+125°C, -55°C		250	ns
STS Delay From CE	t_{DSC}	Low to High Transition, Referenced to Low to High CE Transition Output Code = 000000000000	1, 2, 10	+25°C		200	ns
				+125°C, -55°C		350	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Devices Characterized at V_{CC} = +15V, V_{EE} = −15V, V_{LOG} = 5.0V Unless Otherwise Specified. Load is 3kΩ, 50pF where applicable. Figures 3, 4, 5, & 6 apply Unless Otherwise Noted.

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMP	HI-574AS/883 HI-574AT/883		UNITS
					MIN	MAX	
CE Pulse Width	t_{HEC}	Minimum CE Pulse Width Required to Start a Conversion	1, 10	+25°C	50		ns
				+125°C, -55°C	300		ns
$\overline{CS}$ to CE Setup	t_{SSC}	Minimum Time Required From a High to Low $\overline{CS}$ Transition to Low to High CE Transition for a Conversion to Start from CE	1, 10	+25°C	50		ns
$\overline{CS}$ Low During CE High	t_{HSC}	Minimum Time Required From a Low to High CE Transition to Low to High $\overline{CS}$ Transition for a Conversion to Start	1, 10	+25°C	50		ns
$R/\overline{C}$ To CE Set-Up	t_{SRC}	Minimum Time Required From a High to Low $R/\overline{C}$ Transition to Low to High CE Transition for a Conversion to Start from CE.	1, 10	+25°C	50		ns
$R/\overline{C}$ Low During CE High	t_{HRC}	Minimum Time Required From a Low to High CE Transition to Low to High $R/\overline{C}$ Transition for a Conversion to Start	1, 10	+25°C	50		ns
A_0 To CE Set-Up	t_{SAC}	Minimum Time Required From a Low to High or High to Low A_0 Transition to Low to High CE Transition to Initiate an 8-bit or 12-bit Conversion, Respectively.	1, 10	+25°C	0		ns
A_0 Valid During CE High	t_{HAC}	Minimum Time Required From a Low to High CE Transition to Low to High or High to Low to Low A_0 Transition to Guarantee a 12-bit or 8-bit Conversion, Respectively.	1, 10	+25°C	50		ns
Access Time From CE	t_{DD}	Output Data Valid, Referenced to Low to High CE Transition Output Code = 000000000000 & 111111111111	1, 2, 10	+25°C		150	ns
				+125°C, -55°C		250	ns
Data Valid After CE Low	t_{HD}	Output Data Valid, Referenced to High to Low CE Transition Output Code = 000000000000 & 111111111111	1, 2, 10	+25°C	25		ns
				+125°C, -55°C	15		ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Devices Characterized at V_{CC} = +15V, V_{EE} = −15V, V_{LOG} = 5.0V Unless Otherwise Specified. Load is 3kΩ, 50pF where applicable. Figures 3, 4, 5, & 6 apply Unless Otherwise Noted.

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMP	HI-574AS/883 HI-574AT/883 MIN	MAX	UNITS
Output Float Delay	t_{HL}	Output Delay to HI-Z, Referenced to High to Low CE Transition Output Code = 000000000000 & 111111111111	1, 2, 10	+25°C, +125°C, -55°C		150	ns
$\overline{CS}$ To CE Setup	t_{SSR}	Minimum Time from $\overline{CS}$ High to Low Transition to CE Low to High Transition to Guarantee Data Valid is Controlled by CE. Output Code = 000000000000 & 111111111111	1, 2, 10	+25°C	50		ns
R/$\overline{C}$ to CE Set-Up	t_{SRR}	Minimum Time from R/$\overline{C}$ Low to High Transition To CE Low to High Transition to Guarantee Data Valid is Controlled by CE. Output Code = 000000000000 & 111111111111	1, 2, 10	+25°C	0		ns
A_0 To CE Set-Up	t_{SAR}	Minimum Time From A_0 High to Low or Low to High Transition to CE Low to High Transition to guarantee the correct byte gets enabled.	1, 10	+25°C	50		ns
$\overline{CS}$ Valid After CE Low	t_{HSR}	Minimum Time from CE High to Low Transition to $\overline{CS}$ Low to High Transition to Guarantee High Impedance State is Controlled by CE.	1, 10	+25°C	0		ns
R/$\overline{C}$ High After CE Low	t_{HRR}	Minimum Time from CE High to Low Transition to R/$\overline{C}$ High to Low Transition to Guarantee Device Will Disable Before Another Conversion is Initiated.	1, 10	+25°C	0		ns
A_0 Valid After CE Low	t_{HAR}	Minimum Time From CE High to Low Transition to A_0 High to Low or Low to High Transition to Guarantee Enabled Byte Does Not Change Until Device Is Disabled	1, 10	+25°C	50		ns

TABLE 4. ELECTRICAL TEST REQUIREMENTS

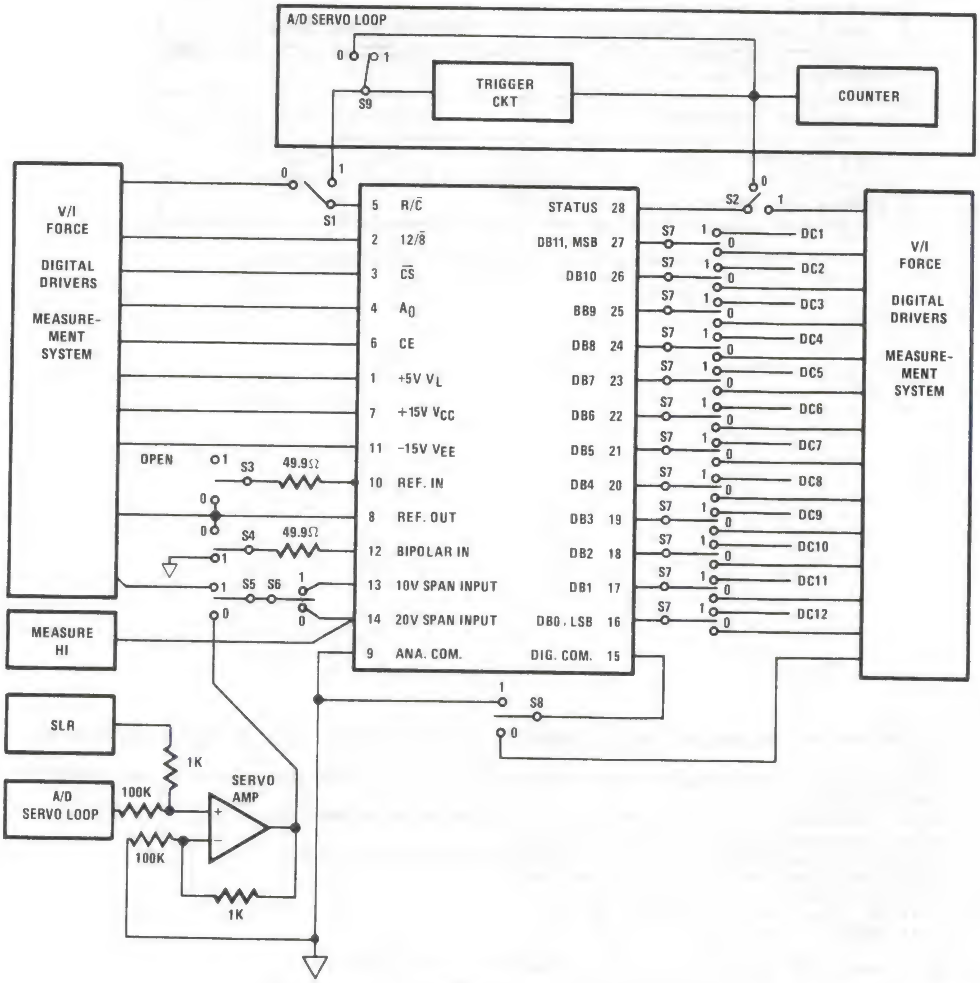
MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

*PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

NOTES:

1. See definitions.
2. A output code of 0000 0000 0000 is guaranteed by an input voltage V_{IN} = -1V and an output code of 1111 1111 1111 is guaranteed by an input voltage V_{IN} = 11V.
3. $P_d = (V_{CC} \cdot I_{CC} + V_{EE} \cdot I_{EE} + V_{LOGIC} \cdot I_{LOGIC})$ Power dissipation shall be calculated using the two output code conditions 0000 0000 0000 and 1111 1111 1111.
4. The reference voltage external load current shall be constant direct current and shall not exceed 2mA.
5. X represents the transition point between two adjacent code-words
   (ie: 0000 0000 000X represents the transition between code-words 0000 0000 0000 and 0000 0000 0001,
   XXXX XXXX XXXX represents the transition between code-words
   0111 1111 1111 and 1000 0000 0000 and
   1111 1111 111X represents the transition between code-words
   1111 1111 1110 and 1111 1111 1111).
6. Implies a falling edge transition from 2.4V to 0.8V, after remaining input pins are set.
7. Implies a falling edge transition from 2.4V to 0.8V, after remaining input pins are set, then, after a minimum of 200ns, a rising edge transition to 2.4V.
8. Implies a rising edge transition from 0.8V to 2.4V after remaining input pins are set.
9. R/$\bar{C}$ Implies a falling edge from 2.4V to a TTL Low, approximately 0.0V.
10. The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
11. A conversion must be performed at the inputted voltage prior to R_i10V and R_i20V measurements.

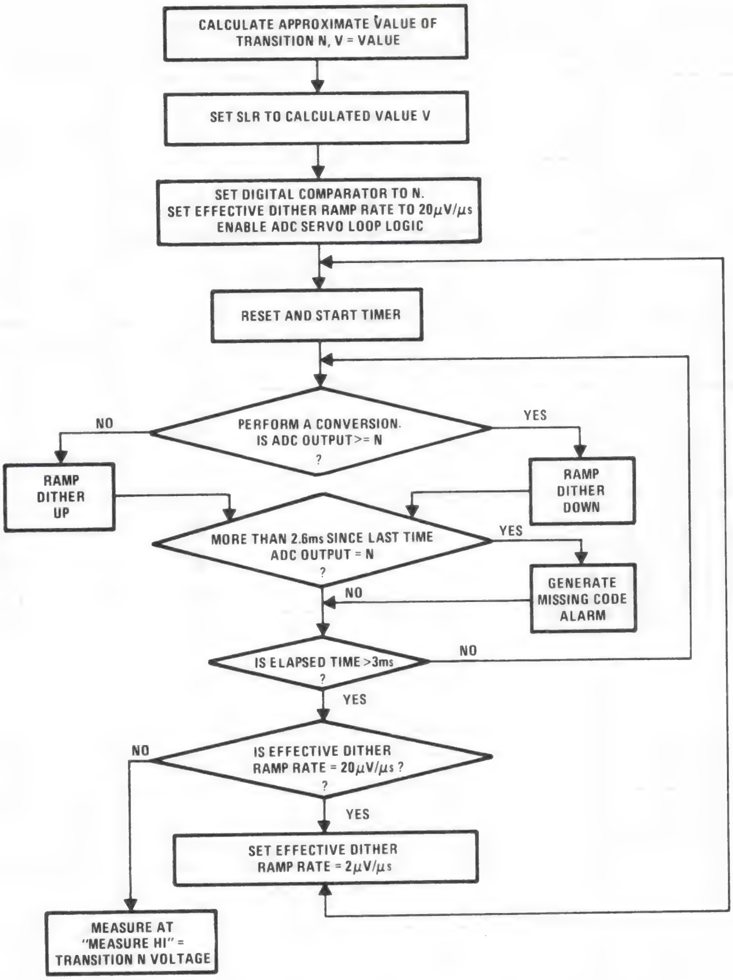
Test Circuit and Test Conditions



NOTES:
1. The connections of the V/I force, digital drivers, and measurement system are software controlled.
2. DC1 → DC12 are input bits of the digital comparator in the A/D servo loop.
3. SLR ==> super linear reference.

FIGURE 1. TEST CIRCUIT

Test Circuit and Test Conditions (Continued)



NOTES:

1. SLR = Super Linear Reference.
2. See Figure 1 for Test Circuit.

FIGURE 2. TEST FLOW FOR ANALOG TO DIGITAL SERVO LOOP

CHART A. GROUP A TEST CONDITIONS

SYMBOL	APPLIED VOLTAGES REF. ANALOG COMMON (FIG. 1, NOTE 1)									APPLIED DIGITAL CODEWORD	DUT DIGITAL OUTPUT CODEWORD	SWITCH POSITIONS	MEASUREMENT SENSE LINES REF. ANA. COMMON			TEMP °C	EQUATIONS & NOTES
	7	11	1	13/14	2	3	4	5	6								
	V_{CC} (V)	V_{EE} (V)	V_{LOG} (V)	V_{IN} (V)	$12/\overline{8}$ (V)	$\overline{CS}$ (V)	A_0 (V)	$R/\overline{C}$ (V)	CE (V)	$DC_1 \leftrightarrow DC_{12}$ MSB ↔ LSB	27 ↔ 16 MSB ↔ LSB	$S_1 \leftrightarrow S_9$	PIN	VALUE	UNIT		
I_{CC1} I_{CC2}	+15 +15	-15 -15	+5.0 +5	-1 11	2.4 2.4	0.8 0.8	0.8 0.8		2.4 2.4		000000000000 111111111111	010111011 010111011	7 7	I_1 I_2	mA mA	+25, +125, -55	$I_{CC1} = I_1$ $I_{CC2} = I_2$
I_{EE1} I_{EE2}	+15 +15	-15 -15	+5 +5	-1 11	2.4 2.4	0.8 0.8	0.8 0.8		2.4 2.4		000000000000 111111111111	010111011 01011011	11 11	I_3 I4	mA mA	+25, +125, -55	$I_{EE1} = I_3$ $I_{EE2} = I4$
I_{LOG1} I_{LOG2}	+15 +15	-15 -15	+5 +5	-1 11	2.4 2.4	0.8 0.8	0.8 0.8		2.4 2.4		000000000000 111111111111	010111011 010111011	1 1	I_5 I_6	mA mA	+25, +125. -55	$I_{LOG1} = I_5$ $I_{LOG2} = I_6$
P_{D1} P_{D2}	+15 +15	-15 -15	+5 +5	-1 11							000000000000 111111111111					+25, +125, -55	$P_{D1} = (I_{CC1})(V_{CC}) + (I_{EE1})(V_{EE}) + (I_{LOG1})(V_{LOG})$ $P_{D2} = (I_{CC2})(V_{CC}) + (I_{EE2})(V_{EE}) + (I_{LOG2})(V_{LOG})$
I_{IL1} thru I_{IL5}	+15	-15	+5.5	-1	0	0	0	0	0			010111011	2 thru 6	I_7 thru I_{11}	μA	+25, +125, -55	I_{IL1} thru I_{IL5} = I_7 thru I_{11} Respectively
I_{IH1} thru I_{IH5}	+15	-15	+5.5	11	2.4	2.4	2.4	2.4	2.4			010111011	2 thru 6	I_{12} thru I_{16}	μA	+25, +125, -55	I_{IH1} thru I_{IH5} = I_{12} thru I_{16} Respectively
I_{IH6} thru I_{IH10}	+15	-15	+5.5	11	5.5	5.5	5.5	5.5	5.5			010111011	2 thru 6	I_{17} thru I_{21}	μA	+25, +125, -55	I_{IH6} thru I_{IH10} = I_{17} thru I_{21} Respectively
I_{ZL1} thru I_{ZL12}	+15	-15	+5.5	11	2.4	0.8	0.8		2.4		000000000000	010111011	16 thru 27	I_{22} thru I_{33}	μA	+25, +125, -55	I_{ZL1} thru I_{ZL12} = I_{22} thru I_{33} Respectively. V_O = 0.0V (Note 9)
I_{ZH1} thru I_{ZH12}	+15	-15	+5.5	-1	2.4	0.8	0.8		2.4		111111111111	010111011	16 thru 27	I_{34} thru I_{45}	μA	+25, +125, -55	I_{ZH1} thru I_{ZH12} = I_{34} thru I_{45} Respectively. V_O = 5.5V (Note 9)
V_{OL1} thru V_{OL13}	+15	-15	+5.0	-1	2.4	0.8	0.8		2.4		000000000000	010111011	16 thru 28	E_1 thru E_{13}	V	+25, +125, -55	V_{OL1} thru V_{OL13} = E_1 thru E_{13} Respectively. I_L = 1.6mA
V_{OH1} thru V_{OH12}	+15	-15	+4.5	11	2.4	0.8	0.8		2.4		111111111111	010111011	16 thru 27	E_{14} thru E_{25}	V	+25, +125, -55	V_{OH1} thru V_{OH12} = E_{14} thru E_{25} Respectively. I_L = -0.5mA

CHART A. GROUP A TEST CONDITIONS (Continued)

SYMBOL	APPLIED VOLTAGES REF. ANALOG COMMON (FIG. 1, NOTE 1)									APPLIED DIGITAL CODEWORD	DUT DIGITAL OUTPUT CODEWORD	SWITCH POSITIONS	MEASUREMENT SENSE LINES REF. ANA. COMMON			TEMP °C	EQUATIONS & NOTES
	7	11	1	13/14	2	3	4	5	6								
	V_{CC} (V)	V_{EE} (V)	V_{LOG} (V)	V_{IN} (V)	$12/\overline{8}$ (V)	$\overline{CS}$ (V)	A_0 (V)	$R/\overline{C}$ (V)	CE (V)	$DC_1 \leftrightarrow DC_{12}$ MSB ↔ LSB	27 ↔ 16 MSB ↔ LSB	$S_1 \leftrightarrow S_9$	PIN	VALUE	UNIT		
V_{REF1}	+15	-15	+5	-1	2.4	0.8	0.8		2.4		000000000000	011111011	8	E_{26}	V	+25, +125, -55	$V_{REF1} = E_{27}$ $I_L = 0mA$
V_{REF2}	+15	-15	+5	-11	2.4	0.8	0.8		2.4		00000000000	010011011	8	E_{27}	V		$V_{REF2} = E_{28}, I_L = 2.0mA$ Bipolar, $V_{FSR} = 20V$
$+P_{SS1}$	13.5 13.5 16.5 16.5	-15 -15 -15 -15	5.0 5.0 5.0 5.0	SERV LOOP	2.4	0.8	0.8	TRIG CKT.	2.4	000000000000 111111111110 000000000000 111111111110	00000000000X 11111111111X 00000000000X 11111111111X	100101111	14	E_{200} E_{201} E_{202} E_{203}	V V V V	+25, +125, -55	$+P_{SS1} = [(E_{203} - E_{202}) - (E_{201} - E_{200})]/[(E_{42X} - E_{41X})/4094]$ Where X = R for +25°C = H for 125°C = L for -55°C
$+P_{SS2}$	11.4 11.4 12.6 12.6	-15 -15 -15 -15	5.0 5.0 5.0 5.0	SERV LOOP	2.4	0.8	0.8	TRIG CKT.	2.4	000000000000 111111111110 000000000000 111111111110	00000000000X 11111111111X 00000000000X 11111111111X	100101111	14	E_{204} E_{205} E_{206} E_{207}	V V V V	+25, +125, -55	$+P_{SS2} = [(E_{207} - E_{206}) - (E_{205} - E_{204})]/[(E_{42X} - E_{41X})/4094]$ Where X = R for +25°C = H for 125°C = L for -55°C
$+P_{SS3}$	+15 +15 +15 +15	-15 -15 -15 -15	4.5 4.5 5.5 5.5	SERV LOOP	2.4	0.8	0.8	TRIG CKT.	2.4	000000000000 111111111110 000000000000 111111111110	00000000000X 11111111111X 00000000000X 11111111111X	100101111	14	E_{208} E_{209} E_{210} E_{211}	V V V V	+25, +125, -55	$+P_{SS3} = [(E_{211} - E_{210}) - (E_{209} - E_{208})]/[(E_{42X} - E_{41X})/4094]$ Where X = R for +25°C = H for 125°C = L for -55°C
$-P_{SS1}$	+15 +15 +15 +15	-13.5 -13.5 -16.5 -16.5	5.0 5.0 5.0 5.0	SERV LOOP	2.4	0.8	0.8	TRIG CKT.	2.4	000000000000 111111111110 000000000000 111111111110	00000000000X 11111111111X 00000000000X 11111111111X	100101111	14	E_{212} E_{213} E_{214} E_{215}	V V V V	+25, +125, -55	$-P_{SS1} = [(E_{215} - E_{214}) - (E_{213} - E_{212})]/[(E_{42X} - E_{41X})/4094]$ Where X = R for +25°C = H for 125°C = L for -55°C
$-P_{SS2}$	+15 +15 +15 +15	-11.4 -11.4 -12.6 -12.6	5.0 5.0 5.0 5.0	SERV LOOP	2.4	0.8	0.8	TRIG CKT.	2.4	000000000000 111111111110 000000000000 111111111110	00000000000X 11111111111X 00000000000X 11111111111X	100101111	14	E_{216} E_{217} E_{218} E_{219}	V V V V	+25°C +125, -55	$-P_{SS2} = [(E_{219} - E_{218} - (E_{217} - E_{216})]/[(E_{42X} - E_{41X})/4094]$ Where X = R for +25°C = H for 125°C = L for -55°C

CHART A. GROUP A TEST CONDITIONS (Continued)

SYMBOL	APPLIED VOLTAGES REF. ANALOG COMMON (FIG 1, NOTE 1)									APPLIED DIGITAL CODEWORD	DUT DIGITAL OUTPUT CODEWORD	SWITCH POSITIONS	MEASUREMENT SENSE LINES REF. ANA. COMMON			TEMP °C	EQUATIONS & NOTES
	7	11	1	13/14	2	3	4	5	6								
	V_{CC} (V)	V_{EE} (V)	V_{LOG} (V)	V_{IN} (V)	$12/\overline{8}$ (V)	$\overline{CS}$ (V)	A_0 (V)	$R/\overline{C}$ (V)	CE (V)	$DC_1 \leftrightarrow DC_{12}$ MSB ↔ LSB	27 ↔ 16 MSB ↔ LSB	$S_1 \leftrightarrow S_9$	PIN	VALUE	UNIT		
V_{IOR}	+15	-15	+5	SERV LOOP	2.4	0.8	0.8	TRIG CKT.	2.4	000000000000	00000000000X	100101111	14	E_{38R}	V	+25	V_{IOR} = $((E_{38R})-(0.5\ AR / 4095))/(AR / 4095)$
V_{IOH}	+15	-15	+5		2.4	0.8	0.8		2.4	000000000000	00000000000X	100101111	14	E_{38H}	V	+125	V_{IOH} ==> Same as V_{IOR} with R = H
V_{IOL}	+15	-15	+5		2.4	0.8	0.8		2.4	000000000000	00000000000X	100101111	14	E_{38L}	V	-55	V_{IOL} ==> Same as V_{IOR} with R = L
B_{ZR}	+15	-15	+5	SERV LOOP	2.4 2.4	0.8 0.8	0.8 0.8	TRIG CKT.	2.4 2.4	011111111111 100000000000	XXXXXXXXXXXX 10000000000X	100000111	14 14	E_{39R} E_{40R}	V V	+25	B_{ZR} = $((E_{39R} + E_{40R})/2)/(B_{AR} /4095)$
B_{ZH}	+15	-15	+5		2.4 2.4	0.8 0.8	0.8 0.8		2.4 2.4	011111111111 100000000000	XXXXXXXXXXX 10000000000X	100000111	14 14	E_{39H} E_{40H}	V V	+125	B_{ZH} ==> Same as B_{ZR} with R = H
B_{ZL}	+15	-15	+5		2.4 2.4	0.8 0.8	0.8 0.8		2.4 2.4	011111111111 100000000000	XXXXXXXXXXXX 10000000000X	100000111	14 14	E_{39L} E_{40L}	V V	-55	B_{ZL} ==> Same as B_{ZR} with R = L
A_{ER}	+15	-15	+5	SERV LOOP	2.4 2.4	0.8 0.8	0.8 0.8	TRIG CKT.	2.4 2.4	000000000000 111111111110	00000000000X 11111111111X	100101111	14 14	E_{41R} E_{42R}	V V	+25	$A_R = (E_{42R} - E_{41R})$ $[(E_{42R} - E_{41R})/4094]$
																+25	A_{ER} = [(AR - 9.99756V)/10V]100
A_{EH}	+15	-15	+5		2.4 2.4	0.8 0.8	0.8 0.8		2.4 2.4	000000000000 111111111110	00000000000X 11111111111X	100101111	14 14	E_{41H} E_{42H}	V V	+125	A_{EH} ==> Same as A_{ER} with R = H
A_{EL}	+15	-15	+5		2.4 2.4	0.8 0.8	0.8 0.8		2.4 2.4	000000000000 111111111110	000000000000X 11111111111X	100101111	14 14	E_{41L} E_{42L}	V V	-55	A_{EL} ==> Same as A_{ER} with R = L
BA_{ER}	+15	-15	+5	SERV LOOP	2.4 2.4	0.8 0.8	0.8 0.8	TRIG CKT.	2.4 2.4	000000000000 111111111110	00000000000X 11111111111X	100000111	14 14	E_{43R} E_{44R}	V V	+25	$BA_R = (E_{44R} - E_{43R})$ + $[(E_{44R} - E_{42R})/4094]$
																+25	BA_{ER} = [(BAR - 19.99512V)/ 20V]100
BA_{EH}	+15	-15	+5		2.4 2.4	0.8 0.8	0.8 0.8		2.4 2.4	000000000000 111111111110	00000000000X 11111111111X	100000111	14 14	E_{43H} E_{44H}	V V	+125	BA_{EH} ==> Same as BA_{ER} with R = H
BA_{EL}	+15	-15	+5		2.4 2.4	0.8 0.8	0.8 0.8		2.4 2.4	000000000000 111111111110	00000000000X 11111111111X	100000111	14 14	E_{43L} E_{44L}	V V	-55	BA_{EL} ==> Same as BA_{ER} with R = L

CHART A. GROUP A TEST CONDITIONS

SYMBOL	APPLIED VOLTAGES REF ANALOG COMMON (FIG. 1, NOTE 1)									APPLIED DIGITAL CODEWORD	DUT DIGITAL OUTPUT CODEWORD	SWITCH POSITIONS	MEASUREMENT SENSE LINES REF. ANA. COMMON			TEMP °C	EQUATIONS & NOTES
	7	11	1	13/14	2	3	4	5	6								
	V_{CC} (V)	V_{EE} (V)	V_{LOG} (V)	V_{IN} (V)	$12/\overline{8}$ (V)	$\overline{CS}$ (V)	A_0 (V)	$R/\overline{C}$ (V)	CE (V)	$DC_1 \leftrightarrow DC_{12}$ MSB ↔ LSB	27 ↔ 16 MSB ↔ LSB	$S_1 \leftrightarrow S_9$	PIN	VALUE	UNIT		
																+25, +125, -55	For Endpoint Linearity Error $L_{E(N)} = ((E(N+45) + E(N+46))/2) - V(IDEAL)/S$ $V(IDEAL) = (N1)(S) + E_{46} - S/2$ N1 = Applied Code Word $S = (E_{45}-E_{46})/4094$
	+15	-15	+5	SERV LOOP	2.4	0.8	0.8	TRIG CKT.	2.4	111111111110	11111111111X	100101111	14	E_{45}	V		
										000000000000	00000000000X			E_{46}			
L_{E1}										000000000001	0000000000XX			E_{47}			L_{E1} With N1 = 1
L_{E2}										000000000010	00000000001X			E_{48}			L_{E2} With N1 = 2
										000000000011	000000000XXX			E_{49}			
L_{E4}										000000000100	00000000010X			E_{50}			L_{E4} With N1 = 4
										000000000111	00000000XXXX			E_{51}			
L_{E6}										000000001000	00000000100X			E_{52}			L_{E6} With N1 = 8
										000000001111	0000000XXXXX			E_{53}			
L_{E8}										000000010000	00000001000X			E_{54}			L_{E8} With N1 = 16
										000000011111	000000XXXXXX			E_{55}			
L_{E10}										000000100000	00000010000X			E_{56}			L_{E10} With N1 = 32
										000000111111	00000XXXXXXX			E_{57}			
L_{E12}										000001000000	00000100000X			E_{58}			L_{E12} With N1 = 64
										000001111111	0000XXXXXXXX			E_{59}			
L_{E14}										000010000000	00001000000X			E_{60}			L_{E14} With N1 = 128
										000011111111	000XXXXXXXXX			E_{61}			
L_{E16}										000100000000	00010000000X			E_{62}			L_{E16} With N1 = 256
										000111111111	00XXXXXXXXXX			E_{63}			

DATA CONVERSION PRODUCTS 6

CHART A. GROUP A TEST CONDITIONS (Continued)

SYMBOL	APPLIED VOLTAGES REF ANALOG COMMON (FIG. 1, NOTE 1) 7 V_{CC} (V)	11 V_{EE} (V)	1 V_{LOG} (V)	13/14 V_{IN} (V)	2 $12/\overline{8}$ (V)	3 $\overline{CS}$ (V)	4 A_0 (V)	5 $R/\overline{C}$ (V)	6 CE (V)	APPLIED DIGITAL CODEWORD $DC_1 \leftrightarrow DC_{12}$ MSB ↔ LSB	DUT DIGITAL OUTPUT CODEWORD 27 ↔ 16 MSB ↔ LSB	SWITCH POSITIONS $S_1 \leftrightarrow S_9$	MEASUREMENT SENSE LINES REF. ANA. COMMON PIN	VALUE	UNIT	TEMP °C	EQUATIONS & NOTES
L_{E18}	+15	-15	+5	SERV LOOP	2.4	0.8	0.8	TRIG CKT.	2.4	001000000000	00100000000X	100101111	14	E_{64}	V	+25, +125, -55	L_{E18} With N1 = 512
										001111111111	0XXXXXXXXXXX			E_{65}			
L_{E20}										010000000000	01000000000X			E_{66}			L_{E20} With N1 = 1024
										011111111111	XXXXXXXXXXXX			E_{67}			
L_{E22}										100000000000	10000000000X			E_{68}			L_{E22} With N1 = 2048
										100011111111	100XXXXXXXXX			E_{69}			
L_{E24}										100100000000	10010000000X			E_{70}			L_{E24} With N1 = 2304
										100111111111	10XXXXXXXXXX			E_{71}			
L_{E26}										101000000000	10100000000X			E_{72}			L_{E26} With N1 = 2560
										101011111111	101XXXXXXXXX			E_{73}			
L_{E28}										101100000000	10110000000X			E_{74}			L_{E28} With N1 = 2816
										101111111111	1XXXXXXXXXXX			E_{75}			
L_{E30}										110000000000	11000000000X			E_{76}			L_{E30} With N1 = 3072
										110011111111	110XXXXXXXXX			E_{77}			
L_{E32}										110100000000	11010000000X			E_{78}			L_{E32} With N1 = 3328
										110111111111	11XXXXXXXXXX			E_{79}			
L_{E34}										111000000000	11100000000X			E_{80}			L_{E34} With N1 = 3584
										111011111111	111XXXXXXXXX			E_{81}			
L_{E36}										111100000000	11110000000X			E_{82}			L_{E36} With N1 = 3840
L_{E38}										Turn on bits that had positive integral linearity error for L_{E1} to L_{E22}	Low Edge			E_{83}			L_{E38} With N1 = Sum of positive L_{E1} to L_{E22}
											High Edge			E_{84}			

CHART A. GROUP A TEST CONDITIONS (Continued)

SYMBOL	APPLIED VOLTAGES REF ANALOG COMMON (FIG. 1, NOTE 1)									APPLIED DIGITAL CODEWORD	DUT DIGITAL OUTPUT CODEWORD	SWITCH POSITIONS	MEASUREMENT SENSE LINES REF. ANA. COMMON			TEMP	EQUATIONS & NOTES
	7	11	1	13/14	2	3	4	5	6								
	V_{CC} (V)	V_{EE} (V)	V_{LOG} (V)	V_{IN} (V)	$12/\overline{8}$ (V)	$\overline{CS}$ (V)	A_0 (V)	$R/\overline{C}$ (V)	CE (V)	$DC_1 \leftrightarrow DC_{12}$ MSB ↔ LSB	27 ↔ 16 MSB ↔ LSB	$S_1 \leftrightarrow S_9$	PIN	VALUE	UNIT	°C	
L_{E40}	+15	-15	+5	SERV LOOP	2.4	0.8	0.8	TRIG CKT.	2.4	Turn on bits that had negative integral linearity error for L_{E1} to L_{E22}	Low Edge	100101111	14	E_{85}	V		L_{E40} With N1 = Sum of negative
											High Edge			E_{86}			L_{E1} to L_{E22}
																+25, +125, -55	For Differential Linearity Error $D_{LE(N)} = (E(N + 88) - E(N + 87))/S$, $S = (E_{87} - E_{88})/4094$
										111111111110	11111111111X			E_{87}			
										000000000000	00000000000X			E_{88}			
D_{LE1}										000000000001	0000000000XX			E_{89}			D_{LE1}
D_{LE2}										000000000010	00000000001X			E_{90}			D_{LE2}
D_{LE3}										000000000011	000000000XXX			E_{91}			D_{LE3}
D_{LE4}										000000000100	00000000010X			E_{92}			D_{LE4}
										000000000110	00000000011X			E_{93}			
D_{LE6}										000000000111	00000000XXXX			E_{94}			D_{LE6}
D_{LE7}										000000001000	00000000100X			E_{95}			D_{LE7}
										000000001110	00000000111X			E_{96}			
D_{LE9}										000000001111	0000000XXXXX			E_{97}			D_{LE9}
D_{LE10}										000000010000	00000001000X			E_{98}			D_{LE10}
										000000011110	00000001111X			E_{99}			
D_{LE12}										000000011111	000000XXXXXX			E_{100}			D_{LE12}
D_{LE13}										000000100000	00000010000X			E_{101}			D_{LE13}
										000000111110	00000011111X			E_{102}			

DATA CONVERSION PRODUCTS 6

CHART A. GROUP A TEST CONDITIONS (Continued)

SYMBOL	APPLIED VOLTAGES REF ANALOG COMMON (FIG. 1, NOTE 1)									APPLIED DIGITAL CODEWORD	DUT DIGITAL OUTPUT CODEWORD	SWITCH POSITIONS	MEASUREMENT SENSE LINES REF. ANA. COMMON			TEMP ^oC	EQUATIONS & NOTES
	7	11	1	13/14	2	3	4	5	6								
	V_{CC} (V)	V_{EE} (V)	V_{LOG} (V)	V_{IN} (V)	$12/\overline{8}$ (V)	$\overline{CS}$ (V)	A_0 (V)	$R/\overline{C}$ (V)	CE (V)	$DC_1 \leftrightarrow DC_{12}$ MSB ↔ LSB	27 ↔ 16 MSB ↔ LSB	$S_1 \leftrightarrow S_9$	PIN	VALUE	UNIT		
D_{LE15}	+15	-15	+5	SERV LOOP	2.4	0.8	0.8	TRIG CKT.	2.4	000000111111	00000XXXXXXX	100101111	14	E_{103}	V	+25, +125 -55	D_{LE15}
D_{LE16}										000001000000	00000100000X			E_{104}			D_{LE16}
										000001111110	00000111111X			E_{105}			
D_{LE18}										000001111111	0000XXXXXXXX			E_{106}			D_{LE18}
D_{LE19}										000010000000	00001000000X			E_{107}			D_{LE19}
										000011111110	00000111111X			E_{108}			
D_{LE21}										000011111111	000XXXXXXXXX			E_{109}			D_{LE21}
D_{LE22}										000100000000	00010000000X			E_{110}			D_{LE22}
										000111111110	00011111111X			E_{111}			
D_{LE24}										000111111111	00XXXXXXXXXX			E_{112}			D_{LE24}
D_{LE25}										001000000000	00100000000X			E_{113}			D_{LE25}
										001111111110	00111111111X			E_{114}			
D_{LE27}										001111111111	0XXXXXXXXXXX			E_{115}			D_{LE27}
D_{LE28}										010000000000	01000000000X			E_{116}			D_{LE28}
										011111111110	01111111111X			E_{117}			
D_{LE30}										011111111111	XXXXXXXXXXXX			E_{118}			D_{LE30}
D_{LE31}										100000000000	10000000000X			E_{119}			D_{LE31}
										100011111110	10001111111X			E_{120}			
D_{LE33}										100011111111	100XXXXXXXXX			E_{121}			D_{LE33}
D_{LE34}										100100000000	10010000000X			E_{122}			D_{LE34}
										100111111110	10011111111X			E_{123}			
D_{LE36}										100111111111	10XXXXXXXXXX			E_{124}			D_{LE36}
D_{LE37}										101000000000	10100000000X			E_{125}			D_{LE37}

CHART A. GROUP A TEST CONDITIONS (Continued)

SYMBOL	APPLIED VOLTAGES REF ANALOG COMMON (FIG. 1, NOTE 1)									APPLIED DIGITAL CODEWORD	DUT DIGITAL OUTPUT CODEWORD	SWITCH POSITIONS	MEASUREMENT SENSE LINES REF. ANA. COMMON			TEMP °C	EQUATIONS & NOTES
	7	11	1	13/14	2	3	4	5	6								
	V_{CC} (V)	V_{EE} (V)	V_{LOG} (V)	V_{IN} (V)	$12/\overline{8}$ (V)	$\overline{CS}$ (V)	A_0 (V)	$R/\overline{C}$ (V)	CE (V)	$DC_1 \leftrightarrow DC_{12}$ MSB ↔ LSB	27 ↔ 16 MSB ↔ LSB	$S_1 \leftrightarrow S_9$	PIN	VALUE	UNIT		
	+15	-15	+5	SERV LOOP	2.4	0.8	0.8	TRIG CKT.	2.4	101011111110	10101111111X	100101111	14	E_{126}	V	+25, +125 -55	
D_{LE39}										101011111111	101XXXXXXXXX			E_{127}			D_{LE39}
D_{LE40}										101100000000	10110000000X			E_{128}			D_{LE40}
										101111111110	10111111111X			E_{129}			
D_{LE42}										101111111111	1XXXXXXXXXXX			E_{130}			D_{LE42}
D_{LE43}										110000000000	11000000000X			E_{131}			D_{LE43}
										110011111110	11001111111X			E_{132}			
D_{LE45}										110011111111	110XXXXXXXXX			E_{133}			D_{LE45}
D_{LE46}										110100000000	11010000000X			E_{134}			D_{LE46}
										110111111110	11011111111X			E_{135}			
D_{LE48}										110111111111	11XXXXXXXXXX			E_{136}			D_{LE48}
D_{LE49}										111000000000	11100000000X			E_{137}			D_{LE49}
										111011111110	11101111111X			E_{138}			
D_{LE51}										111011111111	111XXXXXXXXX			E_{139}			D_{LE51}
D_{LE52}										111100000000	11110000000X			E_{140}			D_{LE52}
D_{LE54}										Turn on Bits that had positive differential linearity error for DLE's 1, 2, 4, 7, 10, 13, 16, 19, 22, 25, 28, 31 Minus 1 LSB	Low Edge High Edge			E_{141} E_{142}			D_{LE54}
D_{LE55}										Turn on Bits that had positive differential linearity error for DLE's 1, 2, 4, 7, 10, 13, 16, 19, 22, 25, 28, 31	High Edge			E_{143}			D_{LE55}

DATA CONVERSION PRODUCTS 6

CHART A. GROUP A TEST CONDITIONS (Continued)

SYMBOL	APPLIED VOLTAGES REF ANALOG COMMON (FIG. 1, NOTE 1) 7 V_{CC} (V)	11 V_{EE} (V)	1 V_{LOG} (V)	13/14 V_{IN} (V)	2 $12/\overline{8}$ (V)	3 $\overline{CS}$ (V)	4 A_0 (V)	5 $R/\overline{C}$ (V)	6 CE (V)	APPLIED DIGITAL CODEWORD $DC_1 \leftrightarrow DC_{12}$ MSB ↔ LSB	DUT DIGITAL OUTPUT CODEWORD 27 ↔ 16 MSB ↔ LSB	SWITCH POSITIONS $S_1 \leftrightarrow S_9$	MEASUREMENT SENSE LINES REF. ANA. COMMON PIN	VALUE	UNIT	TEMP °C	EQUATIONS & NOTES
D_{LE57}										Turn on Bits that had negative differential linearity error for DLE's 1, 2, 4, 7, 10, 13, 16, 19, 22, 25, 28, 31 Minus 1 LSB	Low Edge High Edge			E_{144} E_{145}			D_{LE57}
D_{LE58}										Turn on Bits that had negative differen tial linearity error for DLE's 1, 2, 4, 7, 10, 13, 16, 19, 22, 25, 28, 31	High Edge			E_{146}			D_{LE58}
R_{i10V} R_{i20V}	+15 +15	-15 -15	+5 +5	5 10								010111011 010110011	13 14	I_{46} I_{47}	mA mA	+25, +125, -55	$R_{i10V} = 5V/I_{46}$ $R_{i20V} = 10V/I_{47}$
$\frac{dV_{IO}}{dT}$	+15	-15	+5													+125 -55	$dV_{IO}/dT = V_{IOH} - V_{IOR}$ $dV_{IO}/dT = V_{IOL} - V_{IOR}$
$\frac{dB_Z}{dT}$	+15	-15	+5													+125 -55	$dB_Z/dT = B_{ZH} - B_{ZR}$ $dB_Z/dT = B_{ZL} - B_{ZR}$
$\frac{dA_E}{dT}$	+15	-15	+5													+125 -55	$dA_E/dT = A_{EH} - A_{ER}$ $dA_E/dT = A_{EL} - A_{ER}$
$\frac{dBA_E}{dT}$	+15	-15	+5													+125 -55	$dBA_E/dT = BA_{EH} - BA_{ER}$ $dBA_E/dT = BA_{EL} - BA_{ER}$
t_{C1}	+15	-15	+5	SERV LOOP	2.4	0.8	2.4	TRIG CKT.	2.4	000000000000	00000000000X	100101111	28	t_1	μs	+25, +125, -55	$t_{C1} = t_1$ Rising Edge to Falling Edge
t_{C2}	+15	-15	+5		2.4	0.8	0.8		2.4	000000000000	00000000000X	100101111	28	t_2	μs	+25, +125, -55	$t_{C2} = t_2$ Rising Edge to Falling Edge
	+15	-15	+5									010111010		t_3	ns	+25, +125, -55	$t_{TD} = t_3$ t_{TD} = Trigger CKT Delay
t_{DS1}	+15	-15	+5	SERV LOOP	2.4	0.8	2.4	TRIG CKT.	2.4	000000000000	00000000000X	100101111	28	t_4	ns		$t_{DS1} = t_4 - t_3 - t_1$ t_4 Meas. Rising Edge to Rising Edge
t_{DS2}	+15	-15	+5		2.4	0.8	0.8		2.4	000000000000	00000000000X	100101111	28	t_5	ns		$t_{DS2} = t_5 - t_3 - t_2$ t_5 Meas. Rising Edge to Rising Edge

Switching Waveform Information

Conversion Length

A Convert Start transition (see Chart B) latches the state of A_0, which determines whether the conversion continues for 12-bits (A_0 low) or stops with 8-bits (A_0 high). If all 12-bits are read following an 8-bit conversion, the three LSBs will read zero and DB3 will read ONE. A_0 is latched because it is also involved in enabling the output buffers (see "Reading the Output Data"). No other control inputs are latched.

CHART B. TRUTH TABLE FOR HI-574A/883 CONTROL INPUTS

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

Conversion Start

A conversion may be initiated as shown in Chart B by a logic transition on any of three inputs: CE, $\overline{CS}$ or R/$\overline{C}$. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same, and if necessary, all three may change state simultaneously. See the Timing Specifications, Convert mode.

The variety of control modes allows a simple interface in most system applications. The Convert Start timing relationships are illustrated in Figure 5.

The output signal STS indicates status of the converter by going high only while a conversion is in progress. While STS is high, the output buffers remain in a high impedance state and data cannot be read. Also, an additional Start Convert will not reset the converter or reinitiate a conversion while STS is high. (However, if A_0 changes state after a conversion begins, an additional Start Convert signal will latch the new state of A_0, possibly causing a wrong cycle length (8 vs. 12-bits) for that conversion).

Reading the Output Data

The output data buffers remain in a high impedance state until four conditions are met: R/$\overline{C}$ high, STS low, CE high and $\overline{CS}$ low. At that time, data lines become active according to the state of inputs 12/$\overline{8}$ and A_0. Timing constraints are illustated in Figure 6.

The 12/$\overline{8}$ input will be tied high or low in most applications, though it is fully TTL/CMOS compatible. With 12/$\overline{8}$ high, all 12 output lines become active simultaneously, for interface to a 12 or 16-bit data bus. The A_0 input is ignored.

With 12/$\overline{8}$ low, the output is organized in two 8 bit bytes, selected one at a time by A_0. This allows an 8 bit data bus to be connected as shown in Figure 10. A_0 is usually tied to the least significant bit of the address bus, for storing the output data in two consecutive memory locations. (With A_0 low, the 8 MSBs only are enabled. With A_0 high, 4 MSBs are disabled, bits 4 through 7 are forced to zero, and the 4 LSBs are enabled). This two byte format is considered "left justified data", for which a decimal (or binary!) point is assumed to the left of byte 1:

BYTE 1	BYTE 2
X X X X X X X X	X X X X 0 0 0 0
MSB	LSB

Further, A_0 may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in Figure 10 will never be enabled at the same time.

A read operation usually begins after the conversion is complete and STS is low. For earliest access to the data however, the read should begin no later than ($t_{DD}+t_{HS}$) before STS goes low. See Figure 6.

STAND-ALONE MODE TIMING (OVER FULL TEMP. RANGE)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	350			ns
t_{DS}	STS Delay from R/$\overline{C}$			600	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	15			ns
t_{HS}	STS Delay After Data Valid	300	700	1200	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	300			ns
t_{DDR}	Data Access Time			250	ns

Switching Waveforms

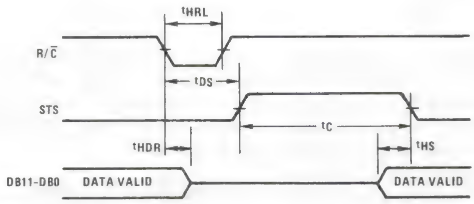


FIGURE 3. LOW PULSE R/C̄-OUTPUTS ENABLED AFTER CONVERSION

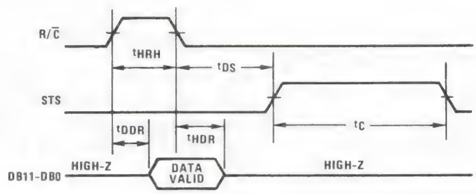


FIGURE 4. HIGH PULSE FOR R/C̄-OUTPUTS ENABLED WHILE R/C̄ HIGH, OTHERWISE HIGH-Z

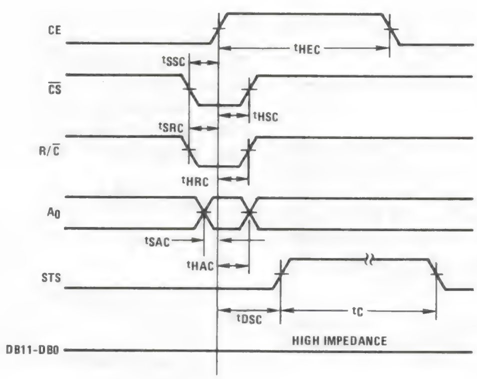


FIGURE 5. CONVERT START TIMING

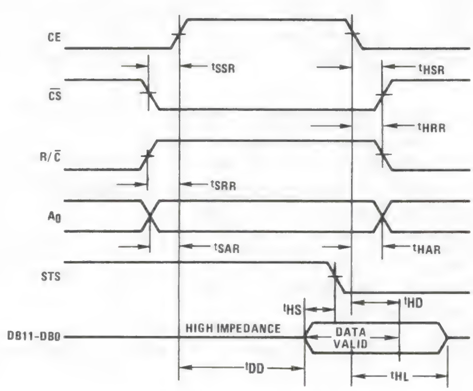
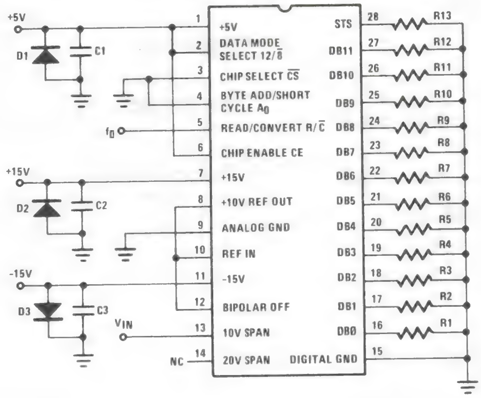


FIGURE 6. READ CYCLE TIMING

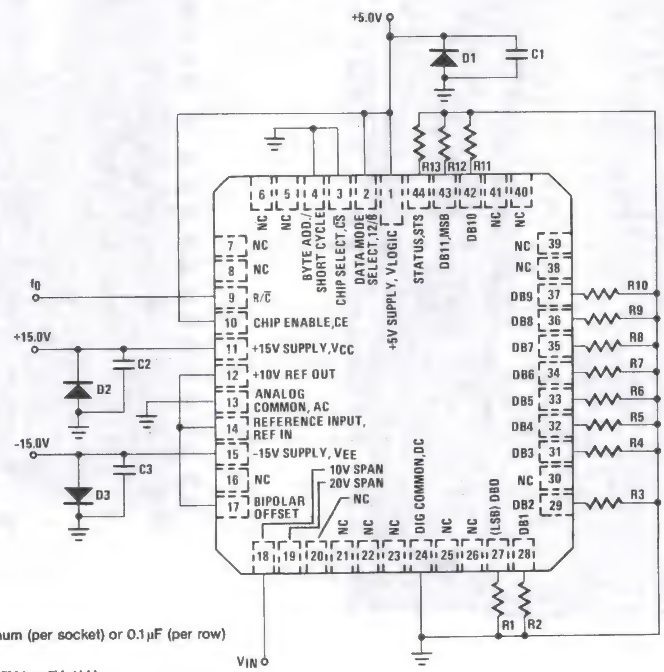
Burn-In Circuits

28 PIN SIDEBRAZED DIP



NOTES:
R1 thru R13 = 10kΩ
C1 thru C3 = 0.01μF minimum (per socket) or 0.1μF (per row)
D1 thru D3 = IN4002
V_{IN} = Triangle waveform, +5V to -5V, 1kHz
f_0 = Square waveform, 10kHz, 90% Duty Cycle, 0V to 5V

44 PIN CERAMIC LEADLESS CHIP CARRIER



NOTES:
R1 thru R13 = 10kΩ
C1 thru C3 = 0.01μF minimum (per socket) or 0.1μF (per row)
D1 thru D3 = IN4002
V_{IN} = Triangle waveform, +5V to -5V, 1kHz
f_0 = Square waveform, 10kHz, 90% Duty Cycle, 0V to 5V

6

DATA CONVERSION PRODUCTS

Die Characteristics

DIE DIMENSIONS:
- ANALOG DIE: 204 x 104 mils
- DIGITAL DIE: 158 x 84 mils

METALLIZATION:
- ANALOG DIE: Type: Al
  Thickness: 16kÅ ± 2kÅ
- DIGITAL DIE: Type: SiAl
  Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
- ANALOG DIE: 1.63×10^5 A/cm^2
- DIGITAL DIE: 1.93×10^5 A/cm^2

TRANSISTOR COUNT
- ANALOG DIE: 317
- DIGITAL DIE: 800

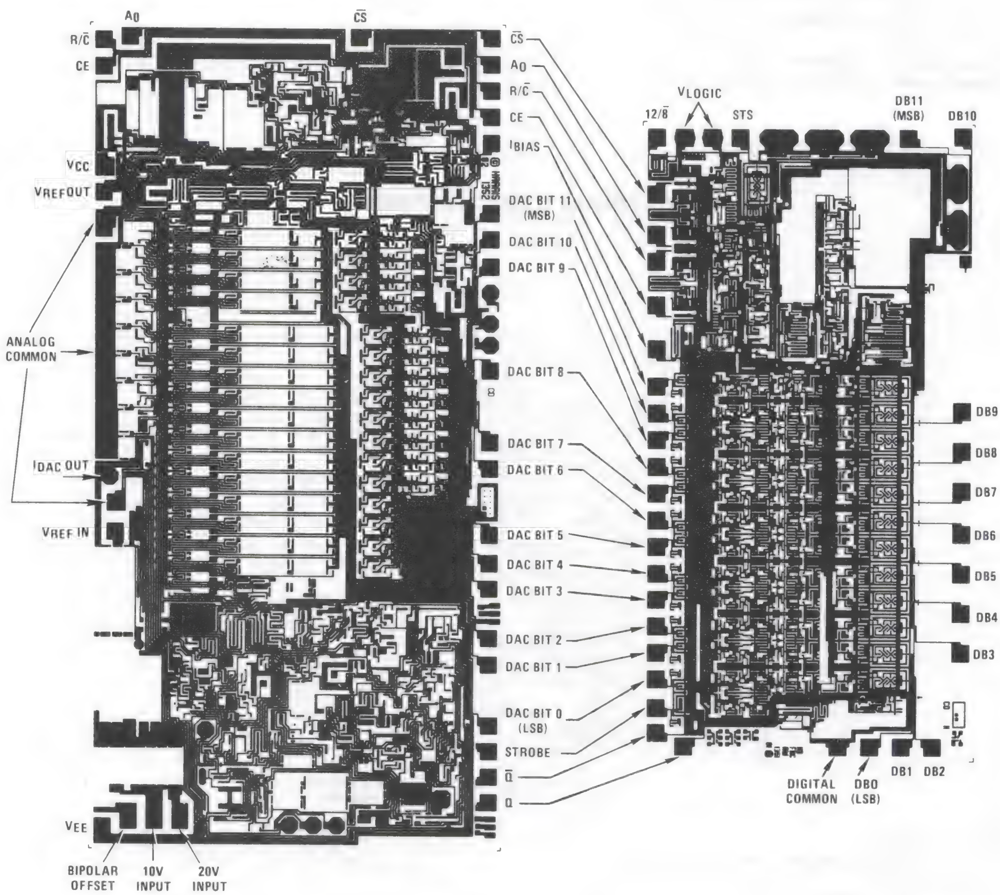
PROCESS:
- ANALOG DIE: Bipolar-DI
- DIGITAL DIE: CMOS-JI

DIE ATTACH: Material: Gold/Silicon Eutectic Alloy
Temperature: 420^{o}C Max

GLASSIVATION:
- ANALOG DIE: Type: Silox
  Thickness: 14kÅ ± 2kÅ
- DIGITAL DIE: Type: Silox
  Thickness: 8kÅ ± 2kÅ

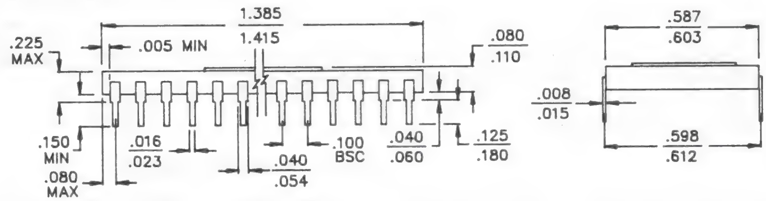
Metallization Mask Layout

HI-574A/883 ANALOG DIE **HI-574A/883 DIGITAL DIE**



Packaging†

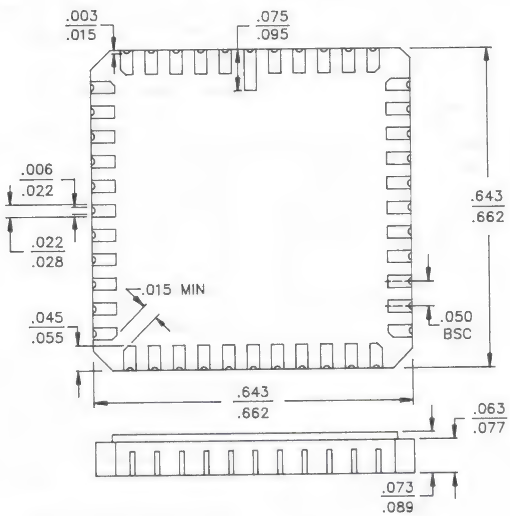
28 PIN SIDEBRAZED DIP



LEAD MATERIAL: Type B
LEAD FINISH: Type C
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-10

44 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-5

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

HI-574A

DESIGN INFORMATION

Fast, Complete 12-Bit A/D Converter With Microprocessor Interface

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Definitions of Specifications

Linearity Error

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs ½LSB (1.22mV for 10 volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1½LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HI-574AT grade is guaranteed for maximum nonlinearity of ±½LSB. This means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HI-574AS grade is guaranteed to ±1LSB max error. An analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user-adjustable.

Differential Linearity Error (No Missing Codes)

A specification which guarantees no missing codes requires that every combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. The HI-574AT grade, guarantees no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HI-574AS grade guarantees no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11-bits must be present; in practice very few of the 12-bit codes are missing.

Unipolar Offset

The first transition should occur at a level ½LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

Bipolar Offset

Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value ½LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

Full Scale Calibration Error

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1½LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 7 and 8. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 volt reference.

Temperature Coefficients

The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{min} or T_{max}.

Power Supply Rejection

The standard specifications for the HI-574A assume use of +5.00 and ±15.00 or ±12.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

Code Width

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 Least Significant Bit (LSB) of the full scale range or 2.44mV out of 10 volts for a 12-bit ADC.

Quantization Uncertainty

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±½LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

Left-Justified Data

The data format used in the HI-574A is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

*Applying the HI-574A**

*Pin numbers correspond to DIP package only.

For each application of this converter, the ground connections, power supply bypassing, analog signal source, digital timing and signal routing on the circuit board must be optimized to assure maximum performance. These areas are reviewed in the following sections, along with basic operating modes and calibration requirements.

PHYSICAL MOUNTING AND LAYOUT CONSIDERATIONS

Layout

Unwanted, parasitic circuit components, (L, R, and C) can make 12-bit accuracy impossible, even with a perfect A/D converter. The best policy is to eliminate or minimize these parasitics through proper circuit layout, rather than try to quantify their effects.

The recommended construction is a double-sided printed circuit board with a ground plane on the component side. Other techniques, such as wire-wrapping or point-to-point wiring on vectorboard, will have an unpredictable effect on accuracy.

In general, sensitive analog signals should be routed between ground traces and kept well away from digital lines. If analog and digital lines must cross, they should do so at right angles.

Power Supplies

Supply voltages to the HI-574A (+15V, -15V and +5V) must be "quiet" and well regulated. Voltage spikes on these lines can affect the converter's accuracy, causing several LSB's to flicker when a constant input is applied. Digital noise and spikes from a switching power supply are especially troublesome. If switching supplies must be used, outputs should be carefully filtered to assure "quiet" DC voltage at the converter terminals.

Further, a bypass capacitor pair on each supply voltage terminal is necessary to counter the effect of variations in supply current. Connect one pair from pin 1 to 15 (V_{LOGIC} supply), one from pin 7 to 9 (V_{CC} to Analog Common) and one from pin 11 to 9 (V_{EE} to Analog Common). For each capacitor pair, a 10μF tantalum type in parallel with a 0.1μF ceramic type is recommended.

Ground Connections

The typical HI-574A ground currents are 5.5mADC into pin 9 (Analog Common) and 7mADC out of pin 15 (Digital Common). These pins should be tied together at the package to guarantee specified performance for the converter. In addition, a wide PC trace should run directly from pin 9 to (usually) 15V common, and from pin 15 to (usually) the +5V Logic Common. If the converter is located some distance from the system's "single point" ground, make only these connections to pins 9 and 15: Tie them together at the package, and back to the system ground with a single path. This path should have low resistance since it will carry about 1.5mA of DC current. (Code dependent currents flow in the V_{CC}, V_{EE} and V_{LOGIC} terminals, but not through the HI-574A's Analog Common or Digital Common).

ANALOG SIGNAL SOURCE

The device driving the HI-574A analog input will see a nominal load of 5kΩ (10V range) or 10kΩ (20V range). However, the other end of these input resistors may change as much as $\pm$400mV with each bit decision, creating abrupt changes in current at the analog input. Thus, the signal source must maintain its output voltage while furnishing these step changes in load current, which occur at 1.6μs intervals. This requires low output impedance and fast settling by the signal source.

The output impedance of an op amp, for example, has an open loop value which, in a closed loop, is divided by the loop gain available at a frequency of interest. The amplifier should have acceptable loop gain at 600kHz for use with the HI-574A. To check whether the output properties of a signal source are suitable, monitor the 574A's input (pin 13 or 14) with an oscilloscope while a conversion is in progress. Each of the twelve disturbances should subside in one microsecond or less. (The comparator decision is made about 1.5μs after each code change from the SAR).

If the application calls for a Sample/Hold to precede the converter, it should be noted that not all Sample/Holds are compatible with the HI-574A in the manner described above. These will require an additional wideband buffer amplifier to lower their output impedance. A simpler solution is to use the Harris HA-5320 Sample/Hold, which was designed for use with the HI-574A.

RANGE CONNECTIONS AND CALIBRATION PROCEDURES

The HI-574A is a "complete" A/D converter, meaning it is fully operational with addition of the power supply voltages, a Start Convert signal, and a few external components as shown in figures 7 and 8. Nothing more is required for most applications.

Whether controlled by a processor or operating in the stand-alone mode, the HI-574A offers four standard input ranges: 0V to +10V, 0V to +20V, $\pm$5V and $\pm$10V. The maximum errors for gain and offset are listed under Specifications. If required, however, these errors may be adjusted to zero as explained below. Power supply and ground connections have been discussed in an earlier section.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Unipolar Connections and Calibration

Refer to figure 7. The resistors shown* are for calibration of offset and gain. If this is not required, replace R2 with a 50Ω, 1% metal film resistor and remove the network on pin 12. Connect pin 12 to pin 9. Then, connect the analog signal to pin 13 for the 0V to 10V range, or to pin 14 for the 0V to 20V range. Inputs to +20V (5V over the power supply) are no problem — the converter operates normally.

Calibration consists of adjusting the converters's most negative output to its ideal value (offset adjustment), then, adjusting the most positive output to its ideal value (gain adjustment). To understand the procedure, note that in principle, one is setting the output with respect to the midpoint of an increment of analog input, as denoted by two adjacent code changes. Nominal value of an increment is one LSB. However, this approach is impractical because nothing "happens" at a midpoint to indicate that an adjustment is complete. Therefore, calibration is performed in terms of the observable code changes instead of the midpoint between code changes.

For example, midpoint of the first LSB increment should be positioned at the origin, with an output code of all 0's. To do this, apply an input of +½LSB (+1.22mV for the 10V range; +2.44mV for the 20V range). Adjust the Offset potentiometer R1 until the first code transition flickers between 0000 0000 0000 and 0000 0000 0001.

Next, perform a Gain Adjust at positive full scale. Again, the ideal input corresponding to the last code change is applied. This is 1½LSB's below the nominal full scale (+9.9963V for 10V range; +19.9927V for 20V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

Bipolar Connections and Calibration

Refer to Figure 8. The gain and offset errors listed under Specifications may be adjusted to zero using potentiometers R1 and R2*. If this isn't required, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

Connect the Analog signal to pin 13 for a ±5V range, or to pin 14 for a ±10V range. Calibration of offset and gain is similar to that for the unipolar ranges as discussed above. First apply a DC input voltage ½LSB above negative full scale (i.e., -4.9988V for the ±5V range, or -9.9976V for the ±10V range). Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1½LSB's below positive full scale (+4.9963V for ±5V range; +9.9927V for ±10V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

*The 100Ω potentiometer R2 provides Gain Adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (LSB equals 2.5mV) or 20.48V (LSB equals 5.0mV) is more convenient. For these, replace R2 by a 50Ω, 1% metal film resistor. Then, to provide Gain Adjust for the 10.24V range, add a 200Ω potentiometer in series with pin 13. For the 20.48V range, add a 500Ω potentiometer in series with pin 14.

Pin Numbers Refer To Sidebraze DIP Package.

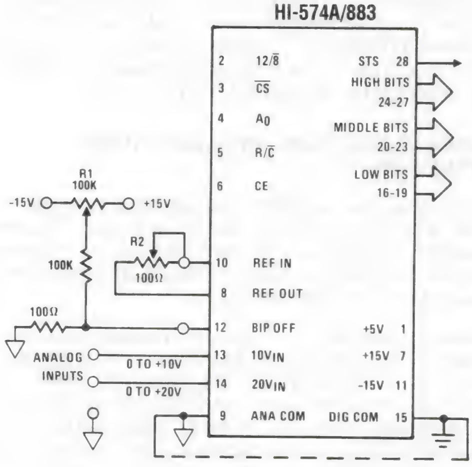


FIGURE 7. UNIPOLAR CONNECTIONS

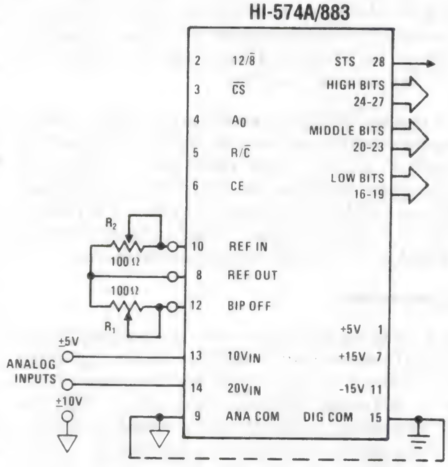


FIGURE 8. BIPOLAR INPUT CONNECTIONS

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Controlling the HI-574A

The HI-574A includes logic for direct interface to most microprocessor systems. The processor may take full control of each conversion, or the converter may operate in the "stand-alone" mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8 or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready—choosing either 12-bits at once or 8 followed by 4, in a left-justified format. The five control inputs are all TTL/CMOS- compatible: (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$ and CE). Chart B illustrates the use of these inputs in controlling the converter's operations. Also, a simplified diagram of the internal control logic is shown in Figure 9.

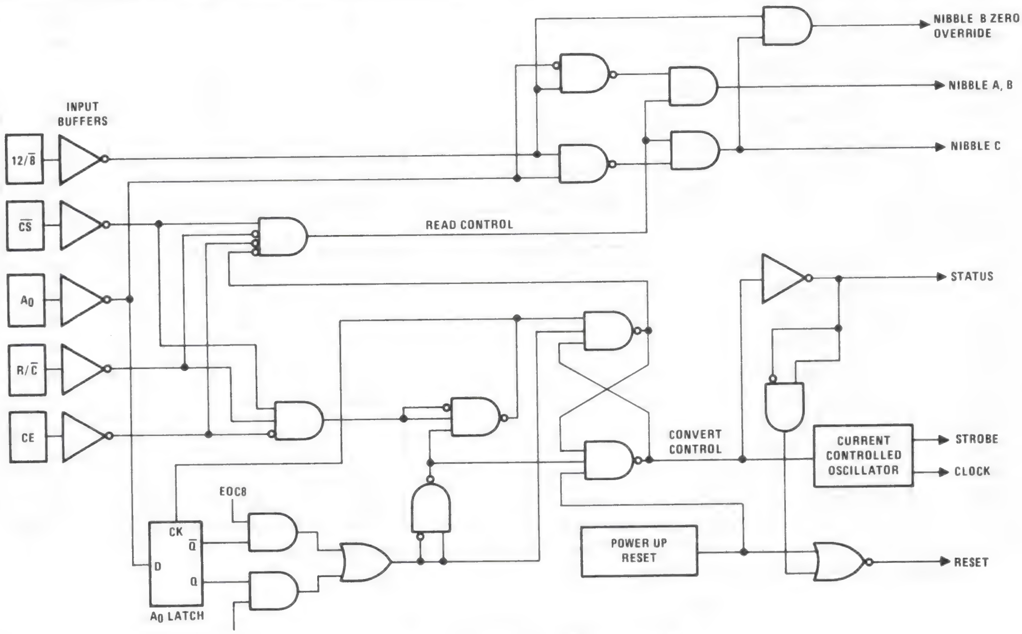


FIGURE 9. HI-574A CONTROL LOGIC

DESIGN INFORMATION (Continued)

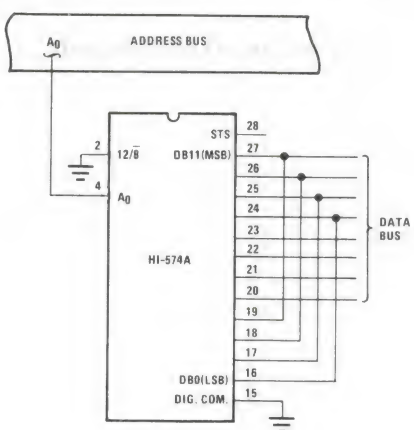
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

HI-574A Timing Specifications

+25°C Unless Otherwise Specified

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
CONVERT MODE					
t_{DSC}	STS Delay from CE	—	100	200	ns
t_{HEC}	CE Pulse Width	50	30	—	ns
t_{SSC}	$\overline{CS}$ to CE Setup	50	—	—	ns
t_{HSC}	$\overline{CS}$ Low During CE High	50	20	—	ns
t_{SRC}	R/$\overline{C}$ to CE Setup	50	—	—	ns
t_{HRC}	R/$\overline{C}$ Low During CE High	50	20	—	ns
t_{SAC}	A_0 to CE Setup	0	0	—	ns
t_{HAC}	A_0 Valid During CE High	50	20	—	ns
t_C	Conversion Time, 12-bit Cycle T_{min} to T_{max}	15	20	25	μs
	8-bit Cycle T_{min} to T_{max}	10	13	17	μs
READ MODE					
t_{DD}	Access Time from CE	—	75	150	ns
t_{HD}	Data Valid after CE low	25	35	—	ns
t_{HL}	Output Float Delay	—	100	150	ns
t_{SSR}	$\overline{CS}$ to CE Setup	50	0	—	ns
t_{SRR}	R/$\overline{C}$ to CE Setup	0	0	—	ns
t_{SAR}	A_0 to CE Setup	50	25	—	ns
t_{HSR}	$\overline{CS}$ Valid after CE Low	0	0	—	ns
t_{HRR}	R/$\overline{C}$ High after CE Low	0	0	—	ns
t_{HAR}	A_0 Valid after CE Low	50	25	—	ns
t_{HS}	STS Delay after Data Valid	300	700	1200	ns

NOTE: Time is measured from 50% level of digital transitions, tested with a 50pF and 3kΩ load. All possible combinations for setup times not listed, see Figure 9.



Pin Numbers Refer To Sidebraze DIP Package.

FIGURE 10. INTERFACE TO AN 8-BIT DATA BUS

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

HI-574A Capacitance Specifications

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
C_I	Logic Input Capacitance	—	5	—	pF
C_O	Logic Output Capacitance	—	5	—	pF

HARRIS

HI-674A/883

Fast, Complete 12-Bit A/D Converter With Microprocessor Interface

September 1988

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Complete 12-Bit A/D Converter with Reference and Clock
- Full 89-, 12-, or 16-Bit Microprocessor Bus Interface
- 250ns Bus Access Time (Max. Over Temp.)
- No Missing Codes Over Temperature
- Minimal Setup Time For Control Signals
- 15µs Maximum Conversion Time
- Low Noise, Via Current Mode Signal Transmission Between Chips
- Byte Enable/Short Cycle (A_0 Input)
  - Guarantees Break-Before-Make Action, Eliminating Bus Contention During Read Operation. Latched by the Start Convert Input (To Set the Conversion Length)
- Faster Version of HI-574A
- Same Pinout as HI-574A
- ±12V to ±15V Operation

Applications

- Military and Industrial Data Acquisition Systems
- Electronic Test And Scientific Instrumentation
- Process Control Systems

Description

The HI-674A/883 is a complete 12-bit Analog-to-Digital Converter, including a +10V reference, clock, three-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice housed in a single package. The bipolar analog die features the Harris Dielectric Isolation process, which provides enhanced AC performance and freedom from latch-up.

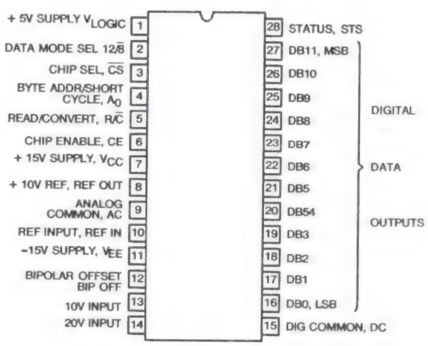
Custom design of each IC (bipolar analog and CMOS digital) has yielded improved performance over existing versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1 LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital ICs. Also, the clock oscillator is current-controlled for excellent stability over temperature. The oscillator is trimmed for a nominal conversion time of 12 ±1µs.

The HI-674A/883 offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity, gain and offset accuracy. The buried zener reference circuit is trimmed for minimum temperature coefficient.

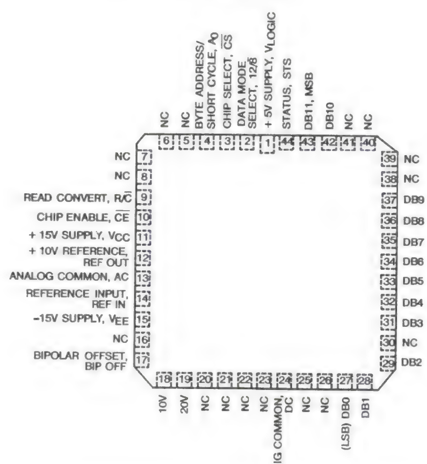
Power requirements are +5V and ±12V to ±15V, with typical dissipation of 385mW at ±12V. Two electrical grades are offered over the -55°C to +125°C temperature range. Both models are available in a 28 pin Sidebrazed DIP, or a 44 pad Ceramic LCC package.

Pinouts

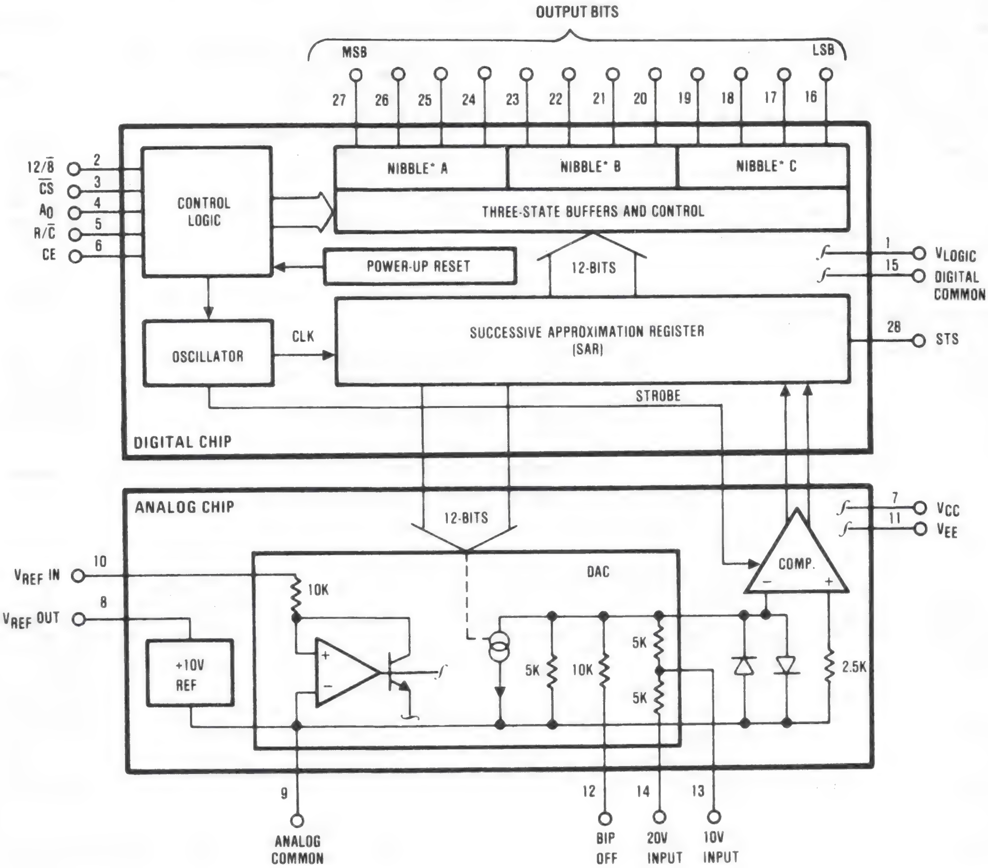
HI1-674A/883 (SIDEBRAZED DIP)
TOP VIEW



HI4-674A/883 (CERAMIC LCC)
TOP VIEW



Functional Diagram



*("NIBBLE" IS A 4-BIT DIGITAL WORD.)

Absolute Maximum Ratings

V_{CC} to Digital Ground . . . . 0 to +16.5V
V_{EE} to Digital Ground . . . . 0 to -16.5V
V_{LOGIC} to Digital Ground . . . . 0 to 7V
Analog Common to Digital Common . . . . ±1V
Control Inputs (CE, $\overline{CS}$, A_O, 12/$\overline{8}$, R/$\overline{C}$) to
  Digital Common. . . . . -0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$) to
  Analog Common . . . . ±16.5V
  20 V_{IN} to Analog Common . . . . ±24V
REF OUT . . . . Indefinite Short to Common
  10ms Short to V_{CC}
Storage Temperature Range . . . . -65°C to +150°C
Lead Temperature (Soldering 10 Seconds) . . . . 275°C
Junction Temperature. . . . . +175°C

Thermal Information

Thermal Resistance, Junction-to-Case (θ_{jc})
  Sidebrazed DIP Package . . . . 12°C/W
  Ceramic LCC Package . . . . 11°C/W
Thermal Resistance, Junction-to-Ambient (θ_{ja})
  Sidebrazed DIP Package . . . . 70°C/W
  Ceramic LCC Package . . . . 38°C/W
Power Dissipation (at +75°C)
  Sidebrazed DIP Package 2.08W
  Ceramic LCC Package 2.27W
Power Dissipation Derating Factor (Above +75°C)
  Sidebrazed DIP Package. . . . . 20.8mW/°C
  Ceramic LCC Package . . . . 22.7mW/°C

Recommended Operating Conditions

Operating Temperature Range. . . . . -55°C +125°C
$+V_{SUPPLY}$ . . . . +15V
$-V_{SUPPLY}$ . . . . -15V
V_{LOGIC} . . . . +5V
V_{REF} . . . . +10V

Analog Input Voltage, $10V_{IN}$ . . . . ±5V or 0 to +10V
Analog Input Voltage $20V_{IN}$. . . . . ±10V or 0 to +20V
Logic Level Low (V_{IL}) . . . . 0V to 0.8V
Logic Level High (V_{IH}). . . . . 2.4V to +5V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested At V_{CC} = +15V, V_{EE} = -15V, V_{LOG} = 5.0V, Unless Otherwise Specified.

(Note 1) DC PARAMETER	SYMBOL	(Figure 1,2 & Note 1, Chart A Apply Unless Otherwise Noted) CONDITIONS	GROUP A SUBGROUPS	TEMP	LIMITS HI-674AS MIN	LIMITS HI-674AS MAX	LIMITS HI-674AT MIN	LIMITS HI-674AT MAX	UNITS
Power Supply Current From V_{CC}	I_{CC}	Output Code = 000000000000 and 111111111111 (Note 2)	1	+25°C		15		15	mA
			2, 3	+125°C, -55°C		16		15	mA
Power Supply Current From V_{EE}	I_{EE}	Output Code = 000000000000 and 111111111111 (Note 2)	1	+25°C		28		28	mA
			2, 3	+125°C, -55°C		32		30	mA
Power Supply Current From V_{LOGIC}	I_{LOG}	Output Code = 000000000000 and 111111111111 (Note 2)	1	+25°C		15		15	mA
			2, 3	+125°C, -55°C		17		17	mA
Power Dissipation	P_d	Calculated Worst Case of 2 Conditions (Note 3)	1	+25°C		720		720	mW
			2, 3	+125°C, -55°C		805		760	mW
Input Low Current	I_{IL}	V_{LOG} = 5.5V $V_{IN}(LOGIC)$ = 0.0V	1	+25°C	-5	5	-5	5	µA
			2, 3	+125°C, -55°C	-5	5	-5	5	µA
Input High Current	I_{IH}	V_{LOG} = 5.5V $V_{IN}(LOGIC)$ = 2.4V	1	+25°C	-5	5	-5	5	µA
			2, 3	+125°C, -55°C	-5	5	-5	5	µA
		V_{LOG} = 5.5V $V_{IN}(LOGIC)$ = 5.5V	1	+25°C	-5	5	-5	5	µA
			2, 3	+125°C, -55°C	-5	5	-5	5	µA
High Impedance State Output Current	I_{ZL}	V_{LOG} = 5.5V V_{IN} = 11.0V Min Output Code = 111111111111 Set R/$\overline{C}$ = Logic "0" Output Bits 1 thru 12 Measured Separately V_O = 0.0V all Bits (Note 2)	1	+25°C	-5	5	-5	5	µA
			2, 3	+125°C, -55°C	-5	5	-5	5	µA

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Devices Tested At V_{CC} = +15V, V_{EE} = -15V, V_{LOG} = 5.0V, Unless Otherwise Specified.

(Note 1) DC PARAMETER	SYMBOL	(Fig. 1,2 & Note 1 Apply Unless Otherwise Noted.) CONDITIONS	GROUP A SUBGROUPS	TEMP	LIMITS HI-674AS MIN	LIMITS HI-674AS MAX	LIMITS HI-674AT MIN	LIMITS HI-674AT MAX	UNITS
High Impedance State Output Current	I_{ZH}	V_{LOG} = 5.5V V_{IN} = -1.0V Max Output Code = 000000000000 Set R/$\overline{C}$ = Logic "0" Output Bits 1 thru 12 Measured Separately V_O = 5.5V All Bits (Note 2)	1	+25°C	-5	5	-5	5	μA
			2, 3	+125°C, -55°C	-5	5	-5	5	μA
Output Logic Voltage Levels	V_{OL}	V_{LOG} = 5.0V Output Code = 000000000000 Measure Output Bits 1 thru 12 & STS I_L = 1.6mA (Note 2)	1	+25°C	-0.5	0.4	-0.5	0.4	V
			2, 3	+125°C, -55°C	-0.5	0.4	-0.5	0.4	V
	V_{OH}	V_{LOG} = 4.5 Output Code = 111111111111 Measure Bits 1 thru 12 I_L = -0.5mA (Note 2)	1	+25°C	2.4	5.5	2.4	5.5	V
			2, 3	+125°C, -55°C	2.4	5.5	2.4	5.5	V
Reference Voltage	V_{REF}	Output Code = 000000000000 Bipolar, VFSR = 20V I_L = 2.0mA (Notes 2, 4)	1	+25°C	9.970	10.030	9.970	10.030	V
			2, 3	+125°C, -55°C	9.950	10.050	9.950	10.050	V
Power Supply Sensitivity To V_{CC}	$+PSS_1$	13.5V ≤ V_{CC} ≤ 16.5V Output Transition = 11111111111X-00000000000X (Note 5)	1	+25°C	-2	2	-1	1	LSB
			2, 3	+125°C, -55°C	-2.5	2.5	-1.5	1.5	LSB
	$+PSS_2$	11.4V ≤ V_{CC} ≤ 12.6V Output Transition = 11111111111X-00000000000X (Note 5)	1	+25°C	-2	2	-1	1	LSB
Power Supply Sensitivity To V_{LOG}	$+PSS_3$	4.5V ≤ V_{LOG} ≤ 5.5V Output Transition = 11111111111X-00000000000X (Note 5)	1	+25°C	-0.5	0.5	-0.5	0.5	LSB
			2, 3	+125°C, -55°C	-0.5	0.5	-0.5	0.5	LSB
Power Supply Sensitivity To V_{EE}	$-PSS_1$	-16.5 ≤ V_{EE} ≤ -13.5V Output Transition = 11111111111X-00000000000X (Note 5)	1	+25°C	-2	2	-1	1	LSB
			2, 3	+125°C, -55°C	-2.5	2.5	-2	2	LSB
	$-PSS_2$	-12.6V ≤ V_{EE} ≤ -11.4V Output Transition = 11111111111X-00000000000X (Note 5)	1	+25°C	-2	2	-1	1	LSB
Unipolar Offset Voltage	V_{IO}	Output Transition = 00000000000X (Note 5)	1	+25°C	-2	2	-2	2	LSB
			2, 3	+125°C, -55°C	-4	4	-3	3	LSB
Bipolar Zero	BZ	Output Transition = XXXXXXXXXXXX Bipolar, VFSR = 20V (Note 5)	1	+25°C	-10	10	-4	4	LSB
			2, 3	+125°C, -55°C	-14	14	-6	6	LSB

6

DATA CONVERSION PRODUCTS

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Devices Tested At $V_{CC} = +15V$, $V_{EE} = -15V$, $V_{LOG} = 5.0V$, Unless Otherwise Specified.

(Note 1) DC PARAMETER	SYMBOL	(Figure 1,2 & Note 1, Apply Unless Otherwise Noted) CONDITIONS	GROUP A SUBGROUPS	TEMP	LIMITS HI-674AS MIN	LIMITS HI-674AS MAX	LIMITS HI-674AT MIN	LIMITS HI-674AT MAX	UNITS
Gain Error	A_E	Output Transition = 00000000000X to 11111111111X (Note 5)	1	+25°C	-0.3	0.3	-0.3	0.3	% of FSR
			2, 3	+125°C, -55°C	-0.8	0.8	-0.55	0.55	
	BPA_E	Bipolar, VFSR = 20V (Note 5)	1	+25°C	-0.3	0.3	-0.3	0.3	% of FSR
			2, 3	+125°C, -55°C	-0.8	0.8	-0.55	0.55	
Integral Linearity Error	L_E	Abbreviated Test (Note 5)	1	+25°C	-1	1	-1/2	1/2	LSB
			2, 3	+125°C, -55°C	-1	1	-1	1	LSB
Differential Linearity Error	DL_E	Abbreviated Test (Note 5)	1	+25°C	-2	2	-1	1	LSB
			2, 3	+125°C, -55°C	-2	2	-1	1	LSB
Input Resistance	R_i10V	10V Span Input (Note 11)	1	+25°C	3.75	6.25	3.75	6.25	KΩ
			2, 3	+125°C, -55°C	3	7	3	7	KΩ
	R_i20V	20V Span Input (Note 11)	1	+25°C	7.50	12.50	7.50	12.50	KΩ
			2, 3	+125°C, -55°C	6	14	6	14	KΩ
Unipolar Offset Voltage Drift	$\frac{dV_{IO}}{dT}$	Output Transition = 00000000000X (Note 5)	2, 3	+125°C, -55°C	-2	2	-1	1	LSB
Bipolar Zero Drift	$\frac{dB_Z}{dT}$	Output Transition = XXXXXXXXXXXX Bipolar, VFSR = 20V (Note 5)	2, 3	+125°C, -55°C	-4	4	-2	2	LSB
Gain Error Drift	$\frac{dA_E}{dT}$	Output Transition = 00000000000X to 11111111111X (Note 5)	2, 3	+125°C, -55°C	-20	20	-10	10	LSB
	$\frac{dBPA_E}{dT}$	Bipolar, VFSR = 20V (Note 5)	2, 3	+125°C, -55°C	-20	20	-10	10	LSB

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested At V_{CC} +15V, V_{EE} = -15V, V_{LOG} = 5.0V, Unless Otherwise Specified.

(Note 1) AC PARAMETER	SYMBOL	(Figure 1,2 & Note 1 Apply Unless Otherwise Noted) CONDITIONS	GROUP A SUBGROUPS	TEMP	LIMITS HI-674AS MIN	HI-674AS MAX	HI-674AT MIN	HI-674AT MAX	UNITS
Conversion Time	t_C	V_{IN} = -1V Max Output Code = 000000000000 8 Bit Cycle (Note 5)	9	+25°C	6	10	6	10	μs
			10, 11	+125°C, -55°C	6	10	6	10	μs
		V_{IN} = 11V Max Output Code = 111111111111 12 Bit Cycle (Note 5)	9	+25°C	9	15	9	15	μs
			10, 11	+125°C, -55°C	9	15	9	15	μs

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Characterized At V_{CC} = +15V, V_{EE} = -15V, V_{LOG} = 5.0V, Unless Otherwise Specified. Load is 3kΩ, 50pF where applicable. Figure 3, 4, 5, & 6 applies Unless Otherwise Noted.

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMP	HI-674AS/883 HI-674AT/883 MIN	MAX	UNITS
STS Delay From R/$\overline{C}$	t_{DS}	Low to High Transition Referenced to High to Low R/$\overline{C}$ Transition. Output Code = 000000000000	1, 5, 10	+25°C		200	ns
				+125°C, -55°C		600	ns
Low R/$\overline{C}$ Pulse Width	t_{HRL}	Minimum R/$\overline{C}$ Pulse Width Required to Start a Conversion	1, 10	+25°C	50		ns
				+125°C, -55°C	350		ns
Data Valid After R/$\overline{C}$ Low	t_{HDR}	Output Data Valid, Referenced to High to Low R/$\overline{C}$ Transition Output Code = 000000000000 & 111111111111	1, 2, 10	+25°C	25		ns
				+125°C, -55°C	15		ns
STS Delay After Data Valid	t_{HS}	STS High to Low Transition Referenced to Valid Output Data Output Code = 000000000000 & 111111111111	1, 2, 10	+25°C	25	850	ns
High R/$\overline{C}$ Pulse Width	t_{HRH}	Minimum R/$\overline{C}$ Pulse Width Required to Enable Output Bits Output Code = 000000000000 & 111111111111	1, 2, 10	+25°C	150		ns
				+125°C, -55°C	300		ns
Data Access Time	t_{DDR}	Output Data Valid, Referenced to Low to High R/$\overline{C}$ Transition Output Code = 000000000000 & 111111111111	1, 2, 10	+25°C		150	ns
				+125°C, -55°C		250	ns
STS Delay From CE	t_{DSC}	Low to High Transition, Referenced to Low to High CE Transition Output Code = 000000000000	1, 2, 10	+25°C		200	ns
				+125°C, -55°C		350	ns

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DATA CONVERSION PRODUCTS

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Devices Characterized At V_{CC} = +15V, V_{EE} = -15V, V_{LOG} = 5.0V, Unless Otherwise Specified. Load is 3kΩ, 50pF where applicable. Figure 3, 4, 5, & 6 applies Unless Otherwise Noted.

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMP	HI-674AS/883 HI-674AT/883 MIN	MAX	UNITS
CE Pulse Width	t_{HEC}	Minimum CE Pulse Width Required to Start a Conversion	1, 10	+25°C	50		ns
				+125°C, -55°C	300		ns
$\overline{CS}$ to CE Setup	t_{SSC}	Minimum Time Required From a High to Low $\overline{CS}$ Transition to Low to High CE Transition for a Conversion to Start from CE	1, 10	+25°C	50		ns
$\overline{CS}$ Low During CE High	t_{HSC}	Minimum Time Required From a Low to High CE Transition to Low to High $\overline{CS}$ Transition for a Conversion to Start	1, 10	+25°C	50		ns
R/$\overline{C}$ To CE Set-Up	t_{SRC}	Minimum Time Required From a High to Low R/$\overline{C}$ Transition to Low to High CE Transition for a Conversion to Start from CE.	1, 10	+25°C	50		ns
R/$\overline{C}$ Low During CE High	t_{HRC}	Minimum Time Required From a Low to High CE Transition to Low to High R/$\overline{C}$ Transition for a Conversion to Start	1, 10	+25°C	50		ns
A_0 To CE Set-Up	t_{SAC}	Minimum Time Required From a Low to High or High to Low A0 Transition to Low to High CE Transition to Initiate an 8-bit or 12-bit Conversion, Respectively.	1, 10	+25°C	0		ns
A_0 Valid During CE High	t_{HAC}	Minimum Time Required From a Low to High CE Transition to Low to High or High to Low to Low A_0 Transition to Guarantee a 12-bit or 8-bit Conversion, Respectively.	1, 10	+25°C	50		ns
Access Time From CE	t_{DD}	Output Data Valid, Referenced to Low to High CE Transition Output Code = 000000000000 & 111111111111	1, 2, 10	+25°C		150	ns
				+125°C, -55°C		250	ns
Data Valid After CE Low	t_{HD}	Output Data Valid, Referenced to High to Low CE Transition Output Code = 000000000000 & 111111111111	1, 2, 10	+25°C	25		ns
				+125°C, -55°C	15		ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Devices Characterized At $V_{CC} = +15V$, $V_{EE} = -15V$, $V_{LOG} = 5.0V$, Unless Otherwise Specified. Load is 3kΩ, 50pF where applicable. Figure 3, 4, 5, & 6 applies Unless Otherwise Noted.

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMP	HI-674AS/883 HI-674AT/883 MIN	MAX	UNITS
Output Float Delay	t_{HL}	Output Delay to HI-Z, Referenced to High to Low CE Transition Output Code = 000000000000 & 111111111111	1, 2, 10	+25°C, +125°C, -55°C		150	ns
$\overline{CS}$ To CE Setup	t_{SSR}	Minimum Time from $\overline{CS}$ High to Low Transition to CE Low to High Transition to Guarantee Data Valid is Controlled by CE. Output Code = 000000000000 & 111111111111	1, 2, 10	+25°C	50		ns
R/$\overline{C}$ to CE Set-Up	t_{SRR}	Minimum Time from R/$\overline{C}$ Low to High Transition To CE Low to High Transition to Guarantee Data Valid is Controlled by CE. Output Code = 000000000000 & 111111111111	1, 2, 10	+25°C	0		ns
A_0 To CE Set-Up	t_{SAR}	Minimum Time From A_0 High to Low or Low to High Transition to CE Low to High Transition to guarantee the correct byte gets enabled.	1, 10	+25°C	50		ns
$\overline{CS}$ Valid After CE Low	t_{HSR}	Minimum Time from CE High to Low Transition to $\overline{CS}$ Low to High Transition to Guarantee High Impedance State is Controlled by CE.	1, 10	+25°C	0		ns
R/$\overline{C}$ High After CE Low	t_{HRR}	Minimum Time from CE High to Low Transition to R/$\overline{C}$ High to Low Transition to Guarantee Device Will Disable Before Another Conversion is Initiated.	1, 10	+25°C	0		ns
A_0 Valid After CE Low	t_{HAR}	Minimum Time From CE High to Low Transition to A_0 High to Low or Low to High Transition to Guarantee Enabled Byte Does Not Change Until Device Is Disabled	1, 10	+25°C	50		ns

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DATA CONVERSION PRODUCTS

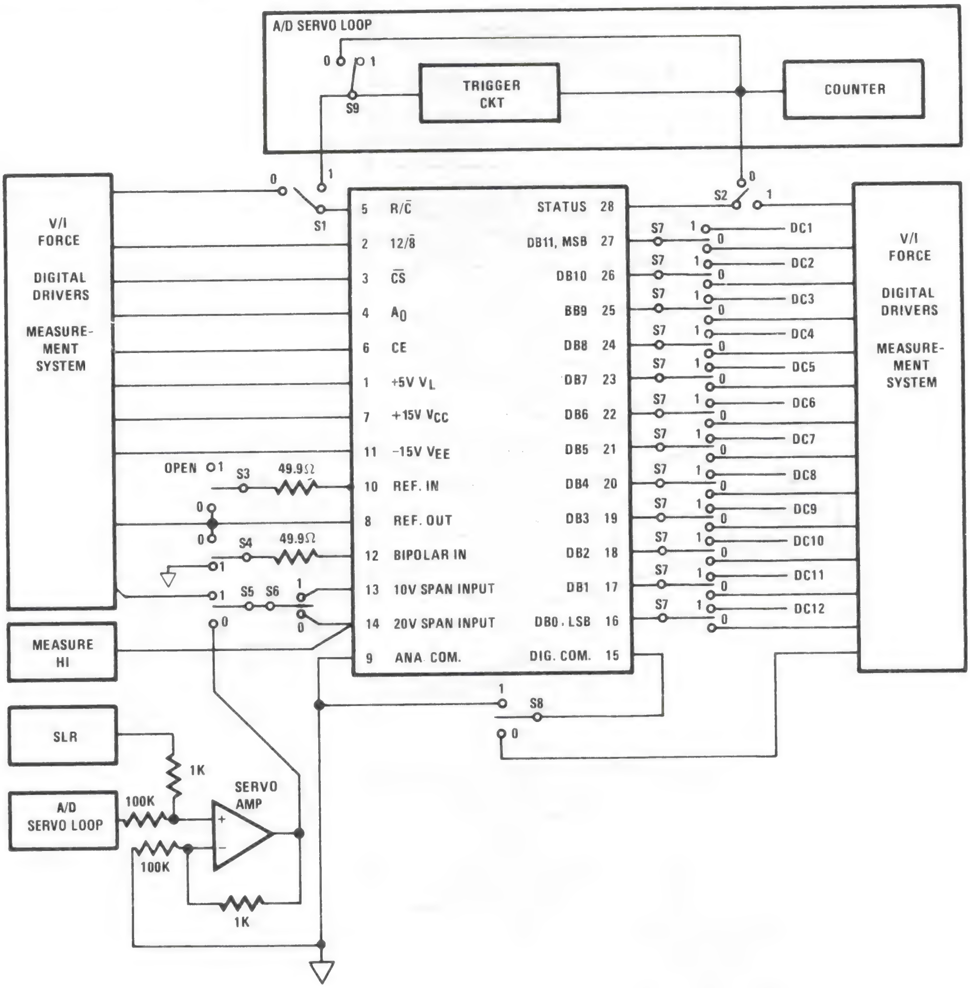
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

*PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

NOTES:
1. See definitions.
2. A output code of 0000 0000 0000 is guaranteed by an input voltage $V_{IN} = -1V$ and an output code of 1111 1111 1111 is guaranteed by an input voltage $V_{IN} = 11V$.
3. $P_d = (V_{CC} * I_{CC} + V_{EE} * I_{EE} + V_{LOGIC} * I_{LOGIC})$ Power dissipation shall be calculated using the two output code conditions 0000 0000 0000 and 1111 1111 1111.
4. The reference voltage external load current shall be constant direct current and shall not exceed 2mA.
5. X represents the transition point between two adjacent code-words
(ie: 0000 0000 000X represents the transition between code-words 0000 0000 0000 and 0000 0000 0001,
XXXX XXXX XXXX represents the transition between code-words
0111 1111 1111 and 1000 0000 0000 and
1111 1111 111X represents the transition between code-words
1111 1111 1110 and 1111 1111 1111).
6. Implies a falling edge transition from 2.4V to 0.8V, after remaining input pins are set.
7. Implies a falling edge transition from 2.4V to 0.8V, after remaining input pins are set, then, after a minimum of 200ns, a rising edge transition to 2.4V.
8. Implies a rising edge transition from 0.8V to 2.4V after remaining input pins are set.
9. $R/\overline{C}$ Implies a falling edge from 2.4V to a TTL Low, approximately 0.0V.
10. The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
11. A conversion must be performed at the inputted voltage prior to R_i10V and R_i20V measurements.

Test Circuit and Test Conditions



NOTES:
1. The connections of the V/I force, digital drivers, and measurement system are software controlled.
2. DC1 → DC12 are input bits of the digital comparator in the A/D servo loop.
3. SLR => super linear reference.

FIGURE 1.TEST CIRCUIT

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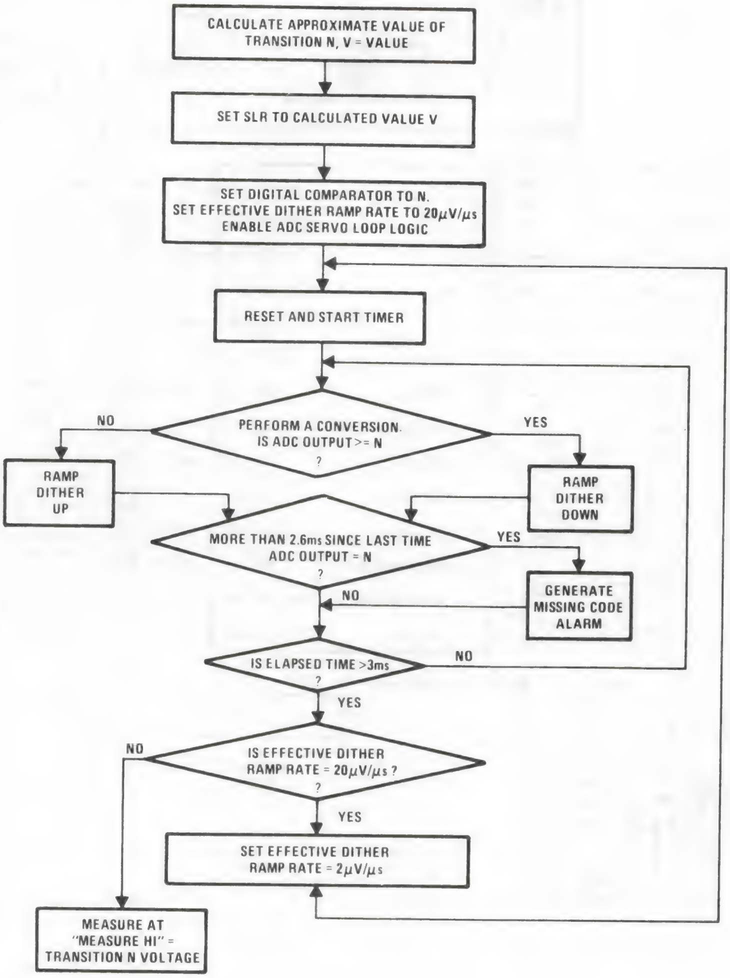
DATA CONVERSION PRODUCTS

Test Circuit and Test Conditions (Continued)



NOTES:

1. SLR = Super Linear Reference.
2. See Figure 1 for Test Circuit.

FIGURE 2. TEST FLOW FOR ANALOG TO DIGITAL SERVO LOOP

CHART A. GROUP A TEST CONDITIONS

SYMBOL	APPLIED VOLTAGES REF. ANALOG COMMON (FIG. 1, NOTE 1) 7 V_{CC} (V)	11 V_{EE} (V)	1 V_{LOG} (V)	13/14 V_{IN} (V)	2 $12/\overline{8}$ (V)	3 $\overline{CS}$ (V)	4 A_0 (V)	5 $R/\overline{C}$ (V)	6 CE (V)	APPLIED DIGITAL CODEWORD $DC_1 \leftrightarrow DC_{12}$ MSB ↔ LSB	DUT DIGITAL OUTPUT CODEWORD 27 ↔ 16 MSB ↔ LSB	SWITCH POSITIONS $S_1 \leftrightarrow S_9$	MEASUREMENT SENSE LINES REF. ANA. COMMON PIN	VALUE	UNIT	TEMP °C	EQUATIONS & NOTES
I_{CC1} I_{CC2}	+15 +15	-15 -15	+5.0 +5	-1 11	2.4 2.4	0.8 0.8	0.8 0.8		2.4 2.4		000000000000 111111111111	010111011 010111011	7 7	I_1 I_2	mA mA	+25, +125,-55	$I_{CC1} = I_1$ $I_{CC2} = I_2$
I_{EE1} I_{EE2}	+15 +15	-15 -15	+5 +5	-1 11	2.4 2.4	0.8 0.8	0.8 0.8		2.4 2.4		000000000000 111111111111	010111011 01011011	11 11	I_3 I_4	mA mA	+25, +125, -55	$I_{EE1} = I_3$ $I_{EE2} = I_4$
I_{LOG1} I_{LOG2}	+15 +15	-15 -15	+5 +5	-1 11	2.4 2.4	0.8 0.8	0.8 0.8		2.4 2.4		000000000000 111111111111	010111011 010111011	1 1	I_5 I_6	mA mA	+25, +125,	$I_{LOG1} = I_5$ $I_{LOG2} = I_6$
P_{D1} P_{D2}	+15 +15	-15 -15	+5 +5	-1 11							000000000000 111111111111					+25, +125, -55	$P_{D1} = (I_{CC1})(V_{CC}) + (I_{EE1})(V_{EE}) + (I_{LOG1})(V_{LOG})$ $P_{D2} = (I_{CC2})(V_{CC}) + (I_{EE2})(V_{EE}) + (I_{LOG2})(V_{LOG})$
I_{IL1} thru I_{IL5}	+15	-15	+5.5	-1	0	0	0	0	0			010111011	2 thru 6	I_7 thru I_{11}	μA	+25, +125, -55	I_{IL1} thru I_{IL5} = I_7 thru I_{11} Respectively
I_{IH1} thru I_{IH5}	+15	-15	+5.5	11	2.4	2.4	2.4	2.4	2.4			010111011	2 thru 6	I_{12} thru I_{16}	μA	+25, +125, -55	I_{IH1} thru I_{IH5} = I_{12} thru I_{16} Respectively
I_{IH6} thru I_{IH10}	+15	-15	+5.5	11	5.5	5.5	5.5	5.5	5.5			010111011	2 thru 6	I_{17} thru I_{21}	μA	+25, +125, -55	I_{IH6} thru I_{IH10} = I_{17} thru I_{21} Respectively
I_{ZL1} thru I_{ZH12}	+15	-15	+5.5	11	2.4	0.8	0.8		2.4		000000000000	010111011	16 thru 27	I_{22} thru I_{33}	μA	+25, +125, -55	I_{ZL1} thru I_{ZL12} = I_{22} thru I_{33} Respectively. V_O = 0.0V (Note 9)
I_{ZH1} thru I_{ZH12}	+15	-15	+5.5	-1	2.4	0.8	0.8		2.4		111111111111	010111011	16 thru 27	I_{34} thru I_{45}	μA	+25, +125, -55	I_{ZH1} thru I_{ZH12} = I_{34} thru I_{45} Respectively. V_O = 5.5V (Note 9)
V_{OL1} thru V_{OL13}	+15	-15	+4.5	-1	2.4	0.8	0.8		2.4		000000000000	010111011	16 thru 28	E_1 thru E_{13}	V	+25, +125, -55	V_{OL1} thru V_{OL13} = E_1 thru E_{13} Respectively. I_L = 1.6mA
V_{OH1} thru V_{OH12}	+15	-15	+4.5	11	2.4	0.8	0.8		2.4		111111111111	010111011	16 thru 27	E_{14} thru E_{25}	V	+25, +125, -55	V_{OH1} thru V_{OH12} = E_{14} thru E_{25} Respectively. I_L = -0.5mA

See Notes at End of Table 4.

CHART A. GROUP A TEST CONDITIONS (Continued)

SYMBOL	APPLIED VOLTAGES REF. ANALOG COMMON (FIG. 1, NOTE 1)									APPLIED DIGITAL CODEWORD	DUT DIGITAL OUTPUT CODEWORD	SWITCH POSITIONS	MEASUREMENT SENSE LINES REF. ANA. COMMON			TEMP C	EQUATIONS & NOTES
	7	11	1	13/14	2	3	4	5	6								
	V_{CC} (V)	V_{EE} (V)	V_{LOG} (V)	V_{IN} (V)	$12/\overline{8}$ (V)	$\overline{CS}$ (V)	A_0 (V)	$R/\overline{C}$ (V)	CE (V)	$DC_1 \longleftrightarrow DC_{12}$ MSB ⟷ LSB	$2^7 \longleftrightarrow 16$ MSB ⟷ LSB	$S_1 \longleftrightarrow S_9$	PIN	VALUE	UNIT		
V_{REF1}	+15	-15	+5	1	2.4	0.8	0.8		2.4		000000000000	011111011	8	E_{26}	V	+25, +125, -55	$V_{REF1} = E_{27}$ $I_L = 0mA$
V_{REF2}	+15	-15	+5	-11	2.4	0.8	0.8		2.4		00000000000	010011011	8	E_{27}	V		$V_{REF2} = E_{28}$, $I_L = 2.0mA$ Bipolar, $V_{FSR} = 20V$
$+P_{SS1}$	13.5 13.5 16.5 16.5	-15 -15 -15 -15	5.0 5.0 5.0 5.0	SERV LOOP	2.4	0.8	0.8	TRIG CKT.	2.4	000000000000 111111111110 000000000000 111111111110	00000000000X 11111111111X 00000000000X 11111111111X	100101111	14	E_{200} E_{201} E_{202} E_{203}	V V V V	+25, +125, -55	$+P_{SS1} = [(E_{203} - E_{202}) - (E_{201} - E_{200})]/ [(E_{42X} - E_{41X})/4094]$ Where X = R for +25°C = H for 125°C = L for -55°C
$+P_{SS2}$	11.4 11.4 12.6 12.6	-15 -15 -15 -15	5.0 5.0 5.0 5.0	SERV LOOP	2.4	0.8	0.8	TRIG CKT.	2.4	000000000000 111111111110 000000000000 111111111110	00000000000X 11111111111X 00000000000X 11111111111X	100101111	14	E_{204} E_{205} E_{206} E_{207}	V V V V	+25, +125, -55	$+P_{SS2} = [(E_{207} - E_{206}) - (E_{205} - E_{204})]/ [(E_{42X} - E_{41X})/4094]$ Where X = R for +25°C = H for 125°C = L for -55°C
$+P_{SS3}$	+15 +15 +15 +15	-15 -15 -15 -15	4.5 4.5 5.5 5.5	SERV LOOP	2.4	0.8	0.8	TRIG CKT.	2.4	000000000000 111111111110 000000000000 111111111110	00000000000X 11111111111X 00000000000X 11111111111X	100101111	14	E_{208} E_{209} E_{210} E_{211}	V V V V	+25, +125, -55	$+P_{SS3} = [(E_{211} - E_{210}) - (E_{209} - E_{208})]/ [(E_{42X} - E_{41X})/4094]$ Where X = R for +25°C = H for 125°C = L for -55°C
$-P_{SS1}$	+15 +15 +15 +15	-13.5 -13.5 -16.5 -16.5	5.0 5.0 5.0 5.0	SERV LOOP	2.4	0.8	0.8	TRIG CKT.	2.4	000000000000 111111111110 000000000000 111111111110	00000000000X 11111111111X 00000000000X 11111111111X	100101111	14	E_{212} E_{213} E_{214} E_{215}	V V V V	+25, +125, -55	$-P_{SS1} = [(E_{215} - E_{214}) - (E_{213} - E_{212})]/ [(E_{42X} - E_{41X})/4094]$ Where X = R for +25°C = H for 125°C = L for -55°C
$-P_{SS2}$	+15 +15 +15 +15	-11.4 -11.4 -12.6 -12.6	5.0 5.0 5.0 5.0	SERV LOOP	2.4	0.8	0.8	TRIG CKT.	2.4	000000000000 111111111110 000000000000 111111111110	00000000000X 11111111111X 00000000000X 11111111111X	100101111	14	E_{216} E_{217} E_{218} E_{219}	V V V V	+25°C +125, -55	$-P_{SS2} = [(E_{219} - E_{218}) - (E_{217} - E_{216})]/ [(E_{42X} - E_{41X})/4094]$ Where X = R for +25°C = H for 125°C = L for -55°C

CHART A. GROUP A TEST CONDITIONS (Continued)

SYMBOL	APPLIED VOLTAGES REF. ANALOG COMMON (FIG. 1, NOTE 1) 7 V_{CC} (V)	11 V_{EE} (V)	1 V_{LOG} (V)	13/14 V_{IN} (V)	2 $12/\overline{8}$ (V)	3 $\overline{CS}$ (V)	4 A_0 (V)	5 $R/\overline{C}$ (V)	6 CE (V)	APPLIED DIGITAL CODEWORD $DC_1 \longleftrightarrow DC_{12}$ MSB ⟷ LSB	DUT DIGITAL OUTPUT CODEWORD 27 ⟷ 16 MSB ⟷ LSB	SWITCH POSITIONS $S_1 \longleftrightarrow S_9$	MEASUREMENT SENSE LINES REF. ANA. COMMON PIN	VALUE	UNIT	TEMP °C	EQUATIONS & NOTES
V_{IOR}	+15	-15	+5	SERV LOOP	2.4	0.8	0.8	TRIG CKT.	2.4	000000000000	00000000000X	100101111	14	E_{38R}	V	+25	V_{IOR} = ((E38R)-(0.5 AR / 4095))/(AR / 4095)
V_{IOH}	+15	-15	+5		2.4	0.8	0.8		2.4	000000000000	00000000000X	100101111	14	E_{38H}	V	+125	V_{IOH} => Same as V_{IOR} with R = H
V_{IOL}	+15	-15	+5		2.4	0.8	0.8		2.4	000000000000	00000000000X	100101111	14	E_{38L}	V	-55	V_{IOL} => Same as V_{IOR} with R = L
B_{ZR}	+15	-15	+5	SERV LOOP	2.4 2.4	0.8 0.8	0.8 0.8	TRIG CKT.	2.4 2.4	011111111111 100000000000	XXXXXXXXXXXX 10000000000X	100000111	14 14	E_{39R} E_{40R}	V V	+25	B_{ZR} = ((E_{39R} + E_{40R})/2)/(B_{AR} /4095)
B_{ZH}	+15	-15	+5		2.4 2.4	0.8 0.8	0.8 0.8		2.4 2.4	011111111111 100000000000	XXXXXXXXXXX 10000000000X	100000111	14 14	E_{39H} E_{40H}	V V	+125	B_{ZH} => Same as B_{ZR} with R = H
B_{ZL}	+15	-15	+5		2.4 2.4	0.8 0.8	0.8 0.8		2.4 2.4	011111111111 100000000000	XXXXXXXXXXXX 10000000000X	100000111	14 14	E_{39L} E_{40L}	V V	-55	B_{ZL} => Same as B_{ZR} with R = L
A_{ER}	+15	-15	+5	SERV LOOP	2.4 2.4	0.8 0.8	0.8 0.8	TRIG CKT.	2.4 2.4	000000000000 111111111110	00000000000X 11111111111X	100101111	14 14	E_{41R} E_{42R}	V V	+25	A_R = (E_{42R} - E_{41R}) [(E_{42R} - E_{41R})/4094]
																+25	A_{ER} = [(A_R - 9.99756V)/10V]100
A_{EH}	+15	-15	+5		2.4 2.4	0.8 0.8	0.8 0.8		2.4 2.4	000000000000 111111111110	00000000000X 11111111111X	100101111	14 14	E_{41H} E_{42H}	V V	+125	A_{EH} => Same as A_{ER} with R = H
A_{EL}	+15	-15	+5		2.4 2.4	0.8 0.8	0.8 0.8		2.4 2.4	000000000000 111111111110	000000000000X 11111111111X	100101111	14 14	E_{41L} E_{42L}	V V	-55	A_{EL} => Same as A_{ER} with R = L
BA_{ER}	+15	-15	+5	SERV LOOP	2.4 2.4	0.8 0.8	0.8 0.8	TRIG CKT.	2.4 2.4	000000000000 111111111110	00000000000X 11111111111X	100000111	14 14	E_{43R} E_{44R}	V V	+25	BA_R = (E_{44R} - E_{43R}) + [(E_{44R} - E_{42R})/4094]
																+25	BA_{ER} = [(BA_R - 19.99512V)/ 20V]100
BA_{EH}	+15	-15	+5		2.4 2.4	0.8 0.8	0.8 0.8		2.4 2.4	000000000000 111111111110	00000000000X 11111111111X	100000111	14 14	E_{43H} E_{44H}	V V	+125	BA_{EH} => Same as BA_{ER} with R = H
BA_{EL}	+15	-15	+5		2.4 2.4	0.8 0.8	0.8 0.8		2.4 2.4	000000000000 111111111110	00000000000X 11111111111X	100000111	14 14	E_{43L} E_{44L}	V V	-55	BA_{EL} => Same as BA_{ER} with R = L

CHART A. GROUP A TEST CONDITIONS

SYMBOL	APPLIED VOLTAGES REF. ANALOG COMMON (FIG. 1, NOTE 1) 7	11	1	13/14	2	3	4	5	6	APPLIED DIGITAL CODEWORD	DUT DIGITAL OUTPUT CODEWORD	SWITCH POSITIONS	MEASUREMENT SENSE LINES REF. ANA. COMMON			TEMP °C	EQUATIONS & NOTES
	V_{CC} (V)	V_{EE} (V)	V_{LOG} (V)	V_{IN} (V)	$12/\overline{8}$ (V)	$\overline{CS}$ (V)	A_0 (V)	$R/\overline{C}$ (V)	CE (V)	$DC_1 \longleftrightarrow DC_{12}$ MSB ⟷ LSB	$27 \longleftrightarrow 16$ MSB ⟷ LSB	$S_1 \longleftrightarrow S_9$	PIN	VALUE	UNIT		
																+25, +125, -55	For Endpoint Linearity Error $L_E(N) = ((E(N+45) + E(N+46))/2) - V(IDEAL)/S$ $V(IDEAL) = (N1)(S) + E_{46} - S/2N1$ = Applied Code Word $S = (E_{45}-E_{46})/4094$
	+15	-15	+5	SERV LOOP	2.4	0.8	0.8	TRIG CKT	2.4	111111111110	11111111111X	100101111	14	E_{45}	V		
										000000000000	00000000000X			E_{46}			
L_{E1}										000000000001	0000000000XX			E_{47}			L_{E1} With N1 = 1
L_{E2}										000000000010	00000000001X			E_{48}			L_{E2} With N1 = 2
										000000000011	000000000XXX			E_{49}			
L_{E4}										000000000100	00000000010X			E_{50}			L_{E4} With N1 = 4
										000000000111	00000000XXXX			E_{51}			
L_{E6}										000000001000	00000000100X			E_{52}			L_{E6} With N1 = 8
										000000001111	0000000XXXXX			E_{53}			
L_{E8}										000000010000	00000001000X			E_{54}			L_{E8} With N1 = 16
										000000011111	000000XXXXXX			E_{55}			
L_{E10}										000000100000	00000010000X			E_{56}			L_{E10} With N1 = 32
										000000111111	00000XXXXXXX			E_{57}			
L_{E12}										000001000000	00000100000X			E_{58}			L_{E12} With N1 = 64
										000001111111	0000XXXXXXXX			E_{59}			
L_{E14}										000010000000	00001000000X			E_{60}			L_{E14} With N1 = 128
										000011111111	000XXXXXXXXX			E_{61}			
L_{E16}										000100000000	00010000000X			E_{62}			L_{E16} With N1 = 256
										000111111111	00XXXXXXXXXX			E_{63}			

CHART A. GROUP A TEST CONDITIONS (Continued)

SYMBOL	APPLIED VOLTAGES REF. ANALOG COMMON (FIG. 1, NOTE 1) 7 VCC (V)	11 VEE (V)	1 VLOG (V)	13/14 VIN (V)	2 $12/\overline{8}$ (V)	3 $\overline{CS}$ (V)	4 A0 (V)	5 $R/\overline{C}$ (V)	6 CE (V)	APPLIED DIGITAL CODEWORD $DC_1 \longleftrightarrow DC_{12}$ MSB ⟷ LSB	DUT DIGITAL OUTPUT CODEWORD 27 ⟷ 16 MSB ⟷ LSB	SWITCH POSITIONS $S_1 \longleftrightarrow S_9$	MEASUREMENT SENSE LINES REF. ANA. COMMON PIN	VALUE	UNIT	TEMP °C	EQUATIONS & NOTES
L_{E18}	+15	-15	+5	SERV LOOP	2.4	0.8	0.8	TRIG CKT.	2.4	001000000000	00100000000X	100101111	14	E_{64}	V	+25, +125, -55	L_{E18} With N1 = 512
										001111111111	0XXXXXXXXXXX			E_{65}			
L_{E20}										010000000000	01000000000X			E_{66}			L_{E20} With N1 = 1024
										011111111111	XXXXXXXXXXXX			E_{67}			
L_{E22}										100000000000	10000000000X			E_{68}			L_{E22} With N1 = 2048
										100011111111	100XXXXXXXXX			E_{69}			
L_{E24}										100100000000	10010000000X			E_{70}			L_{E24} With N1 = 2304
										100111111111	10XXXXXXXXXX			E_{71}			
L_{E26}										101000000000	10100000000X			E_{72}			L_{E26} With N1 = 2560
										101011111111	101XXXXXXXXX			E_{73}			
L_{E28}										101100000000	10110000000X			E_{74}			L_{E28} With N1 = 2816
										101111111111	1XXXXXXXXXXX			E_{75}			
L_{E30}										110000000000	11000000000X			E_{76}			L_{E30} With N1 = 3072
										110011111111	110XXXXXXXXX			E_{77}			
L_{E32}										110100000000	11010000000X			E_{78}			L_{E32} With N1 = 3328
										110111111111	11XXXXXXXXXX			E_{79}			
L_{E34}										111000000000	11100000000X			E_{80}			L_{E34} With N1 = 3584
										111011111111	111XXXXXXXXX			E_{81}			
L_{E36}										111100000000	11110000000X			E_{82}			L_{E36} With N1 = 3840
L_{E38}										Turn on bits that had positive integral linearity error for L_{E1} to L_{E22}	Low Edge			E_{83}			L_{E38} With N1 = Sum of positive L_{E1} to L_{E22}
											High Edge			E_{84}			

CHART A. GROUP A TEST CONDITIONS (Continued)

SYMBOL	APPLIED VOLTAGES REF. ANALOG COMMON (FIG. 1, NOTE 1) 7	11	1	13/14	2	3	4	5	6	APPLIED DIGITAL CODEWORD	DUT DIGITAL OUTPUT CODEWORD	SWITCH POSITIONS	MEASUREMENT SENSE LINES REF. ANA. COMMON			TEMP °C	EQUATIONS & NOTES
	V_{CC} (V)	V_{EE} (V)	V_{LOG} (V)	V_{IN} (V)	$12/\overline{8}$ (V)	$\overline{CS}$ (V)	A_0 (V)	$R/\overline{C}$ (V)	CE (V)	$DC_1 \longleftrightarrow DC_{12}$ MSB ⟷ LSB	$2^7 \longleftrightarrow 16$ MSB ⟷ LSB	$S_1 \longleftrightarrow S_9$	PIN	VALUE	UNIT		
L_{E40}	+15	-15	+5	SERV LOOP	2.4	0.8	0.8	TRIG CKT	2.4	Turn on bits that had negative integral linearity error for L_{E1} to L_{E22}	Low Edge	100101111	14	E_{85}	V		L_{E40} With N1 = Sum of negative L_{E1} to L_{E22}
											High Edge			E_{86}			
																+25, +125, -55	For Differential Linearity Error $D_{LE}(N) = (E(N+88) - E(N+87))/S$, $S = (E_{87} - E_{88})/4094$
										111111111110	11111111111X			E_{87}			
										000000000000	00000000000X			E_{88}			
D_{LE1}										000000000001	0000000000XX			E_{89}			D_{LE1}
D_{LE2}										000000000010	00000000001X			E_{90}			D_{LE2}
D_{LE3}										000000000011	000000000XXX			E_{91}			D_{LE3}
D_{LE4}										000000000100	00000000010X			E_{92}			D_{LE4}
										000000000110	00000000011X			E_{93}			
D_{LE6}										000000000111	00000000XXXX			E_{94}			D_{LE6}
D_{LE7}										000000001000	00000000100X			E_{95}			D_{LE7}
										000000001110	00000000111X			E_{96}			
D_{LE9}										000000001111	0000000XXXXX			E_{97}			D_{LE9}
D_{LE10}										000000010000	00000001000X			E_{98}			D_{LE10}
										000000011110	00000001111X			E_{99}			
D_{LE12}										000000011111	000000XXXXXX			E_{100}			D_{LE12}
D_{LE13}										000000100000	00000010000X			E_{101}			D_{LE13}
										000000111110	00000011111X			E_{102}			

CHART A. GROUP A TEST CONDITIONS (Continued)

	APPLIED VOLTAGES REF. ANALOG COMMON (FIG. 1, NOTE 1)									APPLIED DIGITAL CODEWORD	DUT DIGITAL OUTPUT CODEWORD	SWITCH POSITIONS	MEASUREMENT SENSE LINES REF. ANA. COMMON				
	7	11	1	13/14	2	3	4	5	6								
SYMBOL	V_{CC} (V)	V_{EE} (V)	V_{LOG} (V)	V_{IN} (V)	$12/\overline{8}$ (V)	$\overline{CS}$ (V)	A_0 (V)	$R/\overline{C}$ (V)	CE (V)	$DC_1 \longleftrightarrow DC_{12}$ MSB ⟷ LSB	27 ⟷ 16 MSB ⟷ LSB	$S_1 \longleftrightarrow S_9$	PIN	VALUE	UNIT	TEMP °C	EQUATIONS & NOTES
D_{LE15}	+15	-15	+5	SERV LOOP	2.4	0.8	0.8	TRIG CKT.	2.4	000000111111	00000XXXXXXX	100101111	14	E_{103}	V	+25, +125 -55	D_{LE15}
D_{LE16}										000001000000	00000100000X			E_{104}			D_{LE16}
										000001111110	00000111111X			E_{105}			
D_{LE18}										000001111111	0000XXXXXXXX			E_{106}			D_{LE18}
D_{LE19}										000010000000	00001000000X			E_{107}			D_{LE19}
										000011111110	00000111111X			E_{108}			
D_{LE21}										000011111111	000XXXXXXXXX			E_{109}			D_{LE21}
D_{LE22}										000100000000	00010000000X			E_{110}			D_{LE22}
										000111111110	00011111111X			E_{111}			
D_{LE24}										000111111111	00XXXXXXXXXX			E_{112}			D_{LE24}
D_{LE25}										001000000000	00100000000X			E_{113}			D_{LE25}
										001111111110	00111111111X			E_{114}			
D_{LE27}										001111111111	0XXXXXXXXXXX			E_{115}			D_{LE27}
D_{LE28}										010000000000	01000000000X			E_{116}			D_{LE28}
										011111111110	01111111111X			E_{117}			
D_{LE30}										011111111111	XXXXXXXXXXXX			E_{118}			D_{LE30}
D_{LE31}										100000000000	10000000000X			E_{119}			D_{LE31}
										100011111110	10001111111X			E_{120}			
D_{LE33}										100011111111	100XXXXXXXXX			E_{121}			D_{LE33}
D_{LE34}										100100000000	10010000000X			E_{122}			D_{LE34}
										100111111110	10011111111X			E_{123}			
D_{LE36}										100111111111	10XXXXXXXXXX			E_{124}			D_{LE36}
D_{LE37}										101000000000	10100000000X			E_{125}			D_{LE37}

DATA CONVERSION PRODUCTS 6

CHART A. GROUP A TEST CONDITIONS (Continued)

SYMBOL	APPLIED VOLTAGES REF. ANALOG COMMON (FIG. 1, NOTE 1) 7: V_{CC} (V)	11: V_{EE} (V)	1: V_{LOG} (V)	13/14: V_{IN} (V)	2: $12/\overline{8}$ (V)	3: $\overline{CS}$ (V)	4: A_0 (V)	5: $R/\overline{C}$ (V)	6: CE (V)	APPLIED DIGITAL CODEWORD $DC_1 \longleftrightarrow DC_{12}$ MSB ⟷ LSB	DUT DIGITAL OUTPUT CODEWORD $2^7 \longleftrightarrow 16$ MSB ⟷ LSB	SWITCH POSITIONS $S_1 \longleftrightarrow S_9$	MEASUREMENT SENSE LINES REF. ANA. COMMON PIN	VALUE	UNIT	TEMP °C	EQUATIONS & NOTES
	+15	-15	+5	SERV LOOP	2.4	0.8	0.8	TRIG CKT	2.4	101011111110	10101111111X	100101111	14	E_{126}	V	+25, +125, -55	
D_{LE39}										101011111111	101XXXXXXXXX			E_{127}			D_{LE39}
D_{LE40}										101100000000	10110000000X			E_{128}			D_{LE40}
										101111111110	10111111111X			E_{129}			
D_{LE42}										101111111111	1XXXXXXXXXXX			E_{130}			D_{LE42}
D_{LE43}										110000000000	11000000000X			E_{131}			D_{LE43}
										110011111110	11001111111X			E_{132}			
D_{LE45}										110011111111	110XXXXXXXXX			E_{133}			D_{LE45}
D_{LE46}										110100000000	11010000000X			E_{134}			D_{LE46}
										110111111110	11011111111X			E_{135}			
D_{LE48}										110111111111	11XXXXXXXXXX			E_{136}			D_{LE48}
D_{LE49}										111000000000	11100000000X			E_{137}			D_{LE49}
										111011111110	11101111111X			E_{138}			
D_{LE51}										111011111111	111XXXXXXXXX			E_{139}			D_{LE51}
D_{LE52}										111100000000	11110000000X			E_{140}			D_{LE52}
D_{LE54}										Turn on Bits	Low Edge			E_{141}			D_{LE54}
										that had positive differential linearity error for DLE's 1, 2, 4, 7, 10, 13, 16, 19, 22, 25, 28, 31 Minus 1 LSB	High Edge			E_{142}			
D_{LE55}										Turn on Bits that had positive differential linearity error for DLE's 1, 2, 4, 7, 10, 13, 16, 19, 22, 25, 28, 31	High Edge			E_{143}			D_{LE55}

CHART A. GROUP A TEST CONDITIONS (Continued)

SYMBOL	APPLIED VOLTAGES REF. ANALOG COMMON (FIG. 1, NOTE 1)									APPLIED DIGITAL CODEWORD	DUT DIGITAL OUTPUT CODEWORD	SWITCH POSITIONS	MEASUREMENT SENSE LINES REF. ANA. COMMON			TEMP °C	EQUATIONS & NOTES
	7	11	1	13/14	2	3	4	5	6								
	V_{CC} (V)	V_{EE} (V)	V_{LOG} (V)	V_{IN} (V)	$12/\overline{8}$ (V)	$\overline{CS}$ (V)	A_0 (V)	$R/\overline{C}$ (V)	CE (V)	$DC_1 \longleftrightarrow DC_{12}$ MSB ⟷ LSB	27 ⟷ 16 MSB ⟷ LSB	$S_1 \longleftrightarrow S_9$	PIN	VALUE	UNIT		
D_{LE57}										Turn on Bits that had negative differential linearity error for DLE's 1, 2, 4, 7, 10, 13, 16, 19, 22, 25, 28, 31 Minus 1 LSB	Low Edge High Edge			E_{144} E_{145}			D_{LE57}
D_{LE58}										Turn on Bits that had negative differential linearity error for DLE's 1, 2, 4, 7, 10, 13, 16, 19, 22, 25, 28, 31	High Edge			E_{146}			D_{LE58}
R_{i10V} R_{i20V}	+15 +15	-15 -15	+5 +5	5 10								010111011 010110011	13 14	I_{46} I_{47}	mA mA	+25, +125, -55	$R_{i10V} = 5V/I_{46}$ $R_{i20V} = 10V/I_{47}$
$\frac{dV_{IO}}{dT}$	+15	-15	+5													+125 -55	$dV_{IO}/dT = V_{IOH} - V_{IOR}$ $dV_{IO}/dT = V_{IOL} - V_{IOR}$
$\frac{dB_Z}{dT}$	+15	-15	+5													+125 -55	$dB_Z/dT = B_{ZH} - B_{ZR}$ $dB_Z/dT = B_{ZL} - B_{ZR}$
$\frac{dA_E}{dT}$	+15	-15	+5													+125 -55	$dA_E/dT = A_{EH} - A_{ER}$ $dA_E/dT = A_{EL} - A_{ER}$
$\frac{dBA_E}{dT}$	+15	-15	+5													+125 -55	$dBA_E/dT = BA_{EH} - BA_{ER}$ $dBA_E/dT = BA_{EL} - BA_{ER}$
t_{C1}	+15	-15	+5	SERV LOOP	2.4	0.8	2.4	TRIG CKT.	2.4	000000000000	00000000000X	100101111	28	t_1	μs	+25, +125, -55	$t_{C1} = t_1$ Rising Edge to Falling Edge
t_{C2}	+15	-15	+5		2.4	0.8	0.8		2.4	000000000000	00000000000X	100101111	28	t_2	μs	+25, +125, -55	$t_{C2} = t_2$ Rising Edge to Falling Edge
	+15	-15	+5									010111010		t_3	ns	+25, +125, -55	$t_{TD} = t_3$ t_{TD} = Trigger CKT Delay
t_{DS1}	+15	-15	+5	SERV LOOP	2.4	0.8	2.4	TRIG CKT.	2.4	000000000000	00000000000X	100101111	28	t_4	ns	-55	$t_{DS1} = t_4 - t_3 - t_1$ t_4 Meas. Rising Edge to Rising Edge
t_{DS2}	+15	-15	+5		2.4	0.8	0.8		2.4	000000000000	00000000000X	100101111	28	t_5	ns		$t_{DS2} = t_5 - t_3 - t_2$ t_5 Meas. Rising Edge to Rising Edge

Switching Waveform Information

Conversion Length

A Convert Start transition (see Chart B) latches the state of A_0, which determines whether the conversion continues for 12-bits (A_0 low) or stops with 8-bits (A_0 high). If all 12-bits are read following an 8-bit conversion, the three LSBs will read zero and DB3 will read ONE. A_0 is latched because it is also involved in enabling the output buffers (see Reading the Output Data"). No other control inputs are latched.

CHART B. TRUTH TABLE FOR HI-674A/883 CONTROL INPUTS

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

Conversion Start

A conversion may be initiated as shown in Chart B by a logic transition on any of three inputs: CE, $\overline{CS}$ or R/$\overline{C}$. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same, and if necessary, all three may change state simultaneously. See the Timing Specifications, Convert mode.

The variety of control modes allows a simple interface in most system applications. The Convert Start timing relationships are illustrated in Figure 5.

The output signal STS indicates status of the converter by going high only while a conversion is in progress. While STS is high, the output buffers remain in a high impedance state and data cannot be read. Also, an additional Start Convert will not reset the converter or reinitiate a conversion while STS is high. (However, if A_0 changes state after a conversion begins, an additional Start Convert signal will latch the new state of A_0, possibly causing a wrong cycle length (8 vs.`12-bits) for that conversion).

Reading the Output Data

The output data buffers remain in a high impedance state until four conditions are met: R/$\overline{C}$ high, STS low, CE high and $\overline{CS}$ low. At that time, data lines become active according to the state of inputs 12/8 and A_0. Timing constraints are illustated in Figure 6.

The 12/$\overline{8}$ input will be tied high or low in most applications, though it is fully TTL/CMOS compatible. With 12/$\overline{8}$ high, all 12 output lines become active simultaneously, for interface to a 12 or 16-bit data bus. The A_0 input is ignored.

With 12/$\overline{8}$ low, the output is organized in two 8 bit bytes, selected one at a time by A_0. This allows an 8 bit data bus to be connected as shown in Figure 10. A_0 is usually tied to the least significant bit of the address bus, for storing the output data in two consecutive memory locations. (With A_0 low, the 8 MSBs only are enabled. With A_0 high, 4 MSBs are disabled, bits 4 through 7 are forced to zero, and the 4 LSBs are enabled). This two byte format is considered left justified data", for which a decimal (or binary!) point is assumed to the left of byte 1:

BYTE 1	BYTE 2
X X X X X X X X	X X X X 0 0 0 0
MSB	LSB

Further, A_0 may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in Figure 10 will never be enabled at the same time.

A read operation usually begins after the conversion is complete and STS is low. For earliest access to the data however, the read should begin no later than ($t_{DD} + t_{HS}$) before STS goes low. See Figure 6.

STAND-ALONE MODE TIMING (OVER FULL TEMP. RANGE)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	350			ns
t_{DS}	STS Delay from R/$\overline{C}$			600	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	15			ns
t_{HS}	STS Delay After Data Valid	25	300	850	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	300			ns
t_{DDR}	Data Access Time			250	ns

Switching Waveforms

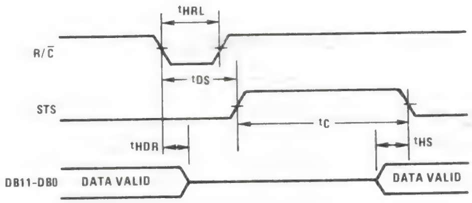


FIGURE 3. LOW PULSE R/C̄-OUTPUTS ENABLED AFTER CONVERSION

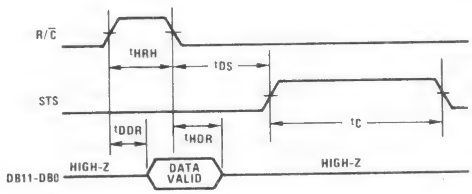


FIGURE 4. HIGH PULSE FOR R/C̄-OUTPUTS ENABLED WHILE R/C̄ HIGH, OTHERWISE HIGH-Z

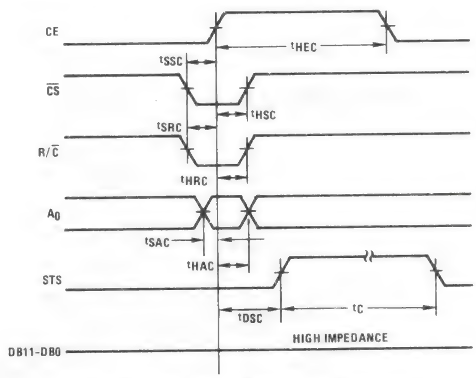


FIGURE 5. CONVERT START TIMING

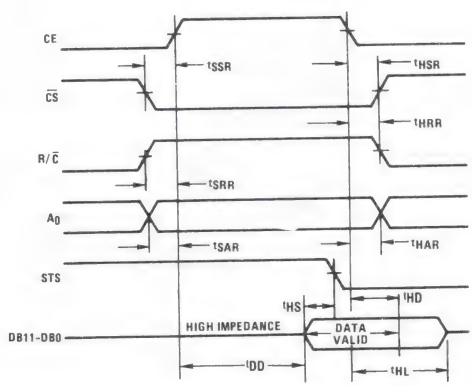
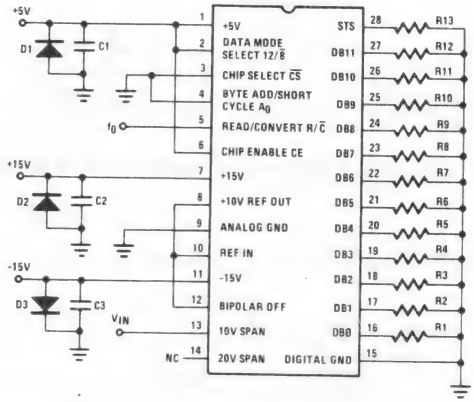


FIGURE 6. READ CYCLE TIMING

6
DATA CONVERSION PRODUCTS

Burn-In Circuits

28 PIN SIDEBRAZED DIP



NOTES:

R1 thru R13 = 10kΩ

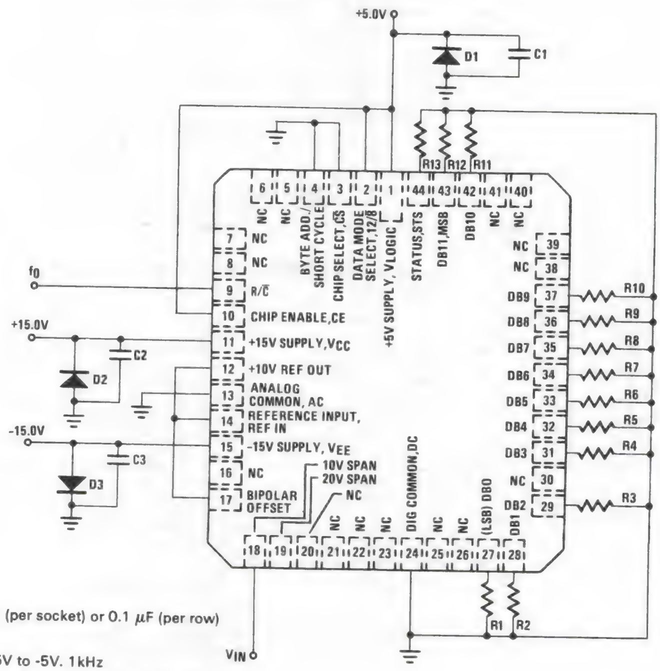
C1 thru C3 = 0.01μF minimum (per socket) or 0.1 μF (per row)

D1 thru D3 = IN4002

V_{IN} = Triangle Wave Form, +5V to -5V. 1kHz

f_0 = square waveform, 10kHz, 90% Duty Cycle, 0V to 5V

44 PIN CERAMIC LEADLESS CHIP CARRIER



NOTES:

R1 thru R13 = 10kΩ

C1 thru C3 = 0.01μF minimum (per socket) or 0.1 μF (per row)

D1 thru D3 = IN4002

V_{IN} = Triangle Wave Form, +5V to -5V. 1kHz

f_0 = square waveform, 10kHz, 90% Duty Cycle, 0V to 5V

Die Characteristics

DIE DIMENSIONS:
- ANALOG DIE: 204 x 104 mils
- DIGITAL DIE: 158 x 84 mils

METALLIZATION:
- ANALOG DIE: Type: Al
  Thickness: 16kÅ ± 2kÅ
- DIGITAL DIE: Type: SiAl
  Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
- ANALOG DIE: 1.63×10^5 A/cm^2
- DIGITAL DIE: 1.93×10^5 A/cm^2

TRANSISTOR COUNT ANALOG DIE: 317
DIGITAL DIE: 800

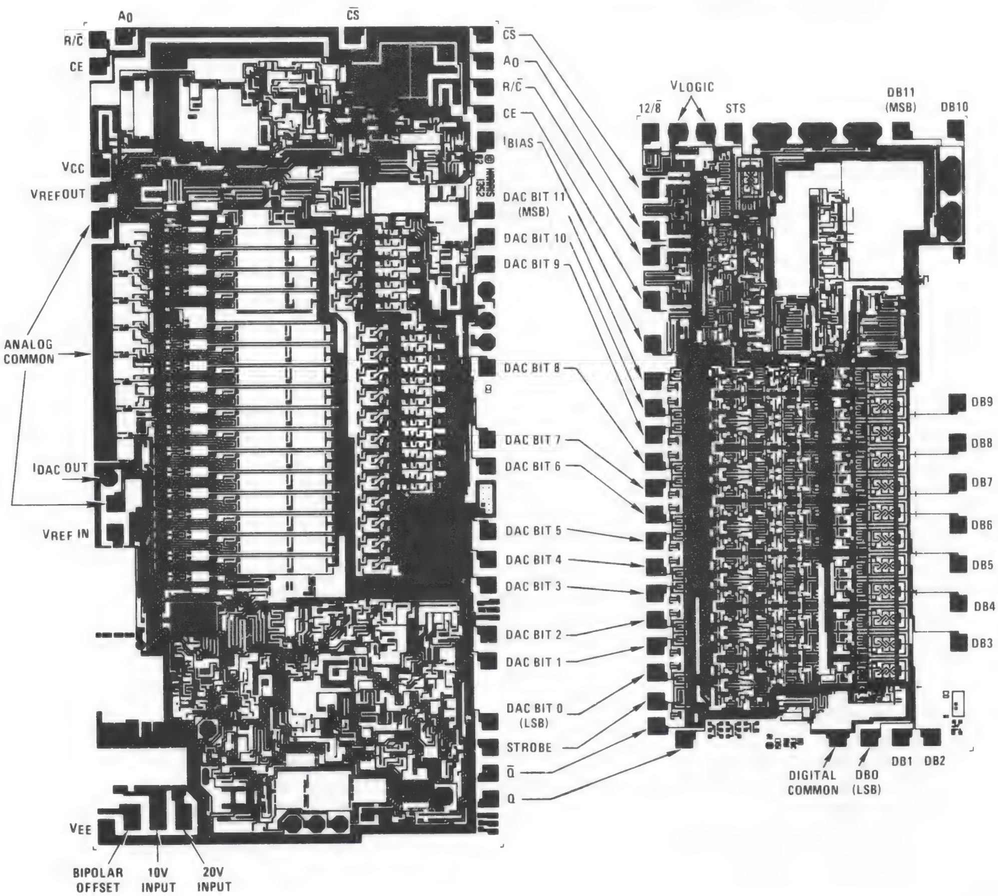
PROCESS: ANALOG DIE: Bipolar-DI
DIGITAL DIE: CMOS-JI

DIE ATTACH: Material: Gold/Silicon Eutectic Alloy
Temperature: 420°C Max

GLASSIVATION:
- ANALOG DIE: Type: Silox
  Thickness: 14kÅ ± 2kÅ
- DIGITAL DIE: Type: Silox
  Thickness: 8kÅ ± 2kÅ

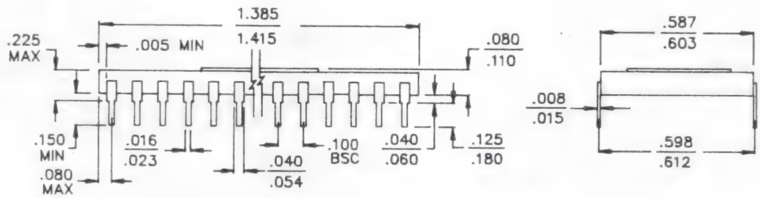
Metallization Mask Layout

HI-674A/883 ANALOG DIE **HI-674A/883 DIGITAL DIE**



Packaging†

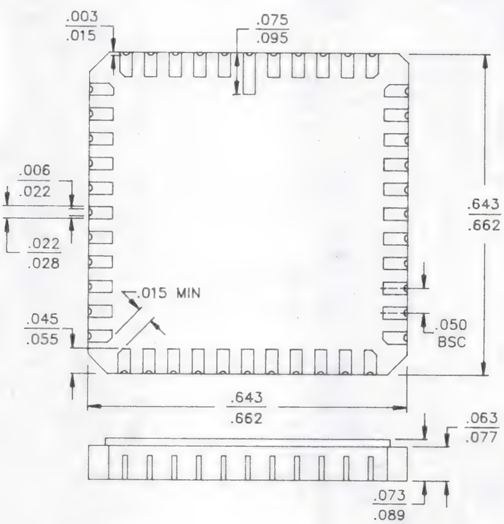
28 PIN CERAMIC DIP



LEAD MATERIAL: Type B
LEAD FINISH: Type C
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-10

44 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-5

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

HI-674A

DESIGN INFORMATION

Fast, Complete 12-Bit A/D Converter With Microprocessor Interface

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Definitions of Specifications

Linearity Error

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs ½LSB (1.22mV for 10 volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1½LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HI-674AT grade is guaranteed for maximum non-linearity of ±½LSB. This means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HI-674AS grade is guaranteed to ±1 LSB max error. An analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user-adjustable.

Differential Linearity Error (No Missing Codes)

A specification which guarantees no missing codes requires that every combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. The HI-674AT grade, guarantees no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HI-674AS grade guarantees no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11-bits must be present; in practice very few of the 12-bit codes are missing.

Unipolar Offset

The first transition should occur at a level ½LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

Bipolar Offset

Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value ½LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

Full Scale Calibration Error

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1½LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 7 and 8. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 volt reference.

Temperature Coefficients

The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{min} or T_{max}.

Power Supply Rejection

The standard specifications for the HI-674A assume use of +5.00 and ±15.00 or ±12.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

Code Width

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 Least Significant Bit (LSB) of the full scale range or 2.44mV out of 10 volts for a 12-bit ADC.

Quantization Uncertainty

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±½LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

Left-Justified Data

The data format used in the HI-674A is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$ This implies a binary point to the left of the MSB.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Applying the HI-674A*

*Pin numbers correspond to DIP package only.

For each application of this converter, the ground connections, power supply bypassing, analog signal source, digital timing and signal routing on the circuit board must be optimized to assure maximum performance. These areas are reviewed in the following sections, along with basic operating modes and calibration requirements.

PHYSICAL MOUNTING AND LAYOUT CONSIDERATIONS

Layout

Unwanted, parasitic circuit components, (L, R, and C) can make 12-bit accuracy impossible, even with a perfect A/D converter. The best policy is to eliminate or minimize these parasitics through proper circuit layout, rather than try to quantify their effects.

The recommended construction is a double-sided printed circuit board with a ground plane on the component side. Other techniques, such as wire-wrapping or point-to-point wiring on vectorboard, will have an unpredictable effect on accuracy.

In general, sensitive analog signals should be routed between ground traces and kept well away from digital lines. If analog and digital lines must cross, they should do so at right angles.

Power Supplies

Supply voltages to the HI-674A (+15V, -15V and +5V) must be "quiet" and well regulated. Voltage spikes on these lines can affect the converter's accuracy, causing several LSB's to flicker when a constant input is applied. Digital noise and spikes from a switching power supply are especially troublesome. If switching supplies must be used, outputs should be carefully filtered to assure "quiet" DC voltage at the converter terminals.

Further, a bypass capacitor pair on each supply voltage terminal is necessary to counter the effect of variations in supply current. Connect one pair from pin 1 to 15 (V_{LOGIC} supply), one from pin 7 to 9 (V_{CC} to Analog Common) and one from pin 11 to 9 (V_{EE} to Analog Common). For each capacitor pair, a 10μF tantalum type in parallel with a 0.1μF ceramic type is recommended.

Ground Connections

The typical HI-674A ground currents are 5.5mADC into pin 9 (Analog Common) and 7mADC out of pin 15 (Digital Common). These pins should be tied together at the package to guarantee specified performance for the converter. In addition, a wide PC trace should run directly from pin 9 to (usually) 15V common, and from pin 15 to (usually) the +5V Logic Common. If the converter is located some distance from the system's "single point" ground, make only these connections to pins 9 and 15: Tie them together at the package, and back to the system ground with a single path. This path should have low resistance since it will carry about 1.5mA of DC current. (Code dependent currents flow in the V_{CC}, V_{EE} and V_{LOGIC} terminals, but not through the HI-674A's Analog Common or Digital Common).

ANALOG SIGNAL SOURCE

The device driving the HI-674A analog input will see a nominal load of 5kΩ (10V range) or 10kΩ (20V range). However, the other end of these input resistors may change as much as ±400mV with each bit decision, creating abrupt changes in current at the analog input. Thus, the signal source must maintain its output voltage while furnishing these step changes in load current, which occur at 950ns intervals. This requires low output impedance and fast settling by the signal source.

The output impedance of an op amp, for example, has an open loop value which, in a closed loop, is divided by the loop gain available at a frequency of interest. The amplifier should have acceptable loop gain at 1MHz for use with the HI-674A. To check whether the output properties of a signal source are suitable, monitor the 674A's input (pin 13 or 14) with an oscilloscope while a conversion is in progress. Each of the twelve disturbances should subside in one half microsecond or less. (The comparator decision is made about 800ns after each code change from the SAR).

If the application calls for a Sample/Hold to precede the converter, it should be noted that not all Sample/Holds are compatible with the HI-674A in the manner described above. These will require an additional wideband buffer amplifier to lower their output impedance. A simpler solution is to use the Harris HA-5320 Sample/Hold, which was designed for use with the HI-674A.

RANGE CONNECTIONS AND CALIBRATION PROCEDURES

The HI-674A is a "complete" A/D converter, meaning it is fully operational with addition of the power supply voltages, a Start Convert signal, and a few external components as shown in figures 7 and 8. Nothing more is required for most applications.

Whether controlled by a processor or operating in the stand-alone mode, the HI-674A offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V and ±10V. The maximum errors for gain and offset are listed under Specifications. If required, however, these errors may be adjusted to zero as explained below. Power supply and ground connections have been discussed in an earlier section.

DESIGN INFORMATION (Continued)

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Unipolar Connections and Calibration

Refer to figure 7. The resistors shown* are for calibration of offset and gain. If this is not required, replace R2 with a 50Ω, 1% metal film resistor and remove the network on pin 12. Connect pin 12 to pin 9. Then, connect the analog signal to pin 13 for the 0V to 10V range, or to pin 14 for the 0V to 20V range. Inputs to +20V (5V over the power supply) are no problem — the converter operates normally.

Calibration consists of adjusting the converters's most negative output to its ideal value (offset adjustment), then, adjusting the most positive output to its ideal value (gain adjustment). To understand the procedure, note that in principle, one is setting the output with respect to the midpoint of an increment of analog input, as denoted by two adjacent code changes. Nominal value of an increment is one LSB. However, this approach is impractical because nothing "happens" at a midpoint to indicate that an adjustment is complete. Therefore, calibration is performed in terms of the observable code changes instead of the midpoint between code changes.

For example, midpoint of the first LSB increment should be positioned at the origin, with an output code of all 0's. To do this, apply an input of +½LSB (+1.22mV for the 10V range; +2.44mV for the 20V range). Adjust the Offset potentiometer R1 until the first code transition flickers between 0000 0000 0000 and 0000 0000 0001.

Next, perform a Gain Adjust at positive full scale. Again, the ideal input corresponding to the last code change is applied. This is 1½LSB's below the nominal full scale (+9.9963V for 10V range; +19.9927V for 20V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

Bipolar Connections and Calibration

Refer to Figure 8. The gain and offset errors listed under Specifications may be adjusted to zero using potentiometers R1 and R2*. If this isn't required, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

Connect the Analog signal to pin 13 for a ±5V range, or to pin 14 for a ±10V range. Calibration of offset and gain is similar to that for the unipolar ranges as discussed above. First apply a DC input voltage ½LSB above negative full scale (i.e., -4.9988V for the ±5V range, or -9.9976V for the ±10V range). Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1½LSB's below positive full scale (+4.9963V for ±5V range; +9.9927V for ±10V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

*The 100Ω potentiometer R2 provides Gain Adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (LSB equals 2.5mV) or 20.48V (LSB equals 5.0mV) is more convenient. For these, replace R2 by a 50Ω, 1% metal film resistor. Then, to provide Gain Adjust for the 10.24V range, add a 200Ω potentiometer in series with pin 13. For the 20.48V range, add a 500Ω potentiometer in series with pin 14.

Pin Numbers Refer To Sidebraze DIP Package.

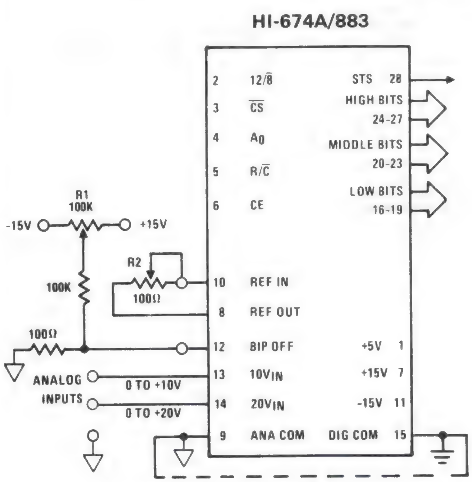


FIGURE 7. UNIPOLAR CONNECTIONS

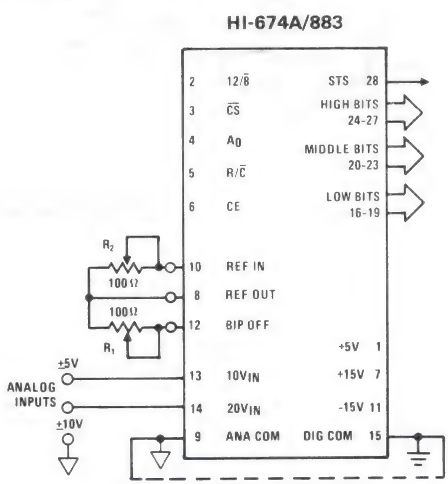


FIGURE 8. BIPOLAR INPUT CONNECTIONS

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Controlling the HI-674A

The HI-674A includes logic for direct interface to most microprocessor systems. The processor may take full control of each conversion, or the converter may operate in the "stand-alone" mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8 or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready — choosing either 12-bits at once or 8 followed by 4, in a left-justified format. The five control inputs are all TTL/CMOS- compatible: (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$ and CE). Chart B illustrates the use of these inputs in controlling the converter's operations. Also, a simplified diagram of the internal control logic is shown in Figure 9.

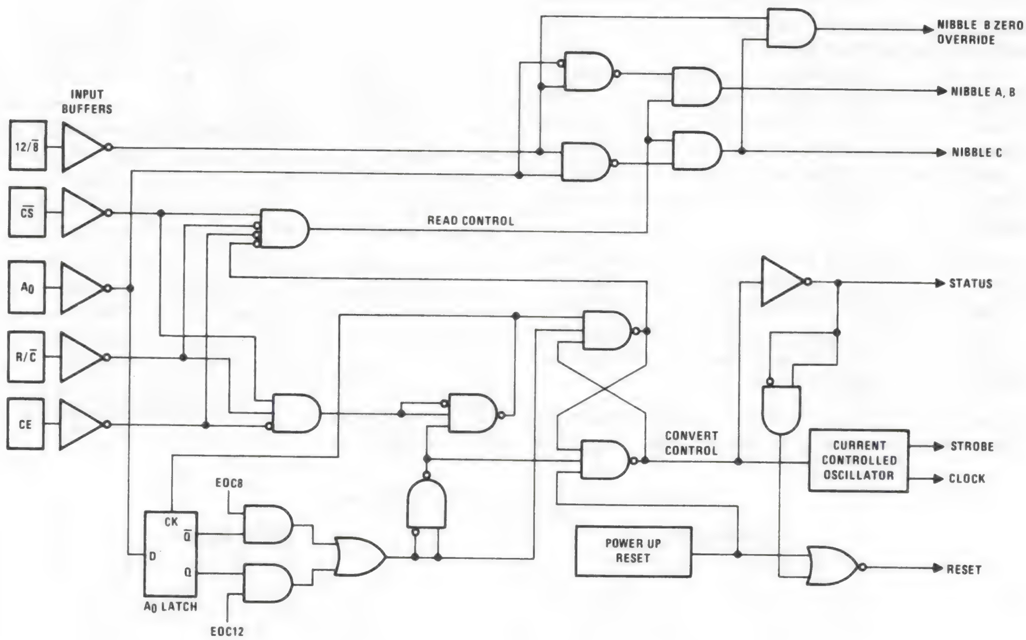


FIGURE 9. HI-674A CONTROL LOGIC

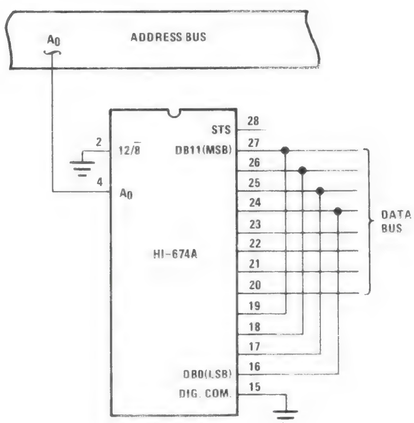
DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

HI-674A Timing Specifications +25°C Unless Otherwise Specified

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
CONVERT MODE					
t_{DSC}	STS Delay from CE	—	100	200	ns
t_{HEC}	CE Pulse Width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE Setup	50	—	—	ns
t_{HSC}	$\overline{CS}$ Low During CE High	50	20	—	ns
t_{SRC}	R/$\overline{C}$ to CE Setup	50	—	—	ns
t_{HRC}	R/$\overline{C}$ Low During CE High	50	20	—	ns
t_{SAC}	A_0 to CE Setup	0	0	—	ns
t_{HAC}	A_0 Valid During CE High	50	20	—	ns
t_c	Conversion Time, 12-bit Cycle T_{min} to T_{max}	9	12	15	μs
	8-bit Cycle T_{min} to T_{max}	6	8	10	μs
READ MODE					
t_{DD}	Access Time from CE	—	75	150	ns
t_{HD}	Data Valid after CE low	25	35	—	ns
t_{HL}	Output Float Delay	—	100	150	ns
t_{SSR}	$\overline{CS}$ to CE Setup	50	0	—	ns
t_{SRR}	R/$\overline{C}$ to CE Setup	0	0	—	ns
t_{SAR}	A_0 to CE Setup	50	25	—	ns
t_{HSR}	$\overline{CS}$ Valid after CE Low	0	0	—	ns
t_{HRR}	R/$\overline{C}$ High after CE Low	0	0	—	ns
t_{HAR}	A_0 Valid after CE Low	50	25	—	ns
t_{HS}	STS Delay after Data Valid	25	300	850	ns

NOTE: Time is measured from 50% level of digital transitions, tested with a 50pF and 3kΩ load. All possible combinations for setup times not listed, see Figure 9.



Pin Numbers Refer To Sidebraze DIP Package.

FIGURE 10. INTERFACE TO AN 8-BIT DATA BUS

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

HI-674A Capacitance Specifications

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
C_I	Logic Input Capacitance	—	5	—	pF
C_O	Logic Output Capacitance	—	5	—	pF

HARRIS

HI-774/883

Fast, Complete 12-Bit A/D Converter With Microprocessor Interface

January 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Complete 12-Bit A/D Converter with Reference and Clock
- Full 8-, 12-, or 16-Bit Microprocessor Bus Interface
- 250ns Bus Access Time (Max. Over Temp.)
- No Missing Codes Over Temperature
- Minimal Setup Time For Control Signals
- 11μMaximum Conversion Time
- Low Noise, Via Current-Mode Signal Transmission Between Chips
- Byte Enable/Short Cycle (A_0 Input)
  - ▶ Guarantees Break-Before-Make Action, Eliminating Bus Contention During Read Operation. Latched by the Start Convert Input (To Set the Conversion Length)
- ±12V to ±15V Operation
- 0 to +10V Unipolar and +/−5V Bipolar input ranges

Applications

- Military and Industrial Data Acquisition Systems
- Electronic Test And Scientific Instrumentation
- Process Control Systems

Description

The HI-774/883 is a complete 12-bit Analog-to-Digital Converter, including a +10V reference, clock, three-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice housed in a single package. The bipolar analog die features the Harris Dielectric Isolation process, which provides enhanced AC performance and freedom from latch-up.

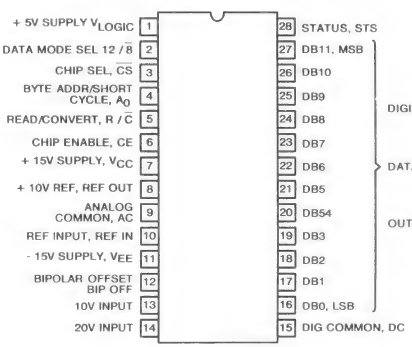
Custom design of each IC (bipolar analog and CMOS digital) has yielded improved performance over existing versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1 LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital ICs. Also, the clock oscillator is current-controlled for excellent stability over temperature. The oscillator is trimmed for a nominal conversion time of 9μs.

The HI-774/883 offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity, gain and offset accuracy. The buried zener reference circuit is trimmed for minimum temperature coefficient.

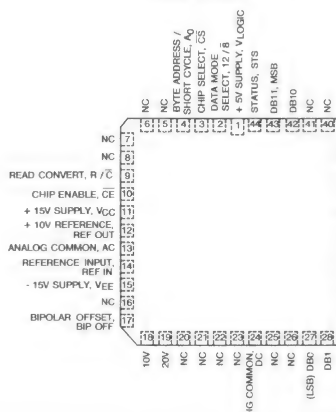
Power requirements are +5V and ±12V to ±15V, with typical dissipation of 385mW at ±12V. Two electrical grades are offered over the -55°C to +125°C temperature range. Both models are available in a 28 pin Sidebrazed DIP, or a 44 pad Ceramic LCC package.

Pinouts

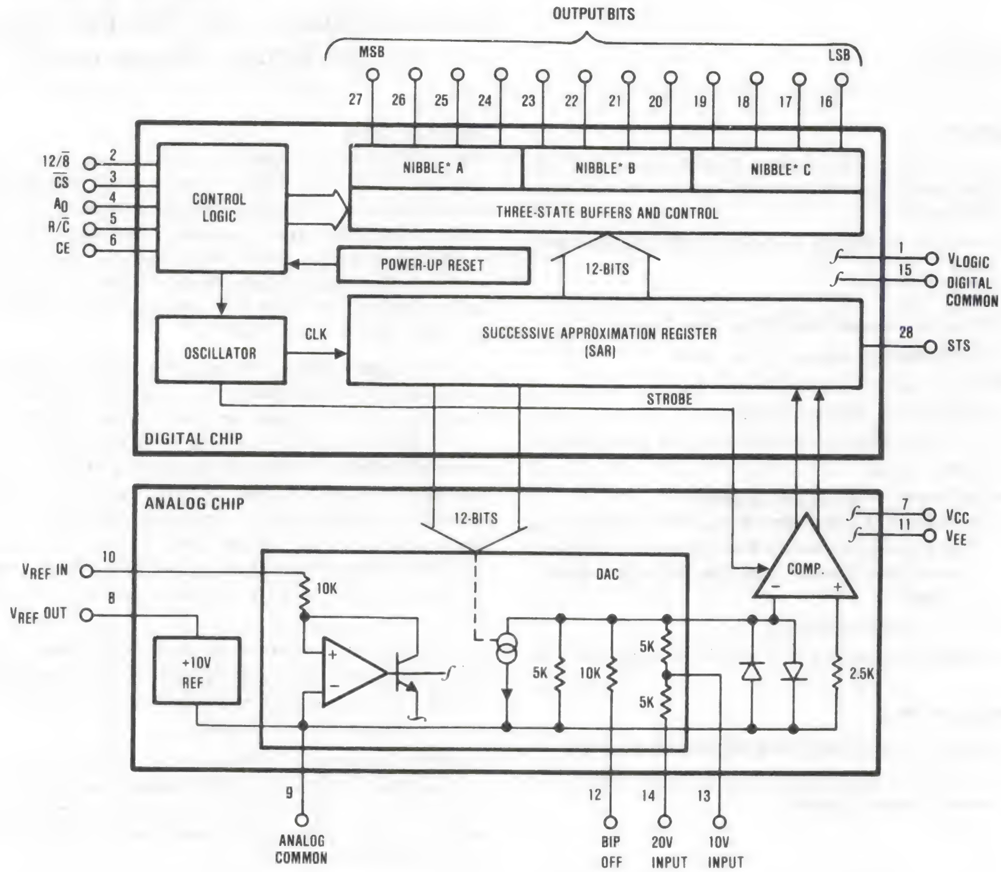
HI1-774/883 (SIDEBRAZED DIP)
TOP VIEW



HI4-774/883 (CERAMIC LCC)
TOP VIEW



Functional Diagram



*("NIBBLE" IS A 4-BIT DIGITAL WORD.)

Absolute Maximum Ratings

V_{CC} to Digital Ground . . . . 0 to +16.5V
V_{EE} to Digital Ground . . . . 0 to -16.5V
V_{LOGIC} to Digital Ground . . . . 0 to 7V
Analog Common to Digital Common . . . . ±1V
Control Inputs (CE, $\overline{CS}$, A0, 12/$\overline{8}$, R/$\overline{C}$) to
Digital Common. . . . . -0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$) to
Analog Common . . . . ±16.5V
20 V_{IN} to Analog Common . . . . ±24V
REF OUT . . . . Indefinite Short to Common
10ms Short to V_{CC}
Storage Temperature Range . . . . -65°C to +150°C
Lead Temperature (Soldering 10 Seconds) . . . . 275°C
Junction Temperature. . . . . +175°C

Thermal Information

Thermal Resistance, Junction-to-Case (θ_{jc})
Sidebrazed DIP Package . . . . 18°C/W
Ceramic LCC Package . . . . 16°C/W
Thermal Resistance, Junction-to-Ambient (θ_{ja})
Sidebrazed DIP Package . . . . 77°C/W
Ceramic LCC Package . . . . 71°C/W
Power Dissipation (at +75°C)
Sidebrazed DIP Package 1.29W
Ceramic LCC Package 1.41W
Power Dissipation Derating Factor (Above +75°C)
Sidebrazed DIP Package. . . . . 12.9mW/°C
Ceramic LCC Package . . . . 14.2mW/°C

Recommended Operating Conditions

Operating Temperature Range. . . . . -55°C +125°C
$+V_{SUPPLY}$ . . . . +15V
$-V_{SUPPLY}$ . . . . -15V
V_{LOGIC}. . . . . +5V
V_{REF} . . . . +10V

Analog Input Voltage, $10V_{IN}$ . . . . ±5V or 0 to +10V
Analog Input Voltage $20V_{IN}$. . . . . **Not Guaranteed***
Logic Level Low (V_{IL}) . . . . 0V to 0.8V
Logic Level High (V_{IH}). . . . . 2.0V to +5V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested At V_{CC} = +15V, V_{EE} = -15V, V_{LOG} = 5.0V, 10V Input Range Only, Unless Otherwise Specified.

(Note 1) DC PARAMETER	SYMBOL	(Figure 1,2 & Note 1, Chart A Apply Unless Otherwise Noted) CONDITIONS	GROUP A SUBGROUPS	TEMP	LIMITS HI-774S MIN	HI-774S MAX	HI-774T MIN	HI-774T MAX	UNITS
Power Supply Current From V_{CC}	I_{CC}	Output Code = 000000000000 and 111111111111 (Note 2)	1	+25°C		15		15	mA
			2, 3	+125°C, -55°C		16		15	mA
Power Supply Current From V_{EE}	I_{EE}	Output Code = 000000000000 and 111111111111 (Note 2)	1	+25°C		28		28	mA
			2, 3	+125°C, -55°C		32		30	mA
Power Supply Current From V_{LOGIC}	I_{LOG}	Output Code = 000000000000 and 111111111111 (Note 2)	1	+25°C		15		15	mA
			2, 3	+125°C, -55°C		17		17	mA
Power Dissipation	P_d	Calculated Worst Case of 2 Conditions (Note 3)	1	+25°C		720		720	mW
			2, 3	+125°C, -55°C		805		760	mW
Input Low Current	I_{IL}	V_{LOG} = 5.5V V_{IN}(LOGIC) = 0.0V	1	+25°C	-5	5	-5	5	μA
			2, 3	+125°C, -55°C	-5	5	-5	5	μA
Input High Current	I_{IH}	V_{LOG} = 5.5V V_{IN}(LOGIC) = 2.0V	1	+25°C	-5	5	-5	5	μA
			2, 3	+125°C, -55°C	-5	5	-5	5	μA
		V_{IN}(LOGIC) = 5.5V	1	+25°C	-5	5	-5	5	μA
			2, 3	+125°C, -55°C	-5	5	-5	5	μA
High Impedance State Output Current	I_{ZL}	V_{LOG} = 5.5V V_{IN} = 11.0V Min Output Code = 111111111111 Set R/$\overline{C}$ = Logic "0" Output Bits 1 thru 12 Measured Separately V_O = 0.0V all Bits (Note 2)	1	+25°C	-5	5	-5	5	μA
			2, 3	+125°C, -55°C	-5	5	-5	5	μA

* The 20V Input Range (Pin 14 DIP pkg, pin 19 LCC pkg) is functional but performance is not guaranteed for the HI-774/883. Tables 1,2,3 are guaranteed for only the 0V to +10V and +/−5V ranges (Pin 13 DIP, 18 LCC). The 20V input (pin 14 or 19) should be left open. The 20V input is tied to the 10V input through 5K Ohms and will effect circuit operation if connected to any potential.

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Devices Tested At V_{CC} = +15V, V_{EE} = -15V, V_{LOG} = 5.0V, 10V Input Range Only, Unless Otherwise Specified.

(Note 1) DC PARAMETER	SYMBOL	(Fig. 1,2 & Note 1 Apply Unless Otherwise Noted.) CONDITIONS	GROUP A SUBGROUPS	TEMP	LIMITS HI-774S MIN	LIMITS HI-774S MAX	LIMITS HI-774T MIN	LIMITS HI-774T MAX	UNITS
High Impedance State Output Current	I_{ZH}	V_{LOG} = 5.5V V_{IN} = -1.0V Max Output Code = 000000000000 Set R/$\overline{C}$ = Logic "0" Output Bits 1 thru 12 Measured Separately V_O = 5.5V All Bits (Note 2)	1	+25°C	-5	5	-5	5	μA
			2, 3	+125°C, -55°C	-5	5	-5	5	μA
Output Logic Voltage Levels	V_{OL}	V_{LOG} = 5.0V Output Code = 000000000000 Measure Output Bits 1 thru 12 & STS I_L = 1.6mA (Note 2)	1	+25°C	-0.5	0.5	-0.5	0.5	V
			2, 3	+125°C, -55°C	-0.5	0.5	-0.5	0.5	V
	V_{OH}	V_{LOG} = 4.5 Output Code = 111111111111 Measure Bits 1 thru 12 I_L = -0.5mA (Note 2)	1	+25°C	2.4	5.5	2.4	5.5	V
			2, 3	+125°C, -55°C	2.4	5.5	2.4	5.5	V
Reference Voltage	V_{REF}	Output Code = 000000000000 Bipolar, VFSR = 20V I_L = 2.0mA (Notes 2, 4)	1	+25°C	9.970	10.030	9.970	10.030	V
			2, 3	+125°C, -55°C	9.950	10.050	9.950	10.050	V
Power Supply Sensitivity To V_{CC}	$+PSS_1$	13.5V ≤ V_{CC} ≤ 16.5V Output Transition = 11111111111X-00000000000X (Note 5)	1	+25°C	-2	2	-1	1	LSB
			2, 3	+125°C, -55°C	-2.5	2.5	-1.5	1.5	LSB
	$+PSS_2$	11.4V ≤ V_{CC} ≤ 12.6V Output Transition = 11111111111X-00000000000X (Note 5)	1	+25°C	-2	2	-1	1	LSB
Power Supply Sensitivity To V_{LOG}	$+PSS_3$	4.5V ≤ V_{LOG} ≤ 5.5V Output Transition = 11111111111X-00000000000X (Note 5)	1	+25°C	-0.5	0.5	-0.5	0.5	LSB
			2, 3	+125°C, -55°C	-0.5	0.5	-0.5	0.5	LSB
Power Supply Sensitivity To V_{EE}	$-PSS_1$	-16.5 ≤ V_{EE} ≤ -13.5V Output Transition = 11111111111X-00000000000X (Note 5)	1	+25°C	-2	2	-1	1	LSB
			2, 3	+125°C, -55°C	-2.5	2.5	-2	2	LSB
	$-PSS_2$	-12.6V ≤ V_{EE} ≤ -11.4V Output Transition = 11111111111X-00000000000X (Note 5)	1	+25°C	-2	2	-1	1	LSB
Unipolar Offset Voltage	V_{IO}	Output Transition = 00000000000X (Note 5)	1	+25°C	-2	2	-2	2	LSB
			2, 3	+125°C, -55°C	-4	4	-3	3	LSB
Bipolar Zero	BZ	Output Transition = XXXXXXXXXXXX Bipolar, VFSR = 20V (Note 5)	1	+25°C	-10	10	-4	4	LSB
			2, 3	+125°C, -55°C	-14	14	-6	6	LSB

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Devices Tested At V_{CC} = +15V, V_{EE} = -15V, V_{LOG} = 5.0V, 10V Input Range Only, Unless Otherwise Specified.

(Note 1) DC PARAMETER	SYMBOL	(Figure 1,2 & Note 1, Apply Unless Otherwise Noted) CONDITIONS	GROUP A SUBGROUPS	TEMP	LIMITS HI-774S MIN	LIMITS HI-774S MAX	LIMITS HI-774T MIN	LIMITS HI-774T MAX	UNITS
Gain Error	A_E	Output Transition = 00000000000X to 11111111111X (Note 5)	1	+25°C	-0.3	0.3	-0.3	0.3	% of FSR
			2, 3	+125°C, -55°C	-0.8	0.8	-0.55	0.55	
	BPA_E	Bipolar, VFSR = 20V (Note 5)	1	+25°C	-0.3	0.3	-0.3	0.3	% of
			2, 3	+125°C, -55°C	-0.8	0.8	-0.55	0.55	FSR
Integral Linearity Error	L_E	Abbreviated Test (Note 5)	1	+25°C	-1	1	-1/2	1/2	LSB
			2, 3	+125°C, -55°C	-1	1	-1	1	LSB
Differential Linearity Error	DL_E	Abbreviated Test (Note 5)	1	+25°C	-2	2	-1	1	LSB
			2, 3	+125°C, -55°C	-2	2	-1	1	LSB
Input Resistance	R_i10V	10V Span Input (Note 11)	1	+25°C	3.75	6.25	3.75	6.25	KΩ
			2, 3	+125°C, -55°C	3	7	3	7	KΩ
	R_i20V	20V Span Input (Note 11)	1	+25°C	7.50	12.50	7.50	12.50	KΩ
			2, 3	+125°C, -55°C	6	14	6	14	KΩ
Unipolar Offset Voltage Drift	$\frac{dV_{IO}}{dT}$	Output Transition = 00000000000X (Note 5)	2, 3	+125°C, -55°C	-2	2	-1	1	LSB
Bipolar Zero Drift	$\frac{dB_Z}{dT}$	Output Transition = XXXXXXXXXXXX Bipolar, VFSR = 20V (Note 5)	2, 3	+125°C, -55°C	-4	4	-2	2	LSB
Gain Error Drift	$\frac{dA_E}{dT}$	Output Transition = 00000000000X to 11111111111X (Note 5)	2, 3	+125°C, -55°C	-20	20	-10	10	LSB
	$\frac{dBPA_E}{dT}$	Bipolar, VFSR = 20V (Note 5)	2, 3	+125°C, -55°C	-20	20	-10	10	LSB

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested At $V_{CC} = +15V$, $V_{EE} = -15V$, $V_{LOG} = 5.0V$, 10V Input Range Only, Unless Otherwise Specified.

(Note 1) AC PARAMETER	SYMBOL	(Figure 1,2 & Note 1 Apply Unless Otherwise Noted) CONDITIONS	GROUP A SUBGROUPS	TEMP	LIMITS HI-774S MIN		HI-774T MIN		UNITS
					MIN	MAX	MIN	MAX	
Conversion Time	t_C	V_{IN} = -1V Max Output Code = 000000000000 8 Bit Cycle (Note 5)	9	+25°C		8.5		8.5	μs
			10, 11	+125°C, -55°C		8.5		8.5	μs
		V_{IN} = 11V Max Output Code = 111111111111 12 Bit Cycle (Note 5)	9	+25°C		11		11	μs
			10, 11	+125°C, -55°C		11		11	μs

TABLE 3.ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Characterized At $V_{CC} = +15V$, $V_{EE} = -15V$, $V_{LOG} = 5.0V$, 10V Input Range Only, Unless Otherwise Specified. Load is 3kΩ, 50pF where applicable. Figure 3, 4, 5, & 6 applies Unless Otherwise Noted.

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMP	HI-774S/883 HI-774T/883 MIN	MAX	UNITS
STS Delay From R/$\overline{C}$	t_{DS}	Low to High Transition Referenced to High to Low R/$\overline{C}$ Transition. Output Code = 000000000000	1, 5, 10	+25°C		200	ns
				+125°C, -55°C		600	ns
Low R/$\overline{C}$ Pulse Width	t_{HRL}	Minimum R/$\overline{C}$ Pulse Width Required to Start a Conversion	1, 10	+25°C	50		ns
				+125°C, -55°C	350		ns
Data Valid After R/$\overline{C}$ Low	t_{HDR}	Output Data Valid, Referenced to High to Low R/$\overline{C}$ Transition Output Code = 000000000000 & 111111111111	1, 2, 10	+25°C	25		ns
				+125°C, -55°C	15		ns
STS Delay After Data Valid	t_{HS}	STS High to Low Transition Referenced to Valid Output Data Output Code = 000000000000 & 111111111111	1, 2, 10	+25°C		300	ns
High R/$\overline{C}$ Pulse Width	t_{HRH}	Minimum R/$\overline{C}$ Pulse Width Required to Enable Output Bits Output Code = 000000000000 & 111111111111	1, 2, 10	+25°C	150		ns
				+125°C, -55°C	300		ns
Data Access Time	t_{DDR}	Output Data Valid, Referenced to Low to High R/$\overline{C}$ Transition Output Code = 000000000000 & 111111111111	1, 2, 10	+25°C		150	ns
				+125°C, -55°C		250	ns
STS Delay From CE	t_{DSC}	Low to High Transition, Referenced to Low to High CE Transition Output Code = 000000000000	1, 2, 10	+25°C		200	ns
				+125°C, -55°C		350	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Devices Characterized At V_{CC} = +15V, V_{EE} = -15V, V_{LOG} = 5.0V, 10V Input Range Only, Unless Otherwise Specified. Load is 3kΩ, 50pF where applicable. Figure 3, 4, 5, & 6 applies Unless Otherwise Noted.

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMP	HI-774S/883 HI-774T/883 MIN	MAX	UNITS
CE Pulse Width	t_{HEC}	Minimum CE Pulse Width Required to Start a Conversion	1, 10	+25°C	50		ns
				+125°C, -55°C	300		ns
$\overline{CS}$ to CE Setup	t_{SSC}	Minimum Time Required From a High to Low $\overline{CS}$ Transition to Low to High CE Transition for a Conversion to Start from CE	1, 10	+25°C	50		ns
$\overline{CS}$ Low During CE High	t_{HSC}	Minimum Time Required From a Low to High CE Transition to Low to High $\overline{CS}$ Transition for a Conversion to Start	1, 10	+25°C	50		ns
R/$\overline{C}$ To CE Set-Up	t_{SRC}	Minimum Time Required From a High to Low R/$\overline{C}$ Transition to Low to High CE Transition for a Conversion to Start from CE.	1, 10	+25°C	50		ns
R/$\overline{C}$ Low During CE High	t_{HRC}	Minimum Time Required From a Low to High CE Transition to Low to High R/$\overline{C}$ Transition for a Conversion to Start	1, 10	+25°C	50		ns
A_0 To CE Set-Up	t_{SAC}	Minimum Time Required From a Low to High or High to Low A0 Transition to Low to High CE Transition to Initiate an 8-bit or 12-bit Conversion, Respectively.	1, 10	+25°C	0		ns
A_0 Valid During CE High	t_{HAC}	Minimum Time Required From a Low to High CE Transition to Low to High or High to Low to Low A_0 Transition to Guarantee a 12-bit or 8-bit Conversion, Respectively.	1, 10	+25°C	50		ns
Access Time From CE	t_{DD}	Output Data Valid, Referenced to Low to High CE Transition Output Code = 000000000000 & 111111111111	1, 2, 10	+25°C		150	ns
				+125°C, -55°C		250	ns
Data Valid After CE Low	t_{HD}	Output Data Valid, Referenced to High to Low CE Transition Output Code = 000000000000 & 111111111111	1, 2, 10	+25°C	25		ns
				+125°C, -55°C	15		ns

6 DATA CONVERSION PRODUCTS

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Devices Characterized At V_{CC} = +15V, V_{EE} = -15V, V_{LOG} = 5.0V, 10V Input Range Only, Unless Otherwise Specified. Load is 3kΩ, 50pF where applicable. Figure 3, 4, 5, & 6 applies Unless Otherwise Noted.

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMP	HI-774S/883 HI-774T/883 MIN	MAX	UNITS
Output Float Delay	t_{HL}	Output Delay to HI-Z, Referenced to High to Low CE Transition Output Code = 000000000000 & 111111111111	1, 2, 10	+25°C, +125°C, -55°C		150	ns
$\overline{CS}$ To CE Setup	t_{SSR}	Minimum Time from $\overline{CS}$ High to Low Transition to CE Low to High Transition to Guarantee Data Valid is Controlled by CE. Output Code = 000000000000 & 111111111111	1, 2, 10	+25°C	50		ns
R/$\overline{C}$ to CE Set-Up	t_{SRR}	Minimum Time from R/$\overline{C}$ Low to High Transition To CE Low to High Transition to Guarantee Data Valid is Controlled by CE. Output Code = 000000000000 & 111111111111	1, 2, 10	+25°C	0		ns
A_0 To CE Set-Up	t_{SAR}	Minimum Time From A_0 High to Low or Low to High Transition to CE Low to High Transition to guarantee the correct byte gets enabled.	1, 10	+25°C	50		ns
$\overline{CS}$ Valid After CE Low	t_{HSR}	Minimum Time from CE High to Low Transition to $\overline{CS}$ Low to High Transition to Guarantee High Impedance State is Controlled by CE.	1, 10	+25°C	0		ns
R/$\overline{C}$ High After CE Low	t_{HRR}	Minimum Time from CE High to Low Transition to R/$\overline{C}$ High to Low Transition to Guarantee Device Will Disable Before Another Conversion is Initiated.	1, 10	+25°C	0		ns
A_0 Valid After CE Low	t_{HAR}	Minimum Time From CE High to Low Transition to A_0 High to Low or Low to High Transition to Guarantee Enabled Byte Does Not Change Until Device Is Disabled	1, 10	+25°C	50		ns

TABLE 4. ELECTRICAL TEST REQUIREMENTS

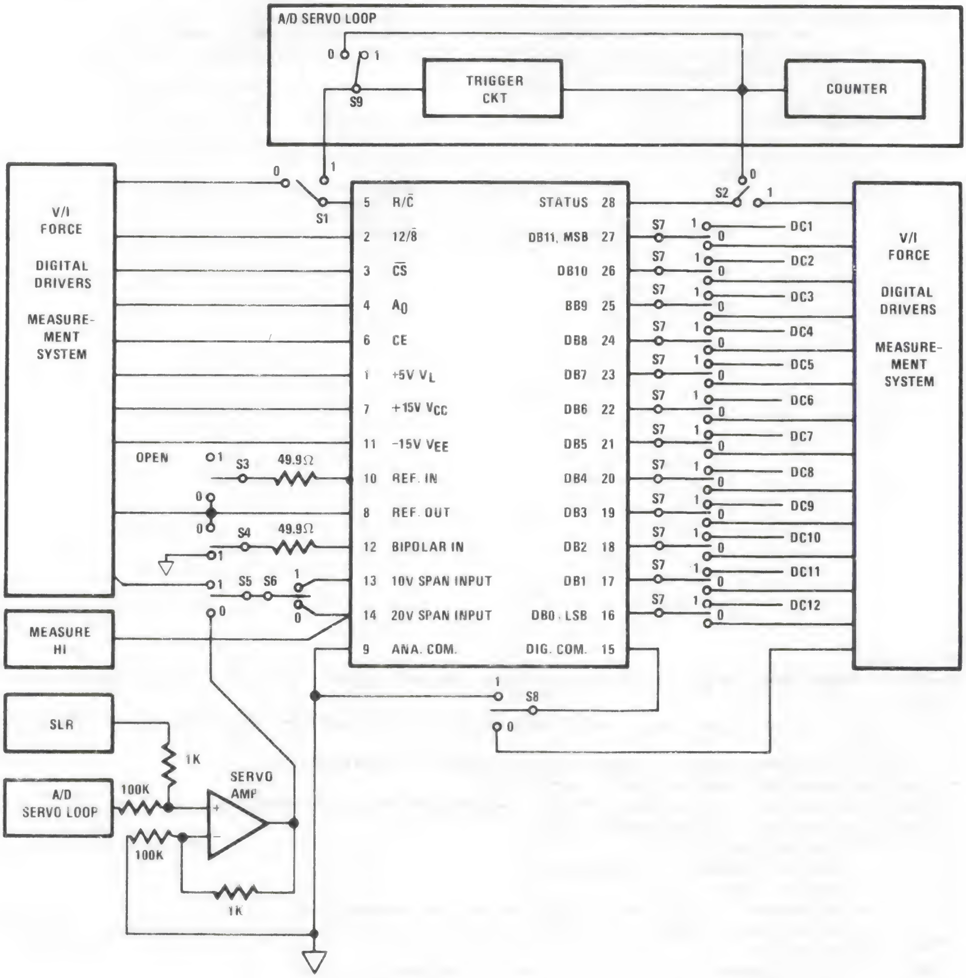
MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

*PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

NOTES:

1. See definitions.
2. A output code of 0000 0000 0000 is guaranteed by an input voltage $V_{IN} = -1V$ and an output code of 1111 1111 1111 is guaranteed by an input voltage $V_{IN} = 11V$.
3. $P_d = (V_{CC} * I_{CC} + V_{EE} * I_{EE} + V_{LOGIC} * I_{LOGIC})$ Power dissipation shall be calculated using the two output code conditions 0000 0000 0000 and 1111 1111 1111.
4. The reference voltage external load current shall be constant direct current and shall not exceed 2mA.
5. X represents the transition point between two adjacent code-words
   (ie: 0000 0000 000X represents the transition between code-words 0000 0000 0000 and 0000 0000 0001,
   XXXX XXXX XXXX represents the transition between code-words
   0111 1111 1111 and 1000 0000 0000 and
   1111 1111 111X represents the transition between code-words
   1111 1111 1110 and 1111 1111 1111).
6. Implies a falling edge transition from 2.0V to 0.8V, after remaining input pins are set.
7. Implies a falling edge transition from 2.0V to 0.8V, after remaining input pins are set, then, after a minimum of 200ns, a rising edge transition to 2.0V.
8. Implies a rising edge transition from 0.8V to 2.0V after remaining input pins are set.
9. R/$\overline{C}$ Implies a falling edge from 2.0V to a TTL Low, approximately 0.0V.
10. The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are charac terized upon initial design release and upon design changes which would affect these characteristics.
11. A conversion must be performed at the inputted voltage prior to Ri10V and Ri20V measurements.

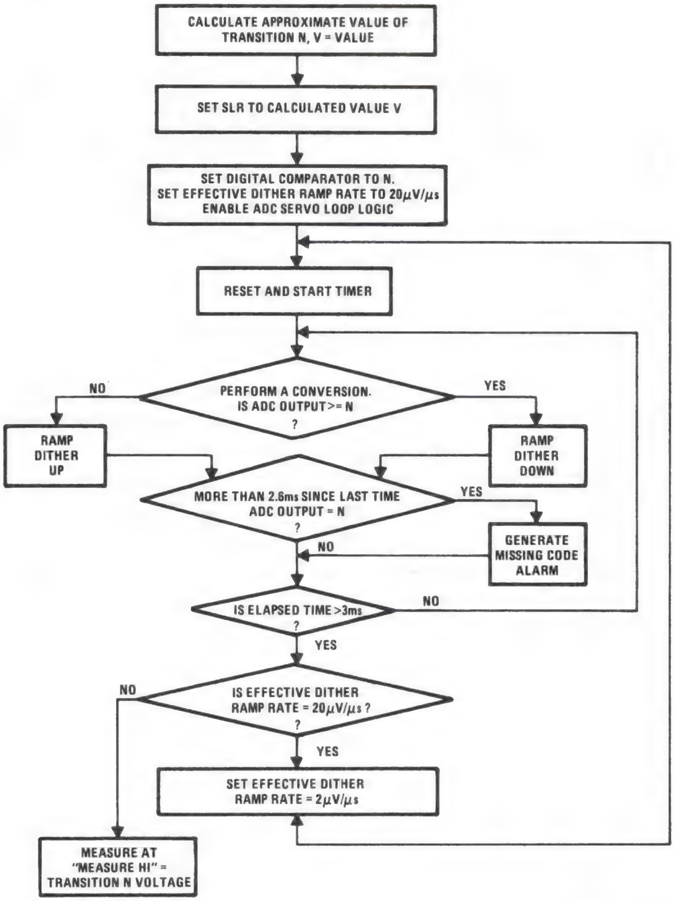
Test Circuit and Test Conditions



NOTES:
1. The connections of the V/I force, digital drivers, and measurement system are software controlled.
2. DC1 → DC12 are input bits of the digital comparator in the A/D servo loop.
3. SLR = > super linear reference.
4. The 20V Analog Input is used in some tests, where applicable, to facilitate automatic test.

FIGURE 1. TEST CIRCUIT

Test Circuit and Test Conditions (Continued)



NOTES:

1. SLR = Super Linear Reference.
2. See Figure 1 for Test Circuit.

FIGURE 2. TEST FLOW FOR ANALOG TO DIGITAL SERVO LOOP

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DATA CONVERSION PRODUCTS

CHART A. GROUP A TEST CONDITIONS

SYMBOL	APPLIED VOLTAGES REF. ANALOG COMMON (FIG. 1, NOTE 1)									APPLIED DIGITAL CODEWORD	DUT DIGITAL OUTPUT CODEWORD	SWITCH POSITIONS	MEASUREMENT SENSE LINES REF. ANA. COMMON			TEMP °C	EQUATIONS & NOTES
	7	11	1	13/14	2	3	4	5	6								
	V_{CC} (V)	V_{EE} (V)	V_{LOG} (V)	V_{IN} (V)	$12/\overline{8}$ (V)	$\overline{CS}$ (V)	A_0 (V)	$R/\overline{C}$ (V)	CE (V)	$DC_1 \longleftrightarrow DC_{12}$ MSB ⟷ LSB	$27 \longleftrightarrow 16$ MSB ⟷ LSB	$S_1 \longleftrightarrow S_9$	PIN	VALUE	UNIT		
I_{CC1} I_{CC2}	+15 +15	-15 -15	+5.0 +5	-1 11	2.0 2.0	0.8 0.8	0.8 0.8		2.0 2.0		000000000000 111111111111	010111011 010111011	7 7	I_1 I_2	mA mA	+25. +125.-55	$I_{CC1} = I_1$ $I_{CC2} = I_2$
I_{EE1} I_{EE2}	+15 +15	-15 -15	+5 +5	-1 11	2.0 2.0	0.8 0.8	0.8 0.8		2.0 2.0		000000000000 111111111111	010111011 01011011	11 11	I_3 I_4	mA mA	+25. +125. -55	$I_{EE1} = I_3$ $I_{EE2} = I_4$
I_{LOG1} I_{LOG2}	+15 +15	-15 -15	+5 +5	-1 11	2.0 2.0	0.8 0.8	0.8 0.8		2.0 2.0		000000000000 111111111111	010111011 010111011	1 1	I_5 I_6	mA mA	+25. +125.	$I_{LOG1} = I_5$ $I_{LOG2} = I_6$
P_{D1} P_{D2}	+15 +15	-15 -15	+5 +5	-1 11							000000000000 111111111111					+25. +125. -55	$P_{D1} = (I_{CC1})(V_{CC})$ $+ (I_{EE1})(V_{EE}) +$ $(I_{LOG1})(V_{LOG})$ $P_{D2} = (I_{CC2})(V_{CC})$ $+ (I_{EE2})(V_{EE}) +$ $(I_{LOG2})(V_{LOG})$
I_{IL1} thru I_{IL5}	+15	-15	+5.5	-1	0	0	0	0	0			010111011	2 thru 6	I_7 thru I_{11}	μA	+25. +125. -55	I_{IL1} thru I_{IL5} = I_7 thru I_{11} Respectively
I_{IH1} thru I_{IH5}	+15	-15	+5.5	11	2.0	2.0	2.0	2.0	2.0			010111011	2 thru 6	I_{12} thru I_{16}	μA	+25. +125. -55	I_{IH1} thru I_{IH5} = I_{12} thru I_{16} Respectively
I_{IH6} thru I_{IH10}	+15	-15	+5.5	11	5.5	5.5	5.5	5.5	5.5			010111011	2 thru 6	I_{17} thru I_{21}	μA	+25. +125. -55	I_{IH6} thru I_{IH10} = I_{17} thru I_{21} Respectively
I_{ZL1} thru I_{ZH12}	+15	-15	+5.5	11	2.0	0.8	0.8		2.0		000000000000	010111011	16 thru 27	I_{22} thru I_{33}	μA	+25. +125. -55	I_{ZL1} thru I_{ZL12} = I_{22} thru I_{33} Respectively. $V_O = 0.0V$ (Note 9)
I_{ZH1} thru I_{ZH12}	+15	-15	+5.5	-1	2.0	0.8	0.8		2.0		111111111111	010111011	16 thru 27	I_{34} thru I_{45}	μA	+25. +125. -55	I_{ZH1} thru I_{ZH12} = I_{34} thru I_{45} Respectively. $V_O = 5.5V$ (Note 9)
V_{OL1} thru V_{OL13}	+15	-15	+4.5	-1	2.0	0.8	0.8		2.0		000000000000	010111011	16 thru 28	E_1 thru E_{13}	V	+25. +125. -55	V_{OL1} thru V_{OL13} = E_1 thru E_{13} Respectively. $I_L = 1.6mA$
V_{OH1} thru V_{OH12}	+15	-15	+4.5	11	2.0	0.8	0.8		2.0		111111111111	010111011	16 thru 27	E_{14} thru E_{25}	V	+25. +125. -55	V_{OH1} thru V_{OH12} = E_{14} thru E_{25} Respectively. $I_L = -0.5mA$

See Notes at End of Table 4.

CHART A. GROUP A TEST CONDITIONS (Continued)

	APPLIED VOLTAGES REF. ANALOG COMMON (FIG. 1, NOTE 1)									APPLIED DIGITAL CODEWORD	DUT DIGITAL OUTPUT CODEWORD	SWITCH POSITIONS	MEASUREMENT SENSE LINES REF. ANA. COMMON				
	7	11	1	13/14	2	3	4	5	6								
SYMBOL	V_{CC} (V)	V_{EE} (V)	V_{LOG} (V)	V_{IN} (V)	$12/\overline{8}$ (V)	$\overline{CS}$ (V)	A_0 (V)	$R/\overline{C}$ (V)	CE (V)	$DC_1 \leftrightarrow DC_{12}$ MSB ↔ LSB	27 ↔ 16 MSB ↔ LSB	$S_1 \leftrightarrow S_9$	PIN	VALUE	UNIT	TEMP °C	EQUATIONS & NOTES
V_{REF1}	+15	-15	+5	-1	2.0	0.8	0.8		2.0		000000000000	011111011	8	E_{26}	V	+25, +125, -55	$V_{REF1} = E_{27}$ $I_L = 0mA$
V_{REF2}	+15	-15	+5	-11	2.0	0.8	0.8		2.0		00000000000	010011011	8	E_{27}	V		$V_{REF2} = E_{28}$, $I_L = 2.0mA$ Bipolar, $V_{FSR} = 20V$
$+P_{SS1}$	13.5 13.5 16.5 16.5	-15 -15 -15 -15	5.0 5.0 5.0 5.0	SERV LOOP	2.0	0.8	0.8	TRIG CKT.	2.0	000000000000 111111111110 000000000000 111111111110	00000000000X 11111111111X 00000000000X 11111111111X	100101111	14	E_{200} E_{201} E_{202} E_{203}	V V V V	+25, +125, -55	$+P_{SS1} = [(E_{203} - E_{202}) - (E_{201} - E_{200})]/[(E_{42X} - E_{41X})/4094]$ Where X = R for +25°C = H for 125°C = L for -55°C
$+P_{SS2}$	11.4 11.4 12.6 12.6	-15 -15 -15 -15	5.0 5.0 5.0 5.0	SERV LOOP	2.0	0.8	0.8	TRIG CKT.	2.0	000000000000 111111111110 000000000000 111111111110	00000000000X 11111111111X 00000000000X 11111111111X	100101111	14	E_{204} E_{205} E_{206} E_{207}	V V V V	+25, +125, -55	$+P_{SS2} = [(E_{207} - E_{206}) - (E_{205} - E_{204})]/[(E_{42X} - E_{41X})/4094]$ Where X = R for +25°C = H for 125°C = L for -55°C
$+P_{SS3}$	+15 +15 +15 +15	-15 -15 -15 -15	4.5 4.5 5.5 5.5	SERV LOOP	2.0	0.8	0.8	TRIG CKT.	2.0	000000000000 111111111110 000000000000 111111111110	00000000000X 11111111111X 00000000000X 11111111111X	100101111	14	E_{208} E_{209} E_{210} E_{211}	V V V V	+25, +125, -55	$+P_{SS3} = [(E_{211} - E_{210}) - (E_{209} - E_{208})]/[(E_{42X} - E_{41X})/4094]$ Where X = R for +25°C = H for 125°C = L for -55°C
$-P_{SS1}$	+15 +15 +15 +15	-13.5 -13.5 -16.5 -16.5	5.0 5.0 5.0 5.0	SERV LOOP	2.0	0.8	0.8	TRIG CKT.	2.0	000000000000 111111111110 000000000000 111111111110	00000000000X 11111111111X 00000000000X 11111111111X	100101111	14	E_{212} E_{213} E_{214} E_{215}	V V V V	+25, +125, -55	$-P_{SS1} = [(E_{215} - E_{214}) - (E_{213} - E_{212})]/[(E_{42X} - E_{41X})/4094]$ Where X = R for +25°C = H for 125°C = L for -55°C
$-P_{SS2}$	+15 +15 +15 +15	-11.4 -11.4 -12.6 -12.6	5.0 5.0 5.0 5.0	SERV LOOP	2.0	0.8	0.8	TRIG CKT.	2.0	000000000000 111111111110 000000000000 111111111110	00000000000X 11111111111X 00000000000X 11111111111X	100101111	14	E_{216} E_{217} E_{218} E_{219}	V V V V	+25°C +125, -55	$-P_{SS2} = [(E_{219} - E_{218}) - (E_{217} - E_{216})]/[(E_{42X} - E_{41X})/4094]$ Where X = R for +25°C = H for 125°C = L for -55°C

CHART A. GROUP A TEST CONDITIONS (Continued)

SYMBOL	APPLIED VOLTAGES REF. ANALOG COMMON (FIG. 1, NOTE 1) 7 V_{CC} (V)	11 V_{EE} (V)	1 V_{LOG} (V)	13/14 V_{IN} (V)	2 $12/\overline{8}$ (V)	3 $\overline{CS}$ (V)	4 A_0 (V)	5 $R/\overline{C}$ (V)	6 CE (V)	APPLIED DIGITAL CODEWORD $DC_1 \longleftrightarrow DC_{12}$ MSB ⟷ LSB	DUT DIGITAL OUTPUT CODEWORD 27 ⟷ 16 MSB ⟷ LSB	SWITCH POSITIONS $S_1 \longleftrightarrow S_9$	MEASUREMENT SENSE LINES REF. ANA. COMMON PIN	VALUE	UNIT	TEMP °C	EQUATIONS & NOTES
V_{IOR}	+15	-15	+5	SERV LOOP	2.0	0.8	0.8	TRIG CKT.	2.0	000000000000	00000000000X	100101111	14	E_{38R}	V	+25	V_{IOR} = ((E38R)-(0.5 AR / 4095))/(AR / 4095)
V_{IOH}	+15	-15	+5		2.0	0.8	0.8		2.0	000000000000	00000000000X	100101111	14	E_{38H}	V	+125	V_{IOH} => Same as V_{IOR} with R = H
V_{IOL}	+15	-15	+5		2.0	0.8	0.8		2.0	000000000000	00000000000X	100101111	14	E_{38L}	V	-55	V_{IOL} => Same as V_{IOR} with R = L
B_{ZR}	+15	-15	+5	SERV LOOP	2.0 2.0	0.8 0.8	0.8 0.8	TRIG CKT.	2.0 2.0	011111111111 100000000000	XXXXXXXXXXXX 10000000000X	100000111	14 14	E_{39R} E_{40R}	V V	+25	B_{ZR} = ((E_{39R} + E_{40R})/2)/(B_{AR} /4095)
B_{ZH}	+15	-15	+5		2.0 2.0	0.8 0.8	0.8 0.8		2.0 2.0	011111111111 100000000000	XXXXXXXXXXX 10000000000X	100000111	14 14	E39H E_{40H}	V V	+125	B_{ZH} => Same as B_{ZR} with R = H
B_{ZL}	+15	-15	+5		2.0 2.0	0.8 0.8	0.8 0.8		2.0 2.0	011111111111 100000000000	XXXXXXXXXXXX 10000000000X	100000111	14 14	E_{39L} E_{40L}	V V	-55	B_{ZL} => Same as B_{ZR} with R = L
A_{ER}	+15	-15	+5	SERV LOOP	2.0 2.0	0.8 0.8	0.8 0.8	TRIG CKT.	2.0 2.0	000000000000 111111111110	00000000000X 11111111111X	100101111	14 14	E_{41R} E_{42R}	V V	+25	A_R = (E_{42R} - E_{41R}) [(E_{42R} - E_{41R})/4094]
																+25	A_{ER} = [(A_R - 9.99756V)/10V]100
A_{EH}	+15	-15	+5		2.0 2.0	0.8 0.8	0.8 0.8		2.0 2.0	000000000000 111111111110	00000000000X 11111111111X	100101111	14 14	E_{41H} E_{42H}	V V	+125	A_{EH} => Same as A_{ER} with R = H
A_{EL}	+15	-15	+5		2.0 2.0	0.8 0.8	0.8 0.8		2.0 2.0	000000000000 111111111110	000000000000X 11111111111X	100101111	14 14	E_{41L} E_{42L}	V V	-55	A_{EL} => Same as A_{ER} with R = L
BA_{ER}	+15	-15	+5	SERV LOOP	2.0 2.0	0.8 0.8	0.8 0.8	TRIG CKT.	2.0 2.0	000000000000 111111111110	00000000000X 11111111111X	100000111	14 14	E_{43R} E_{44R}	V V	+25	BA_R = (E_{44R} - E_{43R}) + [(E_{44R} - E_{42R})/4094]
																+25	BA_{ER} = [(BA_R - 19.99512V)/ 20V]100
BA_{EH}	+15	-15	+5		2.0 2.0	0.8 0.8	0.8 0.8		2.0 2.0	000000000000 111111111110	00000000000X 11111111111X	100000111	14 14	E_{43H} E_{44H}	V V	+125	BA_{EH} => Same as BA_{ER} with R = H
BA_{EL}	+15	-15	+5		2.0 2.0	0.8 0.8	0.8 0.8		2.0 2.0	000000000000 111111111110	00000000000X 11111111111X	100000111	14 14	E_{43L} E_{44L}	V V	-55	BA_{EL} => Same as BA_{ER} with R = L

CHART A. GROUP A TEST CONDITIONS

	APPLIED VOLTAGES REF. ANALOG COMMON (FIG. 1, NOTE 1)									APPLIED DIGITAL CODEWORD	DUT DIGITAL OUTPUT CODEWORD	SWITCH POSITIONS	MEASUREMENT SENSE LINES REF. ANA. COMMON				
	7	11	1	13/14	2	3	4	5	6								
SYMBOL	V_{CC} (V)	V_{EE} (V)	V_{LOG} (V)	V_{IN} (V)	$12/\overline{8}$ (V)	$\overline{CS}$ (V)	A_0 (V)	$R/\overline{C}$ (V)	CE (V)	$DC_1 \longleftrightarrow DC_{12}$ MSB ⟷ LSB	27 ⟷ 16 MSB ⟷ LSB	$S_1 \longleftrightarrow S_9$	PIN	VALUE	UNIT	TEMP °C	EQUATIONS & NOTES
																+25, +125, -55	For Endpoint Linearity Error $L_E(N) = ((E(N+45) + E(N+46))/2) - V(IDEAL)/S$ $V(IDEAL) = (N1)(S) + E_{46} - S/2$ N1 = Applied Code Word $S = (E_{45}-E_{46})/4094$
	+15	-15	+5	SERV LOOP	2.0	0.8	0.8	TRIG CKT.	2.0	111111111110	11111111111X	100101111	14	E_{45}	V		
										000000000000	00000000000X			E_{46}			
L_{E1}										000000000001	0000000000XX			E_{47}			L_{E1} With N1 = 1
L_{E2}										000000000010	00000000001X			E_{48}			L_{E2} With N1 = 2
										000000000011	000000000XXX			E_{49}			
L_{E4}										000000000100	00000000010X			E_{50}			L_{E4} With N1 = 4
										000000000111	00000000XXXX			E_{51}			
L_{E6}										000000001000	00000000100X			E_{52}			L_{E6} With N1 = 8
										000000001111	0000000XXXXX			E_{53}			
L_{E8}										000000010000	00000001000X			E_{54}			L_{E8} With N1 = 16
										000000011111	000000XXXXXX			E_{55}			
L_{E10}										000000100000	00000010000X			E_{56}			L_{E10} With N1 = 32
										000000111111	00000XXXXXXX			E_{57}			
L_{E12}										000001000000	00000100000X			E_{58}			L_{E12} With N1 = 64
										000001111111	0000XXXXXXXX			E_{59}			
L_{E14}										000010000000	00001000000X			E_{60}			L_{E14} With N1 = 128
										000011111111	000XXXXXXXXX			E_{61}			
L_{E16}										000100000000	00010000000X			E_{62}			L_{E16} With N1 = 256
										000111111111	00XXXXXXXXXX			E_{63}			

DATA CONVERSION PRODUCTS 6

CHART A. GROUP A TEST CONDITIONS (Continued)

SYMBOL	APPLIED VOLTAGES REF. ANALOG COMMON (FIG. 1, NOTE 1)									APPLIED DIGITAL CODEWORD	DUT DIGITAL OUTPUT CODEWORD	SWITCH POSITIONS	MEASUREMENT SENSE LINES REF. ANA. COMMON			TEMP °C	EQUATIONS & NOTES
	7	11	1	13/14	2	3	4	5	6								
	V_{CC} (V)	V_{EE} (V)	V_{LOG} (V)	V_{IN} (V)	$12/\overline{8}$ (V)	$\overline{CS}$ (V)	A_0 (V)	$R/\overline{C}$ (V)	CE (V)	$DC_1 \longleftrightarrow DC_{12}$ MSB ⟷ LSB	27 ⟷ 16 MSB ⟷ LSB	$S_1 \longleftrightarrow S_9$	PIN	VALUE	UNIT		
L_{E18}	+15	-15	+5	SERV LOOP	2.0	0.8	0.8	TRIG CKT	2.0	001000000000	00100000000X	100101111	14	E_{64}	V	+25, +125, -55	L_{E18} With N1 = 512
										001111111111	0XXXXXXXXXXX			E_{65}			
L_{E20}										010000000000	01000000000X			E_{66}			L_{E20} With N1 = 1024
										011111111111	XXXXXXXXXXXX			E_{67}			
L_{E22}										100000000000	10000000000X			E_{68}			L_{E22} With N1 = 2048
										100011111111	100XXXXXXXXX			E_{69}			
L_{E24}										100100000000	10010000000X			E_{70}			L_{E24} With N1 = 2304
										100111111111	10XXXXXXXXXX			E_{71}			
L_{E26}										101000000000	10100000000X			E_{72}			L_{E26} With N1 = 2560
										101011111111	101XXXXXXXXX			E_{73}			
L_{E28}										101100000000	10110000000X			E_{74}			L_{E28} With N1 = 2816
										101111111111	1XXXXXXXXXXX			F_{75}			
L_{E30}										110000000000	11000000000X			E_{76}			L_{E30} With N1 = 3072
										110011111111	110XXXXXXXXX			E_{77}			
L_{E32}										110100000000	11010000000X			E_{78}			L_{E32} With N1 = 3328
										110111111111	11XXXXXXXXXX			E_{79}			
L_{E34}										111000000000	11100000000X			E_{80}			L_{E34} With N1 = 3584
										111011111111	111XXXXXXXXX			E_{81}			
L_{E36}										111100000000	11110000000X			E_{82}			L_{E36} With N1 = 3840
L_{E38}										Turn on bits that had positive integral linearity error for L_{E1} to L_{E22}	Low Edge			E_{83}			L_{E38} With N1 = Sum of positive L_{E1} to L_{E22}
											High Edge			E_{84}			

CHART A. GROUP A TEST CONDITIONS (Continued)

SYMBOL	APPLIED VOLTAGES REF. ANALOG COMMON (FIG. 1, NOTE 1)									APPLIED DIGITAL CODEWORD	DUT DIGITAL OUTPUT CODEWORD	SWITCH POSITIONS	MEASUREMENT SENSE LINES REF. ANA. COMMON			TEMP °C	EQUATIONS & NOTES
	7	11	1	13/14	2	3	4	5	6								
	V_{CC} (V)	V_{EE} (V)	V_{LOG} (V)	V_{IN} (V)	$12/\overline{8}$ (V)	$\overline{CS}$ (V)	A_0 (V)	$R/\overline{C}$ (V)	CE (V)	$DC_1 \longleftrightarrow DC_{12}$ MSB ⟷ LSB	$27 \longleftrightarrow 16$ MSB ⟷ LSB	$S_1 \longleftrightarrow S_9$	PIN	VALUE	UNIT		
L_{E40}	+15	-15	+5	SERV LOOP	2.0	0.8	0.8	TRIG CKT.	2.0	Turn on bits that had negative integral linearity error for L_{E1} to L_{E22}	Low Edge	100101111	14	E_{85}	V		L_{E40} With N1 = Sum of negative L_{E1} to L_{E22}
											High Edge			E_{86}			
																+25, +125, -55	For Differential Linearity Error $D_{LE}(N) = (E(N + 88) - E(N + 87))/S$. $S = (E_{87} - E_{88})/4094$
										111111111110	11111111111X			E_{87}			
										000000000000	00000000000X			E_{88}			
D_{LE1}										000000000001	0000000000XX			E_{89}			D_{LE1}
D_{LE2}										000000000010	00000000001X			E_{90}			D_{LE2}
D_{LE3}										000000000011	000000000XXX			E_{91}			D_{LE3}
D_{LE4}										000000000100	00000000010X			E_{92}			D_{LE4}
										000000000110	00000000011X			E_{93}			
D_{LE6}										000000000111	00000000XXXX			E_{94}			D_{LE6}
D_{LE7}										000000001000	00000000100X			E_{95}			D_{LE7}
										000000001110	00000000111X			E_{96}			
D_{LE9}										000000001111	0000000XXXXX			E_{97}			D_{LE9}
D_{LE10}										000000010000	00000001000X			E_{98}			D_{LE10}
										000000011110	00000001111X			E_{99}			
D_{LE12}										000000011111	000000XXXXXX			E_{100}			D_{LE12}
D_{LE13}										000000100000	00000010000X			E_{101}			D_{LE13}
										000000111110	00000011111X			E_{102}			

DATA CONVERSION PRODUCTS 6

CHART A. GROUP A TEST CONDITIONS (Continued)

SYMBOL	APPLIED VOLTAGES REF. ANALOG COMMON (FIG. 1, NOTE 1)									APPLIED DIGITAL CODEWORD	DUT DIGITAL OUTPUT CODEWORD	SWITCH POSITIONS	MEASUREMENT SENSE LINES REF. ANA. COMMON			TEMP C	EQUATIONS & NOTES
	7	11	1	13/14	2	3	4	5	6								
	V_{CC} (V)	V_{EE} (V)	V_{LOG} (V)	V_{IN} (V)	$12/\overline{8}$ (V)	$\overline{CS}$ (V)	A_0 (V)	$R/\overline{C}$ (V)	CE (V)	$DC_1 \longleftrightarrow DC_{12}$ MSB ⟷ LSB	27 ⟷ 16 MSB ⟷ LSB	$S_1 \longleftrightarrow S_9$	PIN	VALUE	UNIT		
D_{LE15}	+15	-15	+5	SERV LOOP	2.0	0.8	0.8	TRIG CKT	2.0	000000111111	00000XXXXXXX	100101111	14	E_{103}	V	+25, +125 -55	D_{LE15}
D_{LE16}										000001000000	00000100000X			E_{104}			D_{LE16}
										000001111110	00000111111X			E_{105}			
D_{LE18}										000001111111	0000XXXXXXXX			E_{106}			D_{LE18}
D_{LE19}										000010000000	00001000000X			E_{107}			D_{LE19}
										000011111110	00000111111X			E_{108}			
D_{LE21}										000011111111	000XXXXXXXXX			E_{109}			D_{LE21}
D_{LE22}										000100000000	00010000000X			E_{110}			D_{LE22}
										000111111110	00011111111X			E_{111}			
D_{LE24}										000111111111	00XXXXXXXXXX			E_{112}			D_{LE24}
D_{LE25}										001000000000	00100000000X			E_{113}			D_{LE25}
										001111111110	00111111111X			E_{114}			
D_{LE27}										001111111111	0XXXXXXXXXXX			E_{115}			D_{LE27}
D_{LE28}										010000000000	01000000000X			E_{116}			D_{LE28}
										011111111110	01111111111X			E_{117}			
D_{LE30}										011111111111	XXXXXXXXXXXX			E_{118}			D_{LE30}
D_{LE31}										100000000000	10000000000X			E_{119}			D_{LE31}
										100011111110	10001111111X			E_{120}			
D_{LE33}										100011111111	100XXXXXXXXX			E_{121}			D_{LE33}
D_{LE34}										100100000000	10010000000X			E_{122}			D_{LE34}
										100111111110	10011111111X			E_{123}			
D_{LE36}										100111111111	10XXXXXXXXXX			E_{124}			D_{LE36}
D_{LE37}										101000000000	10100000000X			E_{125}			D_{LE37}

CHART A. GROUP A TEST CONDITIONS (Continued)

SYMBOL	APPLIED VOLTAGES REF. ANALOG COMMON (FIG. 1, NOTE 1)									APPLIED DIGITAL CODEWORD	DUT DIGITAL OUTPUT CODEWORD	SWITCH POSITIONS	MEASUREMENT SENSE LINES REF. ANA. COMMON			TEMP °C	EQUATIONS & NOTES
	7	11	1	13/14	2	3	4	5	6								
	V_{CC} (V)	V_{EE} (V)	V_{LOG} (V)	V_{IN} (V)	$12/\overline{8}$ (V)	$\overline{CS}$ (V)	A_0 (V)	$R/\overline{C}$ (V)	CE (V)	$DC_1 \longleftrightarrow DC_{12}$ MSB ⟷ LSB	27 ⟷ 16 MSB ⟷ LSB	$S_1 \longleftrightarrow S_9$	PIN	VALUE	UNIT		
	+15	-15	+5	SERV LOOP	2.0	0.8	0.8	TRIG CKT.	2.0	101011111110	10101111111X	100101111	14	E126	V	+25, +125	
D_{LE39}										101011111111	101XXXXXXXXX			E127		-55	D_{LE39}
D_{LE40}										101100000000	10110000000X			E128			D_{LE40}
										101111111110	10111111111X			E129			
D_{LE42}										101111111111	1XXXXXXXXXXX			E130			D_{LE42}
D_{LE43}										110000000000	11000000000X			E131			D_{LE43}
										110011111110	11001111111X			E132			
D_{LE45}										110011111111	110XXXXXXXXX			E133			D_{LE45}
D_{LE46}										110100000000	11010000000X			E134			D_{LE46}
										110111111110	11011111111X			E135			
D_{LE48}										110111111111	11XXXXXXXXXX			E136			D_{LE48}
D_{LE49}										111000000000	11100000000X			E137			D_{LE49}
										111011111110	11101111111X			E138			
D_{LE51}										111011111111	111XXXXXXXXX			E139			D_{LE51}
D_{LE52}										111100000000	11110000000X			E140			D_{LE52}
D_{LE54}										Turn on Bits that had positive differential linearity error for DLE's 1, 2, 4, 7, 10, 13, 16, 19, 22, 25, 28, 31 Minus 1 LSB	Low Edge High Edge			E141 E142			D_{LE54}
D_{LE55}										Turn on Bits that had positive differential linearity error for DLE's 1, 2, 4, 7, 10, 13, 16, 19, 22, 25, 28, 31	High Edge			E143			D_{LE55}

CHART A. GROUP A TEST CONDITIONS (Continued)

SYMBOL	APPLIED VOLTAGES REF. ANALOG COMMON (FIG. 1, NOTE 1) 7 VCC (V)	11 VEE (V)	1 VLOG (V)	13/14 VIN (V)	2 $12/\overline{8}$ (V)	3 $\overline{CS}$ (V)	4 A0 (V)	5 $R/\overline{C}$ (V)	6 CE (V)	APPLIED DIGITAL CODEWORD DC1 ⟷ DC12 MSB ⟷ LSB	DUT DIGITAL OUTPUT CODEWORD 27 ⟷ 16 MSB ⟷ LSB	SWITCH POSITIONS S1 ⟷ S9	MEASUREMENT SENSE LINES REF. ANA. COMMON PIN	VALUE	UNIT	TEMP C	EQUATIONS & NOTES
D_{LE57}										Turn on Bits that had negative differential linearity error for DLE's 1, 2, 4, 7, 10, 13, 16, 19, 22, 25, 28, 31 Minus 1 LSB	Low Edge High Edge			E_{144} E_{145}			D_{LE57}
D_{LE58}										Turn on Bits that had negative differential linearity error for DLE's 1, 2, 4, 7, 10, 13, 16, 19, 22, 25, 28, 31	High Edge			E_{146}			D_{LE58}
R_{I10V} R_{I20V}	+15 +15	-15 -15	+5 +5	5 10								010111011 010110011	13 14	I_{46} I_{47}	mA mA	+25, +125, -55	$R_{I10V} = 5V/I_{46}$ $R_{I20V} = 10V/I_{47}$
$\frac{dV_{IO}}{dT}$	+15	-15	+5													+125 -55	$dV_{IO}/dT = V_{IOH} - V_{IOR}$ $dV_{IO}/dT = V_{IOL} - V_{IOR}$
$\frac{dB_Z}{dT}$	+15	-15	+5													+125 -55	$dB_Z/dT = B_{ZH} - B_{ZR}$ $dB_Z/dT = B_{ZL} - B_{ZR}$
$\frac{dA_E}{dT}$	+15	-15	+5													+125 -55	$dA_E/dT = A_{EH} - A_{ER}$ $dA_E/dT = A_{EL} - A_{ER}$
$\frac{dBA_E}{dT}$	+15	-15	+5													+125 -55	$dBA_E/dT = BA_{EH} - BA_{ER}$ $dBA_E/dT = BA_{EL} - BA_{ER}$
t_{C1}	+15	-15	+5	SERV LOOP	2.0	0.8	2.0	TRIG CKT.	2.0	000000000000	00000000000X	100101111	28	t_1	μs	+25, +125, -55	$t_{C1} = t_1$ Rising Edge to Falling Edge
t_{C2}	+15	-15	+5		2.0	0.8	0.8		2.0	000000000000	00000000000X	100101111	28	t_2	μs	+25, +125, -55	$t_{C2} = t_2$ Rising Edge to Falling Edge
	+15	-15	+5									010111010		t_3	ns	+25, +125, -55	$t_{TD} = t_3$ t_{TD} = Trigger CKT Delay
t_{DS1}	+15	-15	+5	SERV LOOP	2.0	0.8	2.0	TRIG CKT.	2.0	000000000000	00000000000X	100101111	28	t_4	ns	-55	$t_{DS1} = t_4 - t_3 - t_1$ t_4 Meas. Rising Edge to Rising Edge
t_{DS2}	+15	-15	+5		2.0	0.8	0.8		2.0	000000000000	00000000000X	100101111	28	t_5	ns		$t_{DS2} = t_5 - t_3 - t_2$ t_5 Meas. Rising Edge to Rising Edge

Switching Waveform Information

Conversion Length

A Convert Start transition (see Chart B) latches the state of A_0, which determines whether the conversion continues for 12-bits (A_0 low) or stops with 8-bits (A_0 high). If all 12-bits are read following an 8-bit conversion, the three LSBs will read zero and DB3 will read ONE. A_0 is latched because it is also involved in enabling the output buffers (see Reading the Output Data"). No other control inputs are latched.

CHART B. TRUTH TABLE FOR HI-774/883 CONTROL INPUTS

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

Conversion Start

A conversion may be initiated as shown in Chart B by a logic transition on any of three inputs: CE, $\overline{CS}$ or R/$\overline{C}$. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same, and if necessary, all three may change state simultaneously. See the Timing Specifications, Convert mode.

The variety of control modes allows a simple interface in most system applications. The Convert Start timing relationships are illustrated in Figure 5.

The output signal STS indicates status of the converter by going high only while a conversion is in progress. While STS is high, the output buffers remain in a high impedance state and data cannot be read. Also, an additional Start Convert will not reset the converter or reinitiate a conversion while STS is high. (However, if A_0 changes state after a conversion begins, an additional Start Convert signal will latch the new state of A_0, possibly causing a wrong cycle length (8 vs. 12-bits) for that conversion).

Reading the Output Data

The output data buffers remain in a high impedance state until four conditions are met: R/$\overline{C}$ high, STS low, CE high and $\overline{CS}$ low. At that time, data lines become active according to the state of inputs 12/8 and A_0. Timing constraints are illustated in Figure 6.

The 12/$\overline{8}$ input will be tied high or low in most applications, though it is fully TTL/CMOS compatible. With 12/$\overline{8}$ high, all 12 output lines become active simultaneously, for interface to a 12 or 16-bit data bus. The A_0 input is ignored.

With 12/$\overline{8}$ low, the output is organized in two 8 bit bytes, selected one at a time by A_0. This allows an 8 bit data bus to be connected as shown in Figure 10. A_0 is usually tied to the least significant bit of the address bus, for storing the output data in two consecutive memory locations. (With A_0 low, the 8 MSBs only are enabled. With A_0 high, 4 MSBs are disabled, bits 4 through 7 are forced to zero, and the 4 LSBs are enabled). This two byte format is considered left justified data", for which a decimal (or binary!) point is assumed to the left of byte 1:

BYTE 1	BYTE 2
X X X X X X X X	X X X X 0 0 0 0
MSB	LSB

Further, A_0 may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in Figure 10 will never be enabled at the same time.

A read operation usually begins after the conversion is complete and STS is low. For earliest access to the data however, the read should begin no later than ($t_{DD} + t_{HS}$) before STS goes low. See Figure 6.

STAND-ALONE MODE TIMING (OVER FULL TEMP. RANGE)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	350			ns
t_{DS}	STS Delay from R/$\overline{C}$			600	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	15			ns
t_{HS}	STS Delay After Data Valid			300	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	300			ns
t_{DDR}	Data Access Time			250	ns

Switching Waveforms

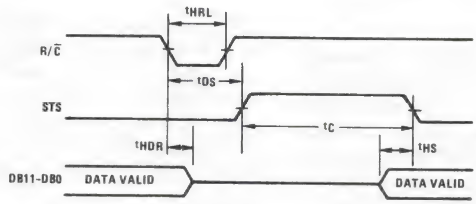


FIGURE 3. LOW PULSE R/C̄-OUTPUTS ENABLED AFTER CONVERSION

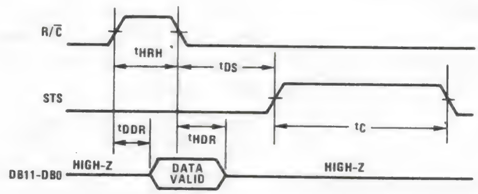


FIGURE 4. HIGH PULSE FOR R/C̄-OUTPUTS ENABLED WHILE R/C̄ HIGH, OTHERWISE HIGH-Z

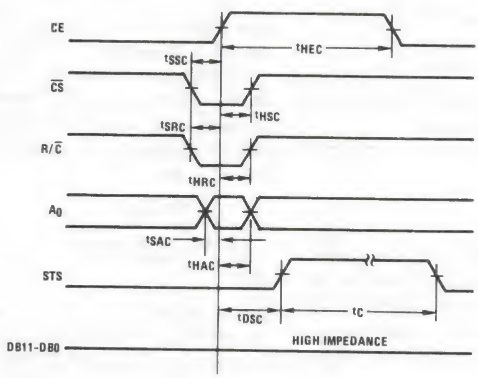


FIGURE 5. CONVERT START TIMING

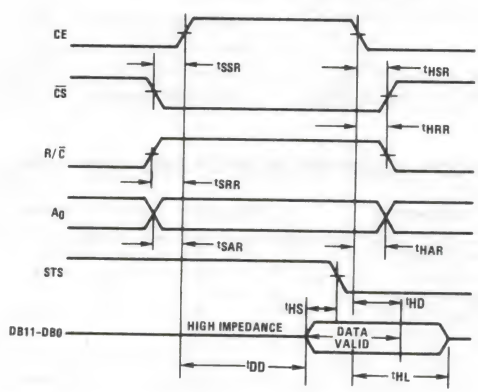
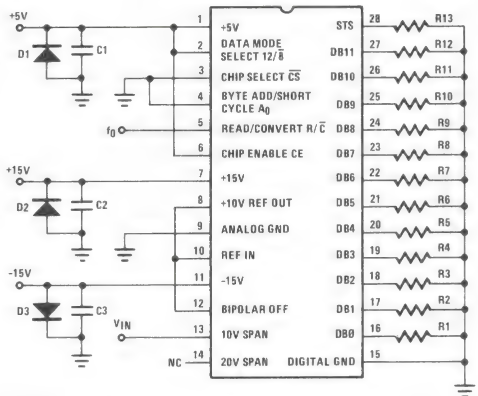


FIGURE 6. READ CYCLE TIMING

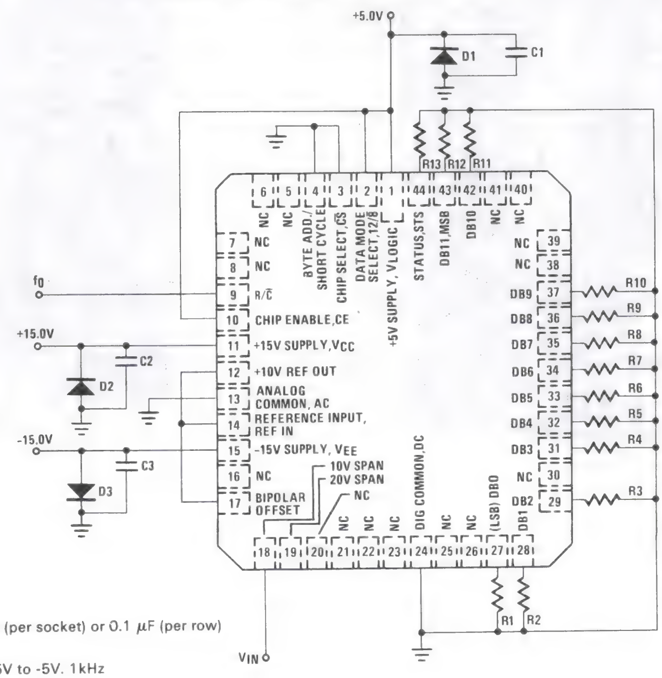
Burn-In Circuits

28 PIN SIDEBRAZED DIP



NOTES:
R1 thru R13 = 10kΩ
C1 thru C3 = 0.01μF minimum (per socket) or 0.1 μF (per row)
D1 thru D3 = IN4002
V_{IN} = Triangle Wave Form, +5V to -5V. 1kHz
f_0 = square waveform, 10kHz, 90% Duty Cycle, 0V to 5V

44 PIN CERAMIC LEADLESS CHIP CARRIER



NOTES:
R1 thru R13 = 10kΩ
C1 thru C3 = 0.01μF minimum (per socket) or 0.1 μF (per row)
D1 thru D3 = IN4002
V_{IN} = Triangle Wave Form, +5V to -5V. 1kHz
f_0 = square waveform, 10kHz, 90% Duty Cycle, 0V to 5V

6

DATA CONVERSION PRODUCTS

Die Characteristics

DIE DIMENSIONS:

ANALOG DIE:	204 x 104 mils
DIGITAL DIE:	190 x 94 mils

METALLIZATION:

ANALOG DIE:	Type: Al
	Thickness: 16kA ± 2kA
DIGITAL DIE:	Type: SiAl
	Thickness: 16kA ± 2kA

WORST CASE CURRENT DENSITY:

ANALOG DIE:	1.71×10^5 A/cm^2
DIGITAL DIE:	1.78×10^5 A/cm^2

TRANSISTOR COUNT ANALOG DIE: 317
DIGITAL DIE: 1800

PROCESS: ANALOG DIE: Bipolar-DI
DIGITAL DIE: CMOS-JI

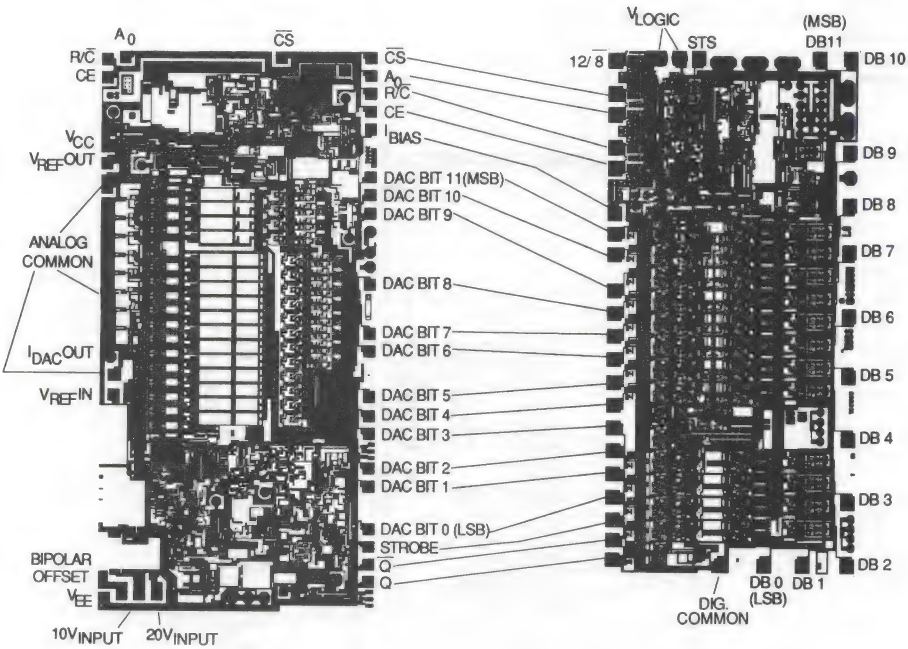
DIE ATTACH: Material: Gold/Silicon Eutectic Alloy
Temperature: 420°C Max

GLASSIVATION:

ANALOG DIE:	Type: Silox
	Thickness: 14kA ± 2kA
DIGITAL DIE:	Type: Silox
	Thickness: 8kA ± 2kA

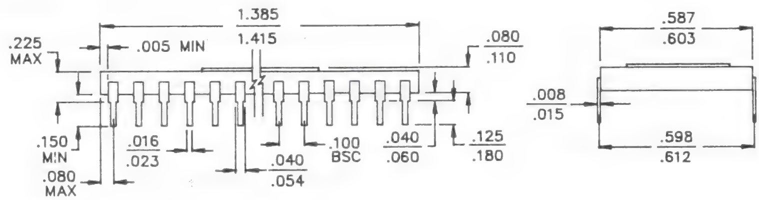
Metallization Mask Layout

HI-774/883 ANALOG DIE **HI-774/883 DIGITAL DIE**



Packaging†

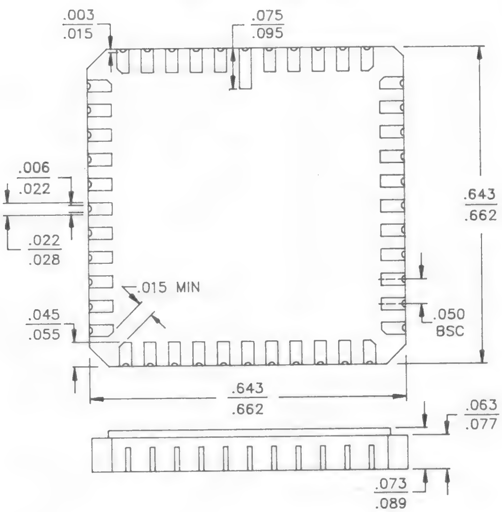
28 PIN CERAMIC DIP



LEAD MATERIAL: Type B
LEAD FINISH: Type C
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-10

44 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-5

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HI-774

DESIGN INFORMATION

Fast, Complete 12-Bit A/D Converter With Microprocessor Interface

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Definitions of Specifications

Linearity Error

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs ½LSB (1.22mV for 10 volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1½LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HI-774T grade is guaranteed for maximum nonlinearity of ±½LSB. This means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HI-774S grade is guaranteed to ±1 LSB max error. An analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user-adjustable.

Differential Linearity Error (No Missing Codes)

A specification which guarantees no missing codes requires that every combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. The HI-774T grade, guarantees no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HI-774S grade guarantees no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11-bits must be present; in practice very few of the 12-bit codes are missing.

Unipolar Offset

The first transition should occur at a level ½LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

Bipolar Offset

Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value ½LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

Full Scale Calibration Error

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1½LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 7 and 8. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 volt reference.

Temperature Coefficients

The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{min} or T_{max}.

Power Supply Rejection

The standard specifications for the HI-774 assume use of +5.00 and ±15.00 or ±12.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

Code Width

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 Least Significant Bit (LSB) of the full scale range or 2.44mV out of 10 volts for a 12-bit ADC.

Quantization Uncertainty

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±½LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

Left-Justified Data

The data format used in the HI-774 is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

*Applying the HI-774**

*Pin numbers correspond to DIP package only.

For each application of this converter, the ground connections, power supply bypassing, analog signal source, digital timing and signal routing on the circuit board must be optimized to assure maximum performance. These areas are reviewed in the following sections, along with basic operating modes and calibration requirements.

PHYSICAL MOUNTING AND LAYOUT CONSIDERATIONS

Layout

Unwanted, parasitic circuit components, (L, R, and C) can make 12-bit accuracy impossible, even with a perfect A/D converter. The best policy is to eliminate or minimize these parasitics through proper circuit layout, rather than try to quantify their effects.

The recommended construction is a double-sided printed circuit board with a ground plane on the component side. Other techniques, such as wire-wrapping or point-to-point wiring on vectorboard, will have an unpredictable effect on accuracy.

In general, sensitive analog signals should be routed between ground traces and kept well away from digital lines. If analog and digital lines must cross, they should do so at right angles.

Power Supplies

Supply voltages to the HI-774 (+15V, -15V and +5V) must be "quiet" and well regulated. Voltage spikes on these lines can affect the converter's accuracy, causing several LSB's to flicker when a constant input is applied. Digital noise and spikes from a switching power supply are especially troublesome. If switching supplies must be used, outputs should be carefully filtered to assure "quiet" DC voltage at the converter terminals.

Further, a bypass capacitor pair on each supply voltage terminal is necessary to counter the effect of variations in supply current. Connect one pair from pin 1 to 15 (V_{LOGIC} supply), one from pin 7 to 9 (V_{CC} to Analog Common) and one from pin 11 to 9 (V_{EE} to Analog Common). For each capacitor pair, a 10μF tantalum type in parallel with a 0.1μF ceramic type is recommended.

Ground Connections

The typical HI-774 ground currents are 5.5mADC into pin 9 (Analog Common) and 7mADC out of pin 15 (Digital Common). These pins should be tied together at the package to guarantee specified performance for the converter. In addition, a wide PC trace should run directly from pin 9 to (usually) 15V common, and from pin 15 to (usually) the +5V Logic Common. If the converter is located some distance from the system's "single point" ground, make only these connections to pins 9 and 15: Tie them together at the package, and back to the system ground with a single path. This path should have low resistance since it will carry about 1.5mA of DC current. (Code dependent currents flow in the V_{CC}, V_{EE} and V_{LOGIC} terminals, but not through the HI-774's Analog Common or Digital Common).

ANALOG SIGNAL SOURCE

The device driving the HI-774 analog input will see a nominal load of 5kΩ (10V range). However, the other end of these input resistors may change as much as ±400mV with each bit decision, creating abrupt changes in current at the analog input. Thus, the signal source must maintain its output voltage while furnishing these step changes in load current. This requires low output impedance and fast settling by the signal source.

The output impedance of an op amp, for example, has an open loop value which, in a closed loop, is divided by the loop gain available at a frequency of interest. The amplifier should have acceptable loop gain at 1.3MHz for use with the HI-774. To check whether the output properties of a signal source are suitable, monitor the 774's input (pin 13) with an oscilloscope while a conversion is in progress.

If the application calls for a Sample/Hold to precede the converter, it should be noted that not all Sample/Holds are compatible with the HI-774 in the manner described above. These will require an additional wideband buffer amplifier to lower their output impedance. A simpler solution is to use the Harris HA-5330 Sample/Hold, which was designed for use with the HI-774.

RANGE CONNECTIONS AND CALIBRATION PROCEDURES

The HI-774 is a "complete" A/D converter, meaning it is fully operational with addition of the power supply voltages, a Start Convert signal, and a few external components as shown in figures 7 and 8. Nothing more is required for most applications.

Whether controlled by a processor or operating in the stand-alone mode, the HI-774 offers two standard input ranges: 0V to +10V, and ±5V. The maximum errors for gain and offset are listed under Specifications. If required, however, these errors may be adjusted to zero as explained below. Power supply and ground connections have been discussed in an earlier section.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Unipolar Connections and Calibration

Refer to figure 7. The resistors shown* are for calibration of offset and gain. If this is not required, replace R2 with a 50Ω, 1% metal film resistor and remove the network on pin 12. Connect pin 12 to pin 9. Then, connect the analog signal to pin 13 for the 0V to 10V range.

Calibration consists of adjusting the converters's most negative output to its ideal value (offset adjustment), then, adjusting the most positive output to its ideal value (gain adjustment). To understand the procedure, note that in principle, one is setting the output with respect to the midpoint of an increment of analog input, as denoted by two adjacent code changes. Nominal value of an increment is one LSB. However, this approach is impractical because nothing "happens" at a midpoint to indicate that an adjustment is complete. Therefore, calibration is performed in terms of the observable code changes instead of the midpoint between code changes.

For example, midpoint of the first LSB increment should be positioned at the origin, with an output code of all 0's. To do this, apply an input of +½LSB (+1.22mV for the 10V range). Adjust the Offset potentiometer R1 until the first code transition flickers between 0000 0000 0000 and 0000 0000 0001.

Next, perform a Gain Adjust at positive full scale. Again, the ideal input corresponding to the last code change is applied. This is 1½LSB's below the nominal full scale (+9.9963V for 10V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

Bipolar Connections and Calibration

Refer to Figure 8. The gain and offset errors listed under Specifications may be adjusted to zero using potentiometers R1 and R2*. If this isn't required, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

Connect the Analog signal to pin 13 for a ±5V range. Calibration of offset and gain is similar to that for the unipolar ranges as discussed above. First apply a DC input voltage ½LSB above negative full scale (i.e., -4.9988V for the ±5V range). Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1½LSB's below positive full scale (+4.9963V for ±5V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

*The 100Ω potentiometer R2 provides Gain Adjust. In some applications, a full scale of 10.24V (LSB equals 2.5mV) is more convenient. For these, replace R2 by a 50Ω, 1% metal film resistor. Then, to provide Gain Adjust for the 10.24V range, add a 200Ω potentiometer in series with pin 13.

Pin Numbers Refer To Sidebraze DIP Package.

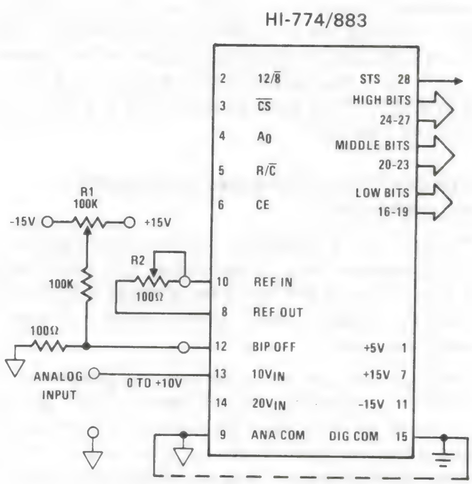


FIGURE 7. UNIPOLAR CONNECTIONS

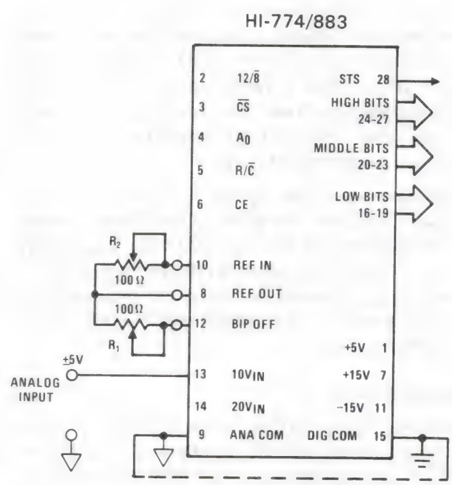


FIGURE 8. BIPOLAR INPUT CONNECTIONS

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Controlling the HI-774

The HI-774 includes logic for direct interface to most microprocessor systems. The processor may take full control of each conversion, or the converter may operate in the "stand-alone" mode, controlled only by the R/C input. Full control consists of selecting an 8 or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready — choosing either 12-bits at once or 8 followed by 4, in a left-justified format. The five control inputs are all TTL/CMOS-compatible: (12/8, CS, A_0, R/C and CE). Chart B illustrates the use of these inputs in controlling the converter's operations. Also, a simplified diagram of the internal control logic is shown in Figure 9.

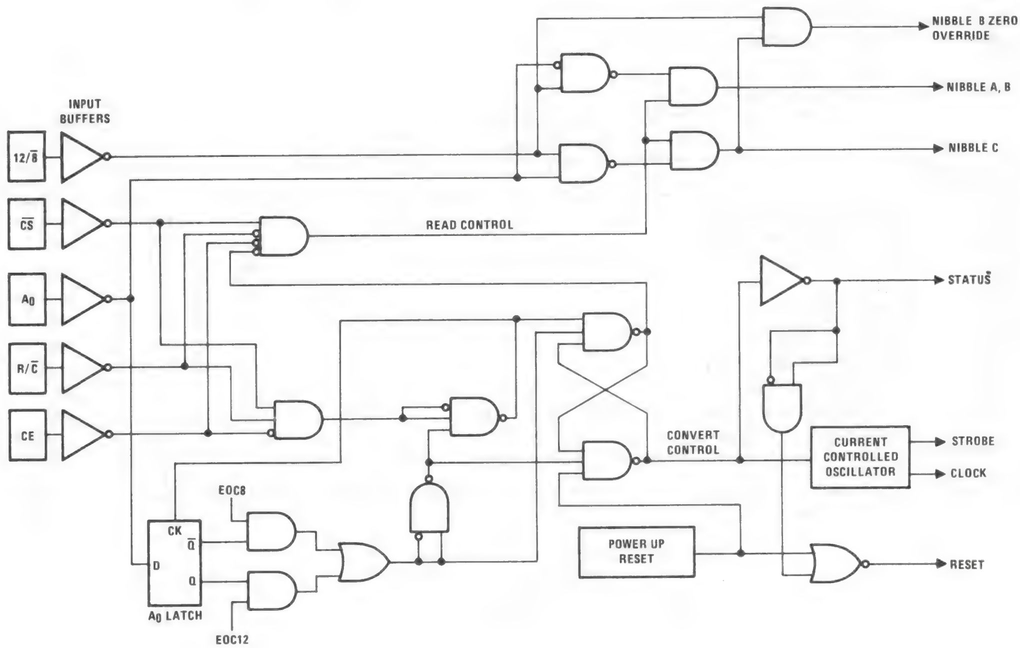


FIGURE 9. HI-774 CONTROL LOGIC

6

DATA CONVERSION PRODUCTS

DESIGN INFORMATION (Continued)

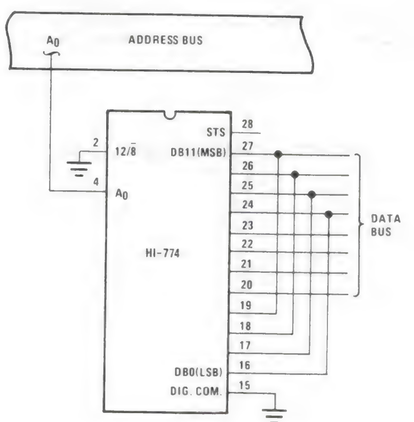
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

HI-774 Timing Specifications

+25°C Unless Otherwise Specified

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
CONVERT MODE					
t_{DSC}	STS Delay from CE	—	100	200	ns
t_{HEC}	CE Pulse Width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE Setup	50	—	—	ns
t_{HSC}	$\overline{CS}$ Low During CE High	50	20	—	ns
t_{SRC}	R/$\overline{C}$ to CE Setup	50	—	—	ns
t_{HRC}	R/$\overline{C}$ Low During CE High	50	20	—	ns
t_{SAC}	A_0 to CE Setup	0	0	—	ns
t_{HAC}	A_0 Valid During CE High	50	20	—	ns
t_c	Conversion Time, 12-bit Cycle T_{min} to T_{max}	—	—	11	μs
	8-bit Cycle T_{min} to T_{max}	—	—	8.5	μs
READ MODE					
t_{DD}	Access Time from CE	—	75	150	ns
t_{HD}	Data Valid after CE low	25	35	—	ns
t_{HL}	Output Float Delay	—	100	150	ns
t_{SSR}	$\overline{CS}$ to CE Setup	50	0	—	ns
t_{SRR}	R/$\overline{C}$ to CE Setup	0	0	—	ns
t_{SAR}	A_0 to CE Setup	50	25	—	ns
t_{HSR}	$\overline{CS}$ Valid after CE Low	0	0	—	ns
t_{HRR}	R/$\overline{C}$ High after CE Low	0	0	—	ns
t_{HAR}	A_0 Valid after CE Low	50	25	—	ns
t_{HS}	STS Delay after Data Valid	—	—	300	ns

NOTE: Time is measured from 50% level of digital transitions, tested with a 50pF and 3KΩ load. All possible combinations for setup times not listed, see Figure 9.



Pin Numbers Refer To Sidebraze DIP Package.

FIGURE 10. INTERFACE TO AN 8-BIT DATA BUS

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

HI-774 Capacitance Specifications

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
C_I	Logic Input Capacitance	—	5	—	pF
C_O	Logic Output Capacitance	—	5	—	pF

HARRIS **HC-55564/883**

Continuously Variable Slope Delta-Modulator (CVSD)

January 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- All Digital
- Requires Few External Parts
- Low Power Drain
- Time Constants Determined by Clock Frequency; No Calibration or Drift Problems: Automatic Offset Adjustment
- Half Duplex Operation Under Digital Control
- Filter Reset Under Digital Control
- Automatic Overload Recovery
- Automatic "Quiet" Pattern Generation
- $\overline{AGC}$ Control Signal Available

Applications

- Voice Transmission Over Data Channels (Modems)
- Voice/Data Multiplexing (Pair Gain)
- Voice Encryption/Scrambling
- Voicemail
- Audio Manipulations: Delay Lines, Time Compression, Echo Generation/Suppression, Special Effects, etc.
- Pagers/Satellites
- Data Aquisition Systems
- Voice I/O for Digital Systems and Speech Synthesis Requiring Small Size, Low Weight, and Ease of Reprogrammability

Description

The HC-55564 is a half duplex modulator/demodulator CMOS intergrated circuit used to convert voice signals into serial NRZ digital data and to reconvert that data into voice. The conversion is by delta-modulation, using the Continuously Variable Slope (CVSD) modulation/de-modulation.

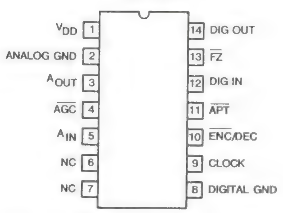
While the signals are compatible with other CVSD circuits, the internal design is unique. The analog loop filters have been replaced by very low power digital filters which require no external timing components. This approach allows inclusion of many desirable features which would be difficult to implement using other approaches.

The fundamental advantages of delta-modulation, along with its simplicity and serial data format, provide an efficient (low data rate/low memory requirements) method for voice digitization. The device may be easily configured with the HC-5512D PCM/CVSD filter.

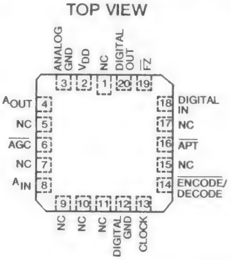
The HC-55564/883 is usable from 9K bits/sec to above 64Kbps. The unit is available in a 14 pin Ceramic DIP or a 20 pad Ceramic LCC package. For more applications information, see Application's Notes 576 and 607 (section 10 of Analog Data Book).

Pinouts

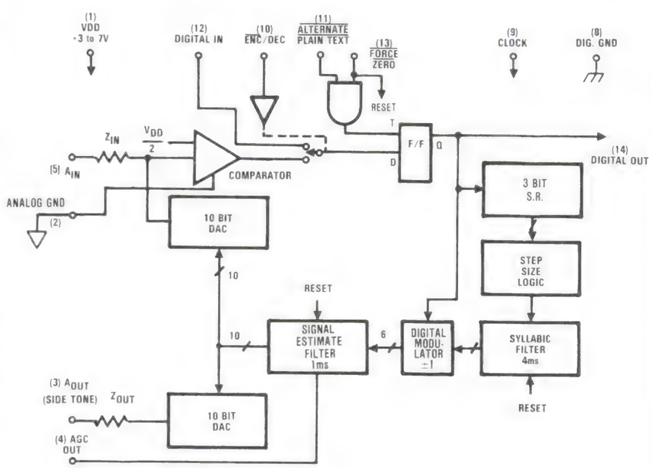
HC1-55564/883 (CERAMIC DIP)
TOP VIEW



HC4-55564/883 (CERAMIC LCC)
TOP VIEW



Functional Diagram



NOTE: Pin Numbers Correspond to DIP Package Only.

Pin Description

PIN NO. 14-PIN DIP	PIN NO. 20-PIN LCC	SYMBOL	DESCRIPTION
1	2	V_{DD}	Positive Supply Voltage. Voltage range is +3.0V to +7.0V.
2	3	Analog GND	Analog Ground connection to D/A ladders and comparator.
3	4	A_{OUT}	Audio Out recovered from 10 bit DAC. May be used as side tone at the transmitter. Presents approximately 150 kilohm source with D.C. offset of $V_{DD}/2$. Within ±2dB of Audio Input. Should be externally A.C. coupled.
4	6	$\overline{AGC}$	Automatic Gain Control output. A logic low level will appear at this output when the recovered signal excursion reaches ½ of full scales value. In each half cycle full scale is $V_{DD}/2$. The mark-space ratio is proportional to the average signal level.
5	8	A_{IN}	Audio Input to comparator. Should be externally coupled. Presents approximately 280 kilohms in series with $V_{DD}/2$.
6, 7	1, 5, 7, 9 10, 11 15, 17	NC	No internal connection is made to these pins.
8	12	Digital GND	Logic ground. 0V reference for all logic inputs and outputs.
9	13	Clock	Sampling rate clock. In the decode mode, must be synchronized with the digital input data such that the data is valid at the positive clock transition. In the encode mode, the digital data is clocked out on the negative going clock transition. The clock rate equals the data rate.
10	14	$\overline{\text{Encode}}$/ Decode	A single CVSD can provide half-duplex operation. The encode or decode function is selected by the logic level applied to this input. A low level selects the encode mode, a high level the decode mode.
11	16	$\overline{APT}$	Alternate Plain Text input. Activating this input caused a digital quieting pattern to be transmitted, however; internally the CVSD is still functional and a signal is still available at the A_{OUT} port. Active low.
12	18	Digital In	Input for the received digital NRZ data.
13	19	$\overline{FZ}$	Force Zero input. Activating this input resets the internal logic and forces the digital output and the recovered audio output into the "quieting" condition. An alternating 1-0 pattern appears at the digital output at ½ the clock rate. When this is decoded by a receive CVSD, a 10mVp-p inaudible signal appears at audio output. Active low.
14	20	Digital Out	Output for transmitted digital NRZ data.

NOTE: No active input should be left in a "floating condition."

Absolute Maximum Ratings

Voltage at Any Pin .... GND -0.3V to V_{DD} +0.3V
Maximum V_{DD} Voltage .... +7.0V
Minimum V_{DD} Voltage .... +3.0V
Junction Temperature .... +175°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering 10 Seconds) .... +275°C
ESD Rating .... < 2000V

CAUTION Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	75°C/W	15°C/W
Ceramic LCC Package	76°C/W	19°C/W

Package Power Dissipation Limit at +75°C for T_J at ≤ +175°C
Ceramic DIP Package 1.33W
Ceramic LCC Package 1.32W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 13.3mW/°C
Ceramic LCC Package .... 13.2mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage (V_{DD} Range) .... +3.0V to +7.0V

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = +5V, fclk = 16kHz, Operating Temperature = -55°C ≤ T_A ≤ +125°C, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	I_{DD}	Encode Mode: A_{IN} = 0V	1	+25°C	-	1.5	mA
			2, 3	+125°C, -55°C	-	1.5	mA
Logic Input High (Note 2)	V_{IH}	Input Level: '1' = +3.5V, '0' = +1.5V	1	+25°C	3.5	-	V
			2, 3	+125°C, -55°C	3.5	-	V
Logic Input Low (Note 2)	V_{IL}	Input Level: '1' = +3.5V, '0' = +1.5V	1	+25°C	-	1.5	V
			2, 3	+125°C, -55°C	-	1.5	V
Logic Output High (Note 3)	V_{OH}	I Load = -40μA	1	+25°C	4.0	-	V
			2, 3	+125°C, -55°C	4.0	-	V
Logic Output Low (Note 3)	V_{OL}	I Load = +0.8mA	1	+25°C	-	0.4	V
			2, 3	+125°C, -55°C	-	0.4	V
Quieting Pattern (Note 8) Amplitude	V_{QP}	$\overline{FZ}$ = 0; Clock Inputs Switched Statically	1	+25°C	-	14	mVp-p
			2, 3	+125°C, -55°C	-	14	mVp-p
AGC Threshold (Note 9)	V_{ATH}	Encode Mode	1	+25°C	0.45	0.65	F.S.
			2, 3	+125°C, -55°C	0.45	0.65	F.S

CAUTION: This device is sensitive to electrosatic discharge. Proper I.C. handling procedures should be followed.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Characterized at: V_{DD} = +5V, T_A = +25°C Operating Temperature, fclk = 16kHz Clock Sampling Rate. $\overline{ENC}$/DEC = $\overline{ENC}$ = Encode Mode, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTE	TEMP	LIMITS MIN	LIMITS MAX	UNITS
Sampling Rate	CLK	A_{IN} = 0.775 V_{RMS} at 20Hz	1, 12	+25°C +125°C, -55°C	9	64	KBS
CLK Duty Cycle	A_{IN}	A_{IN} = 0.775 V_{RMS} at 100Hz	12	+25°C +125°C, -55°C	30	70	%
Audio Input Voltage	A_{IN}	A_{IN} at 100Hz	4, 12	+25°C +125°C, -55°C	-	1.2	V_{RMS}
Audio Output Voltage	A_{OUT}	A_{IN} at 100Hz	5, 12	+25°C +125°C, -55°C	-	1.2	V_{RMS}
Input Impedance	Z_{IN}	A_{IN} at 100Hz	6, 12	+25°C +125°C, -55°C	150	500	kΩ
Output Impedance	Z_{OUT}	A_{IN} at 100Hz	6, 12	+25°C +125°C, -55°C	35	225	kΩ
Transfer Gain	A_{E-D}	A_{IN} = 0.775 V_{RMS} at 100Hz	11, 12	+25°C -55°C, +125°C	-2	+2	dB
Resolution	RES	A_{IN} at 100Hz	12, 13	+25°C	0.3	-	% of Supply
MIN Step Size	MSS		7, 12	+25°C	0.02	0.08	% of Supply
Clamping Threshold	V_{CTH}		10, 12	+25°C	0.70	0.90	F.S.

NOTES:

1. There is one NR (Non-Return Zero) data bit per clock period. Data is clocked out on the negative clock edge. Data is clocked into the CVSD on the positive going edge (see Figure 2). Clock may be run at less than 9Kbps.
2. Logic inputs are CMOS compatible at supply voltage and are diode protected. Digital data input is NRZ at clock rate.
3. Logic outputs are CMOS compatible at supply voltage and will withstand short-circuits to V_{DD} or ground; however, the short circuit duty cycle must not exceed 5% in order to maintain an acceptable current density level. Digital data output is NRZ and changes with negative clock transitions. Each output will drive two LS TTL loads.
4. Recommended voice input range for best voice performance. Should be externally A.C. coupled.
5. May be used for side-tone in encode mode. Should be externally A.C. coupled. Varies with audio input level by ±dB.
6. Presents series impedance with audio signal. Zero signal reference is approximately $V_{DD}/2$.
7. The minimum audio output voltage change that can be produced by the internal DAC.
8. The "quieting" pattern or idle-channel audio output steps at 1/2 the bit rate, changing state on negative clock transitions.
9. A logic '0' will appear at the AGC output pin when the recovered signal reaches 1/2 of full-scale value (positive or negative), i.e. at $V_{DD}/2$ ±25% of V_{DD}.
10. The recovered signal will be clamped, and the computation will be inhibited, when the recovered signal reaches 3/4 of full-scale value, and will unclamp when it falls below this value (positive or negative).
11. No load condition measured from audio in to audio out.
12. The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
13. The minimum audio input voltage above which encoding is guaranteed to take place.

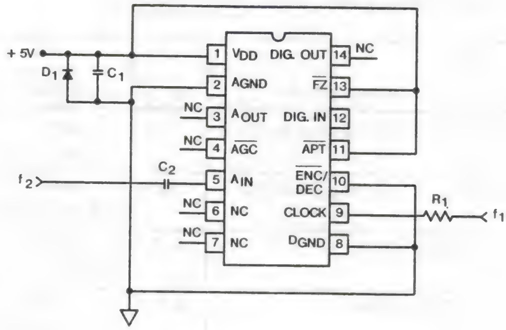
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 3)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3
Group A Test Requirements	1, 2, 3
Groups C & D Endpoints	1

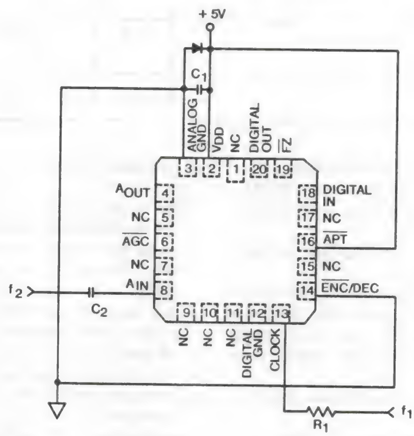
* PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

Burn-In Circuits

HC-55564/883 (CERAMIC DIP)



HC-55564/883 (CERAMIC LCC)



NOTES:

R_1 = 10KΩ ±5Ω, 1/4 Watt (per socket)

f_1 = 16kHz TTL Levels, 50% Duty Cycle, Square Wave

f_2 = ≃ 200Hz (Approximate); 3Vp-p Sinewave (or triangular wave), centered around ground.

C_1 = 0.01µF (per socket), or 0.1µF (per row) minimum.

C_2 = 0.1µF (per socket) minimum.

D_1 = IN4002 or Equivalent (per board)

Die Characteristics

DIE DIMENSIONS:
154 x 93 x 19 mils

METALLIZATION:
Type: SiAl
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
2.0 x 10^5A/cm^2
This device meets Glassivation Integrity Test requirement per Mil-Std-883 Method 2021 and Mil-M-38510 paragraph 3.5.5.4.

GLASSIVATION:
Type: Silox
Thickness: 8kÅ ± 1kÅ

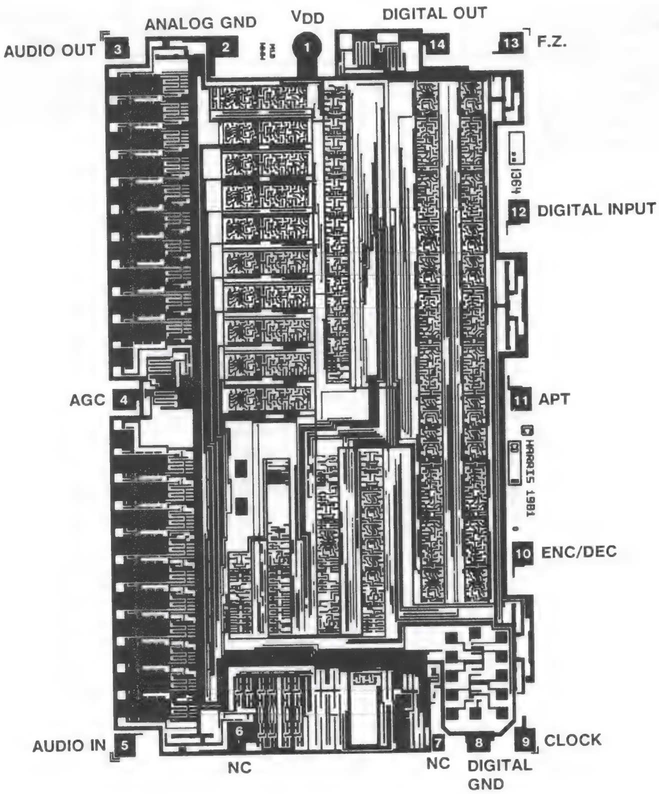
TRANSISTOR COUNT: 1896

PROCESS: CMOS; SAJI

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

Metallization Mask Layout

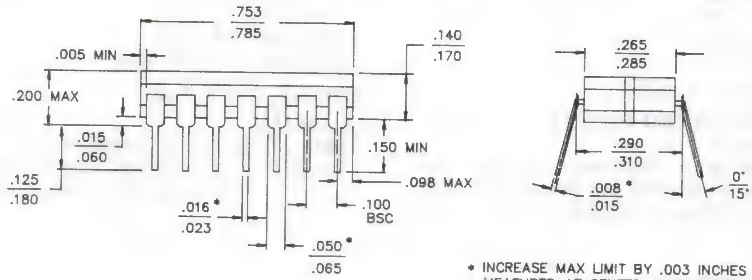
HC-55564/883



NOTE: Pad Numbers Correspond to DIP Package Only.

Packaging†

14 PIN CERAMIC DIP

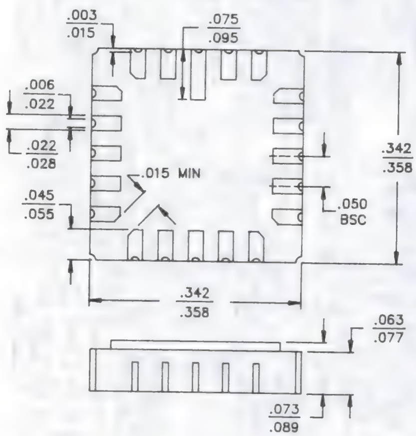


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-1

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

DESIGN INFORMATION

Continuously Variable Slope Delta-Modulator (CVSD)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance

The following typical performance distortion graphs were realized with the test configuration of Figure 1. The measurement vehicle for Total Harmonic Distortion (THD) was an HP-339A distortion measurement set, and for 2nd and 3rd harmonic distortion, an HP-3582A spectrum analyzer. All measurement conditions were at V_{DD} = +5V, and 2nd and 3rd harmonic distortion measurements were C-message filtered. 0dB = $1.2V_{RMS}$.

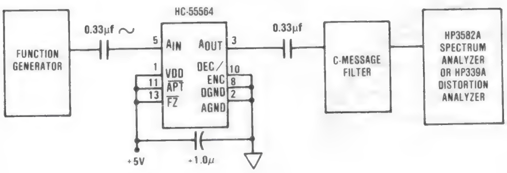


FIGURE 1. TEST AND MEASUREMENT CIRCUIT

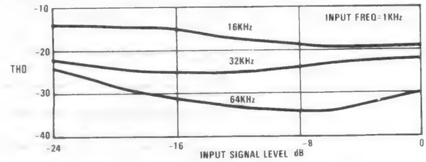


FIGURE 2. CVSD SIGNAL LEVEL vs. TOTAL HARMONIC DISTORTION

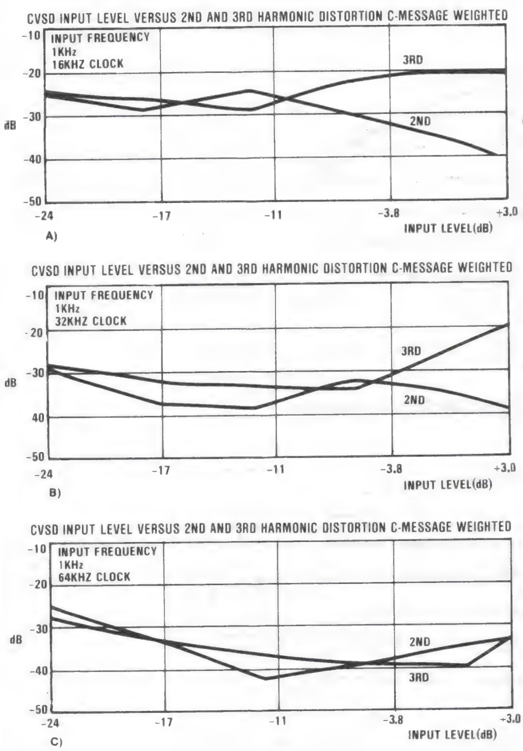


FIGURE 3A, B, C. CVSD INPUT LEVEL vs. 2ND AND 3RD HARMONIC DISTORTION

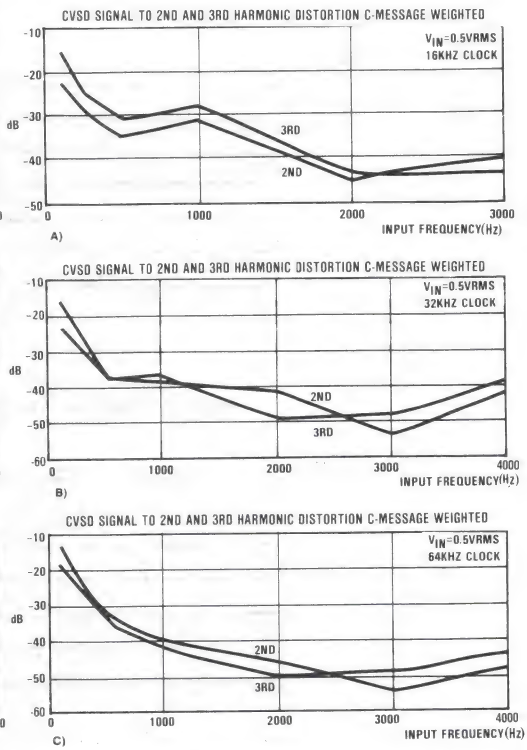


FIGURE 4A, B, C. CVSD INPUT FREQUENCY vs. 2ND AND 3RD HARMONIC DISTORTION

6

DATA CONVERSION PRODUCTS

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance (Continued)

Figures 5, 6, and 7 illustrate the typical frequency response of the HC-55564 for varying input levels and for varying sampling rates. To prevent slope overload (slew limiting), the 0dB boundry should not be exceeded. The frequency response is directly proportional to the sampling clock rate. The flat bandwidth at 0dB doubles for every 16kHz increase in sampling rate. The output levels were measured in the encode mode, without filtering, from A_{IN} to A_{OUT}, at V_{DD} = +5V, 0dB = 1.2V_{RMS}.

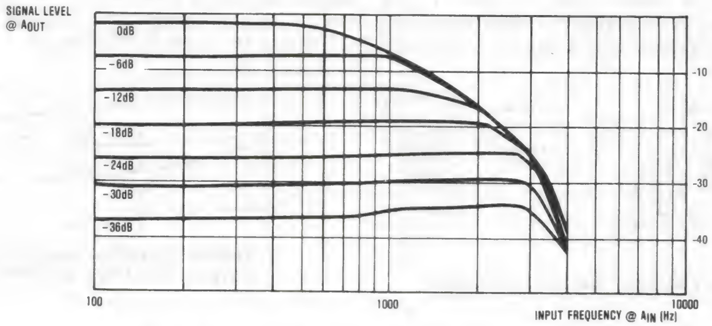


FIGURE 5. TRANSFER FUNCTION FOR CVSD AT 16Kbps

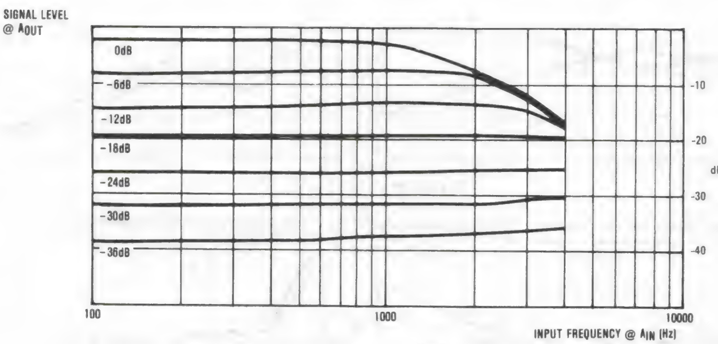


FIGURE 6. TRANSFER FUNCTION FOR CVSD AT 32Kbps

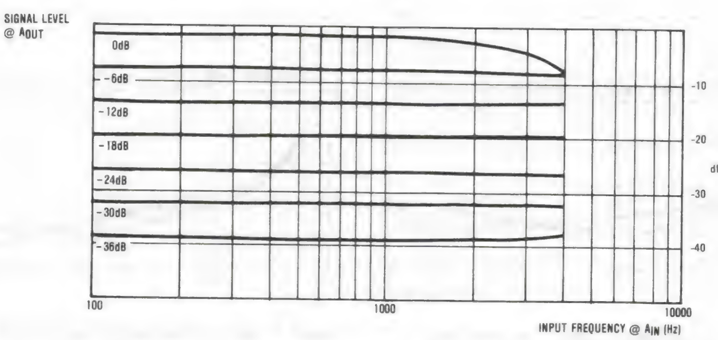


FIGURE 7. TRANSFER FUNCTION FOR CVSD AT 64Kbps

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Interface Circuit for HC-55564 CVSD

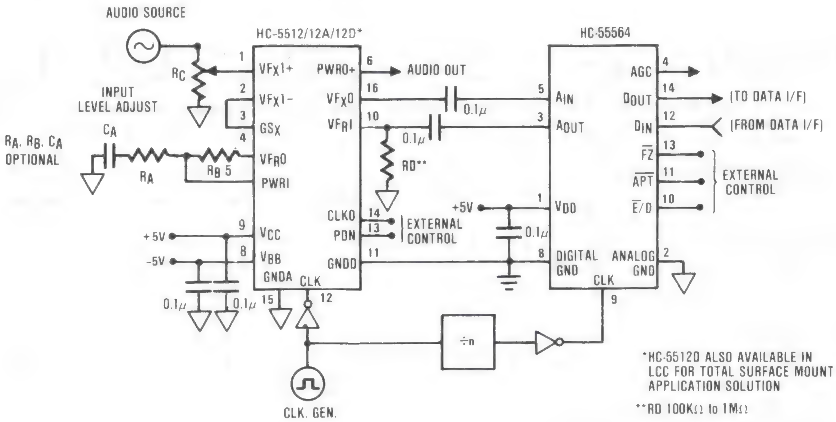
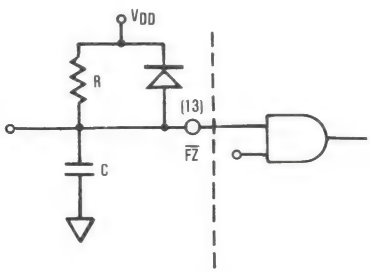


FIGURE 8.

CVSD Hookup for Evaluation

The circuit in Figure 8 is sufficient to evaluate the voice quality of the CVSD, since when encoding the feedback signal at the audio output pin is the reconstructed audio input signal. CVSD design considerations are as follows:

1. Care should be taken in layout to maintain isolation between analog and digital signal paths for proper noise consideration .
2. Power supply decoupling is necessary as close to the device as possible A 0.1μF should be sufficient.
3. Ground, then power, must be present before any input signals are applied to the CVSD. Failure to observe this may cause a latchup condition which may be destructive. Latchup may be removed by cycling the power off/on. A power-up reset circuit may be used that strobes Force Zero (Pin 13) during power-up as follows:



4. Analog (signal) ground (Pin 2) should be externally tied to Pin 8 and power ground. It is recommended that the A_{IN} and A_{OUT} ground returns connect only to Pin 2.
5. Digital inputs and outputs are compatible with standard CMOS logic using the same supply voltage. All unused logic inputs must be tied to the appropriate logic level for desired operation. TTL outputs will require 1kΩ pull-up resistors. Pins 4 and 14 will each drive CMOS logic or one low power TTL input.
6. Since the Audio Out pins are internally D.C. biased to $V_{DD}/2$, A.C. coupling is required In general, a value of 0.1μF is sufficient for A.C. coupling of the CVSD audio pins to a filter circuit.
7. The $\overline{AGC}$ output may be externally integrated to drive an $\overline{AGC}$ pre-amp, or it could drive an LED indicator through a buffer to indicate proper speaking volume.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Timing Waveforms

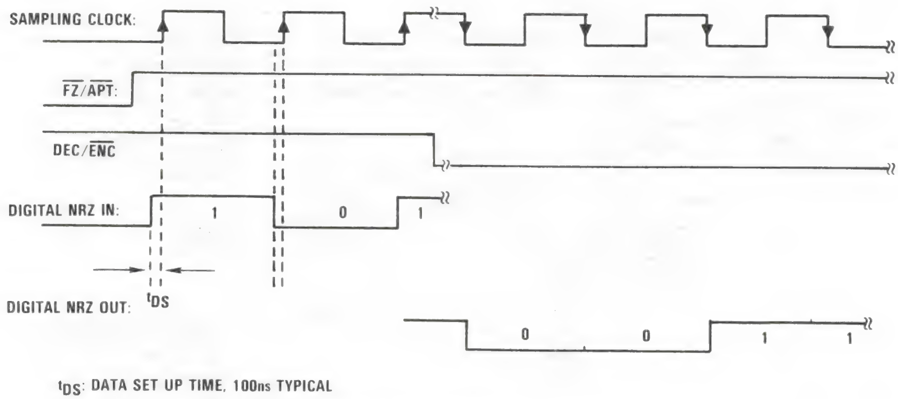
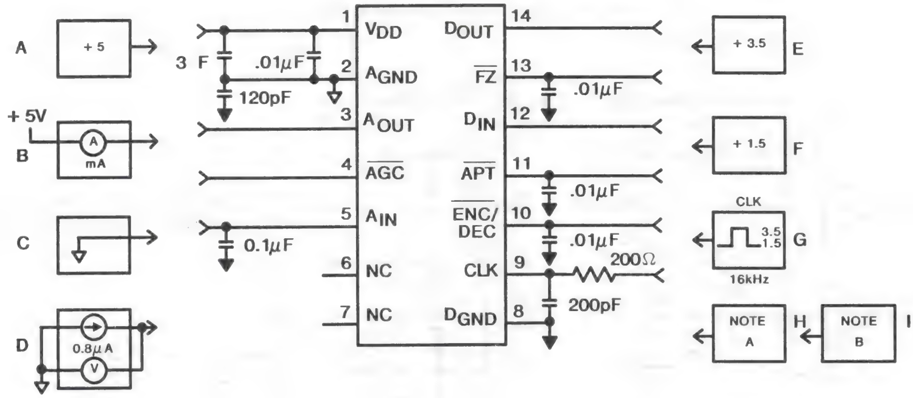


FIGURE 9. CVSD TIMING DIAGRAM

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Test Configuration



TEST NO.	TEST NAME	IC PIN NUMBERS 1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	I_{DD} Supply Current	B	NA	NA	NA	C	NA	NA	NA	G	F	E	F	E	NA
2	V_{IH} Input Logic 1	A	NA	NA	NA	NA	NA	NA	NA	G	E	E	E	E	NA
3	V_{IL} Input Logic 0	A	NA	NA	NA	NA	NA	NA	NA	G	F	F	F	F	NA
4	V_{OL} Dig Out Logic 0	A	NA	NA	D	NA	NA	NA	NA	H	E	E	F	E	D
5	V_{OL} AGC Out Logic 0	A	NA	NA	D	NA	NA	NA	NA	G	E	E	E	E	D
6	V_{OH} Dig Out Logic 1	A	NA	NA	D	NA	NA	NA	NA	I	E	E	E	E	D
7	V_{OH} AGC Out Logic 1	A	NA	NA	D	NA	NA	NA	NA	E	E	E	E	E	D

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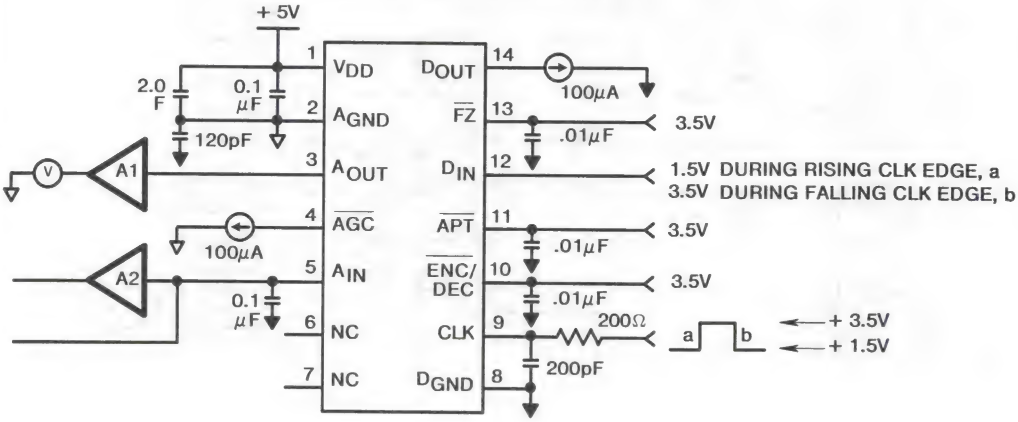
DATA CONVERSION PRODUCTS

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

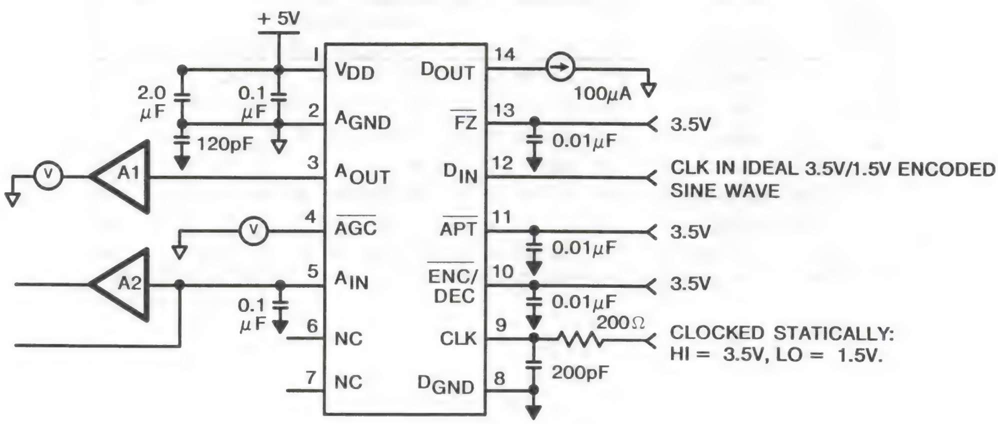
Test Configuration (Continued)

TEST: V_{QP}, QUIETING PATTERN AMPLITUDE



A1, A2 OP Amps are buffers for measurements taken at A_{IN} and A_{OUT}.
The difference in measurements at A_{OUT} when D_{IN} is HI and D_{IN} is LO is V_{QP}.

TEST: V_{ATH}, $\overline{AGC}$ THRESHOLD



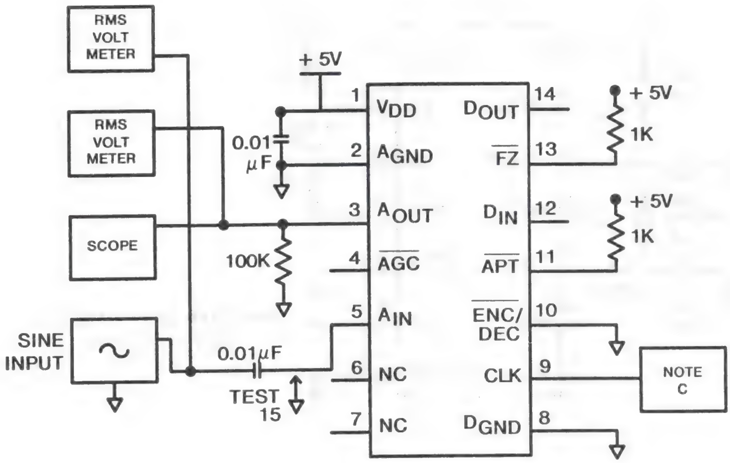
A1, A2 OP Amps are buffers for measurements taken at A_{IN} and A_{OUT}.
For each CLK Cycle, measure A_{OUT} and AGC for CLK = HI and CLK = LO.
Following A_{OUT} wave form bit by bit, $\overline{AGC}$ LO is A_{OUT} voltage where $\overline{AGC}$ output goes from HI to LO. AGC HI is A_{OUT} voltage where $\overline{AGC}$ output goes from LO back to HI. V_{ATH} is the fraction of full scale of ($\overline{AGC}$ HI - $\overline{AGC}$ LO).

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Test Configuration (Continued)

TEST: 10 THROUGH 16



TEST	TEST NAME	SINE WAVE CONDITIONS
10	Clock Sampling Rate	Sine Input 20Hz, 0.775 V_{RMS}
11	Clock Duty Cycle	Sine Input 100Hz, 0.775 V_{RMS}
12	Transfer Gain	Sine Input 100Hz, 0.775 V_{RMS}
13	Audio Input/Output (A_{IN}/A_{OUT}) Voltage Test	Sine Input 300Hz
14	Resolution	Sine Input 100Hz
15	Minimum Step Size	A_{IN} Grounded
16	Clamping Threshold	Sine Input 100Hz

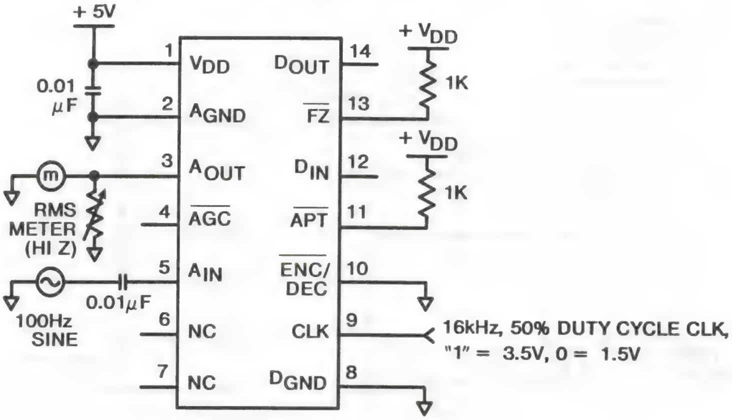
* Resistor used only on Test 10 and 11.

DESIGN INFORMATION (Continued)

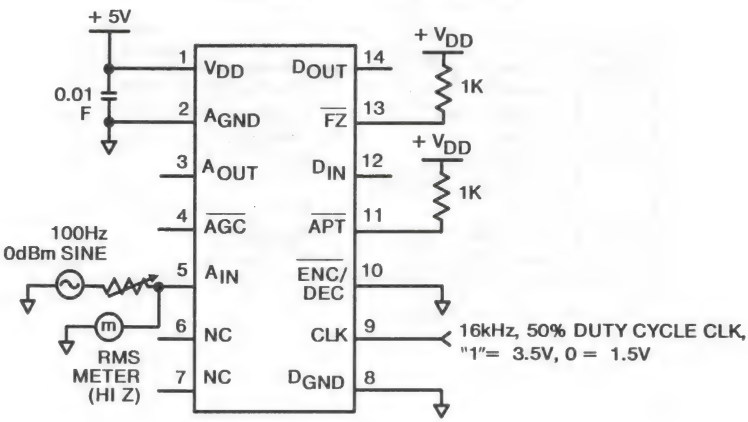
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Test Configuration (Continued)

TEST: Z_{IN}, AUDIO OUTPUT IMPEDENCE



TEST: Z_{IN}, AUDIO INPUT IMPEDENCE



NOTES:

A: Clocked statically for 3 cycles.

B: Clocked statically for 5 cycles.

C: Clock used for Clock Sampling Rate test is a variable frequency square wave.Clock used for Clock Duty Cycle test is 16kHz variable duty cycle. All levels of clock are 3.5 = high and 1.5 = low. Clock used for Transfer Gain, Audio Input/Output and Resolution test is 16kHz 50% duty cycle.

ANALOG

Sample and Hold Amplifiers

7

SAMPLE AND HOLD AMPLIFIER DATA SHEETS

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

HARRIS HA-2420/883

January 1989

Fast Sample and Hold

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Maximum Acquisition Time (10V Step to 0.1%).......4μs
  (10V Step to 0.01%).....6μs
- Maximum Drift Current (Max. Over Temp.)..........10nA
- TTL Compatible Control Input
- Power Supply Rejection ....≥ 80dB

Applications

- Data Acquisition Systems
- D to A Deglitcher
- Auto Zero Systems
- Peak Detector
- Gated Op Amp

Description

The HA-2420/883 is a monolithic circuit consisting of a high performance operational amplifier with its output in series with an ultra-low leakage analog switch and MOSFET input unity gain amplifier.

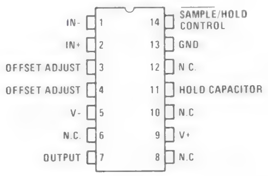
With an external hold capacitor connected to the switch output, a versatile, high performance sample-and-hold or track-and-hold circuit is formed. When the switch is closed, the device behaves as an operational amplifier, and any of the standard op amp feedback networks may be connected around the device to control gain, frequency response, etc. When the switch is opened the output will remain at its last level.

Performance as a sample-and-hold compares very favorably with other monolithic, hybrid, modular, and discrete circuits. Accuracy to better than 0.01% is achievable over the temperature range. Fast acquisition is coupled with superior droop characteristics, even at high temperatures. High slew rate, wide bandwidth, and low acquisition time produce excellent dynamic characteristics. The ability to operate at gains greater than 1 frequently eliminates the need for external scaling amplifiers.

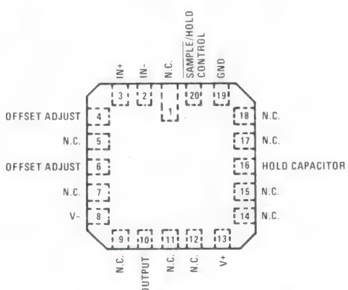
The device may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc. For more information, please see Application Note 517.

Pinouts

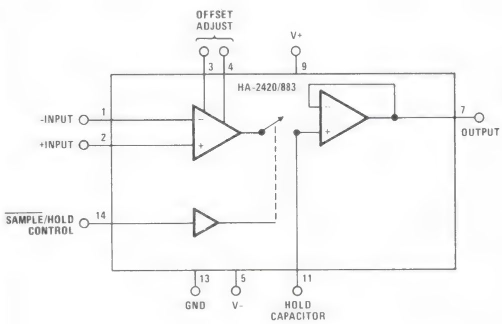
HA1-2420/883 (CERAMIC DIP)
TOP VIEW



HA4-2420/883 (CERAMIC LCC)
TOP VIEW



Functional Diagram



NOTE: Pin Numbers Correspond to DIP Package Only.

7 SAMPLE & HOLD AMPLIFIERS

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage .... ±24V
Digital Input Voltage ($\overline{S}$/H Pin) .... +8V, -15V
Output Current .... Short Circuit Protected
Storage Temperature Range .... $-65^oC < T_A < +150^oC$
Lead Temperature (Soldering 10 Seconds) .... 275^oC
Junction Temperature .... $+175^oC$
Thermal Resistance, Junction-to-Case (θ_{jc})
Ceramic DIP Package .... $24^oC/W$
Ceramic LCC Package .... $20^oC/W$
Thermal Resistance, Junction-to-Ambient (θ_{ja})
Ceramic DIP Package .... $96^oC/W$
Ceramic LCC Package .... $88^oC/W$
Power Dissipation
Ceramic DIP Package .... 1.03W @ $+75^oC$
Ceramic LCC Package .... 1.14W @ $+75^oC$
Power Dissipation Derating Factor (Above $+75^oC$)
Ceramic DIP Package .... $10mW/^oC$
Ceramic LCC Package .... $11.4mW/^oC$
ESD Classification .... ≤ 2000V

Recommended Operating Conditions

Operating Temperature Range .... $-55^oC < T_A < +125^oC$
Operating Supply Voltage ($\pm V_{SUPPLY}$) .... ±15V
Analog Input Voltage (V_S) .... ±10V
Logic Level Low (V_{IL}) .... 0V to 0.8V
Logic Level High (V_{IH}) .... 2.0V to 5.0V

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at V+ = +15V; V- = -15V; V_{IL} = 0.8V (Sample); V_{IH} = 2.0V (Hold); C_H = 1000pF, -Input Tied to Output, Unless Otherwise Specified

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}		1	$+25^oC$	-4	4	mV
			2, 3	$-55^oC, +125^oC$	-6	6	mV
Input Bias Current	I_{B+}		1	$+25^oC$	-200	200	nA
			2, 3	$-55^oC, +125^oC$	-400	400	nA
	I_{B-}		1	$+25^oC$	-200	200	nA
			2, 3	$-55^oC, +125^oC$	-400	400	nA
Input Offset Current	I_{IO}		1	$+25^oC$	-50	50	nA
			2, 3	$-55^oC, +125^oC$	-100	100	nA
Open Loop Voltage Gain	$+A_{VS}$	$R_L = 2k\Omega$, C_L = 50pF,	1	$+25^oC$	25k	—	V/V
		V_{OUT} = +10V	2, 3	$-55^oC, +125^oC$	25k	—	V/V
	$-A_{VS}$	$R_L = 2k\Omega$, C_L = 50pF,	1	$+25^oC$	25k	—	V/V
		V_{OUT} = -10V	2, 3	$-55^oC, +125^oC$	25k	—	V/V
Common Mode Rejection Ratio	-CMRR	V+ = 25V, V- = -5V,	1	$+25^oC$	80	—	dB
		V_{OUT} = +10V, $V_{\overline{S}/H}$ = 10.8V	2, 3	$-55^oC, +125^oC$	80	—	dB
	+CMRR	V+ = 5V, V- = -25V,	1	$+25^oC$	80	—	dB
		V_{OUT} = -10V, $V_{\overline{S}/H}$ = -9.2V	2, 3	$-55^oC, +125^oC$	80	—	dB
Output Current	$+I_O$	V_{OUT} = +10V	1	$+25^oC$	+15.0	—	mA
	$-I_O$	V_{OUT} = -10V	1	$+25^oC$	-15.0	—	mA
Output Voltage Swing	$+V_{OP}$	$R_L = 2k\Omega$, C_L = 50pF	1	$+25^oC$	+10.0	—	V
			2, 3	$-55^oC, +125^oC$	+10.0	—	V
	$-V_{OP}$	$R_L = 2k\Omega$, C_L = 50pF	1	$+25^oC$	—	-10.0	V
			2, 3	$-55^oC, +125^oC$	—	-10.0	V
Power Supply Current	$+I_{CC}$		1	$+25^oC$	—	5.5	mA
	$-I_{CC}$		1	$+25^oC$	-3.5	—	mA
Power Supply Rejection Ratio	+PSRR	V+ = 10V, 20V	1	$+25^oC$	80	—	dB
		V- = -15V, -15V	2, 3	$-55^oC, +125^oC$	80	—	dB
	-PSRR	V+ = 15V, 15V	1	$+25^oC$	80	—	dB
		V- = -10V, -20V	2, 3	$-55^oC, +125^oC$	80	—	dB
Digital Input Current	I_{IN1}	V_{IN1} = 0V	1	$+25^oC$	—	800	μA
			2, 3	$-55^oC, +125^oC$	—	800	μA
	I_{IN2}	V_{IN2} = 5.0V	1	$+25^oC$	—	20	μA
			2, 3	$-55^oC, +125^oC$	—	20	μA
Digital Input Voltage	V_{IL}		1	$+25^oC$	—	0.8	V
			2, 3	$-55^oC, +125^oC$	—	0.8	V
	V_{IH}		1	$+25^oC$	2.0	—	V
			2, 3	$-55^oC, +125^oC$	2.0	—	V
Drift Current	I_D	V_{IN} = 0V, $R_L = 2k\Omega$, C_L = 50pF, $\overline{S}$/H = 4.0V	2	$+125^oC$	-10	10	nA

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at V+ = +15V, V- = -15V, V_{IL} = 0.8V (Sample), V_{IH} = 2.0V (Hold), C_H = 1000pF, -Input Tied to Output, Unless Otherwise Specified

A.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMP	LIMITS MIN	LIMITS MAX	UNITS
Hold Step Error	V_{ERROR}	V_{IN} = 0V, 4V, $t_{rise}(V_{\overline{S}/H})$ = 30ns	4	+25°C	-20	20	mV
Transient Response Rise Time & Fall Time	$TR_{(tr)}$	C_L = 50pF, R_L = 2kΩ, A_V = +1, V_{OUT} = 200mV peak-to-peak	4	+25°C	—	100	ns
	$TR_{(tf)}$	C_L = 50pF, R_L = 2kΩ, A_V = +1, V_{OUT} = 200mV peak-to-peak	4	+25°C	—	100	ns
Transient Response Overshoot	$TR_{(+OS)}$	C_L = 50pF, R_L = 2kΩ, A_V = +1, V_{OUT} = 200mV peak-to-peak	4	+25°C	—	40	%
	$TR_{(-OS)}$	C_L = 50pF, R_L = 2kΩ, A_V = +1, V_{OUT} = 200mV peak-to-peak	4	+25°C	—	40	%
Transient Response Slew Rate	$TR_{(+SR)}$	C_L = 50pF, R_L = 2kΩ, A_V = +1, V_{OUT} = 10V peak-to-peak	4	+25°C	3.5	—	V/μs
	$TR_{(-SR)}$	C_L = 50pF, R_L = 2kΩ, A_V = +1, V_{OUT} = 10V peak-to-peak	4	+25°C	3.5	—	V/μs

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at V+ = +15V, V- = -15V, V_{IL} = 0.8V (Sample), V_{IH} = 2.0V (Hold), C_H = 1000pF, -Input Tied to Output, Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMP	LIMITS MIN	LIMITS MAX	UNITS
Hold Mode Feedthru Attentuation	V_{atten}	R_L = 2kΩ, C_L = 50pF, A_V = +1, V_{IN} = $20V_{p-p}$, f_{IN} = 50kHz	1	+25°C, -55°C, +125°C	70	—	dB
Gain Bandwidth Product	GBWP	R_L = 2kΩ, C_L = 50pF, A_V = +1, V_{IN} = $100mV_{p-p}$	1	+25°C,	2.5	—	MHz
Acquisition Time (0.1%)	$+t_{acq}$ (0.1%)	R_L = 2kΩ, C_L = 50pF, A_V = +1, V_{OUT} = 0V, +10V	1	+25°C,	—	4	μs
	$-t_{acq}$ (0.1%)	R_L = 2kΩ, C_L = 50pF, A_V = +1, V_{OUT} = 0V, -10V	1	+25°C,	—	4	μs
Acquisition Time (0.01%)	$+t_{acq}$ (0.01%)	R_L = 2kΩ, C_L = 50pF, A_V = +1, V_{OUT} = 0V, +10V	1	+25°C,	—	6	μs
	$-t_{acq}$ (0.01%)	R_L = 2kΩ, C_L = 50pF, A_V = +1, V_{OUT} = 0V, -10V	1	+25°C,	—	6	μs

NOTE: 1. The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1, 2 & 3)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 4
Group A Test Requirements	1, 2, 3, 4
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Test Circuits

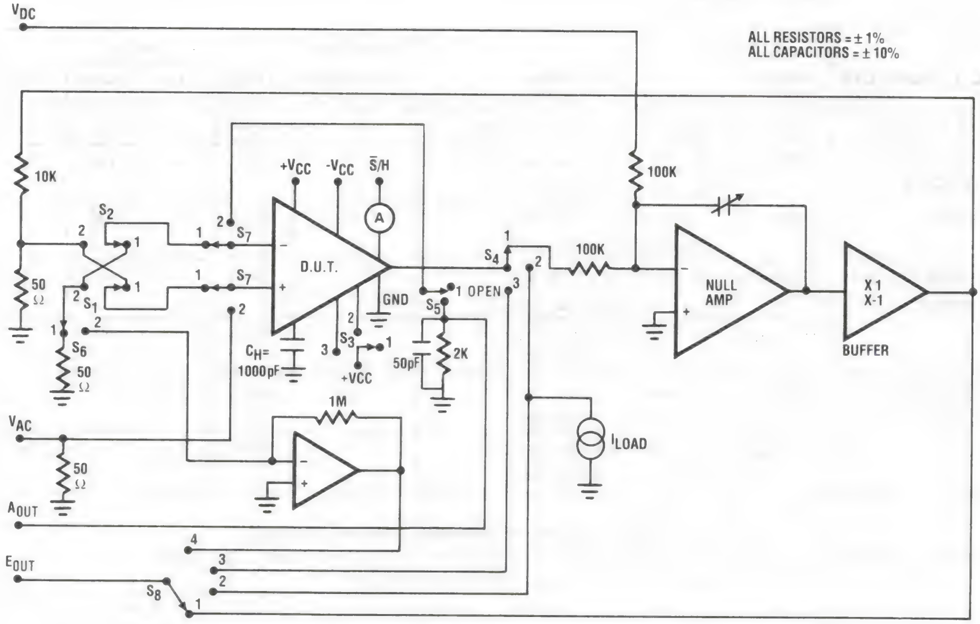
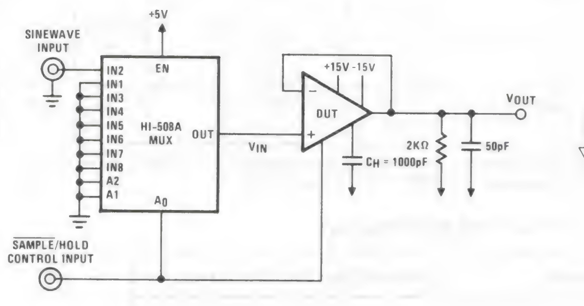


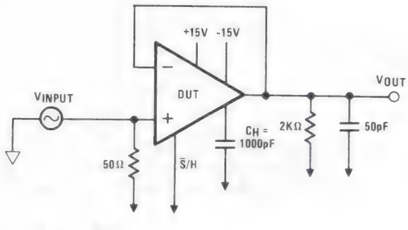
FIGURE 1.

Test Fixture Schematic (Switch Positions S_1 - S_8 Determine Configuration. See Chart A)

HOLD MODE FEEDTHROUGH ATTENUATION



GAIN BANDWIDTH PRODUCT



NOTE:
Compute Hold Mode Feedthrough Attenuation from the Formula:

$$\text{Feedthrough Attenuation} = 20 \log \left(\frac{V_{OUT}\ \text{HOLD}}{V_{IN}\ \text{HOLD}} \right)$$

Where V_{OUT} HOLD = Peak-Peak Value of Output Sinewave During the Hold Mode

GBWP is the Frequency of V_{INPUT} at which:

$$20 \log \left(\frac{V_{OUT}}{V_{INPUT}} \right) = -3\text{dB}$$

CHART A. TEST CIRCUIT CONDITIONS (SEE TEST CIRCUIT — FIGURE 1)

PARAMETER	NOTES	APPLY (IN VOLTS DC)					SWITCH POSITION								MEASURE		MEASURED PARAMETER	
		+V	-V	VDC	S/H	E_{OUT}	S1	S2	S3	S4	S5	S6	S7	S8	VALUE	UNITS	EQUATION	UNITS
V_{IO}		15	-15	0	0.8	—	1	1	1	1	1	1	1	1	E1	V	V_{IO} = E1/200	mV
I_{IO}		15	-15	0	0.8	—	—	—	—	—	—	—	—	—		V	$I_{IO} = (E7-E10)/10^6$	nA
I_{B+}		15	-15	0	0.8	—	2	2	1	1	1	2	1	4	E7	V	$I_{B+} = E7/10^6$	nA
I_{B-}		15	-15	0	0.8	—	1	1	1	1	1	2	1	4	E10	V	$I_{B-} = E10/10^6$	nA
$+A_{VS}$	1	15	-15	0	0.8	—	1	1	1	1	2	1	1	1	E25	V	$+A_{VS} = 20\log_{10}$ [(E25-E26)/200]	dB
	1	15	-15	-10	0.8	—	1	1	1	1	2	1	1	1	E26	V		
$-A_{VS}$	1	15	-15	0	0.8	—	1	1	1	1	2	1	1	1	E27	V	$-A_{VS} = 20\log_{10}$ [(E27-E28)/200]	dB
	1	15	-15	+10	0.8	—	1	1	1	1	2	1	1	1	E28	V		
-CMRR	4	25	-5	-10	10.8	—	1	1	1	1	1	1	1	1	E17	V	$-CMRR = 20\log_{10}$ [10/((E1-E17)/200)]	dB
+CMRR	5	5	-25	+10	-9.2	—	1	1	1	1	1	1	1	1	E18	V	$+CMRR = 20\log_{10}$ [10/((E1-E18)/200)]	dB
$+I_O$		15	-15	-13	0.8	10	1	1	1	3	1	1	1	3	I21	mA	$+I_O$ = I21	mA
$-I_O$		15	-15	+13	0.8	-10	1	1	1	3	1	1	1	3	I22	mA	$-I_O$ = I22	mA
$+V_{OP}$	1	15	-15	-14	0.8	—	1	1	1	3	2	1	1	3	E23	V	$+V_{OP}$ = E23	V
$-V_{OP}$	1	15	-15	+14	0.8	—	1	1	1	3	2	1	1	3	E24	V	$-V_{OP}$ = E24	V
$+I_{CC}$		15	-15	0	0.8	—	1	1	1	1	1	1	1	1		mA		mA
$-I_{CC}$		15	-15	0	0.8	—	1	1	1	1	1	1	1	1		mA		mA
+PSRR		10	-15	0	0.8	—	1	1	1	1	1	1	1	1	E13	V	$+PSRR = 20\log_{10}$ [10/(E13-E14)]	dB
		20	-15	0	0.8	—	1	1	1	1	1	1	1	1	E14	V		
-PSRR		15	-10	0	0.8	—	1	1	1	1	1	1	1	1	E15	V	$-PSRR = 20\log_{10}$ [10/(E15-E16)]	dB
		15	-20	0	0.8	—	1	1	1	1	1	1	1	1	E16	V		
I_{IN1}		15	-15	0	0	—	1	1	1	1	1	1	1	1	$I_{S/H}$	μA		μA
I_{IN2}		15	-15	0	5	—	1	1	1	1	1	1	1	1	$I_{S/H}$	μA		μA
I_D	1, 6	15	-15	0	4.0	—	1	1	1	3	2	1	2	1	A_{OUT}	mV	$I_D = C_H \times \Delta V/\Delta T$	nA
Hold Step Error	1, 6	15	-15	0	0	—	1	1	1	3	2	1	2	1	A_{OUT1}	mV	$V_{error} = \lvert A_{OUT1}-A_{OUT2}\rvert$	mV
		15	-15	0	4.0	—	1	1	1	3	2	1	2	1	A_{OUT2}	mV		
$TR_{(tr)}$	2	15	-15	—	0.8	—	1	1	1	3	2	1	2	1	A_{OUT}	See Notes	$TR_{(tr)}$ = 10% to 90%	ns
$TR_{(tf)}$	2	15	-15	—	0.8	—	1	1	1	3	2	1	2	1	A_{OUT}	See Notes	$TR_{(tf)}$ = 90% to 10%	ns
$TR_{(+OS)}$	2	15	-15	—	0.8	—	1	1	1	3	2	1	2	1	A_{OUT}	See Notes	$TR_{(+OS)} = (V_{peak}-V_{final})/V_{final} \times 100$	%
$TR_{(-OS)}$	2	15	-15	—	0.8	—	1	1	1	3	2	1	2	1	A_{OUT}	See Notes	$TR_{(-OS)} = (V_{peak}-V_{final})/V_{final} \times 100$	%
$TR_{(+SR)}$	3	15	-15	—	0.8	—	1	1	1	3	2	1	2	1	A_{OUT}	See Notes	$TR_{(+SR)} = \Delta V/\Delta T$	V/μs
$TR_{(-SR)}$	3	15	-15	—	0.8	—	1	1	1	3	2	1	2	1	A_{OUT}	See Notes	$TR_{(-SR)} = \Delta V/\Delta T$	V/μs

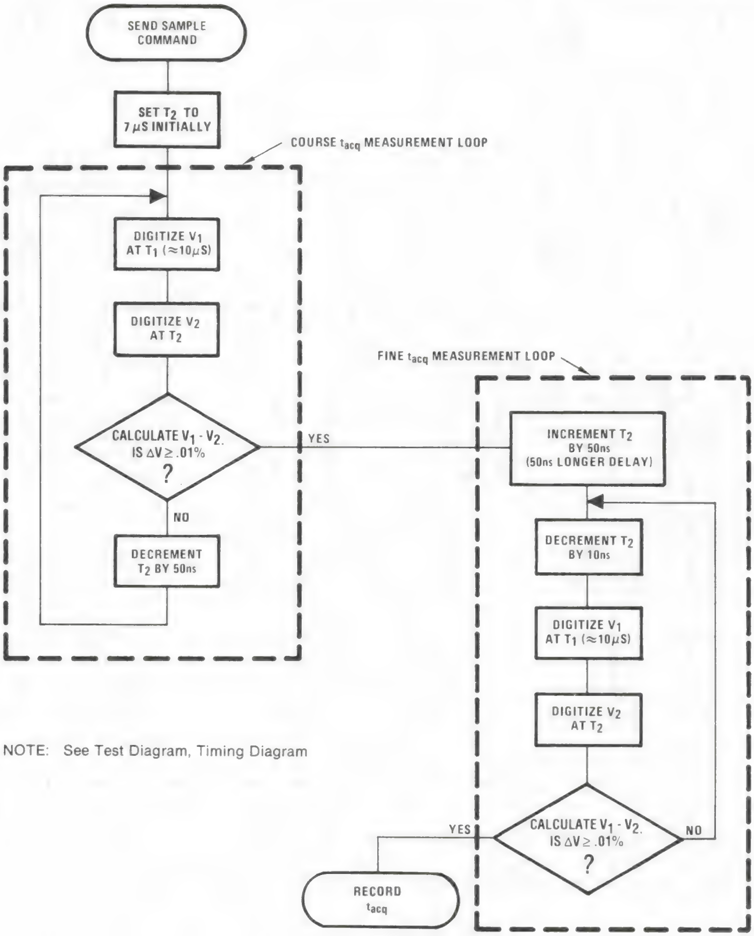
NOTES:
1. $R_{LDC} = 2k\Omega$
2. $V_{OUT} = 200mV_{p-p}$, $R_L = 2k\Omega$, $C_L = 50pF$
3. V_{OUT} = 10V Step, $R_L = 2k\Omega$, $C_L = 50pF$
4. Package GND held at +10V for this test.
5. Package GND held at -10V for this test.
6. $V_{AC} = 0V$

SAMPLE & HOLD AMPLIFIERS 7

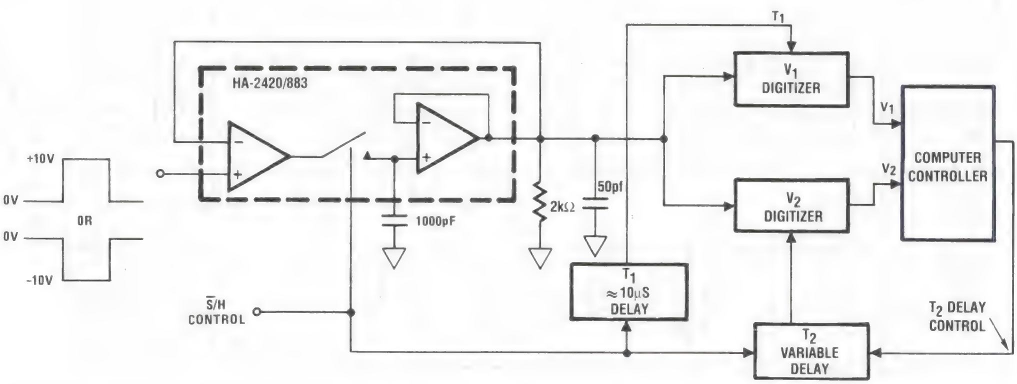
Test Circuits (Continued)

ACQUISITION TIME

(t_{acq} to 0.01% is shown, t_{acq} to 0.1% is done in the same manner)

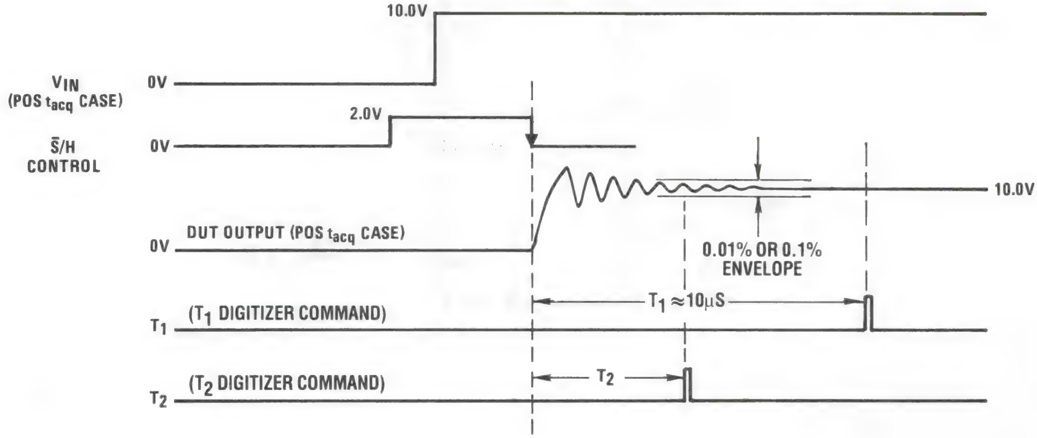


NOTE: See Test Diagram, Timing Diagram

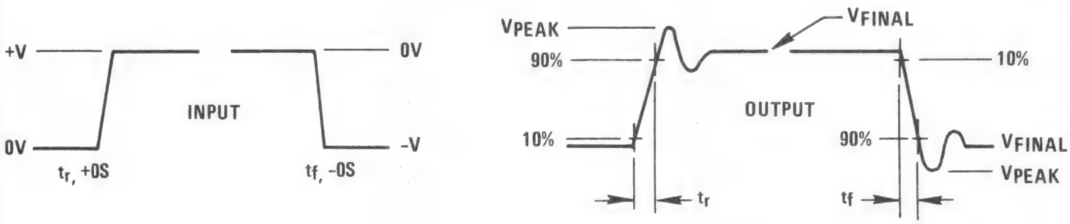


Timing Waveforms

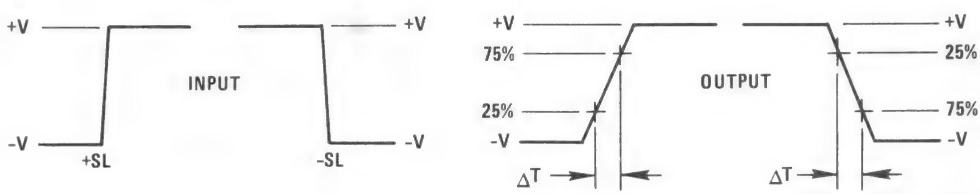
TIMING DIAGRAM FOR ACQUISITION TIME, (POSITIVE t_{acq} CASE)



OVERSHOOT, RISE & FALL TIME WAVEFORMS

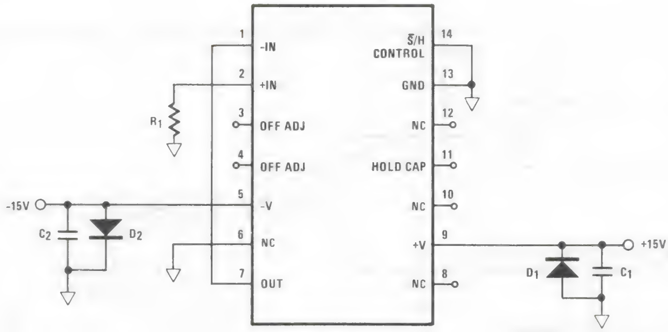


SLEW RATE WAVEFORMS



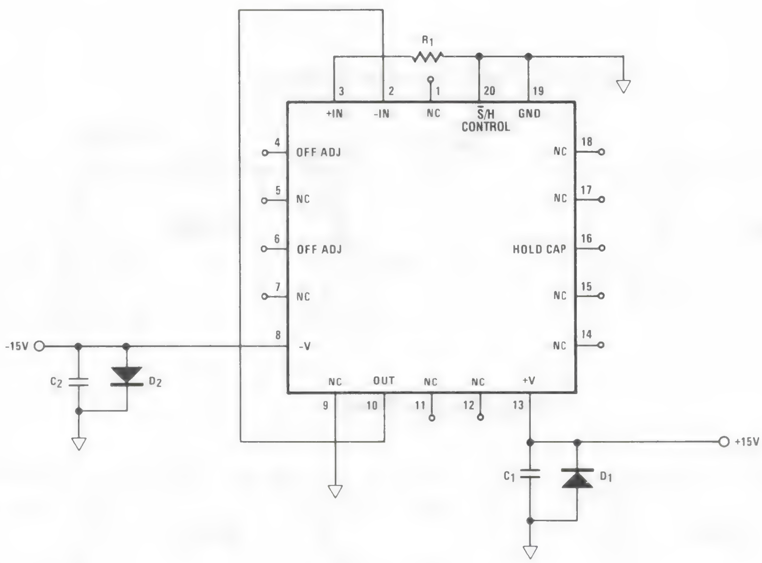
Burn-In Circuits

HA-2420/883 (CERAMIC DIP)



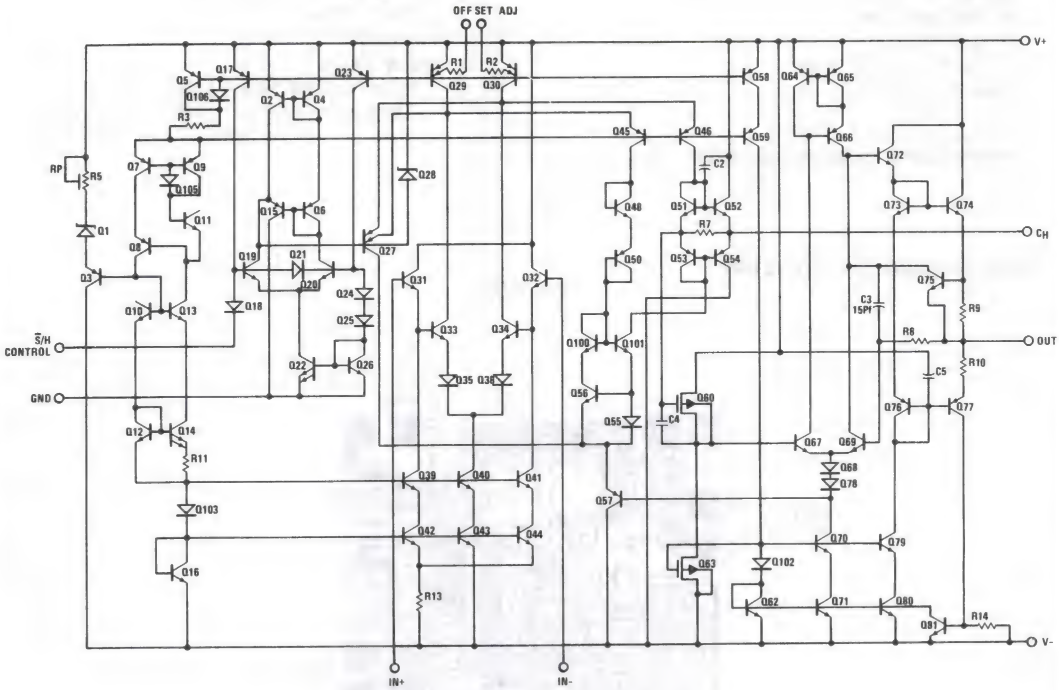
R_1 = 100kΩ, ±5% (per socket)
C_1 = C_2 = 0.1μF (one per row) or
0.01μF (one per socket)
D_1 = D_2 = 1N4002 or equivalent (per board)

HA-2420/883 (CERAMIC LCC)



R_1 = 100kΩ, ±5% (per socket)
C_1 = C_2 = 0.1μF (one per row) or
0.01μF (one per socket)
D_1 = D_2 = 1N4002 or equivalent (per board)

Schematic Diagram



7

SAMPLE & HOLD AMPLIFIERS

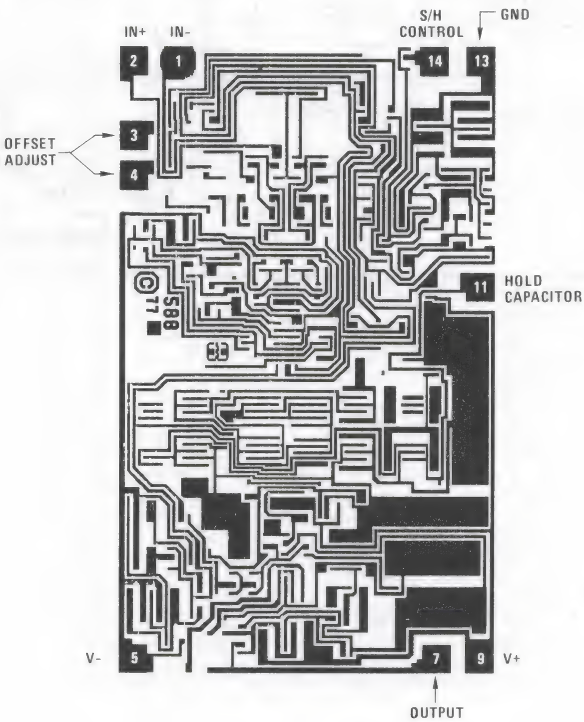
Die Characteristics

DIE DIMENSIONS: 97 x 61 x 19 mils
METALLIZATION
Type: Al
Thickness: 16kÅ ± 2kÅ
GLASSIVATION
Type: Silox
Thickness: 14kÅ ± 2kÅ
WORST CASE CURRENT DENSITY: 1.7×10^5 A/cm^2

TRANSISTOR COUNT:
HA-2420/883 78
PROCESS: Bipolar-DI
DIE ATTACH
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

Metallization Mask Layout

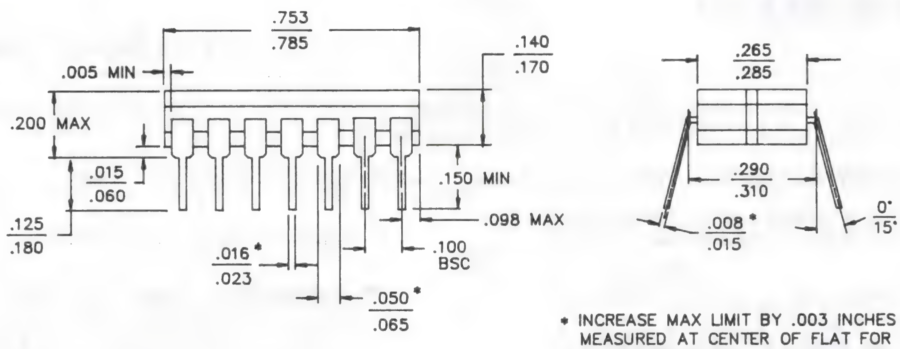
HA-2420/883



NOTE: Pad Numbers Correspond to DIP Package Only.

Packaging†

14 PIN CERAMIC DIP

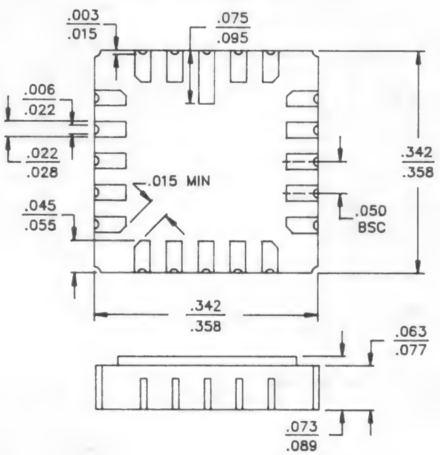


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-1

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in inches.

† MIL-M-38510 Compliant Materials, Finishes & Dimensions.

HARRIS

HA-2420

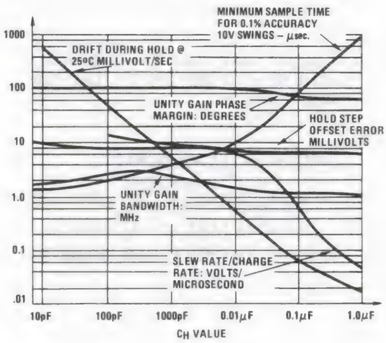
DESIGN INFORMATION

Fast Sample and Hold

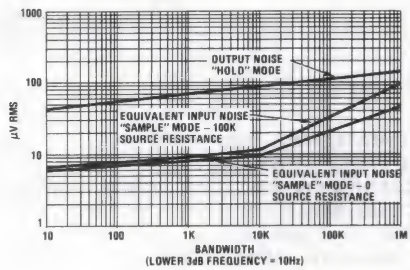
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: V_{SUPPLY} = ±15VDC, T_A = +25°C, C_H = 1000pF

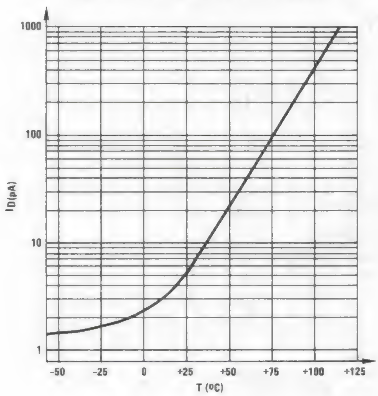
TYPICAL SAMPLE AND HOLD PERFORMANCE AS A FUNCTION OF HOLDING CAPACITOR



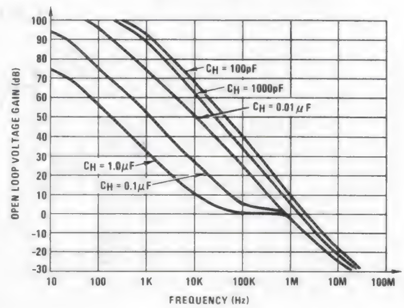
BROADBAND NOISE CHARACTERISTICS



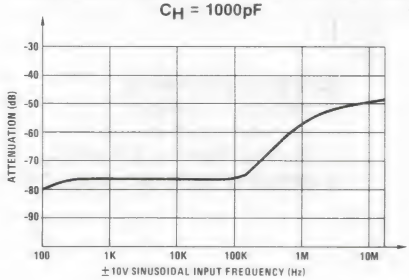
DRIFT CURRENT vs. TEMPERATURE



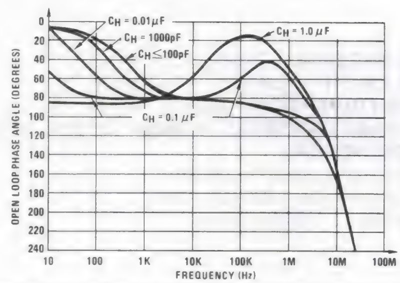
OPEN LOOP FREQUENCY RESPONSE



HOLD MODE FEEDTHROUGH ATTENTUATION C_H = 1000pF



OPEN LOOP PHASE RESPONSE



DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Offset and Gain Adjustment

HOLD STEP vs. INPUT VOLTAGE

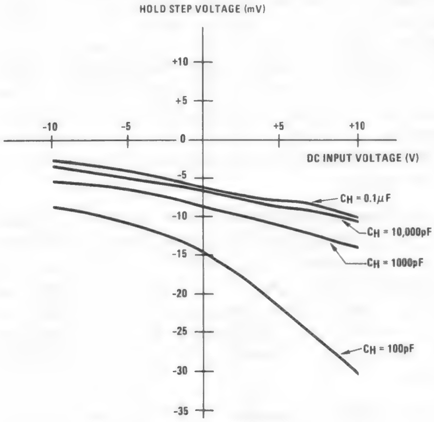


FIGURE 1.

BASIC SAMPLE-AND-HOLD
(TOP VIEW)

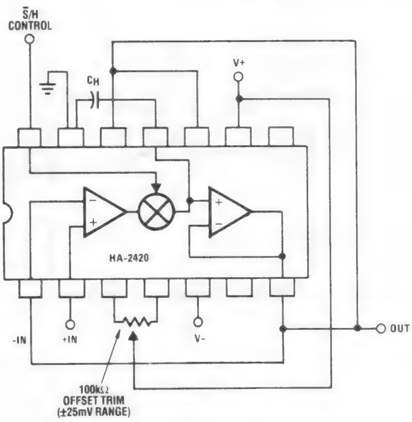


FIGURE 2.

OFFSET ADJUSTMENT

The offset voltage of the HA-2420 may be adjusted using a 100kΩ trim pot, as shown in Figure 2. The recommended adjustment procedure is:

1. Apply zero volts to the sample-and-hold input, and a square wave to the S̄/H control.
2. Adjust the trim pot for zero volts output in the hold mode.

GAIN ADJUSTMENT

The linear variation in pedestal voltage with sample-and-hold input voltage causes a -0.06% gain error (C_H = 1000pF). In some applications (D/A deglitcher, A/D converter) the gain error can be adjusted elsewhere in the system, while in other applications it must be adjusted at the sample-and-hold. The two circuits shown below demonstrate how to adjust gain error at the sample-and-hold.

The recommended procedure for adjusting gain error is:

1. Perform offset adjustment.
2. Apply the nominal input voltage that should produce a +10V output.
3. Adjust the trim pot for +10V output in the hold mode.
4. Apply the nominal input voltage that should produce a -10V output.
5. Measure the output hold voltage ($V_{-10\ NOMINAL}$). Adjust the trim pot for an output hold voltage of

$$\frac{(V_{-10\ NOMINAL}) + (-10V)}{2}$$

INVERTING CONFIGURATION

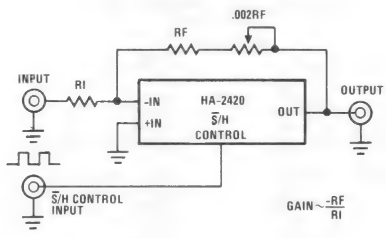


FIGURE 3.

NONINVERTING CONFIGURATION

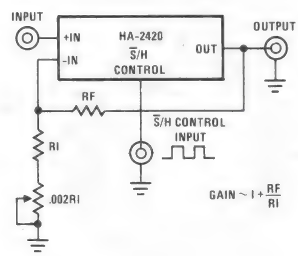


FIGURE 4.

HARRIS

HA-5330/883

Very High Speed Precision Monolithic Sample and Hold Amplifier

January 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragragh 1.2.1
- Maximum Acquisition (10V Step to 0.1%) 500ns
  (10V Step to 0.01%) 900ns
- TTL Compatible Control Input
- Power Supply Rejection .... ≥86dB
- Low Droop Rate (Max at +125°C) 100μV/μs
- Wide Supply Range .... ±11V to ±18V
- Internal Hold Capacitor
- Low Output Resistance

Applications

- Precision Data Acquisition Systems
- D/A Converter Deglitching
- Auto-Zero Circuits
- Peak Detectors

Description

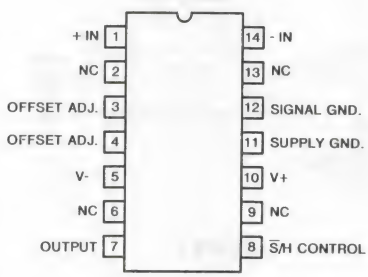
The HA-5330/883 is a very fast sample and hold amplifier designed primarily for use with high speed A/D converters. It utilizes the Harris Dielectric Isolation process to achieve a 900ns acquisition time to 12-bit accuracy and a droop rate of 100μV/μs at +125°C. The circuit consists of an input transconductance amplifier capable of producing large amounts of charging current, a low leakage analog switch, and an integrating output stage which includes a 90pF hold capacitor.

The analog switch operates into a virtual ground, so charge injection on the hold capacitor is constant and independent of V_{IN}. Charge injection is held to a low value by compensation circuits and, if necessary, the resulting 0.5mV (TYP) hold step error can be adjusted to zero via the Offset Adjust terminals. Compensation is also used to minimize leakage currents which cause voltage droop in the Hold mode.

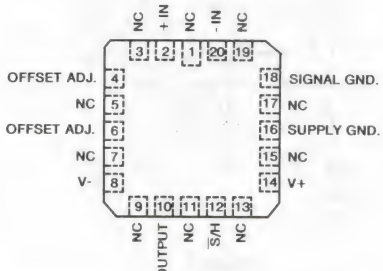
The HA-5330/883 will operate at reduced supply voltages (to ±11V) with a reduced signal range. This monolithic device is available in a Ceramic 14-pin DIP, and a 20 pad Ceramic LCC package.

Pinouts

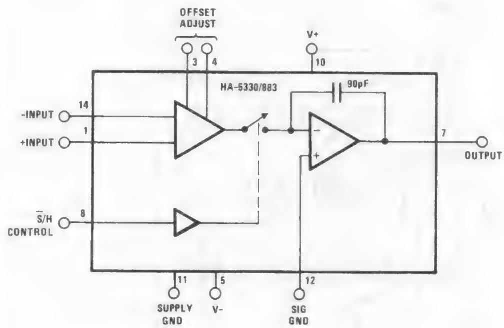
HA1-5330/883 (CERAMIC DIP)
TOP VIEW



HA4-5330/883 (CERAMIC LCC)
TOP VIEW



Functional Diagram



NOTE: Pin Numbers Correspond to DIP Package Only.

Absolute Maximum Ratings

Voltage Between V+ and Supply/Signal GND .... +20V
Voltage Between V- and Supply/Signal GND .... -20V
Voltage Between Supply GND and Signal GND .... ±2.0V
Differential Input Voltage .... ±24V
Digital Input Voltage ($\overline{S}$/H Pin) .... +8V, -6V
Output Current (Note 1) 17mA
Storage Temperature Range .... $-65^oC < T_A < +150^oC$
Lead Temperature (Soldering 10 Seconds) .... +275°C
Junction Temperature .... +175°C
ESD Classification .... < 2000V

NOTE: 1. Internal power dissipation may limit output current below ±17mA.

Thermal Information

Thermal Resistance, Junction-to-Ambient (θ_{jc})
Ceramic DIP Package .... 15°C/W
Ceramic LCC Package .... 19°C/W
Thermal Resistance, Junction-to-Ambient (θ_{ja})
Ceramic DIP Package .... 75°C/W
Ceramic LCC Package .... 76°C/W
Power Dissipation (at +75°C)
Ceramic DIP Package 1.33W
Ceramic LCC Package 1.32W
Power Dissipation Derating Factor (Above +75°C)
Ceramic DIP Package .... 13.3W mW/°C
Ceramic LCC Package .... 13.2W mW/°C

Recommended Operating Conditions

Operating Temperature Range .... $-55^oC < T_A < +125^oC$
Operating Supply Voltage (V_{SUPPLY}) .... ±15V
Analog Input Voltage (V_S) .... ±10V
Logic Level Low (V_{IL}) .... 0V to 0.8V
Logic Level High (V_{IH}) .... 2.0V to 5.0V

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at V+ = +15V; V- = -15V; V_{IL} = 0.8V (Sample); V_{IH} = 2.0V (Hold); C_H = Internal = 90pF, -Input Tied to Output, SIG. GND = SUPPLY GND; Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}		1	+25°C	-2	2	mV
			2, 3	+125°C, -55°C	-2	2	mV
Input Bias Current	I_B+		1	+25°C	-500	500	nA
			2, 3	+125°C, -55°C	-500	500	nA
	I_B-		1	+25°C	-500	500	nA
			2, 3	+125°C, -55°C	-500	500	nA
Input Offset Current	I_{IO}		1	+25°C	-500	500	nA
			2, 3	+125°C, -55°C	-500	500	nA
Open Loop Voltage Gain	$+A_{VOL}$	R_L = 1kΩ	1	+25°C	2×10^6	-	V/V
		V_{OUT} = +10V	2, 3	+125°C, -55°C	2×10^6	-	V/V
	$-A_{VOL}$	R_L = 1kΩ	1	+25°C	2×10^6	-	V/V
		V_{OUT} = -10V	2, 3	+125°C, -55°C	2×10^6	-	V/V
Common Mode Rejection Ratio	-CMRR	V+ = 25V, V- = -5V	1	+25°C	86	-	dB
		V_{OUT} = 10V, $V_{\overline{S}/H}$ = 10.8V	2, 3	+125°C, -55°C	86	-	dB
	+CMRR	V+ = 5V, V- = -25V	1	+25°C	86	-	dB
		V_{OUT} = -10V, $V_{\overline{S}/H}$ = -9.2V	2, 3	+125°C, -55°C	86	-	dB
Output Current	$+I_O$	V_{OUT} = +10V	1	+25°C	10	-	mA
			2, 3	+125°C, -55°C	10	-	mA
	$-I_O$	V_{OUT} = -10V	1	+25°C	-	-10	mA
			2, 3	+125°C, -55°C	-	-10	mA
Output Voltage Swing	$+V_{OUT}$	R_L = 1kΩ	1	+25°C	+10.0	-	V
			2, 3	+125°C, -55°C	+10.0	-	V
	$-V_{OUT}$	R_L = 1kΩ	1	+25°C	-	-10.0	V
			2, 3	+125°C, -55°C	-	-10.0	V
Power Supply Current	$+I_{CC}$		1	+25°C	-	22	mA
			2, 3	+125°C, -55°C	-	22	mA
	$-I_{CC}$		1	+25°C	-23	-	mA
			2, 3	+125°C, -55°C	-23	-	mA
Power Supply Rejection Ratio	+PSRR	V+ = +13.5V, +16.5V	1	+25°C	86	-	dB
		V- = -15V, -15V	2, 3	-55°C, +125°C	86	-	dB
	-PSRR	V+ = +15V, +15V	1	+25°C	86	-	dB
		V- = -13.5V, -16.5V	2, 3	-55°C, +125°C	86	-	dB
Digital Input Current	I_{IN1}	V_{IN1} = 0V	1	+25°C	-	40	μA
			2, 3	+125°C, -55°C	-	40	μA
	I_{IN2}	V_{IN2} = 5.0V	1	+25°C	-	40	μA
			2, 3	+125°C, -55°C	-	40	μA
Digital Input Voltage	V_{IL}		1	+25°C	-	0.8	V
			2, 3	+125°C, -55°C	-	0.8	V
	V_{IH}		1	+25°C	2.0	-	V
			2, 3	+125°C, -55°C	2.0	-	V
Output Voltage Droop Rate	V_D		2	+125°C	-100	100	μV/μs

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

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SAMPLE & HOLD AMPLIFIERS

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at V+ = +15V, V- = -15V, V_{IL} = 0.8V (Sample), V_{IH} = 2.0V (Hold), C_H = Internal = 90pF, SIG. GND. = SUPPLY GND., -Input Tied to Output, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMP	LIMITS MIN	LIMITS MAX	UNITS
Acquisition Time 0.1%	$+t_{acq}$ (0.1%)	$R_L = 2k\Omega$, $C_L = 50pF$, $A_V = +1$ $V_{OUT} = 0V, +10V$	2	+25°C	-	500	ns
				+125°C, -55°C	-	500	ns
	$-t_{acq}$ (0.1%)	$R_L = 2k\Omega$, $C_L = 50pF$, $A_V = +1$ $V_{OUT} = 0V, -10V$	2	+25°C	-	500	ns
				+125°C, -55°C	-	500	ns
Acquisition Time 0.01%	$+t_{acq}$ (0.01%)	$R_L = 2k\Omega$, $C_L = 50pF$, $A_V = +1$ $V_{OUT} = 0V, +10V$	2	+25°C	-	900	ns
				+125°C, -55°C	-	900	ns
	$-t_{acq}$ (0.01%)	$R_L = 2k\Omega$, $C_L = 50pF$, $A_V = +1$ $V_{OUT} = 0V, -10V$	2	+25°C	-	900	ns
				+125°C, -55°C	-	900	ns
Output Voltage Droop Rate	V_D		2	+25°C, -55°C	-10	10	µV/µs

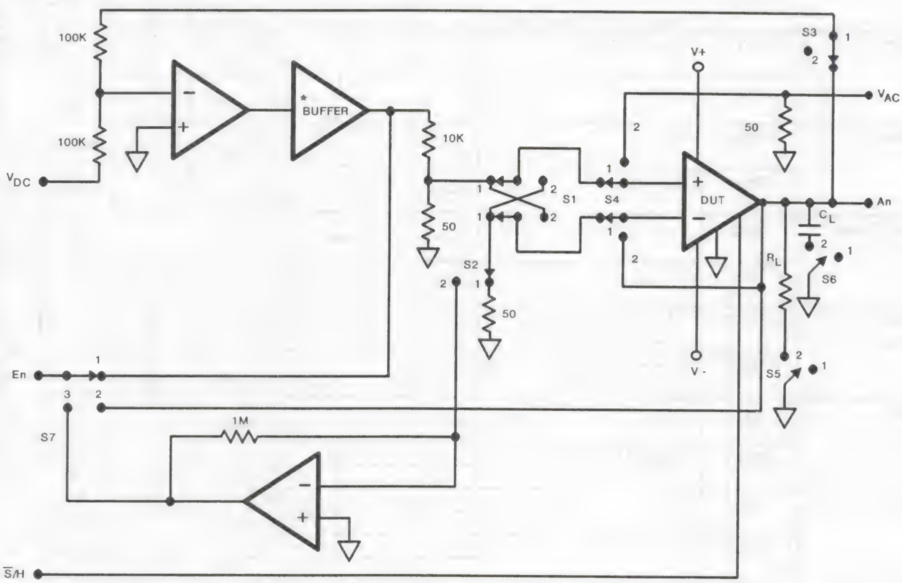
NOTE: 2. The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1, 3)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3
Group A Test Requirements	1, 2, 3
Groups C & D Endpoints	1

*PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

Test Circuit



*BUFFER = + 1 WITH S1 = 1
BUFFER = - 1 WITH S1 = 2

Test Circuit (Continued)

CHART A. TEST CIRCUIT CONDITIONS (SEE TEST CIRCUIT)

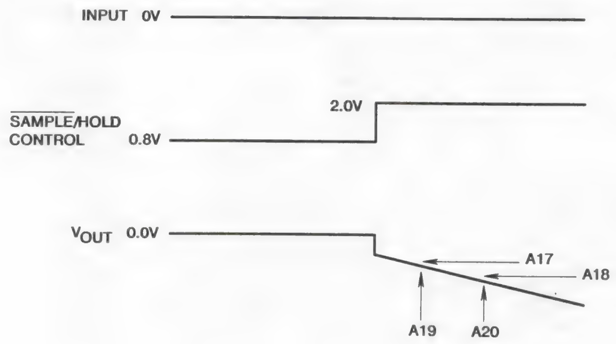
PARAMETERS	NOTE	APPLY (IN VOLTS) OR MEASURE (m)						SWITCH POSITION							MEASURE		MEASURED PARAMETER OR EQUATION	UNITS
		V+	V-	VDC	$\overline{S}$/H	En	An	S1	S2	S3	S4	S5	S6	S7	VALUE	UNIT		
V_{IO}	-	+15	-15	0.0	0.8	m	-	1	1	1	1	1	1	1	E1	V	$V_{IO} = -E1/200$	mV
I_{IO}	-	+15	-15	0.0	0.8	-	-	-	-	-	-	-	-	-	-	V	$I_{IO} = (I_{B+})-(I_{B-})$	nA
I_{B+}	-	+15	-15	0.0	0.8	m	-	2	2	1	1	1	1	3	E7	V	$I_{B+} = (E1-E7)/10^6$	nA
I_{B-}	-	+15	-15	0.0	0.8	m	-	1	2	1	1	1	1	3	E10	V	$I_{B-} = (E1-E10)/10^6$	nA
$+I_{CC}$	-	+15	-15	0.0	0.8	-	-	1	1	1	1	1	1	1	-	mA	Measure $+V_{CC}$ Current	mA
$-I_{CC}$	-	+15	-15	0.0	0.8	-	-	1	1	1	1	1	1	1	-	mA	Measure $-V_{CC}$ Current	mA
-PSRR	- -	+15 +15	-13.5 -16.5	0.0 0.0	0.8 0.8	m m	-	1	1	1	1	1	1	1	E13 E14	V V	$-PSSR = 20Log_{10} \left\lvert \frac{3V}{(E13-E14)/200} \right\rvert$	dB
+PSRR	- -	+13.5 +16.5	-15 -15	0.0 0.0	0.8 0.8	m m	-	1	1	1	1	1	1	1	E15 E16	V V	$+PSRR = 20Log_{10} \left\lvert \frac{3V}{(E15-E16)/200} \right\rvert$	dB
+CMRR	3	+5	-25	+10	-9.2	m	-	1	1	1	1	1	1	1	E17	V	$+CMRR = 20Log_{10} \left\lvert \frac{10V}{(E1-E17)/200} \right\rvert$	dB
-CMRR	4	+25	-5	-10	+10.8	m	-	1	1	1	1	1	1	1	E18	V	$-CMRR = 20Log_{10} \left\lvert \frac{10V}{(E1-E18)/200} \right\rvert$	dB
I_{IN1}	-	+15	-15	0.0	0.0	-	-	1	1	1	1	1	1	1	-	µA	Measure $\overline{S}$/H Current	µA
I_{IN2}	-	+15	-15	0.0	5.0	-	-	1	1	1	1	1	1	1	-	µA	Measure $\overline{S}$/H Current	µA
Droop Rate	-	+15	-15	0.0	2.0	-	m m	1	1	2	2	2	1	2	A17, A19 A18, A20	V, ms V, ms	$\text{Droop Rate} = \frac{A18-A17}{A20-A19}$, A20-A19 = 10ms	µA/µs
$-I_O$	-	+15	-15	-13	0.8	-10mA	-	1	1	1	1	1	1	2	-	V	Measure En Volts	V
$+I_O$	-	+15	-15	+13	0.8	+10mA	-	1	1	1	1	1	1	2	-	V	Measure En Volts	V
$+V_{OUT}$	5	+15	-15	-14	0.8	m	-	1	1	1	1	2	1	2	E23	V		V
$-V_{OUT}$	5	+15	-15	+14	0.8	m	-	1	1	1	1	2	1	2	E24	V		V
$+A_{VOL}$	5 -	+15 +15	-15 -15	0.0 -10	0.8 0.8	m m	- -	1 1	1 1	1 1	1 1	2 2	1 1	1 1	E25 E26	V V	$+A_{VOL} = 20Log_{10} \left\lvert \frac{10V}{(E25-E26)/200} \right\rvert$	dB
$-A_{VOL}$	5 -	+15 +15	-15 -15	0.0 +10	0.8 0.8	m m	- -	1 1	1 1	1 1	1 1	2 2	1 1	1 1	E27 E28	V V	$-A_{VOL} = 20Log_{10} \left\lvert \frac{10V}{(E27-E28)/200} \right\rvert$	dB

NOTES:

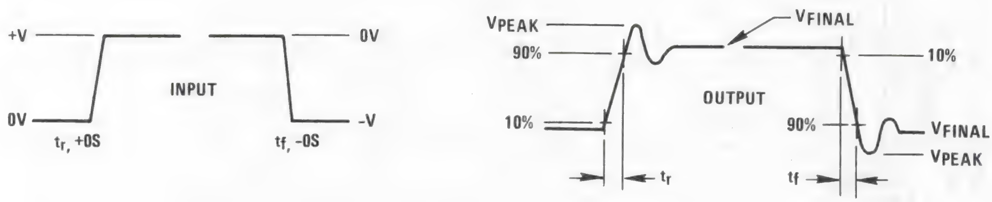
3. Package GND to -10V for this test.
4. Package GND to +10V for this test.
5. $R_{LDC} = 1k\Omega$.

Timing Waveforms

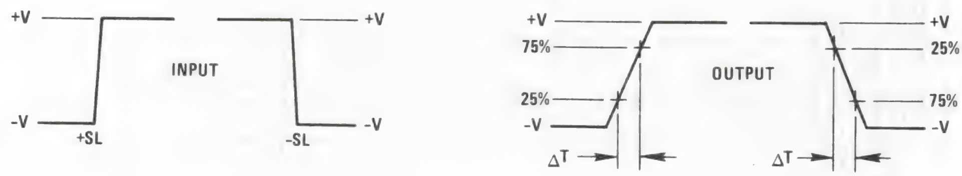
DROOP RATE WAVEFORMS



OVERSHOOT, RISE & FALL TIME WAVEFORMS

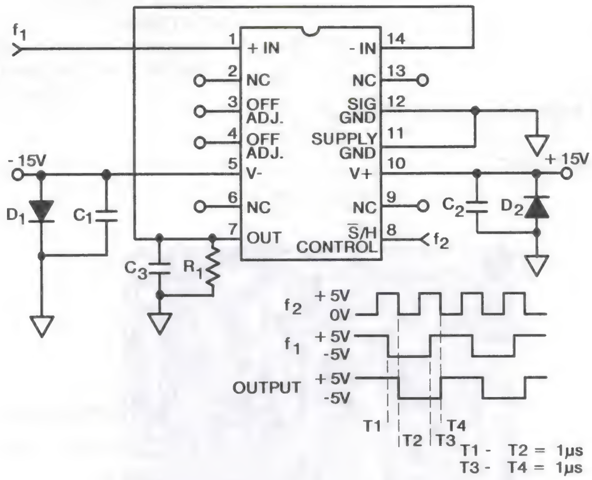


SLEW RATE WAVEFORMS

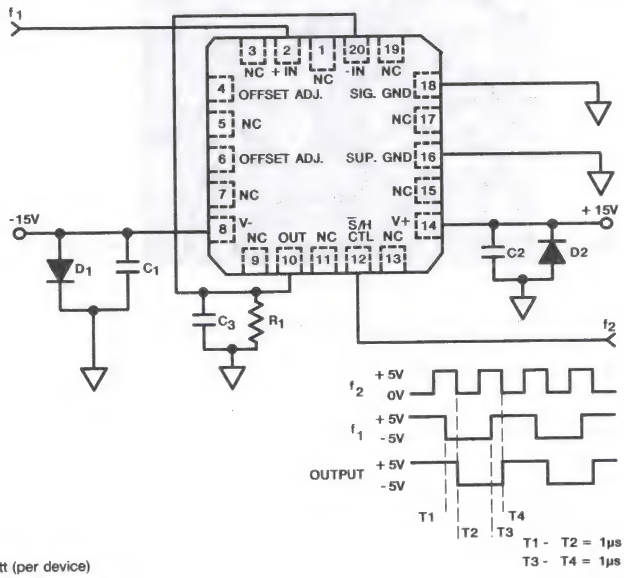


Burn-In Circuits

HA-5330/883 (CERAMIC DIP)



HA-5330/883 (CERAMIC LCC)



NOTES:

R_1 = 510Ω, 5%, 1/2 Watt (per device)

$C_1 = C_2$ =0.1μF (per device)

C_3 = 47pF, 10%, 50V (per device)

$D_1 = D_2$ = 1N4002 or Equivalent (per board)

f_2 = 250kHz, TTL Levels, 50% Duty Cycle

f_1 = 125kHz, +5V to -5V, 50% Duty Cycle

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SAMPLE & HOLD AMPLIFIERS

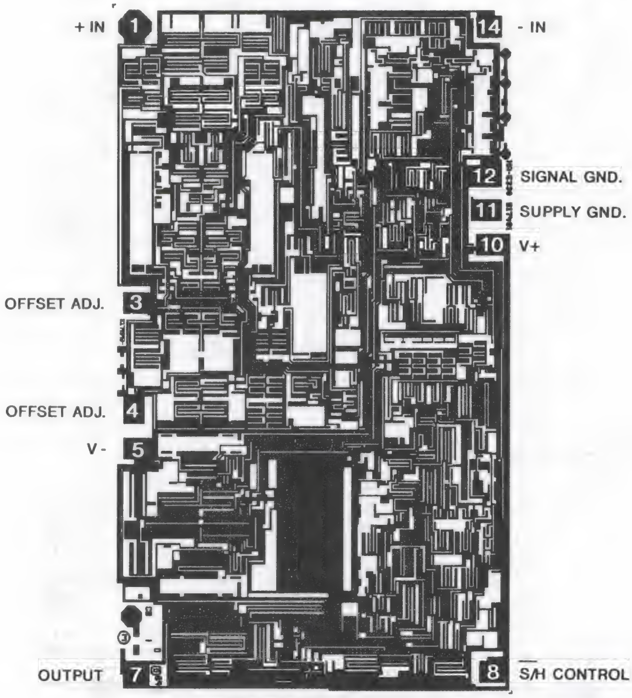
Die Characteristics

DIE DIMENSIONS: 99 x 166 x 19 mils
METALLIZATION:
Type: Al
Thickness: 16kÅ ± 2kÅ
GLASSIVATION:
Type: Silox
Thickness: 14kÅ ± 2.0kÅ
WORST CASE CURRENT DENSITY: $1.36 \times 10^5 A/cm^2$

TRANSISTOR COUNT:
HA-5330/883 205
PROCESS: Bipolar DI
DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP - 460°C (Max)
Ceramic LCC - 420°C (Max)

Metallization Mask Layout

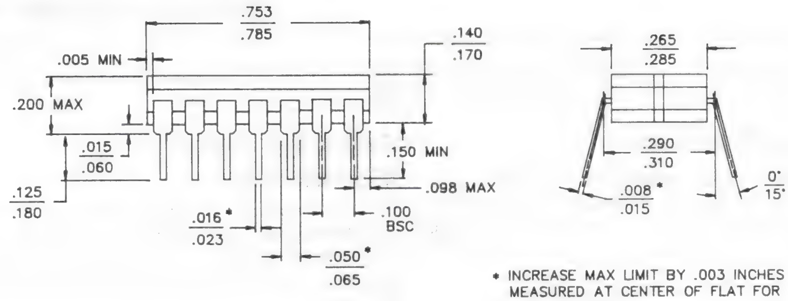
HA-5330/883



NOTE: Pad Numbers Correspond to DIP Package Only.

Packaging†

14 PIN CERAMIC DIP

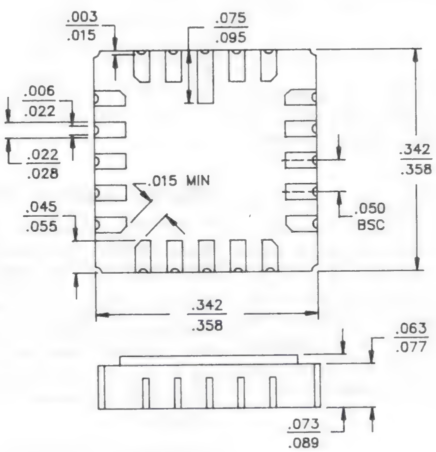


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ±10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-1

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ±10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$ Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

7 SAMPLE & HOLD AMPLIFIERS

HARRIS

HA-5330

DESIGN INFORMATION

Very High Speed Precision Monolithic Sample and Hold Amplifier

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Applying the HA-5330

The HA-5330 has the uncommitted differential inputs of an op amp, allowing the Sample/Hold function to be combined with many conventional op amp circuits. See the Harris Application Note 517 for a collection of circuit ideas.

Layout

A printed circuit board with ground plane is recommended for best performance. Bypass capacitors (0.01 to 0.1μF, ceramic) should be provided from each power supply terminal to the Supply Gnd terminal on pin 11.

Applications

The HA-5330 is configured as a unity gain noninverting amplifier by simply connecting the output (pin 7) to the inverting input (pin 14). As an input device for a fast, successive-appoximation A/D converter, it offers an extremely high throughput rate. Also, the HA-5330's pedestal error is adjustable to zero by using an Offset Adjust potentiometer (10K to 50K) center tapped to V-.

The ideal ground connections are pin 12 (Signal Ground) directly to the system Signal Ground (Analog Ground), and pin 11 (Supply Ground) directly to the system Supply Common.

Hold Capacitor

The HA-5330 includes a 90pF MOS hold capacitor, sufficient for most high speed applications (the Electrical Characterisitics section is based on this internal capacitor).

Output Stage

The HA-5330 output circuit does not include short circuit protection, and consequently its output impedance remains low at high frequencies. Thus, the step changes in load current which occur during an A/D conversion are absorbed at the $\overline{S}$/H output with minimum voltage error. A momentary short circuit to ground is permissible, but the output is not designed to tolerate a short of indefinite duration. D.C. Output Resistance at +25°C is typically $1 \times 10^{-5}\Omega$ for Sample Mode and 0.2Ω for Hold Mode.

Glossary of Terms

Acquisition Time:

The time required following a "sample" command, for the output to reach its final value within ±0.1% or ±0.01%. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

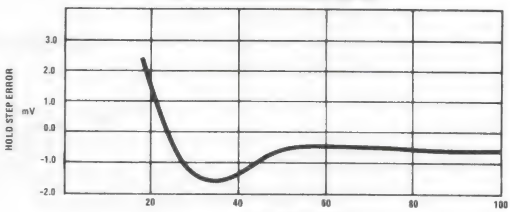
Aperture Time:

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is that interval between the conditions of 10% open and 90% open.

Hold Step Error:

Hold step error is the output shift due to charge transfer from the sample to the hold mode. It is also referred to as "offset step" or "pedestal error".

HOLD STEP ERROR vs $\overline{S}$/H CONTROL RISE TIME



Effective Aperture Delay Time (EADT):

The difference between propagation time from the analog input to the $\overline{S}$/H switch, and digital delay time between the Hold command and opening of the switch.

EADT may be positive, negative or zero. If zero, the $\overline{S}$/H amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors will correspond to a value of V_{IN} that occured before the Hold command.

Aperture Uncertainty:

The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at V+ = +15V, V- = -15V, V_{IL} = 0.8V (Sample), V_{IH} = 2.0V (Hold), C_H = Internal = 90pF, SIG. GND. = Supply GND., -Input Tied to Output; Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYP	UNITS
Hold Step Error	V_{IN} = 0V, V_{IH} = +3.5V t_r = 22ns	+25°C	0.5	mV
Rise Time	V_i =200mV Step R_L = 2kΩ, C_L = 50pF	+25°C	70	ns
Overshoot	V_i =200mV Step R_L = 2kΩ, C_L = 50pF	+25°C	10	%
Slew Rate	V_i =20V Step R_L = 2kΩ, C_L = 50pF	+25°C	90	V/µs
Aperture Time	From Computer Simulation Only	+25°C	20	ns
Effective Aperture Delay Time		+25°C	-25	ns
Aperture Uncertainty		+25°C	0.1	ns
Hold Mode Settling Time (0.01%)		+25°C	100	ns
Hold Mode Feedthrough Attenuation	$20V_{p-p}$, 100kHz	Full	-88	dB
Output Resistance				
Hold Mode	D.C.	+25°C	0.2	Ω
Sample Mode	D.C.	+25°C	10^{-5}	Ω
Input Resistance	From Computer Simulation Only	Full	15 x 10^6	Ω
Input Capacitance		+25°C	3	pF
Total Output Noise				
Sample	D.C. to 4.0MHz	+25°C	230	μV_{RMS}
Hold	D.C. to 4.0MHz	+25°C	190	μV_{RMS}

ANALOG

ASICs

8

PAGE

HARRIS SEMICONDUCTOR CICD

Harris Custom/Semicustom IC capabilities are outlined in this section for your high performance systems designs.

FOCUS
• Serve the high-rel strategic and tactical government ASIC systems, high-performance commercial and industrial systems, and commercial secure communications systems.

LEADERSHIP
• Top supplier of custom and semicustom analog and digital rad hard and non-rad hard ICs • Stable government supplier with long-term commitment to served markets. Part of Harris Corporation, major vertically integrated defense contractor • Authority on military standards, certification, and testing issues — class "B" and class "S" facilities • Radiation Hardened Custom/Semicustom Leader • Secure Communications leader • Proven knowledge-based, front-to-back CAE tools based on open system framework concept, as well as Daisy™, Mentor™, CAE systems • SOI process leadership - next generation hardness technology • VHSIC process capabilities • Mixed analog/digital for custom/ applications • Multiple CMOS, Bipolar and BIMOS processing capabilities • Leadership in strategic programs • High-performance commercial ASICs — high voltage, high temperature, harsh environment experience

Contact CICD Marketing for more information (407) 729-5757

HSC1000RH Radiation Hardened Dual Level Metal CMOS Standard Cell Library

Features

- Low power CMOS process
- 2.0 micron channel lengths (1.25 micron effective)
- Dual level metal interconnect
- Guaranteed hardened against radiation
  - > Total dose. . . . . > 2×10^5 RAD-Si
  - > Data upset. . . . . > 1×10^9 RAD-Si/s
  - > Latch-Up free to. . . . . > 1×10^{12} RAD-Si/s
  - > Functional after 10^6 total dose radiation
- 800ps typical 2-input nand gate delay with a fanout = 2
- 100MHz Flip-Flop Toggle Frequency
- Supports gate counts to 13K
- Over 200 primitive and macrocell functions
- Complex function megacells
- Supported on Harris Architect™, Daisy™ and Mentor Graphics™ Design Systems
- CMOS/TTL compatible I/O's
- Military temperature ranges
- Proven reliable and manufacturable process
- Extensive packaging options
- Screening and qualification to Mil-Std-883C Method 5004/5005, Class B
- Space and class 'S' screens and qualifications
- Function compatible with the HSC1000 Non-Radiation Hardened Library

Dual Level Metal CMOS Standard Cell Library HSC1000

Features

- Low power CMOS process
- 1.5 micron channel lengths (1.0 micron effective)
- Dual level metal interconnect
- 800ps typical 2-input nand gate delay with a fanout = 2
- 100MHz flip-flop toggle frequency
- Supports gate counts to 25K
- Over 200 primative and macrocell functions
- Complex function megacells
- RAM and ROM Module Compilers
- Supported on Harris Architect™, Daisy™ and Mentor Graphics® Design Systems
- CMOS/TTL compatible I/O's
- Commercial-Industrial-Military Temperature Ranges
- Proven reliable and manufacturable process
- Extensive packaging options
- Screening and qualification to Mil-Std-883C Method 5004/5005, Class B
- Space and class 'S' screens and qualifications
- Function compatible with the HSC 1000RH Radiation Hardened Library

SEMICUSTOM CELL LIBRARY

CMOS/Analog/Digital Cell Library
Features
• Fast turn, low risk ASIC with high performance • High level of integration provides "system on a chip" capability • Switched-capacitor methods provide wide variety of analog circuit functions. • Low power — CMOS technology • ±5 volt or 0-10 volt power supply operation • Available now for Custom Applications • CMOS and TTL inputs and outputs • 32 analog cells — operational amplifiers, comparators, voltage references and bias circuits, switch cells • Multiple packaging options • Military Class B or S equivalent flow

SEMICUSTOM DESIGN TOOLS

Toolkit for Daisy™
Features
• Compatible with standard Daisy platforms — supports standard Daisy Tools • Supports Harris Standard Cell, Gate Array* and Compiled Functions* • Schematic capture, simulation and netlisting for SSI, MSI, LSI Macrofunctions and RAM/ROM Compilers • 1.5 micron Non-rad Hard (HSC1000) and 2.0 micron Rad Hard (HSC1000RH) Libraries are available today • Simulation capabilities include min/typ/max delays for all functions. Post radiation simulation supported for HSC1000RH • Back annotation of fanout and routed delays • Supports DED II and ACE Schematic Capture — DeMorgan Symbols for many functions • Additional Harris tools enhance Daisy productivity > Chip Statistics > Design Plotting > Som Maker > Fanout Checker > PinLister > TCAL • Classified design area with Daisy available at Harris

*Gate Array support planned for Q2, CY 1989, Compiler Support provided as a Harris custom service.

Toolkit For Mentor Graphics®
Features
• Supports Harris Standard Cell, Gate Array* and Compiled Functions* • Schematic capture, simulation and netlisting for SSI, MSI, LSI Macrofunctions and RAM/ROM Compilers • Accurate, efficient behavioral models • Ability to integrate with Mentor Graphics Board-Level Simulations • 1.5 micron Non-rad Hard (HSC1000) and 2.0 micron Rad Hard (HSC1000RH) Libraries are available today • Simulation capabilities include min/typ/max delays for all functions • Post radiation simulation supported for HSC1000RH • Back annotation of fanout delays • Additional Harris Design Management Tools enhance Mentor Graphics productivity: > Comprehensive Electrical Rule Checking (ERCs) > Design Statistics Generation > Tester Interface > Design Status (Audit Trail) > Design Transfer

*Gate Array support planned for Q2, CY 1989, Compiler Support provided as a Harris custom service.

CUSTOM/SEMICUSTOM CIRCUIT TECHNOLOGY

Process	Minimum Feature Size (Drawn Microns)	Rad Tol/Rad-Hard	Levels of Metal
MOS			
PMOS (Digital)	7.5		1
MGCMOS (metal gate)(Digital)	7.5		1
SAJI I (Digital)	5.0	RT/RH	1
SAJI IV (Digital)	3.0	RT/RH	1
Scaled SAJI IV (Digital)	2.5	RT/RH	1
SAJI VH (Digital)	2.0	RH	2
SAJI IVA (Analog/Digital)	3.0	RT	1
RH-7 (VHSIC-LIKE) (Analog/Digital)	1.2	RH	2
L7	1.5	RT	2
Gamma III (Digital)	1.2	RH	2
S7 (Digital)	1.2	RT	2
BIPOLAR			
High Freq. Process (HFP) (Analog)	5.0	RH	1
Linear ALPS (Analog)	4.0	RH	1
High Current Linear (HCL) (Analog)	5.0	RH	1
Advanced Low Power Schottky (Digital)	4.0	RH	1
BIMOS* (Digital)	2.0		1
Very High Freq. Process (VHFP) (Analog/Digital)	4.0	RH	2
GaAs			
DIGI-1,-11	1.0		
MMIC	.5		

8

ASICs

CUSTOM BIPOLAR ANALOG PROCESSES

CUSTOM BIPOLAR LINEAR PROCESSES

Process	Type	h_{fe} NPN	h_{fe} PNP	F_T(MHz) NPN	F_T(MHz) PNP	BV_{CEO} NPN	BV_{CEO} PNP	Rad-Hard Option	Applications
Junction Isolation	—	150	50	300	2	40	40	No	• Low-to-medium frequency amplifiers • Low Speed, non-saturated logic
Dielectric Isolation	Switching NPN	50	—	500	—	7	—	Yes	• Mixed digital/analog switching • Sense amplifiers • Line drivers • Line receivers
Dielectric Isolation	BiFET*	150	100	600	300	40	40	Yes	• Analog switches • Operational amplifiers • Sample-and-holds
Dielectric Isolation	High Frequency	150	100	600	300	40	40	Yes	• High-frequency amplifiers • Rad-hard amplifiers • Comparators
Dielectric Isolation	High Current	150	100	500	250	40	40	Yes	• Power relay drivers • Clock drivers • Voltage regulators
Dielectric Isolation	High Voltage	225	50	200	25	100	90	Yes	• High-voltage amplifiers
Dielectric Isolation	CMOS/ Bipolar	150	100	600	300	35†	35**	Yes	• Analog switches • High-performance amplifiers • Data conversion • Pin diode driver
Dielectric Isolation	NPN Schottky	50	—	500	—	8	—	Yes	• Flash converters • Sense amplifiers
Dielectric Isolation	VHFP	100	100	1.5 GHz	1.0 GHz	15V	15V	Yes	• High Speed amplifiers • Mixed analog/digital

*V_P = 1V to 2V, BV_{DSS} = 20V, **V_{TP} = 1V to 3V, BV_{DSS} = 40V, †V_{TN} = 1V to 3V, BV_{DSS} = 40V

CUSTOM INTERFACE PROCESSES

CUSTOM INTERFACE PROCESSES

Process	Features	Isolation	Operating Voltage	Output Drive	Rad-Hard Option	Applications
SLIC	NPN; PNP	Dielectric	>65 Volts	25MA	Yes	• Subscriber Line • Interface Ckts.
High-Current Linear	NPN; PNP NiCr Resistors Schottky Diodes	Dielectric	>40 Volts	500MA	Yes	• Power Mosfet Driver • Bubble Memory Function Driver • Voltage Regulators
Std. Lin.	NPN; PNP NiCr Resistors	Dielectric	>35 Volts	50MA	Yes	• Current Booster
JI JFET	NPN; PNP JFETs NiCr Resistors	Junction	>35 Volts	50MA	Yes	• Amp. with JFET input
High Freq. Linear	NPN; PNP NiCr Resistors JFETs	Dielectric	>30 Volts	100MA	Yes	• Amplifiers • Precision J-FET Op-Amps
MSIA (Gold Doped)	NPN; NiCr Resistors	Dielectric	>20 Volts	200MA	Yes	• CCD clock driver
LCMOS	P-Channel P-Channel	Dielectric	>30 Volts	80MA	Yes	• Interface Switches • Analog Multiplexers
BIPMOS	N-Channel P-Channel NPN; PNP	Dielectric	>35 Volts	50MA	Yes	• Op-Amps • Comparators • Sample and Hold
CMOS Si-Gate	N-Channel P-Channel NPN; PNP NiCr Resistors	Dielectric	>25 Volts	25MA	Yes	• Analog Multiplexer • D-to-A Converters

ANALOG

Harris Quality and Reliability

9

PAGE

Harris Quality & Reliability

Introduction

Success in the integrated circuit industry means more than simply meeting or exceeding the demands of today's market. It also includes anticipating and accepting the challenges of the future. It results from a process of continuing improvement and evolution, with perfection as the constant goal.

Harris Semiconductor's commitment to supply only top value integrated circuits has made quality improvement a mandate for every person in our work force — from circuit designer to manufacturing operator, from hourly employee to corporate executive. Price is no longer the only determinant in marketplace competition. Quality, reliability, and performance enjoy significantly increased importance as measures of value in integrated circuits.

Quality in integrated circuits cannot be added on or considered after the fact. It begins with the development of capable process technology and product design. It continues in manufacturing, through effective controls at each process or step. It culminates in the delivery of products which meet or exceed the expectations of the customer.

The Role of The Quality Organization

The emphasis on building quality into the design and manufacturing processes of a product has resulted in a significant refocus of the role of the Quality organization. In addition to facilitating the development of SPC and DOX programs and working with manufacturing to establish control charts, Quality professionals are involved in the measurement of equipment capability, standardization of inspection equipment and processes, procedures for chemical controls, analysis of inspection data and feedback to the manufacturing areas, coordination of efforts for process and product improvement, optimization of environmental or raw materials quality, and the development of quality improvement programs with vendors.

At critical manufacturing operations, process and product quality is analyzed through random statistical sampling and product monitors. The Quality organization's role is changing from policing quality to leadership and coordination of quality programs or procedures through auditing, sampling, consulting, and managing Quality Improvement projects.

To support specific market requirements, or to ensure conformance to military or customer specifications, the Quality organization still performs many of the conventional quality functions (e.g., group testing for military products or wafer lot acceptance). But, true to the philosophy that quality is everyone's job, much of the traditional on-line measurement and control of quality characteristics is where it belongs — with the people who make the product. The Quality organization is there to provide leadership and assistance in the deployment of quality techniques, and to monitor progress.

The Improvement Process

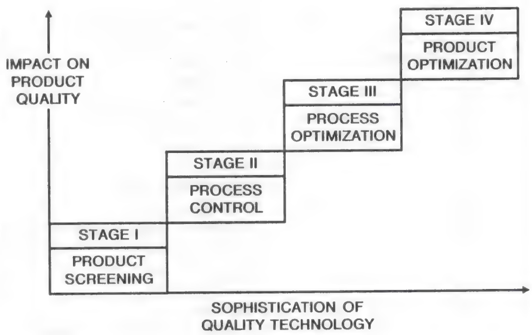


FIGURE 1. STAGES OF STATISTICAL QUALITY TECHNOLOGY

Harris Semiconductor's quality methodology is evolving through the stages shown in Figure 1. In 1981 we embarked on a program to move beyond Stage I, and we are currently in the transition from Stage II to Stage III, as more and more of our people become involved in quality activities. The traditional "quality" tasks of screening, inspection, and testing are being replaced by more effective and efficient methods, putting new tools into the hands of all employees. Table 1 illustrates how our quality systems are changing to meet today's needs.

TABLE 1. TYPICAL ON-LINE MANUFACTURING/QUALITY FUNCTIONS

AREA	FUNCTION	MANUFACTURING CONTROLS	QA/QC MONITOR AUDIT
Wafer Fab	• JAN Self-Audit		X
	• Environmental		
	– Room/Hood Particulates	X	X
	– Temperature/Humidity	X	X
	– Water Quality		X
	• Product		
	– Junction Depth	X	
	– Sheet Resistivities	X	
	– Defect Density	X	X
	– Critical Dimensions	X	X
	– Visual Inspection	X	X
	– Lot Acceptance		X
	• Process		
	– Film Thickness	X	X
	– Implant Dosages	X	
	– Capacitance Voltage Changes	X	X
	– Conformance to Specification	X	X
	• Equipment		
	– Repeatability	X	X
	– Profiles	X	X
	– Calibration		X
	– Preventive Maintenance	X	X
Assembly	• JAN Self-Audit		X
	• Environmental		
	– Room/Hood Particulates	X	X
	– Temperature/Humidity	X	X
	– Water Quality		X
	• Product		
	– Documentation Check		X
	– Dice Inspection	X	X
	– Wire Bond Pull Strength/Controls	X	X
	– Die Sear Controls		X
	– Pre-Seal Visual	X	X
	– Fine/Gross Leak	X	X
	– PIND Test	X	
	– Lead Finish Visuals, Thickness	X	X
	– Die Shear		X
	– Solderability		X
	• Process		
	– Operator Quality Performance	X	X
	– Saw Controls	X	
	– Die Attach Temperatures	X	X
	– Seal Parameters	X	
	– Seal Temperature Profile	X	X
	– Sta-Bake Profile	X	
	– Temp Cycle Chamber Temperature	X	X
	– ESD Protection	X	X
	– Plating Bath Controls	X	
	– Mold Parameters	X	X
Test	• JAN Self-Audit		X
	• Temperature/Humidity	X	X
	• ESD Controls	X	
	• Temperature Test Calibration	X	
	• Test System Calibration	X	
	• Test Procedures		X
	• Control Unit Compliance	X	
	• Lot Acceptance Conformance	X	
	• Group A Lot Acceptance		X
Probe	• JAN Self-Audit		X
	• Wafer Repeat Correlation	X	
	• Visual Requirements	X	X
	• Documentation	X	X
	• Process Performance	X	X

TABLE 1. TYPICAL ON-LINE MANUFACTURING/QUALITY FUNCTIONS (CONTINUED)

AREA	FUNCTION	MANUFACTURING CONTROLS	QA/QC MONITOR AUDIT
Burn-In	• JAN Self-Audit		X
	• Functionality Board Check	X	
	• Oven Temperature Controls	X	
	• Procedural Conformance		X
Brand	• JAN Self-Audit		X
	• ESD Controls	X	X
	• Brand Permanency	X	X
	• Temperature/Humidity	X	X
	• Procedural Conformance		X
QCI Inspection	• JAN Self-Audit		X
	• Group B Conformance		X
	• Group C and D Conformance		X

Designing For Manufacturability

Assuring quality and reliability in integrated circuits begins with good product and process design. This has always been a strength in Harris Semiconductor's quality approach. We have a very long lineage of high reliability, high performance products that have resulted from our commitment to design excellence. All Harris products are designed to meet the stringent quality and reliability requirements of the most demanding end equipment applications, from military and space to industrial and telecommunications. The application of new tools and methods has allowed us to continuously upgrade the design process.

Each new design is evaluated throughout the development cycle to validate the capability of the new product to meet the end market performance, quality, and reliability objectives.

The validation process has four major components:

1. Design simulation/optimization
2. Layout verification
3. Product demonstration
4. Reliability assessment.

Harris designers have an extensive set of very powerful Computer-Aided Design (CAD) tools to create and optimize product designs (see Table 2).

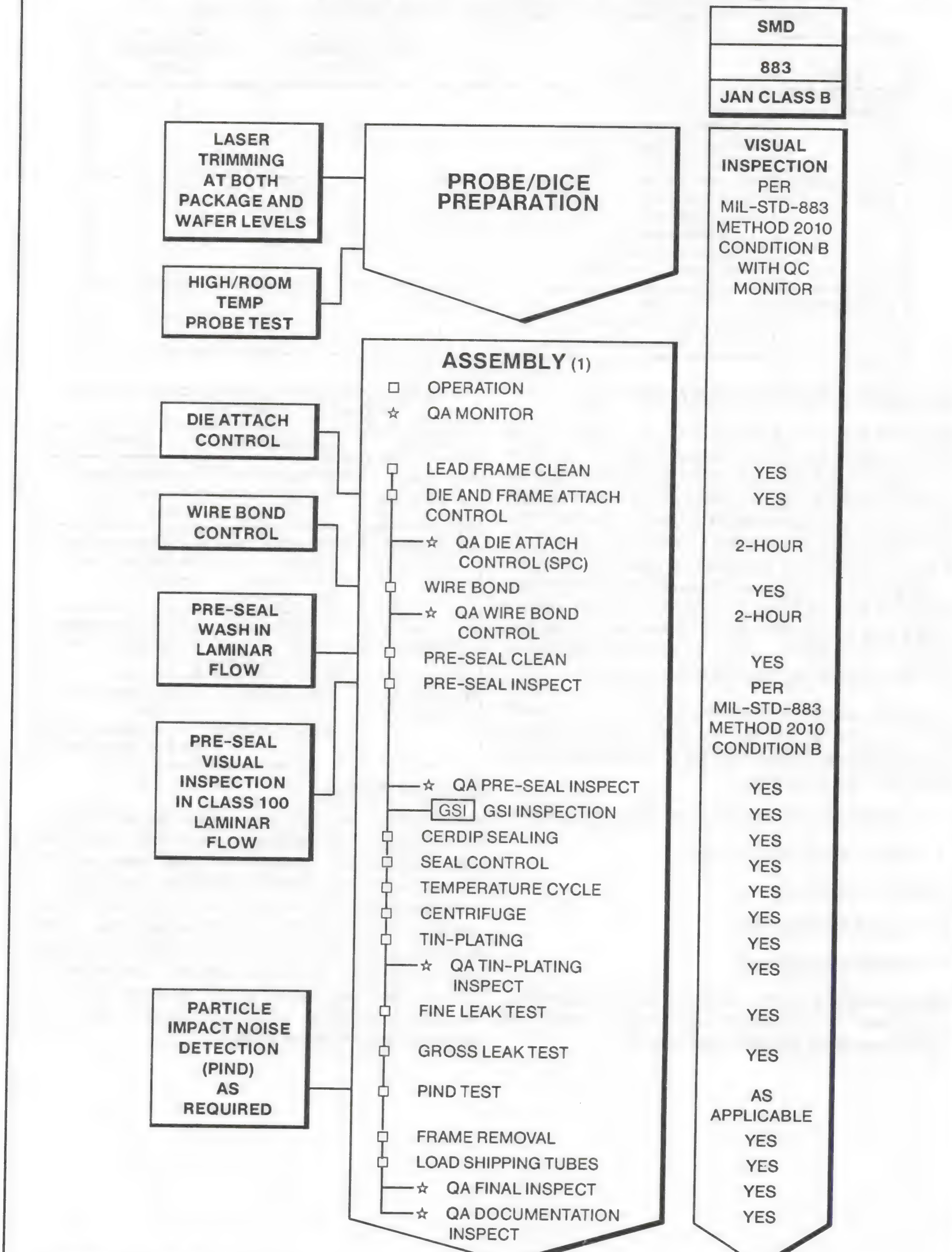
TABLE 2. APPROACH AND IMPACT OF STATISTICAL QUALITY TECHNOLOGY

STAGE		APPROACH	IMPACT
I	Product Screening	• Stress and Test • Defective Prediction	• Limited Quality • Costly • After-The-Fact
II	Process Control	• Statistical Process Control • Just-In-Time Manufacturing	• Identifies Variability • Reduces Costs • Real Time
III	Process Optimization	• Design of Experiments • Process Simulation	• Minimizes Variability • Before-The-Fact
IV	Product Optimization	• Design for Producibility • Product Simulation	• Insensitive to Variability • Designed-In Quality • Optimal Results

Special Testing

Harris Semiconductor offers several standard screen flows to support a customer's need for additional testing and reliability assurance. These flows include environmental stress testing, burn-in, and electrical testing at temperatures other than +25°C. The flows shown on pages 9-6 and 9-7 indicate the Harris standard screening processes. In addition, Harris can supply products tested to customer specifications both for electrical requirements and for non-standard environmental stress screening. Consult your field sales representative for details.

Harris Semiconductor Standard Processing Flows



(1) Example for a Cerdip Package Part

Harris Semiconductor Standard Processing Flows

(Continued)

TEST (2)	SMD / 883 / JAN CLASS B
□ ELECTRICAL TEST SORTING OPERATION	YES
□ SERIALIZE	IF APPLICABLE
□ PRE BURN-IN ELECTRICAL TEST	YES
□ BURN-IN (3)	160-HOUR @ +125°C, OR PER SLASH SHEET
□ POST BURN-IN TEST	YES
☆ ALTERNATE GROUP A	YES
□ APPLY BURN-IN PDA (AS APPLICABLE)	YES
□ SOLDERDIP	YES
□ FINE LEAK TEST	YES
□ GROSS LEAK TEST	YES
□ BRAND	YES
□ EXTERNAL VISUAL	YES
☆ QUALITY CONFORMANCE INSPECTION	GROUP A, B, C, D
□ FINAL DATA REVIEW	YES

□ OPERATION

☆ QA MONITOR

- AC/DC SINGLE INSERTION TEST CAPABILITY; HIGH/LOW TEMP
- BURN-IN
- QUALITY CONFORMANCE GROUPS A, B, C, AND D AS REQUIRED
- DELTAS PER SLASH SHEET REQUIREMENT IF APPLICABLE
- IN-HOUSE MASS SPEC CAPABILITY
- COMPUTERIZED LOT TRACEABILITY MONITORING SYSTEM

PACKAGE & SHIP OR STOCK

(2) -55°C TO +125°C

(3) Burn-In test temperatures can be increased and time reduced per regression tables in Mil-Std-883, Method 1015.

TABLE 3. SUMMARIZING CONTROL APPLICATIONS

FAB			
• Diffusion – Junction Depth – Sheet Resistivities – Oxide Thickness – Implant Dose Calibration – Uniformity	• Thin Film – Film Thickness – Uniformity – Refractive Index – Film Composition	• Photo Resist – Critical Dimension – Resist Thickness – Etch Rates	• Measurement Equipment – Critical Dimension – Film Thickness – 4 Point Probe – Ellipsometer
ASSEMBLY			
• Pre-Seal – Die Prep Visuals – Yields – Die Attach Heater Block – Die Shear – Wire Pull – Saw Blade Wear – Pre-Cap Visuals	• Post-Seal – Internal Package Moisture – Tin Plate Thickness – PIND Defect Rate – Solder Thickness – Leak Tests – Module Rm. Solder Pot Temp. – Seal – Temperature Cycle	• Measurement – XRF – Radiation Counter – Thermocouples – GM-Force Measurement	
TEST			
	– Handlers/Test Systems – Defect Pareto Charts – Lot % Defective – ESD Failures per Month	– Monitor Failures – Lead Strengthening Quality – After Burn-In PDA	
OTHER			
• IQC – Vendor Performance – Material Criteria – Quality Levels	• Environment – Water Quality – Clean Room Control	• IQC Measurement/Analysis – XRF – ADE – 4 Point Probe – Chemical Analysis Equipment	

Controlling and Improving the Manufacturing Process – SPC/DOX

Statistical process control (SPC) is the basis for quality control and improvement at Harris Semiconductor. Harris manufacturing people use over 1,000 Shewhart control charts to determine the normal variabilities in processes, materials, and products. Critical process variables are measured and control limits are plotted on the control charts. Appropriate action is taken if the charts show that a variable is outside the process control limits or indicates a trend toward the limit. These same control charts are powerful tools for use in reducing variations in processing, materials, and products. Table 3 lists some typical manufacturing applications of control charts at Harris Semiconductor.

But SPC is only part of the solution. Processes which operate in statistical control are not always capable of meeting engineering requirements. The conventional way of dealing with this in the semiconductor industry has been to implement 100% screening or inspection steps to remove defects, but these techniques are insufficient to meet today's demands for the highest reliability and perfect quality performance.

Harris still uses screening and inspection to "grade" products and to satisfy specific customer requirements for burn-in, multiple temperature test insertions, environmental screening, and visual inspection as value-added testing options. However, inspection and screening are limited in their ability to reduce product defects to the levels expected by today's buyers. In addition, screening and inspection have an associated expense, which raises product cost.

Harris engineers are, instead, using Design of Experiments (DOX), a scientifically disciplined mechanism for evaluating and implementing improvements in product processes, materials, equipment, and facilities. These improvements are aimed at reducing the number of defects by studying the key variables controlling the process, and optimizing the procedures or design to yield the best result. This approach is a more time-

TABLE 4. HARRIS I.C. DESIGN TOOLS

DESIGN STEP	PRODUCTS	
	ANALOG	DIGITAL
Functional Simulation	Slice	Silos Proteous Socrates
Parametric Simulation	Slice Monte Carlo	Slice
Schematic Capture	Note 1	Daisy SDA-Mass Comp
Functional Checking	Note 1	SDA-LVS
Rules Checking	Calma-DRC	Harris Dash
Parasitic Extraction	Note 1	SDA-LVS

NOTE 1. Tools are in Development.

consuming method of achieving quality perfection, but a better product results from the efforts, and the basic causes of product nonconformance can be eliminated.

SPC, DOX, and design for manufacturability, coupled with our 100% test flows, combine in a product assurance program that delivers the quality and reliability performance demanded for today and for the future.

Average Outgoing Quality (AOQ)

Average Outgoing Quality is a yardstick for our success in quality manufacturing. The average outgoing electrical defective is determined by randomly sampling units from each lot and is measured in parts per million (PPM). The current procedures and sampling plans outlined in MIL-STD-883 and MIL-M-38510 are used by our quality inspectors.

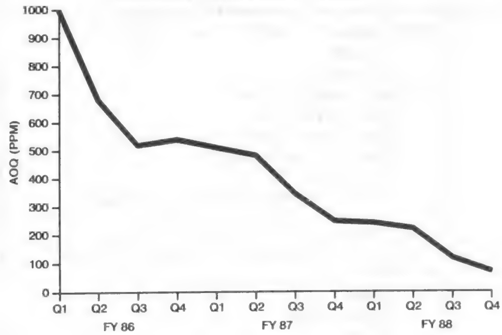


FIGURE 2. DEFECTIVE PARTS PER MILLION

The focus on this quality parameter has resulted in a continuous improvement over the past three years. AOQ has improved from 1,000 PPM to less than 100 PPM, and the goal for 1989 is to continue improvement toward a goal of 0 PPM.

Training

The basis of a successful transition from conventional quality programs to more effective, total involvement is training. Extensive training of personnel involved in product manufacturing began in 1984 at Harris, with a comprehensive development program in statistical methods. Using the resources of the University of Tennessee, private consultants, and internally developed programs, training of over 2,000 engineers, supervisors, and operators/technicians has been completed.

Nearly 1,000 operators, 100 supervisors, and more than 800 engineers have been trained in SPC methods, providing them with tools to improve the overall level of uniformity of Harris products. Almost 300 engineers have received training in DOX methods: learning to evaluate changes in process operations, set up new processes, select or accept new equipment, evaluate materials, select vendors, compare two or more pieces of equipment, and compare two or more process techniques.

Over the past four years, Harris has also deployed a comprehensive training program for hourly operators and supervisors in job requirements and functional skills. All hourly manufacturing employees participate (see Table 5).

TABLE 5. SUMMARY OF TRAINING PROGRAMS

COURSE	AUDIENCE	LENGTH	TOPICS COVERED
SPC	Manufacturing Operators	8 Hours	Basic Philosophy, Statistical Calculations Graphing Techniques, Pareto Charts, Control Charts
SPC	Manufacturing Supervisors	21 Hours	Basic Philosophy, Statistical Calculations Graphing Techniques, Pareto Charts, Control Charts, Testing for Inspector Agreement, Cause & Effect Diagrams, 1 & 2 Sample Methods
SPC	Engineers and Managers	48 Hours	Basic Philosophy, Graphical Methods, Control Charts, Rational Subgrouping, Variance Components, 1 & 2 Sample Methods, Pareto Charts, Cause & Effect Diagrams
DOX (Design of Experiments)	Engineers and Managers	88 Hours	Factorial Designs, Fractional Factorial Designs, Blocking Designs, Variance Components, Computer Usage, Normal Probability Plotting
RSM (Response Surface Methods)	Engineers and Managers	40 Hours	Steepest Ascent, Central Composite Designs, Box-Behnken Designs, Computer Usage, Contour Plotting, Second Order Response Surfaces
Continuous Improvement Methods	Manufacturing Supervisors	12 Hours	Basic Philosophy, Pareto Analysis, Imagineering, Run Charts, Cause & Effect Diagrams, Histograms, Ideas of Control Charts
SPC- The Essentials	Department-Level Work Groups	20 Hours	Basic Philosophy, of Continous Improvement, Imagineering Pareto Charts, Cause & Effect Diagrams, Flow Charts, Graphical Display, Control Charts, Ideas of Experiment

Incoming Materials

With statistical procedures in place to improve quality in the manufacturing operation, the impact of silicon, chemicals, gases, and other materials used in processing the product has become more measurable. Quality and consistency are important; it is logical to feed the manufacturing line with materials manufactured by vendors using equivalent statistical controls.

In order to ensure optimum quality of materials purchased from vendors, Harris initiated and coordinated an aggressive program to link key suppliers to our manufacturing operations. This network is formed by certifying strategic vendors who meet the highest quality standards while demonstrating a commitment to the use of statistical controls in their manufacturing operations.

SPC seminars, development of open working relationships, understanding of manufacturing needs and vendor capabilities, and continual improvement programs are all part of the certification process. Certified suppliers have passed stringent quality and SPC audits, while continuing to supply material with 100% conformance to Harris requirements.

In addition to the certification process, Harris has worked to promote improved quality in the performance of all our qualified vendors, who must meet rigorous incoming inspection criteria (see Table 6).

TABLE 6. INCOMING QUALITY CONTROL MATERIAL QUALITY CONFORMANCE

MATERIAL	INCOMING INSPECTIONS	VENDOR DATA REQUIREMENTS
Silicon	• Resistivity • Crystal Orientation • Dimensions • Edge Conditions • Taper • Thickness • Total Thickness Variation • Backside Criteria • Oxygen • Carbon	• Equipment Capability Control Charts – Oxygen – Resistivity • Control Charts Related to – Enhanced Gettering – Total Thickness Variation – Total Indicated Reading – Particulates • Certificate of Analysis for all Critical Parameters
Chemicals/Photoresists/ Gases	• Chemicals – Assay – Major Contaminants • Molding Compounds – Spiral Flow – Thermal Characteristics • Gases – Impurities • Photoresists – Viscosity – Film Thickness – Solids – Pinholes	• Certificate of Analysis on all Critical Parameters • Control Charts – Assay – Contaminants – Water – Selected Parameters • Control Charts – Assay – Contaminants • Control Charts on – Photospeed – Thickness – UV Absorbance – Filterability – Water – Contaminants
Thin Film Materials	• Assay • Selected Contaminants	• Control Charts – Assay – Contaminants – Dimensional Characteristics • Certificate of Analysis for all Critical Parameters
Assembly Materials	• Visual Inspection • Physical Dimension Checks • Lead Integrity • Glass Composition • Bondability • Intermetallic Layer Adhesion • Ionic Contaminants • Thermal Characteristics • Lead Coplanarity • Plating Thickness • Hermeticity	• Certificate of Analysis • Process Control Charts on Outgoing Product Checks and In-Line Process Controls

Manufacturing Science - CAM, JIT

In addition to SPC and DOX as key tools to control the product and processes, Harris is deploying other management mechanisms in the factory. On first examination, these tools appear to be directed more at schedules and capacity. However, they have a significant impact on quality results.

Computer Aided Manufacturing (CAM)

CAM is a computer based inventory and productivity management tool which allows personnel to quickly identify production line problems and take corrective action. In addition, CAM improves scheduling and allows Harris to more quickly respond to changing customer requirements and aids in managing work in process (WIP) and inventories.

The use of CAM has resulted in significant improvements in many areas. Better wafer lot tracking has facilitated a number of process improvements by correlating yields to process variables. In several places CAM has greatly improved capacity utilization through better planning and scheduling. Queues have been reduced and cycle times have been shortened — in some cases by as much as a factor of 2.

The most dramatic benefit has been the reduction of WIP inventory levels, in one area by 500%. This results in fewer lots in the area and a resulting quality improvement. In wafer fab, defect rates are lower because wafers spend less time in production areas awaiting processing. Lower inventory also improves morale and brings a more orderly flow to the area. CAM facilitates all of these advantages.

Just In Time (JIT)

A key adjunct to the CAM activity is Just In Time (JIT) material management. This is more than an inventory reduction technique: in many cases it involves reorganization of facilities and people. The essential concept is to form work units that are responsible for doing the whole job rather than bits of it. An employee has control over equipment, maintenance, cleanliness, scheduling, material, quality, and improvements.

In one Harris example, a photoresist flow consisting of several steps was previously organized in the classical departmentalized way. The inspection and etch areas were in different serial locations from the deposition and alignment areas. Work piled up at the slowest operation (inspection), and quality problems detected there were decoupled from the areas producing them by 20 to 30 feet and at least one day. Rework rates were very high; scrap was unacceptable.

When the area was reorganized into GT (group technology) cells (a basic concept of JIT), the inspection and alignment areas were physically coupled and people were organized into teams. The whole job (finished, defect-free wafers) was assigned to the GT cell (see Figure 3). Rework rates decreased 70%, scrap rates decreased 45%, and probe yields increased by 50%. This is only one of hundreds of examples of how JIT has improved our factory performance.

The JIT program/system works. This cultural change is vital and the benefits derived are impressive.

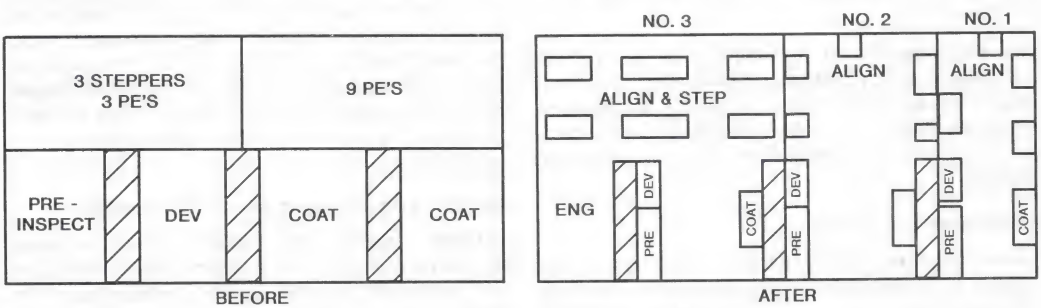


FIGURE 3. GROUP TECHNOLOGY CELL

9

HARRIS QUALITY & RELIABILTY

Measurement

Analytical Services Laboratory

Harris facilities, engineering, manufacturing, and product assurance are supported by the Analytical Services Laboratory. Organized into chemical or microbeam analysis methodology, staff and instrumentation from both labs cooperate in fully integrated approaches necessary to complete analytical studies. The capabilities of each area are shown below.

SPECTROSCOPIC METHODS: Colorimetry, Optical Emission, Ultraviolet Visible, Fourier Transform-Infrared, Flame Atomic Absorption, Furnace Organic Carbon Analyzer, Mass Spectrometer.

CHROMATOGRAPHIC METHODS: Gas Chromatography, Ion Chromatography.

THERMAL METHODS: Differential Scanning Colorimetry, Thermogravimetric Analysis, Thermomechanical Analysis.

PHYSICAL METHODS: Profilometry, Microhardness, Rheometry.

CHEMICAL METHODS: Volumetric, Gravimetric, Specific Ion Electrodes.

ELECTRON MICROSCOPE: Transmission Electron Microscopy, Scanning Electron Microscope.

X-RAY METHODS: Energy Dispersive X-ray Analysis (SEM), Wavelength Dispersive X-ray Analysis (SEM), X-ray Fluorescence Spectrometry, X-ray Diffraction Spectrometry.

SURFACE ANALYSIS METHODS: Scanning Auger Microprobe, Electron Spectroscope/Chemical Analysis, Secondary Ion Mass Spectrometry, Ion Scattering Spectrometry, Ion Microprobe.

The department also maintains ongoing working arrangements with commercial, university, and equipment manufacturers' technical service laboratories, and can obtain any materials analysis in cases where instrumental capabilities are not available in our own facility.

Calibration Laboratory

Another important resource in the product assurance system is Harris Semiconductor's Calibration Lab. This area is responsible for calibrating the electronic, electrical, electro/mechanical, and optical equipment used in both the production and engineering areas. The accuracy of instruments used at Harris in calibration is traceable to the National Bureau of Standards. The lab maintains a system which conforms to the current revision of MIL-STD-45662, "Calibration System Requirements."

Each instrument requiring calibration is assigned a calibration interval based upon stability, purpose, and degree of use. The equipment is labeled with an identification tag on which is specified both the date of the last calibration and of the next required calibration. The Calibration Lab reports on a regular basis to each user department. Equipment out of calibration is taken out of service until calibration is performed. The Quality organization performs periodic audits to assure proper control in the using areas. Statistical procedures are used where applicable in the calibration process.

Failure Analysis Laboratory

The Failure Analysis Laboratory's capabilities encompass the isolation and identification of all failure modes/failure mechanisms, preparing comprehensive technical reports, and assigning appropriate corrective actions. Research vital to understanding the basic physics of the failure is also undertaken.

Failure analysis is a method of enhancing product reliability and determining corrective action. It is the final and crucial step used to isolate potential reliability problems that may have occurred during reliability stressing. Accurate analysis results are imperative to assess effective corrective actions. To ensure the integrity of the analysis, correlation of the failure mechanism to the initial electrical failure is essential.

A general failure analysis procedure has been established in accordance with the current revision of MIL-STD-883, Section 5003. The analysis procedure was designed on the premise that each step should provide information on the failure without destroying information to be obtained from subsequent steps. The exact steps for an analysis are determined as the situation dictates. Records are maintained by laboratory personnel and contain data, the failure analyst's notes, and the formal Product Analysis Report.

Reliability

Reliability Assessment and Enhancement

At Harris Semiconductor, reliability is built into every product by emphasizing quality throughout manufacturing. This starts by ensuring the excellence of the design, layout, and manufacturing process. The quality of the raw materials and workmanship is monitored using statistical process control (SPC) to preserve the reliability of the product. The primary and ultimate goal of these efforts is to provide full performance to the product specification throughout its useful life. Product reliability is maintained through the following sources: Qualifications, In-Line Reliability Monitors, Failure Analysis.

Qualifications

Qualifications at Harris de-emphasize the sole dependence on production product which is only available late in the development cycle. The focus is primarily on the use of test vehicles to establish design ground rules for the product and the process that will eliminate any wearout mechanisms during the useful life of the product. However, to comply with the military requirements concerning reliability, product qualifications are performed.

In-line Reliability Monitors

In-line reliability monitors provide immediate feedback to manufacturing regarding the quality of workmanship, quality of raw materials, and the ultimate reliability implications. The rudimentary implementation of this monitoring is the "First Line of Defense," which is a pass/fail acceptance procedure based on control charts and trend analysis. The second level of monitoring is referred to as the "Early Warning System" and incorporates wafer level reliability concepts for extensive diagnostic and characterization capabilities of various components that may impact the device reliability or stability. The quick feedback from these schemes allows more accurate correlation to process steps and corrective actions.

Failure Analysis

Failure analysis of various product failures provides a means for determining critical failure mechanisms. This information is used to identify those mechanism that should be detectable by qualification procedures or in-line monitors. Failure analysis involves elaborate confirmation of the failure mechanism creating the product malfunction.

Reliability Fundamentals

Reliability, by its nature, is a mixture of engineering and probability statistics. This combination has derived a vocabulary of terms essential for describing the reliability of a device or system. Since reliability involves a measurement of time, it is necessary to accelerate the failures which may occur. This, then, introduces terms like "activation energy" and "acceleration factor," which are needed to relate results of stressing to normal operating conditions (see Table 7). Also, to assess product reliability requires failures. Therefore, only a statistical sample can be used to determine the model of the failure distribution for the entire population of product.

TABLE 7. FAILURE RATE PRIMER

GLOSSARY OF TERMS

TERMS/DEFINITION	UNITS/DESCRIPTION
FAILURE RATE λ For Semiconductors, usually expressed in FITs. Represents useful life failure rate (which implies a constant failure rate). FITs are not applicable for infant mortality or wearout failure rate expressions.	**FIT - Failure In Time** 1 FIT - 1 failure in 10^9 device hours. Equivalent to 0.0001%/1000 hours FITs = $\dfrac{\text{\# Failures}}{\text{\# Devices x \# hours stress x AF}} \times 10^9 \times m$ m - Factor to establish Confidence Interval 10^9 - Establishes in terms of FITs AF - Acceleration Factor at temperature for a given failure mechanism
MTTF - Mean Time To Failure For semiconductors, MTTF is the average or mean life expectancy of a device. If an exponential distribution is assumed then the mean time to fail of the population will be when 63% of the parts have failed.	Mean Time is measured usually in hours or years. 1 Year = 8760 hours When working with a constant failure rate the MTTF can be calculated by taking the reciprocal of the failure rate. MTTF = l/λ (exponential model) Example: =10 FITs at +55°C The MTTF is: MTTF = l/λ = 0.1 x 10^9 hours = 100M hours
CONFIDENCE INTERVAL (C. I.) Establishes a Confidence Interval for failure rate predictions. Usually the upper limit is most significant in expressing failure rates.	Example: "10 FITs @ a 95% C. I. @ 55°C" means *only* that you are 95% certain the the FITs <10 at +55°C use conditions.

Failure Rate Calculations

Reliability data for products may be composed of several different failure mechanisms and requires careful combining of diverse failure rates into one comprehensive failure rate. Calculating the failure rate is further complicated because failure mechanisms are thermally accelerated at varying rates and thereby have differing accelerating factors. Additionally, this data is usually obtained a variety of life tests at unique stress temperatures. The equation below accounts for these considerations and then inserts a statistical factor to obtain the confidence interval for the failure rate.

$$FIT = \left(\sum_{i=1}^{B} \frac{X_i}{\sum_{j=1}^{K} TDH_j \quad AF_{ij}} \right) x\ 10^9 \quad x\ M$$

B = # of distinct possible failure mechanisms

K = # of life tests being combined

X_i = # of failures for a given failure mechanism i = 1, 2, . . . B

TDG_j = Total device hours of test time (unaccelerated) for Life $Test_j$

AF_{ij} = Acceleration factor for appropriate failure mechanism i = 1, 2, . . . K

M = Statistical factor for calculating the upper confidence limit (M is a function of the total number of failures and an estimate of the standard deviation of the failure rates)

In the failure rate calculation, Acceleration Factors (AF_{ij}) are used to derate the failure rate from thermally accelerated Life Test conditions to a failure rate indicative of use temperatures. Though no standards exist, a temperature of +55°C has been popular and allows some comparison of product failure rates. All Harris Semiconductor Reliability Reports will derate to +55°C at both the 60% and 95% confidence intervals.

Acceleration Factors

The Acceleration Factors (AF) are determined from the Arrhenius Equation. This equation is used to describe physiochemical reaction rates and is an appropriate model for expressing the thermal acceleration of semiconductor failure mechanisms.

$$AF = \quad EXP \left[\frac{E_a}{K} \left(\frac{1}{T_{use}} - \frac{1}{T_{stress}} \right) \right]$$

AF = Acceleration Factor

E_a = Thermal Activation Energy in eV from Table 8

K = Boltzmann's Constant (8.62 x 10^{-5} eV/°K)

Both T_{use} and T_{stress} (in degrees Kelvin) include the internal temperature rise of the device and therefore represent the junction temperature. With the use of the Arrhenius Equation, the thermal Activation Energy (E_a) term is a major influence on the result. This term is usually empirically derived and can vary widely.

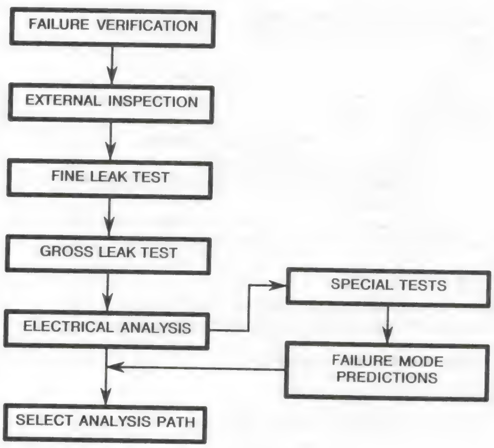


FIGURE 4. NON-DESTRUCTIVE

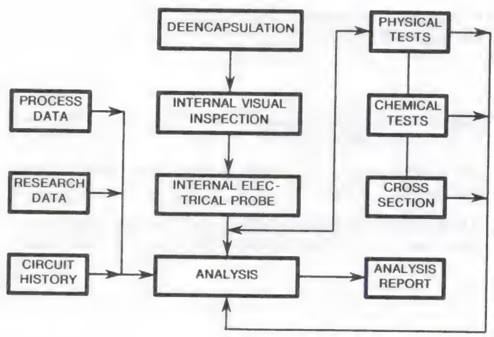


FIGURE 5. DESTRUCTIVE

Activation Energy

To determine the Activation Energy (E_a) of a mechanism (see Table 8) you must run at least two (preferably more) tests at different stresses (temperature and/or voltage). The stresses will provide the time to failure (Tf) for the populations which will allow the simultaneous solution for the Activation Energy by putting the experimental results into the following equations.

$$\ln\ (t_{f1}) = C + \frac{E_a}{KT_1}$$

$$\ln\ (t_{f2}) = C + \frac{E_a}{KT_2}$$

Then, by subtracting the two equations, the Activation Energy becomes the only variable, as shown.

$$\ln(t_{f1}) - \ln(t_{f2}) = E_a/k(1/T1-1/T2)$$

$$E_a = K^* ((\ln(t_{f1}) - \ln(t_{f2}))/(1/T1 - 1/T2))$$

The Activation Energy may be estimated by graphical analysis plots. Plotting ln time and ln temperature then provides a convenient nomogram that solves (estimates) the Activation Energy.

Table 9 is a summary of military generic groups by process descriptions.

All Harris Reliability Reports from qualifications and Group C1 (all high temperature operating life tests) will provide the data on all factors necessary to calculate and verify the reported failure rate (in FITs) using the methods outlined in this primer.

TABLE 8. FAILURE MECHANISM

FAILURE MECHANISM	ACTIVATION ENERGY	SCREENING AND TESTING METHODOLOGY	CONTROL METHODOLOGY
Oxide Defects	0.3 - 0.5eV	High temperature operating life (HTOL) and voltage stress. Defect density test vehicles.	Statistical Process Control of oxide parameters, defect density control, and voltage stress testing.
Silicon Defects (Bulk)	0.3 - 0.5eV	HTOL & voltage stress screens.	Vendor Statistical Quality Control programs, and Statistical Process Control on thermal processes.
Corrosion	0.45eV	Highly accelerated stress tesing (HAST)	Passivation dopant control, hermetic seal control, improved mold compounds, and product handling.
Assembly Defects	0.5 - 0.7eV	Temperature cycling, temperature and mechanical shock, and environmental stressing.	Vendor Statistical Quality Control programs, Statistcal Process Control of assembly processes proper handling methods.
Electromigration - Al Line - Contact	 0.6eV 0.9eV	Test vehicle characterizations at highly elevated temperatures.	Design ground rules, wafer process statistical process steps, photoresist, metals and passivation
Mask Defects/ Photoresist Defects	0.7eV	Mask FAB comparator, print checks, defect density monitor in FAB, voltage stress test and HTOL.	Clean room control, clean mask, pellicles Statistical Process Control or photoresist-/etch processes.
Contamination	1.0eV	C-V stress at oxide/interconnect, wafer FAB device stress test (EWS) and HTOL.	Statistical Process Control of C-V data, oxide/ interconnect cleans, high integrity glassivation and clean assembly processes.
Charge Injection	1.3eV	HTOL & oxide characterization.	Design ground rules, wafer level Statistical Process Control and critical dimensions for oxides.

Qualification Procedures

New products are reliably introduced to market by the proper use of design techniques and strict adherence to process layout ground rules. Each design is reviewed from its conception through early production to ensure compliance to minimum failure rate standards. Ongoing monitoring of reliability performance is accomplished through compliance to 883C and standard Quality Conformance Inspection as defined in Method 5005.

New process/product qualifications have two major requirements imposed. First is a check to verify the proper use of process methodology, design techniques, and layout ground rules. Second is a series of stress tests designed to accelerate failure mechanisms and demonstrate the reliability of integrated circuits.

From the earliest stages of a new product's life, the design phase, through layout, and in every step of the manufacturing process, reliability is an integral part of every Harris Semiconductor product. This kind of attention to detail "from the ground up" is the reason why our customers can expect the highest quality for any application.

TABLE 9. HIGH TEMPERATURE OPERATING LIFE TEST SUMMARY

GROUP C

GENERIC GROUP	GROUP NAME	PROCESS DESCRIPTION	QUANTITY	QUANTITY FAILURE	HOURS @ 125°C	FAILURE RATE FITs @ 55°C 60% CI
D-49-3	Op. Amplifiers	Std. Linear, DI w/NiCr resistors	3482	6	3,215,708	62
D-49-4	Op. Amplifiers	Std. Linear, DI w/NiCr resistors	324	1	429,945	17
D-53	High Voltage Op. Amplifiers	High voltage DI	315	0	284,943	20
D-56	Data Acquisition	High beta high frequency, DI, NiCr	1022	5	1,868,349	100
F-103	Telecommunications	SAJI IVA	199	0	403,960	5
F-81-3	A/D Converters	SAJI IVA	201	0	183,222	10
F-81-4	A/D Converters	SAJI IVA	217	1	328,000	12
F-82	Switches & Mux	DI Al Gate & Si Gate MOS	121	0	82,836	23
F-99-3	Active Filters	SAJI IVA	196	1	184,262	24
F-99-4	Active Filters	SAJI IVA	407	1	470,324	9
G-85	Op. Amplifiers	Std. Linear, MOS, & High Frequency JFET	532	1	535,728	11
G-86	Comparators	Combination, Std. Linear & MOS	154	0	153,400	25
G-94-3	Switches & Mux	DI Al & Si Gate Linear CMOS	4351	41	7,443,054	103
G-94-4	Switches & Mux	DI Al & Si Gate Linear CMOS	906	0	889,816	20
C-41-4	CMOS RAMs	SAJI CMOS	2418	19	2,247,526	31
C-41-5	CMOS RAMs	SAJI CMOS	1104	10	1,105,094	53
C-42-4	CMOS PROMs & HPALs	SAJI CMOS	2645	28	4,074,728	61
C-105-4	Microprocessor and Peripherals	SAJI CMOS	3638	12	4,099,002	17

NOTE: All infant mortality failures (up to 168 hours or equivalent) have been removed from products sampled.

FLOW - PRODUCT DEVELOPMENT	RELIABILITY FOCUS
PRODUCT DEFINITION REVIEW	• Assumes Process Development Required
	* * *
CONCEPT REVIEW	• Evaluate Reliability Risks Factors • Attain Commitment for Test Vehicle (T.V.) Development
	* * *
DESIGN REVIEW PART 1	• Review Test Vehicle Development and Stress Test Plan • Review Package Requirements • Review Latent Failure Mechanism History for Design Sensitivity and Elimination • Review Ground Rules for Design and Elimination of Wearout Mechanisms • Review Process Characterization, Statistical Control & Capability which are Design Considerations
	* * *
DESIGN REVIEW PART 2	• Review Test Vehicle Stress Results • Review Device Modeling & Simulations • Review Process Variability & Producibility • Define Wafer Reliability Monitor Vehicles, Application of Early Warning System
	* * *
LAYOUT REVIEW PART 1	• Verify Wearout Mechanisms are Eliminated by Design & Process Control (Test Vehicle + SPC) • Evaluate Design of Chip to Package Risk Factors • Review Ground Rule Checks (DRCs) • Establish Reliability Test, Stress and Failure Analysis Capabilities. Project Failure Rate Based on T.V. Data.
	* * *
LAYOUT REVIEW 2	• Review Burn-In Diagrams for Production and Qualification • Review Overall Qualification Plan & Begin Balance of Life Test
	* * *
EVALUATION REVIEW	• Review Product Characterization to Data Sheet, ESD, Latch-up & DPA Results & Define Corrective Actions • Review of Life Test Data & Failure Mechanisms. Define Corrective Actions • Utilize Statistical Design of Experiments (DOX) if Required to Adjust Process or Design • Define Necessary Changes to Eliminate Any Systematic Failure Mechanism • If Mature Process - Grant Generic Release
	* * *
NEW PRODUCT TRANSFER	• Qualification Requirements Complete and Presented. Meet FIT Rate Requirements • Review Infant Mortality (I.M.) Burn-in Results. If Greater Than 1% at 125°C Determine I.M. Burn-in Requirements
	* * *
MANUFACTURE	• Reliabiltiy Monitors: ▸ Real Time Early Warning Wafer Level Reliability control ▸ Real Time Reliability Control of Burn-in PDA with Control Charts ▸ Add-On Life Testing: - Mil Std Group C & D - Industrial/Commercial Life Testing • Trend Analysis of Reliability Performance Used to Develop Product Improvements • Special Studies
	* * *
SHIPMENT	• High Quality and Reliability Products to Harris Customers
	* * *
CONTINUOUS IMPROVEMENT	• Failure Analysis - Determine Assignable Cause of Failure • Closed Loop Corrective Action Process • Continuous Improvement Objectives in Product Reliability & Quality

FIGURE 6. NEW PROCESS PRODUCT DEVELOPMENT AND LIFE CYCLE

ANALOG

Application Notes

10

APPLICATION NOTE INDEX

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Application Note Index (Continued)

Application Note Index (Continued)

Application Note Abstracts

AN#	TITLE	ABSTRACTS	PAGE
509	A Simple Comparator Using The HA-2620	Performance characteristics, application schematics, output parameter control methods.	10-9
514	The HA-2400 PRAM Four Channel Operational Amplifier	HA-2400 PRogrammable Analog Microcircuit description, frequency compensation, applications (analog multiplexer, non-inverting programmable gain amplifier, inverting programmable gain amplifier, programmable attenuator, programmable adder-subtractor, phase selector, phase detector, synchronous rectifier, balanced modulator, integrator, ramp generator, track and hold, sample and hold, sine wave oscillator, multivibrator, active filter, programmable power supply, comparator, multiplying D/A converter).	10-10
515	Operational Amplifier Stability: Input Capacitance Considerations	Input capacitance and stability, capacitive feedback compensation, guidelines for compensation requirements.	10-17
517	Applications of a Monolithic Sample and Hold/Gated Op Amp	General Sample and Hold information and fourteen specific applications, including filtered Sample & Hold DAC de-glitcher, Integrate-Hold-Reset, gated op amp, etc.	10-19
519	Operational Amplifiers Noise Prediction.	Noise model and equations, procedure for computing total output noise, example, broadband noise measurement, spot noise prediction techniques, typical spot noise curves, popcorn noise discussion.	10-24
520	CMOS Analog Multiplexers and Switches; Application Considerations	Switch selection criteria, datasheet definitions, care and feeding of multiplexers and switches, digital interface, practical multiplexer applications alternative to CMOS switches and multiplexers.	10-28
521	Getting The Most Out CMOS Devices for Analog Switching Jobs	CMOS versus bipolar device performances, over voltage and channel interaction conditions, JI technology and latch-up, floating-body JI technology, fool-proof CMOS analog multiplexer, other DI benefits.	10-37
522	Digital to Analog Converter Terminology	Explains DAC terminology, Resolution Gain Error, Offset Error, Linearity Error, Differential Linearity Error, Drift, Settling Time, etc.	10-44
524	Digital to Analog Converter High Speed ADC Applications	Use of High Speed DAC's in tracking, servo, and successive approximation Analog to Digital Converters. Design ideas for Data Acquisition Systems.	10-47
525	HA-5190/5195 Fast Settling Operational Amplifier	Internal schematic, prototyping considerations, frequency compensation, performance enhancement methods, applications.	10-50
526	HA-5190/5195 Video Applications	Video applications, video response tests, S/N ratio measurements, power supply requirements temperature considerations, design hints, prototyping tips, RF AGC amplifier, DC gain controlled video amplifier.	10-54
531	Analog Switch Applications in A/D Data Conversion Systems	System configurations, analog switch types, CMOS switch selection guidelines, alternate uses of CMOS switches.	10-59

Application Note Abstracts (Continued)

AN#	TITLE	ABSTRACTS	PAGE
532	Common Questions Concerning CMOS Analog Switches	Power supply considerations, input overvoltage protection, single supply operation, various questions about Harris D.I. switches.	10-63
534	Additional Information on the HI-300 Series Switch	"ON" resistance, leakage currents, switching speeds, power supply requirements, internal switch operation and schematics, single supply operation, charge injection, power supplies conditions and protective circuitry.	10-67
535	Design Considerations for a Data Acquisition System (DAS)	A collection of guidelines for the design of a Data Acquisition System. Includes signal conditioning, transducers, single-ended vs. differential signal paths, low level signals, filters, Programmable Gain Amplifiers, sampling rate, and computer interfacing.	10-72
538	Monolithic Sample/Hold Combines Speed and Precision	Description and electrical specifications for the HA-5320 Sample/Hold Amplifiers, explanation of errors sources, and HA-5320 applications.	10-79
540	HA-5170 Precision Low Noise J-FET Input Operational Amplifier	Internal design and technology, J-FET noise discussion, trimming of offset voltage, single op amp Instrumentation Amplifier, sine wave oscillator, high impedance transducer interface, current source/sink and current sense circuits.	10-85
541	Using HA-2539/2540 Very High Slew-Rate Wideband Operational Amplifiers	Prototyping considerations, output short circuit protection, offset voltage adjustment, frequency compensation, composite amplifier scheme, DC error reduction, boosting output current, increasing output signal swing, cascade amplifier, video gain block, high frequency oscillator, wideband signal splitter.	10-89
543	New High Speed Switch Offers Sub-50ns Switching Times	Application enhancement using the HI-201HS, high speed multiplexers, high speed sample and hold, analog switch and op amp circuitry, integrator with start/reset, low pass filter with select break frequency, amplifier with programmable gain, future applications.	10-93
544	Micropower Op Amp Family, HA-514X, HA-515X	Operation, noise performance, applications (remote sensor loop transmitter, charge pool power supply, low power microphone preamplifier, AGC with squelch control, Wein bridge oscillator, bar code scanner, monostable multivibrator).	10-100
546	A Method of Calculating HA-2625 Gain Bandwidth Product vs. Temperature	A method of calculating Gain Bandwidth product performance versus temperature for the HA-2625 Op Amp.	10-106
548	A Designer's Guide for the HA-5033 Video Buffer	Operation, video performance, video parameter specifications, Y parameters, applications (flash converter pre-driver, coaxial line driver, video gain block, high speed sample and hold, audio drivers, crystal oscillator).	10-110

Application Note Abstracts (Continued)

APP NOTE

FOR YOUR INFORMATION

No. 509

Harris Analog

A SIMPLE COMPARATOR USING THE HA-2620

G. G. Miller

The input current and impedance of a comparator circuit frequently loads the source and reference signals enough to cause significant errors. This problem is frequently eliminated by using a high impedance operational amplifier between the signal and the comparator. Figure 1 shows a simple circuit in which the operational amplifier is used as a comparator which is capable of driving approximately ten logic gates. The input impedance of the HA-2620 is typically 500 MΩ. The input current is typically 1 nA. The minimum output current of 15 mA is obtainable with an output swing of up to ±10 volts.

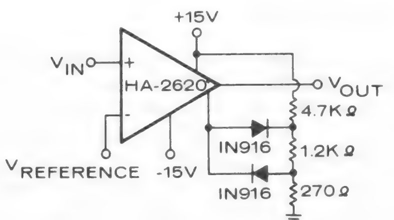


FIGURE 1 - HIGH IMPEDANCE COMPARATOR

The bandwidth control point is a very high impedance point having the same voltage as the amplifier output. The output swing can be conveniently limited by clamping the swing of the bandwidth control point. The maximum current through the clamp diodes is approximately 300 μA. The switching time is dependent on the output voltage swing and the stray capacitance at the bandwidth control point.

Figure 2 shows the waveforms for the comparator. The stray capacitance at the bandwidth control point can be reduced considerably below that of the breadboard circuit; this would improve the switching time. The switching time begins to increase more rapidly as the overdrive is reduced below 10 mV and is approximately 1μs for an overdrive of 5 mV. Dependable switching can be obtained with an overdrive as small as 1 mV. However, the switching time increases to almost 12 μs.

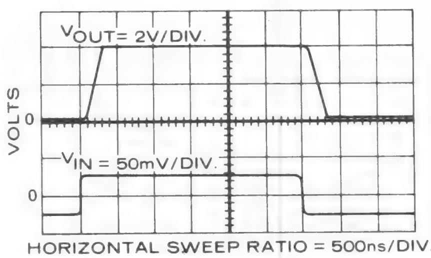


FIGURE 2 - WAVEFORMS FOR HA-2620 COMPARATOR

A common mode range of ±11 volts and a differential input range of ±12 volts makes the HA-2620 a very versatile comparator. The HA-2620 can sink or supply a minimum of 15 mA. The ability to externally clamp the output to any desired range makes the HA-2620 a very flexible comparator which is capable of driving unusual loads.

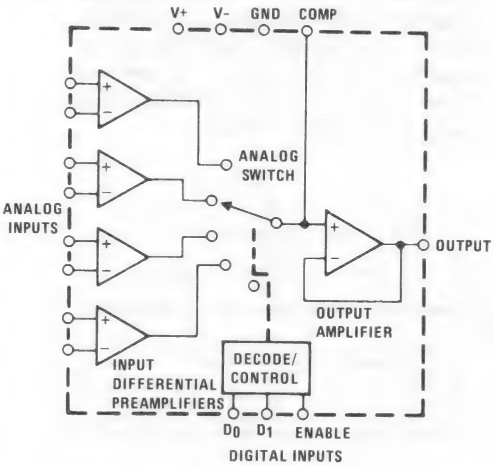
No. 514 Harris Analog

THE HA-2400 PRAM FOUR CHANNEL OPERATIONAL AMPLIFIER

By Don Jones

Introduction

Harris Semiconductor has announced a new linear device, the HA-2400/HA-2405 Four Channel Operational Amplifier. This combines the functions of an analog switch and a high performance operational amplifier, and makes practical a large number of new linear circuit applications.



A functional diagram of the HA-2400 is shown above. There are four preamplifier sections, one of which is selected through the DTL/TTL compatible inputs and connected to the output amplifier. The selected analog input terminals and the output terminal form a high performance operational amplifier.

In actuality, the circuit consists of four conventional op-amp input circuits connected in parallel to a conventional op-amp output circuit. The decode/control circuitry furnishes operating current only to the selected input section.

Circuit Connections

These input control the selection of the amplifier input channels in accordance with the truth table below:

GAIN, VOLTS/VOLT NON-INVERTING	INVERTING	C_{COMP} pF	BANDWIDTH (TYPICAL) (-3dB), MHz	SLEW RATE (TYPICAL) VOLTS/μs
1	–	15	8.0	15
2	1	7	8.0	20
3	2	4	8.0	22
5	4	3	6.0	25
8	7	2	5.0	30
>10	>9	0	40 ÷ GAIN	50

The digital inputs can be driven with any DTL or TTL circuit which uses a standard +5.0V supply.

Compensation

Frequency compensation for closed loop stability is recommended for closed loop gains less than 10. This is accomplished by connection of a single external capacitor from Pin 12 to A. C. ground (the V+ supply is recommended). The following table shows the minimum suggested compensation for various closed loop gains, with the resultant bandwidth and slew rate. Obviously, when the four channels are connected with different feedback networks, the channel with the lowest closed loop gain will govern the required compensation.

D_1	D_0	ENABLE	CHANNEL 1	CHANNEL 2	CHANNEL 3	CHANNEL 4
L	L	H	ON	OFF	OFF	OFF
L	H	H	OFF	ON	OFF	OFF
H	L	H	OFF	OFF	ON	OFF
H	H	H	OFF	OFF	OFF	ON
L or H	L or H	L	OFF	OFF	OFF	OFF

$0V \leq L \leq +0.8V$ $+2.0V \geq H \geq +5.0V$

Compensation capacitors of greater value can be used to obtain lower bandwidth, greater

phase margin, and reduced overshoot, at the expense of proportionately reduced slew rate.

External lead-lag networks could also be used to optimize bandwidth and/or slew rate at a particular gain.

Applications

Any circuit function which can be constructed using a conventional operational amplifier can also be constructed using any channel of the HA-2400. Similar or different networks can be wired from the output to each channel input pair. The device can therefore be used to select and condition different input signals, or to select between different op-amp functions to be performed on a single input signal.

To wire a particular op-amp function to a channel, simply connect the appropriate network between the two inputs for that channel and the common output in the same manner as in wiring a conventional op-amp. It is often possible to design with fewer external components than would be required in wiring four separate op-amps (see Application Numbers 2 and 3 on the following pages). It should be remembered that the networks for unselected channels may still constitute a load at the amplifier output and the signal input, as if the unselected input terminals were disconnected from the network.

If offset adjustment is required, it can generally be accomplished by resistive summation at either of the inputs for each channel (see Application Number 8).

The analog input terminals of the OFF channels draw the same bias current as the ON inputs. The maximum differential input voltage of these terminals must be observed and their voltage levels must never exceed the supply voltages.

When the Enable input is held low, all four input channels are disconnected from the output. When this occurs, the output voltage will generally slowly drift towards the negative supply. If a zero volt output condition is required, one channel should be wired as a voltage follower with its positive input grounded.

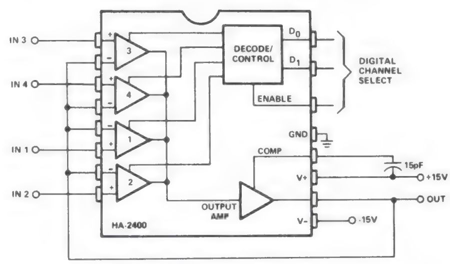
The amplifier output impedance remains low, even when the inputs are disabled; so it is not generally practical to wire the outputs of two or more devices directly together. The compensation pins of two devices, however, could be wired together to produce a switch with one output and more than four input channels.

The voltage at the compensation pin is about 0.7V more positive than the output signal, but has a very high source impedance. Maximum current from this pin is about 300μA, which makes it a convenient point for limiting the output swing through clamping diodes and divider networks (see Application Number 13).

Even if the application only requires a single channel to be switched on and off, it is often more economical to use the HA-2400, rather than a separate analog switch and high performance op-amp. Unused analog channel inputs should be grounded. Unused digital inputs may be wired to ground for a permanent "low" input, or either left open or wired to +5.0V for a permanent "high" input.

Illustrated on the following pages are a few of the thousands of possible applications for the Four Channel Operational Amplifier. These will give the reader a general impression of how the units can be connected; and probably will help generate many other ideas for applications. Also included are some "challenges" for the reader to modify the illustrated designs to perform different functions.

Applications No. 1



ANALOG MULTIPLEXER WITH BUFFERED INPUT AND OUTPUT

This circuit is used for analog signal selection or time division multiplexing. As shown, the feedback signal places the selected amplifier channel in a voltage follower (non-inverting unity gain) configuration, and provides very high input impedance and low output impedance. The single package replaces four input buffer amplifiers, four analog switches with decoding, and one output buffer amplifier.

For low level input signals, gain can be added to one or more channels by connecting the (−) inputs to a voltage divider between output and ground. Bandwidth is approximately 8 MHz, and the output will slew from one level to another at about 15.0V per microsecond.

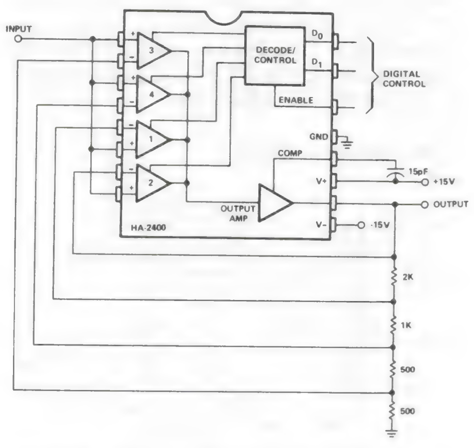
Expansion to multiplex 5 to 12 channels can be accomplished by connecting the compensation pins of two or three devices together, and using the output of only one of the devices. The Enable input on the unselected devices must be low.

Expansion to 16 or more channels is accomplished in a straightforward manner by connecting outputs of 4 four-channel multiplexers to the inputs of another four-channel multiplexer.

Differential signals can be handled by two identical multiplexers addressed in parallel.

Inverting amplifier configurations can also be used, but the feedback resistors may cause crosstalk from the output to unselected inputs.

Applications No.2



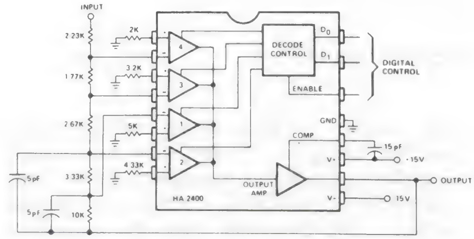
AMPLIFIER, NON-INVERTING PROGRAMMABLE GAIN

This is a non-inverting amplifier configuration with feedback resistors chosen to produce a gain of 0, 1, 2, 4, or 8 depending on the Digital Control inputs.

Comparators at the output could be used for automatic gain selection for auto-ranging meters, etc.

CHALLENGE: Design a circuit using only two HA-2400's which can be programmed to any of 16 different gains.

Applications No.3

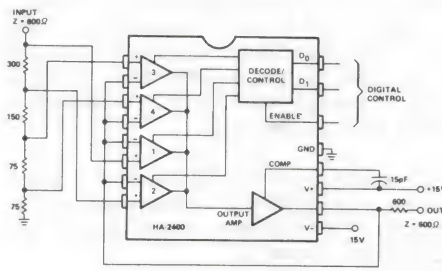


AMPLIFIER, INVERTING PROGRAMMABLE GAIN

The circuit above can be programmed for a gain of 0, −1, −2, −4 or −8.

This could also have been accomplished with one input resistor and one feedback resistor per channel in the conventional manner, but this would require eight resistors rather than five.

Applications No.4

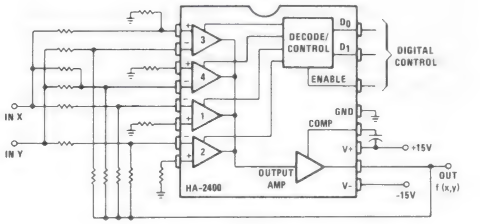


ATTENUATOR PROGRAMMABLE

This circuit performs the function of dividing the input signal by a selected constant (1, 2, 4, 8, or ∞ as illustrated). To multiply by a selected constant, see circuit No. 2. While T, π, or L sections could be used in the input attenuator, this is not necessary since the amplifier loading is negligible and a constant input impedance is maintained. The circuit is thus much simpler and more accurate than the usual method of constructing a constant impedance ladder and switching sections in and out with analog switches.

Two identical circuits may be used to attenuate a balanced line.

Applications No.5

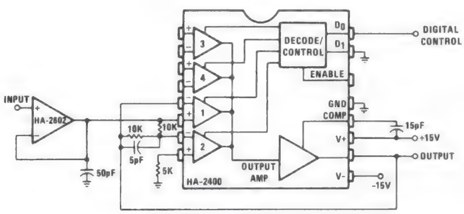


ADDER/SUBTRACTOR PROGRAMMABLE FUNCTION

The circuit shown above can be programmed to give the output functions $-K_1X$, $-K_2Y$, $-(K_3X + K_4Y)$, or $K_5X - K_6Y$. Obviously, many other functions of one or more variables can be constructed, including combinations with analog multiplier or logarithmic modules.

This device opens up many new design approaches in digitally controlled analog computation or signal manipulation.

Applications No.6

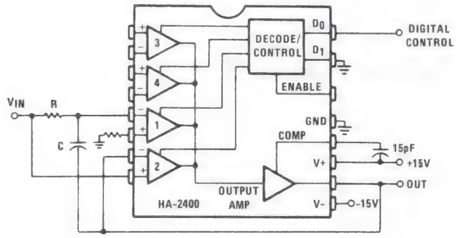


PHASE SELECTOR/PHASE DETECTOR/
SYNCHRONOUS RECTIFIER/BALANCED MODULATOR

This circuit passes the input signal at unity gain, either unchanged, or inverted depending on the Digital Control input. A buffered input is shown, since low source impedance is essential. Gain can be added by modifications to the feedback networks. Signals up to 100 kHz can be handled with 20.0V peak-to-peak output. The circuit becomes a phase detector by driving the Digital Control input with a reference phase at the same frequency as the input signal, the average D. C. output being proportional to the phase difference, with zero volts at $^{+}90^{o}$. By connecting the output to a comparator, which in turn drives the Digital Control, a synchronous full-wave rectifier is formed.

With a low frequency input signal and a high frequency digital control signal, a balanced (surpressed carrier) modulator is formed.

Applications No.7

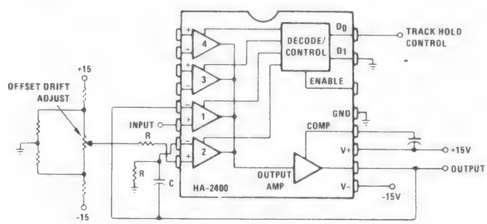


INTEGRATOR/RAMP GENERATOR
WITH INITIAL CONDITION RESET

It is difficult in practice to set the initial conditions accurately in an integrator. This usually requires wiring contacts of a mechanical relay across the capacitor - - leakage currents of solid state switches produce integration inaccuracy. The scheme shown above eliminates these reliability and accuracy problems.

Channel 1 is wired as a conventional integrator, Channel 2 as a voltage follower. When Channel 2 is switched on, the output will follow V_{IN}, and C will discharge to maintain zero volts across it. When Channel 1 is then switched on the output will initially be at the instantaneous value of V_{IN}, and then will commence integrating towards the opposite polarity. This circuit is particularly suitable for timing ramp generation using a fixed D. C. input. Many variations are possible, such as programmable time constant integrators.

Applications No.8



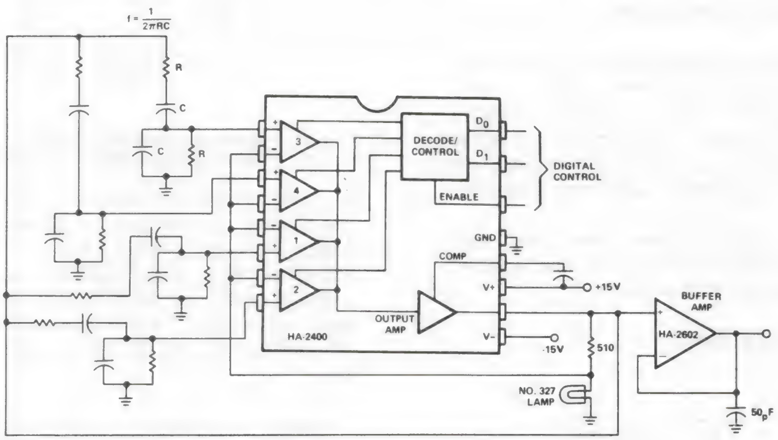
TRACK AND HOLD/SAMPLE AND HOLD

Channel 1 is wired as a voltage follower and

is turned on during the track/sample time. If the product of R x C is sufficiently short compared to the period of maximum output frequency, or sample time, C will charge to the output level. Channel 2 is an integrator with zero input signal. When Channel 2 is then turned on, the output will remain at the voltage across C.

An even simpler circuit can be made by wiring one channel as an amplifier, choosing the compensation capacitor to yield the minimum required bandwidth or slew rate. When the Enable input is pulled low, the output will tend to remain at its last level, because of the charge remaining on the compensating capacitor.

Applications No.9

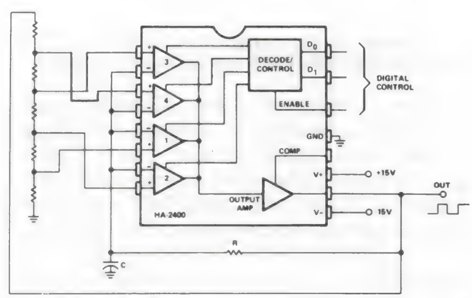


SINE WAVE OSCILLATOR PROGRAMMABLE FREQUENCY

Any oscillator which can be constructed using an op-amp, such as the twin-T, phase shift, crystal controlled types, etc. can be made programmable by using the HA-2400. Illustrated above is a Wien Bridge type, which is very popular for signal generators, since it is easily tunable over a wide frequency range, and has a very low distortion sine wave output. The frequency determining networks can be designed from about 10Hz to greater than 1MHz. Output level is about 6.0V RMS. By substituting a programmable attenuator (Circuit No. 4) for the Buffer Amplifier, a very versatile sine wave source for automatic testing, etc. can be constructed.

CHALLENGE: A high Q, narrow band filter can be made by feeding back greater than 1/3 of the output to the negative input. Design a circuit using the HA-2400 and an RC network which can be programmed either to generate or to detect an audio tone of the same frequency. Such a circuit would be quite useful for data communications.

Applications No.10



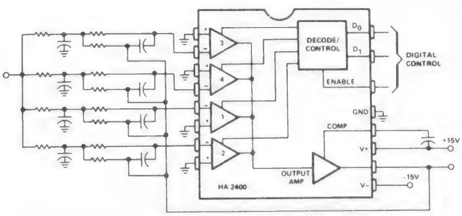
MULTIVIBRATOR, FREE RUNNING, PROGRAMMABLE FREQUENCY

This is the simplest of any programmable oscillator circuit, since only one stable timing capacitor is required. The output square wave is about 25.0V peak-to-peak and has

rise and fall times of about 0.5 μs. If a programmable attenuator circuit (No. 4) is placed between the output and the divider network, 16 frequencies can be produced with two HA-2400's and still only one timing capacitor.

A precision programmable square-triangle generator can also be constructed by adapting circuit described in Harris Application Note 507 to the HA-2400.

Applications No.11



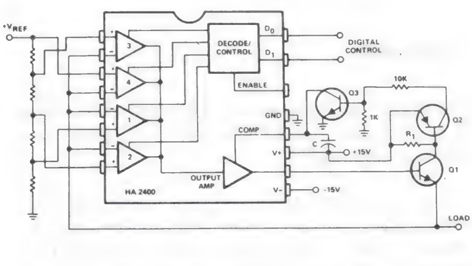
ACTIVE FILTER PROGRAMMABLE

Shown above is a second order low pass filter with programmable cutoff frequency. This circuit should be driven from a low source impedance since there are paths from the output to the input through the unselected networks.

Virtually any filter function which can be constructed with a conventional op-amp can be made programmable with the HA-2400.

A useful variation would be to wire one channel as a unity gain amplifier, so that one could select the unfiltered signal, or the same signal filtered in various manners. These could be cascaded to provide a wide variety of programmable filter functions.

Applications No.12

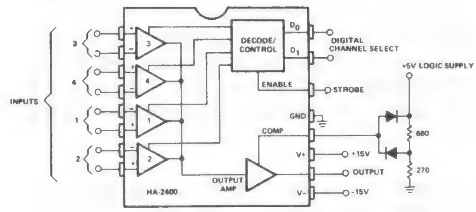


POWER SUPPLY PROGRAMMABLE

Many systems require one or more relatively low current voltage sources which can be programmed to a few predetermined levels. It is no longer necessary to purchase a programmable power supply with far more capability than needed. The circuit shown above produces positive output levels, but could be modified for negative or bipolar outputs. Q1 is the series regulator transistor, selected for the required current and power capability. R1, Q2 and Q3 form an optional short circuit protection circuit, with R1 chosen to drop about 0.7V at the maximum output current. The compensation capacitor, C. should be chosen to keep the overshoot, when switching, to an acceptable level.

CHALLENGE: Design a supply using only two HA-2400's which can be programmed to 16 binary weighted (or 10 BCD weighted) output levels.

Applications No.13



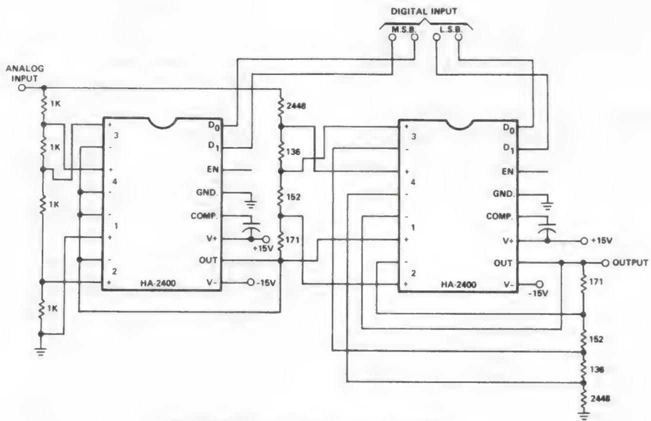
COMPARATOR, FOUR CHANNEL

When operated open loop without compensation, the HA-2400 becomes a comparator with four selectable input channels. The clamping network at the compensation pin limits the output voltage to allow DTL or TTL digital circuits to be driven with a fanout of up to ten loads.

Output rise and fall times will be about 100ns for differential input signals of several hundred millivolts, but will be in the microsecond region for small differential signals.

The circuit can be used to compare several signals against each other or against fixed references; or a single signal can be compared against several references. A "window comparator", which assures that a signal is within a voltage range, can be formed by monitoring the output polarity while rapidly switching between two channels with different reference inputs and the same signal input.

Applications No. 14



MULTIPLYING D TO A CONVERTER

The circuit above performs the function, $V_{OUT} = V_{IN} \cdot \frac{N}{16}$, where N is the binary number from 0 to 15 formed by the digital input. If the analog input is a fixed D.C. reference, the circuit is a conventional 4-bit D to A. The input could also be a variable or A.C. signal, in which case the output is the product of the analog signal and the digital signal.

The circuit on the left is a programmable attenuator with weights of 0, 1/4, 1/2 or 3/4. The circuit on the right is a non-inverting adder which adds weights to the first output of 0, 1/16, 1/8 or 3/16.

If four quadrant multiplication is required, place the Phase Selector circuit (No. 6) in series with either the analog input or output. The D_0 input of that stage becomes the + or – sign bit of the digital input.

More Challenges

One of our favorite college textbooks paused at each climactic point with a statement to the effect that, "Proof of the following theorem is omitted, and is suggested as an exercise for the student."

The following is a list of some additional applications in which we believe the HA-2400 will prove very valuable. The "proofs", at present, remain as exercises for our ingenious readers.

- A to D Converter, Dual Slope Integrating
- Active Filter, State Variable Type with Programmable Frequency and/or Programmable "Q"
- Amplifier with Programmable D.C. Level Shift
- Chopper Amplifiers
- Crossbar Switches
- Current Source, Programmable
- F.M. Stereo Modulator
- F.S.K. Modem
- Function Generators, Programmable
- Gyrator, Programmable
- Monostable Multivibrator, Programmable
- Multiplier, Pulse Averaging
- Peak Detector with Reset
- Resistance Bridge Amplifier/Comparator with Programmable Range
- Sense Amp/Line Receiver with Programmable Threshold
- Spectrum Analyzer, Scanning Type
- Sweep Generator, Programmable
- Switching Regulator
- Touch-Tone™ Generator/Detector (Use Harris HD-0165 Keyboard Encoder I.C.)

Feedback

We believe we have only scratched the surface of possible applications for a multiple channel operational amplifier.

If you have a solution for any of the previous "challenges" or any new application, please let us know. Anything from a one word description to a tested design will be welcome.

APP NOTE

FOR YOUR INFORMATION

No. 515

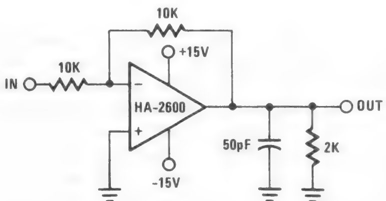
Harris Analog

OPERATIONAL AMPLIFIER STABILITY: INPUT CAPACITANCE CONSIDERATIONS

Author: Don Jones

This note deals with stabilization and optimization of A.C. response in operational amplifiers. One of the more common difficulties in applying operational amplifiers will be discussed.

Let's consider the unity gain inverting amplifier circuit shown below:



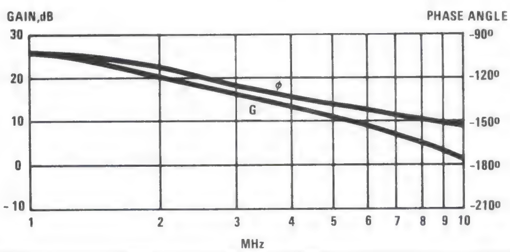
This appears to be a straightforward application with reasonable component values.

But, with the input grounded, the circuit output shows an oscillation at about 5MHz.

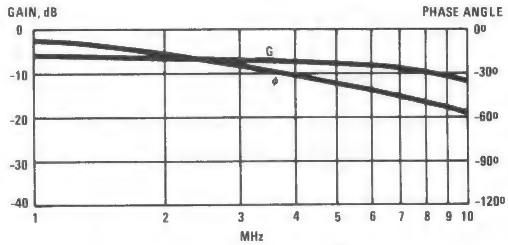
Even more surprising, if the same device is connected as a voltage follower with the same load, it is perfectly stable. Since the inverting amplifier has 6dB less feedback than the voltage follower, shouldn't it be more stable?

The culprit here is capacitance at the amplifier inverting input. The HA-2600 in the TO-99 can has an input capacitance of about 2 or 3pF. When soldered on a P.C. card, or inserted in a socket, wiring capacitance might add another 3 to 6pF. With only 5K effective resistance at this point, 5 to 10pF seems pretty negligible, doesn't it? But let's find out.

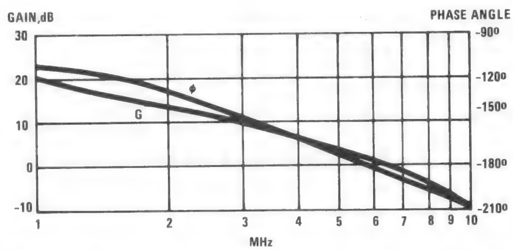
The open loop amplitude and phase response characteristics of the amplifier between 1 and 10MHz looks like this:



The characteristics of the feedback network alone with 5pF capacitance to ground looks like this:

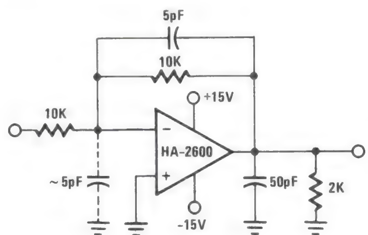


Combining these two graphs by algebraically adding the dB gains together and adding the phase shifts together gives us the open loop response at the summing point:



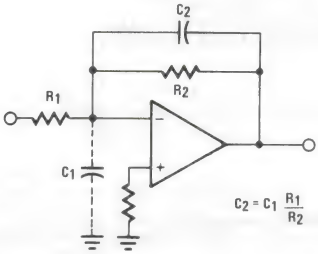
We can see that on the composite response curves, the phase shift crosses 180° at 5.5MHz, and that there is still about +2dB of gain at this frequency. Therefore, closing the loop automatically creates an oscillator.

How can we overcome this effect? If we add a capacitor across the feedback resistor, we can cancel the effects of the input capacitance:



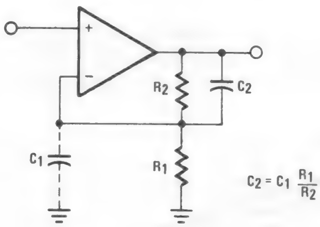
If the feedback capacitance matches the input capacitance, the response curves of the feedback network alone will be a flat -6dB and 0° across the frequency band. The composite curves will then show a bandwidth of 7.5MHz and a positve phase margin of 33°. So the circuit will now be quite stable. It's amazing how much difference that small capacitance can make.

The general scheme for compensation of various circuit types is shown below:

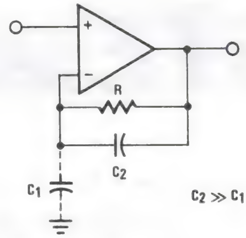


(Include high frequency source impedance in R_1.)

INVERTING AMPLIFIER



NON-INVERTING AMPLIFIER



FOLLOWER WITH FEEDBACK RESISTOR

It's not really necessary to know the exact value of stray capacitance, C_1 for most layouts, about 5 to 10pF is a good guess. Unless you are trying to squeeze out the last Hz of frequency response, it doesn't hurt to guess on the high side. At higher gains, where C_2 calculates out to less than 1 or 2pF, it isn't necessary to use C_2 — but it won't disturb anything if you do use it.

If you are uncertain about whether compensation is necessary, check the pulse response or frequency response of the closed loop stage. Hook a pulse generator to the input, and adjust the amplitude for about a 200 millivolt step at the output — if the output overshoot is less than 40% of the step, the circuit will be stable. Alternately, check the small signal frequency response of the stage if the high frequency peaking is less than +6dB, more than the low frequency gain, the circuit is stable. Of course, you can increase the compensation capacitor if you need even smoother response.

The phenomena we have described are not peculiar to any one amplifier type. Wideband amplifiers require a little more care in the design of feedback networks; but the same type oscillations will show up on 741 type amplifiers with higher feedback resistor values.

APP NOTE

FOR YOUR INFORMATION

No. 517

Harris Analog

APPLICATIONS OF MONOLITHIC SAMPLE-AND-HOLD AMPLIFIERS

DON JONES AND AL LITTLE

Introduction

The sample-and-hold or track-and-hold function is very widely used in linear systems. This function is readily available in modular, hybrid, and monolithic form.

All high quality sample-and-hold circuits must meet certain requirements:

(1) The holding capacitor must charge up and settle to its final value as quickly as possible.

(2) When holding, the leakage current at the capacitor must be as near zero as possible to minimize voltage drift with time.

(3) Other sources of error must be minimized.

Design of a sample-and-hold involves a number of compromises in the above requirements. The amplifier or other device feeding the analog switch must have high current capability and be able to drive capacitive loads with stability. The analog switch must have both low ON resistance and extremely low OFF leakage currents. But, leakage currents of most analog switches (except the dielectrically isolated types) run to several hundred nanoamperes at elevated temperatures. The analog switch must have very low coupling between the digital input and analog output, because any spikes generated at the instant of turn-off will change the charge on the capacitor. The output amplifier must have extremely low bias current over the temperature range, and also must have low offset drift and sufficient slew rate.

Another design consideration is whether to make the input differential or single ended. A single ended sample/hold amplifier has a fixed gain, usually +1, so that it simply provides the sample/hold function. In contrast, a differential input sample-and-hold amplifier is designed to be configured with external feedback, just like an op amp. It may be used to form a filter, integrator, inverting or non-inverting amplifier with gain, etc. This allows the designer to combine any number of op amp signal conditioning circuits with the sample-and-hold function. All Harris sample-and-hold amplifiers are designed with differential inputs to take advantage of this capability.

The HA-2420/2425

The HA-2420/2425 is one of the most versatile monolithic sample-and-hold integrated circuits. A functional diagram is shown in Figure 1.

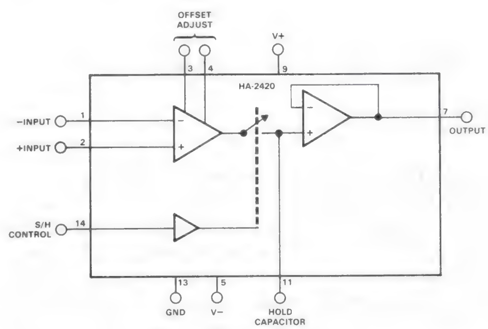


FIGURE 1 - HA-2420/2425 FUNCTIONAL DIAGRAM

The input amplifier stage is a high performance operational amplifier with excellent slew rate, and the ability to drive high capacitance loads without instability. The switching element is a highly efficient bipolar transistor stage with extremely low leakage in the OFF condition. The output amplifier is a MOSFET input unity gain follower to achieve extremely low bias current.

MOSFET inputs are generally not used for D.C. amplifiers because their offset voltage drift is difficult to control. In this configuration, however, negative feedback is generally applied between the output and inputs of the entire device, and the effect of this offset drift at the inputs is divided by the open loop gain of the input amplifier stage.

10

APPLICATION NOTES

The HA-5320

The HA-5320 is a high speed monolithic sample/hold circuit which includes its own 100pF hold capacitor. Unlike the HA-2420/2425, this device utilizes an input transconductance amplifier and an integrating output stage as shown in Figure 2. The hold capacitor is charged through a low leakage analog switch at the virtual ground node of the output amplifier. In this configuration, charge injection at the transition from sample to hold is constant over the entire input/output voltage range. Additional hold capacitance may be added to the HA-5320 for improved droop rate, at the expense of increased acquisition time.

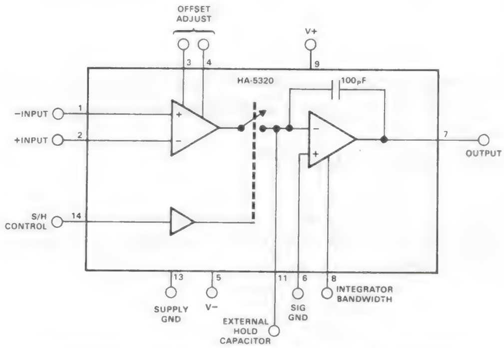


FIGURE 2 - HA-5320 FUNCTIONAL DIAGRAM

The HA-5330

The HA-5330 is a monolithic sample/hold amplifier optimized for very high speed performance, acquiring a 10V step to 0.01% in 500ns. Its circuit topology is similar to the HA-5320 (Figure 3), but there is no provision for external capacitance. The integrated 90pF capacitor provides excellent performance alone; external leakage paths and noise pickup are avoided in this design by not exposing the integrator input node to an external pin.

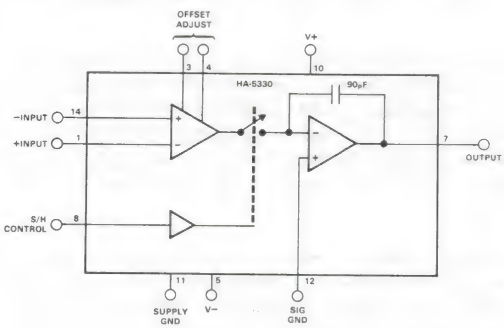


FIGURE 3 - HA-5330 FUNCTIONAL DIAGRAM

Sample-Hold-Hold Applications

A number of basic applications are shown on the following pages. These devices are exceptionally versatile, since they can be wired into any of the hundreds of feedback configurations possible with any operational amplifier. In many applications the device will replace both an operational amplifier and a sample-and-hold module.

The larger the value of the hold capacitor, the longer time it will hold the signal without excessive drift; however, it will also reduce the charging rate/slew rate and the amplifier bandwidth during sampling. So the capacitance value must be optimized for each particular application. Drift during holding tends to double for every 10°C rise in ambient temperature. The holding capacitor should have extremely high insulation resistance and low dielectric absorption-polystyrene (below +85°C), Teflon, or mica types are recommended.

For least drift during holding, leakage paths on the P.C. board and on the device package surface must be minimized. The output voltage is nearly equal to the voltage on C_H for the HA-2420. The output line may be used as a guard ring surrounding the line to C_H. Since the potentials are nearly equal, very low leakage currents will flow. The two package pins surrounding the C_H pin are not internally connected, and may be used as guard pins to reduce leakage on the package surface. A suggested P.C. guard ring layout is shown in Figure 4. The hold capacitor in the HA-5320 operates at virtual ground. For this device, a guard ring must be connected to the SIG GND terminal (pin 6) instead of the output.

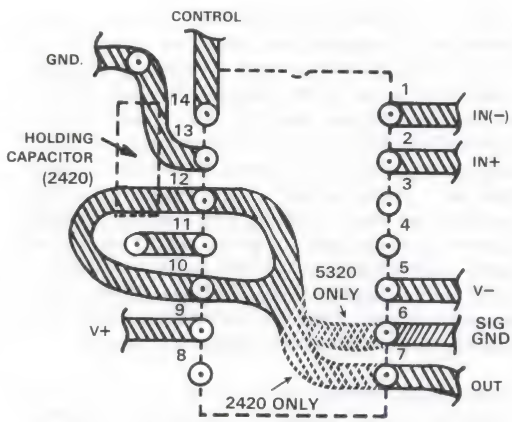


FIGURE 4 - GUARD RING LAYOUT (BOTTOM VIEW)

Since the internal hold capacitor is not accessable in the HA-5330, no P.C. layout consideration to minimize leakage is necessary.

Although the hold capacitor is configured differently for the

three sample/hold devices as shown in Figure 5, most applications are common to all. For simplicity, the hold capacitor has been excluded from circuit diagrams in the following examples and the S/H's are depicted as op amps with a sample/hold control. This symbol is intended to remind the user of the "op amp" capability of these devices.

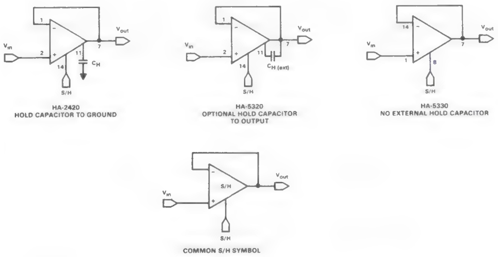


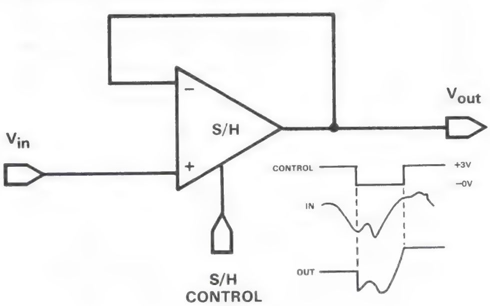
FIGURE 5 - SIMPLIFIED S/H SYMBOL (UNITY GAIN CONFIGURATION)

Application No. 1

Feedback is the same as a conventional op amp voltage follower which yields a unity gain, non-inverting output. This hookup also has a very high input impedance.

The only difference between a track-and-hold and a sample-and-hold is the time period during which the switch is closed. In track-and-hold operation, the switch is closed for a relatively long period during which the output signal may change appreciably; the output will hold the level present at the instant the switch is opened. In sample-and-hold operation, the switch is closed only for the period of time necessary to fully charge the holding capacitor.

BASIC TRACK-AND-HOLD/SAMPLE-AND-HOLD



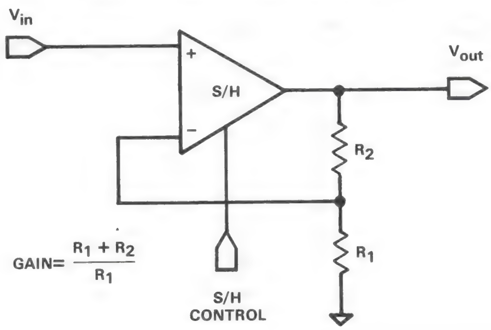
Application No. 2

This is the standard non-inverting amplifier feedback circuit.

It illustrates one of the many ways in which a sample/hold amplifier may be used to perform both op amp and sampling functions, eliminating the need for a separate scaling amplifier and sample-and-hold module.

In general, it is usually best design practice to scale the gain such that the largest expected signal will give an output close to + or − 10 volts. Drift current is essentially independent of output level, and less percentage drift will occur in a given time for a larger output signal.

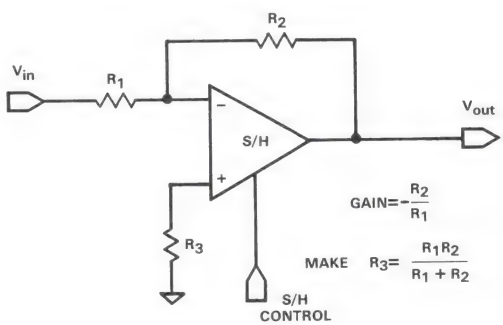
SAMPLE-AND-HOLD WITH GAIN



Application No. 3

This illustrates another application in which the hookup versatility of a sample/hold often eliminates the need for a separate operational amplifier and sample-and-hold module. This hookup will have somewhat higher input to output feedthrough during "hold," than the non-inverting connection, since output impedance is the open-loop value during "hold," and feedthrough will be: $\frac{V_{IN} R_O}{R_1 + R_2 + R_O}$

INVERTING SAMPLE-AND-HOLD

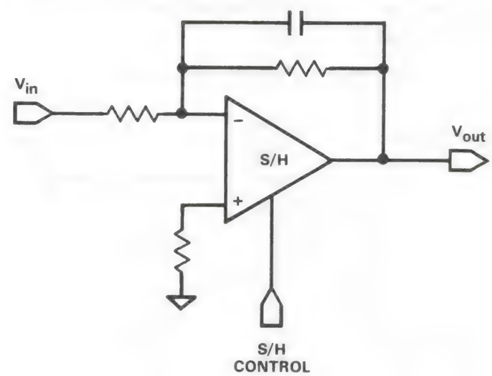


Application No. 4

It is often required that a signal be filtered prior to sampling. This can be accomplished with only one device. Any of the inverting and non-inverting filters which can be built with op

amps can be implemented. However, it is necessary that the sampling switch be closed for sufficient time for the filter to settle when active filter types are connected around the device.

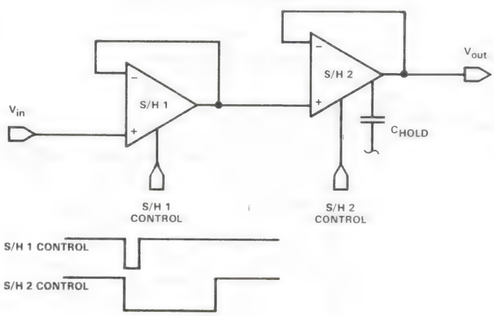
FILTERED SAMPLE-AND-HOLD



Application No. 5

Short sample times require a low value holding capacitor, while long, accurate hold times require a high value holding capacitor. So, achieving a very long hold with a short sample appears to be contradictory. However, it can be accomplished by cascading two S/H circuits, the first with a low value capacitor, the second with a high value. Then the second S/H can sample for as long a time as the first circuit can accurately hold the signal.

CASCADED SAMPLE-AND-HOLD



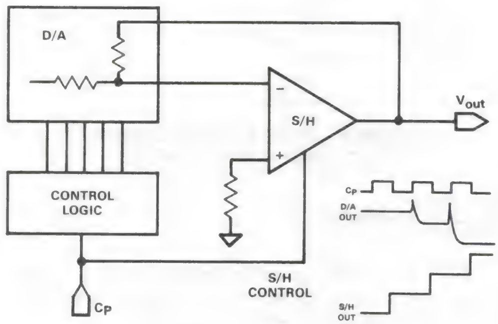
Application No. 6

The word "glitch" has been a universal slang expression among electronics people for an unwanted transient condition. In D to A converters, the word has achieved semi-official status for an output transient which occurs when the digital input address is changed.

In the illustration, the sample/hold amplifier does double duty, serving as a buffer amplifier as well as a glitch remover, delaying the output by ½ clock cycle.

The sample/hold may be used to remove many other types of "glitches" in a system. If a delayed sample pulse is required, this can be generated using a dual monostable multivibrator I.C.

DE-GLITCHER

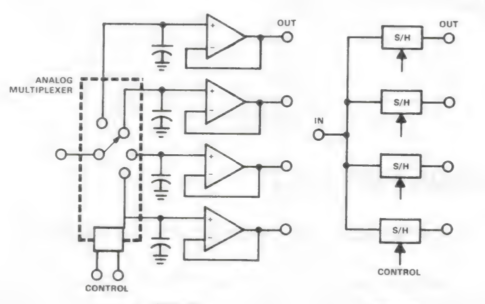


Application No. 7

This circuit reconstructs and separates analog signals which have been time division multiplexed.

The conventional method, shown on the left, has several restrictions, particularly when a short dwell time and a long, accurate hold time is required. The capacitors must charge from a low impedance source through the resistance and current limiting characteristics of the multiplexer. When holding, the high impedance lines are relatively long and subject to noise pickup and leakage. When FET input buffer amplifiers are used for low leakage, severe temperature offset errors are often introduced.

DE-MULTIPLEXER



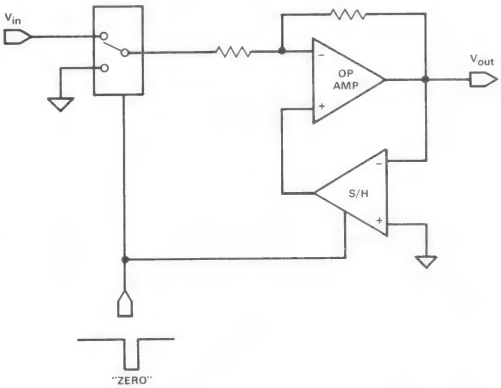
Application No. 8

This basic circuit has widespread applications in instrumentation, A/D conversion, DVM's and DPM's to eliminate offset drift errors by periodically rezeroing the system. Basically, the input is periodically grounded, the output offset is then sampled and fed back to cancel the error.

The system illustrated automatically zeros a high gain amplifier. Care in the actual design is necessary to assure that the zeroing loop is dynamically stable. A second sample-and-hold could be added in series with the output to remove the output discontinuity.

Many variations of this scheme are possible to suit the individual system.

AUTOMATIC OFFSET ZEROING

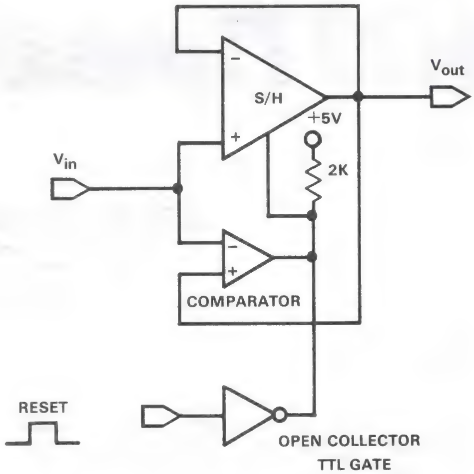


Application No. 9

This accurate, low drift peak detector circuit combines the basic sample-and-hold connection with a comparator. When the input signal level exceeds the voltage being stored in the S/H, the comparator trips, and a new sample of the input is taken. The S/H offset pot should be adjusted for a slight positive offset, so that the comparator will trip back when the new peak is acquired; otherwise the comparator would remain "on" and the S/H would follow the peak back down.

To make a negative peak detector, reverse the comparator inputs and adjust the S/H for a negative offset.

The reset function, which is difficult to achieve in other peak detector circuits, forces a new sample at the instantaneous input level.



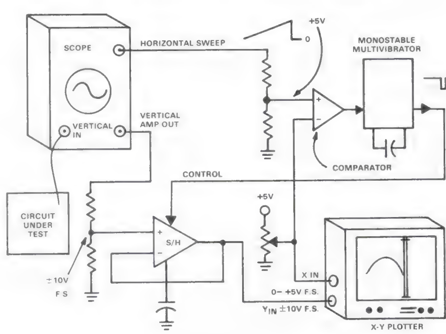
Application No. 10

This useful application illustrates how fast repetitive waveforms can be slowed down using sampling techniques. The input signal is much too fast to be tracked directly by the X-Y recorder, but sampling allows the recorder to be driven as slow as necessary.

To operate, the waveform is first synched in on the scope. Then the potentiometer connected to the recorder X input is slowly advanced, and the waveform will be reproduced. The S/H amplifier samples for a very short interval once each horizontal sweep of the scope. The sampling instant is determined by the potentiometer at the instant when the horizontal sweep waveform corresponds to the X position of the recorder.

This principle can be applied to many systems for waveform analysis, etc.

PLOT HIGH SPEED WAVEFORMS WITH SAMPLING TECHNIQUES



APP NOTE

FOR YOUR INFORMATION

No. 519

Harris Analog

OPERATIONAL AMPLIFIER NOISE PREDICTION

By Richard Whitehead

Introduction

When working with op amp circuits an engineer is frequently required to predict the total RMS output noise in a given bandwidth for a certain feedback configuration. While op amp noise can be expressed in a number of ways, "spot noise" (RMS input voltage noise or current noise which would pass through 1Hz wide bandpass filters centered at various discrete frequencies), affords a universal method of predicting output noise in any op amp configuration.

The Noise Model

Figure 1 is a typical noise model depicting the noise voltage and noise current sources that are added together in the form of root mean square to give the total equivalent input voltage noise (RMS), therefore:

$$E_{ni} = \sqrt{e_{ni}^2 + I_{ni}^2 R_g^2 + 4KTR_g} \quad \text{where,}$$

E_{ni} is the total equivalent input voltage noise of the circuit.

e_{ni} is the equivalent input voltage noise of the amplifier.

$I_{ni}^2 R_g^2$ is the voltage noise generated by the current noise.

$4KTR_g$ expresses the thermal noise generated by the external resistors in the circuit where $K = 1.38 \times 10^{-23}$ joules/^oK; $T = 300^oK$ (27^oC) and $R_g = \left(\frac{R_1 R_3}{R_1 + R_3}\right) + R2$

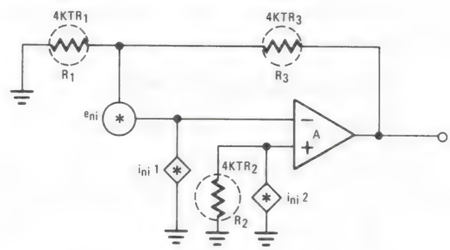


Figure 1

The total RMS output noise (E_{no}) of an amplifier stage with gain = G in the bandwidth between f_1 and f_2 is:

$$E_{no} = G\left(\int_{f_1}^{f_2} E_{ni}^2 df^{1/2}\right)$$

Note that in the amplifier stage shown, G is the non-inverting gain $\left(G = 1 + \frac{R2}{R1}\right)$ regardless of which input is normally driven.

Procedure for Computing Total Output Noise

1. Refer to the voltage noise curves for the amplifier to be used.
2. Enter values of $e_{ni}2$ line (a) of the table below from the curve labeled "Noise spectral density" (the values must be squared).
3. From the current noise curves for the

amplifier, obtain the values of i_{ni}^2 for each of the frequencies in the table, and multiply each by R_g^2, entering the products in line (b) of the table.

4. Obtain the value of $4KTR_g$ from Figure 14, and enter it on line (c) of the table. This is constant for all frequencies. The $4KTR_g$ value must be adjusted for temperatures other than normal room temperature.

5. Total each column in the table on line (d). This total is E_{ni}^2.

	10Hz	100Hz	1KHz	10KHz	100KHz
(a) e_{ni}^2					
(b) $I_{ni}^2R_g^2$					
(c) $4KTR_g$					
(d) E_{ni}^2					

6. On linear scale graph paper enter each of the values for E_{ni}^2 vs. frequency. In most cases, sufficient accuracy can be obtained simply by joining the points on the graph with straight line segments.

7. For the bandwidth of interest, calculate the area under the curve by adding the areas of trapezoidal segments. This procedure assumes a perfectly square bandpass condition; to allow for the more normal -6db/octave bandpass skirts, multiply the upper (-3db) frequency by 1.57 to obtain the effective bandwidth of the circuit, before computing the area. The total area obtained is equivalent to the square of the total input noise over the given bandwidth.

8. Take the square root of the area found above and multiply by the gain (G) of the circuit to find the total Output RMS noise.

A TYPICAL EXAMPLE

It is necessary to find the output noise of the circuit shown below between 1KHz and 24KHz.

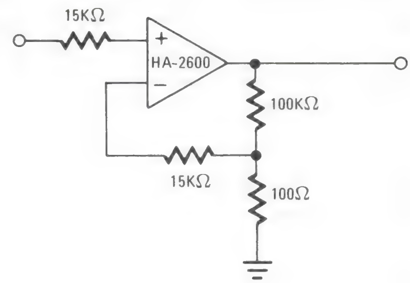
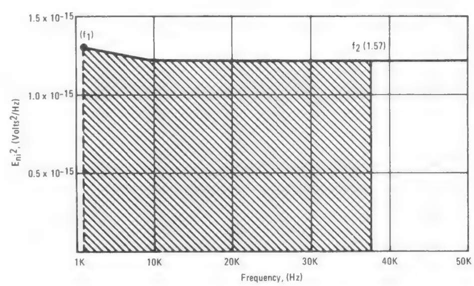


Figure 2
The HA-2600 In a Typical G = 1000 Circuit

Values are selected from Figures 5, 5a and 14 to fill in the table as shown below. An R_g of 30KΩ was selected.

	10Hz	100Hz	1KHz	10KHz	100KHz
(a) e_{ni}^2	3.6×10^{-15}	1.156×10^{-15}	7.84×10^{-16}	7.29×10^{-16}	7.29×10^{-16}
(b) $I_{ni}^2R_g^2$	9.9×10^{-16}	1.89×10^{-16}	3.15×10^{-17}	7.2×10^{-18}	7.2×10^{-18}
(c) $4KTR_g$	4.968×10^{-16}	4.968×10^{-16}	4.968×10^{-16}	4.968×10^{-16}	4.968×10^{-16}
(d) E_{ni}^2	5.09×10^{-15}	1.86×10^{-15}	1.31×10^{-15}	1.23×10^{-15}	1.23×10^{-15}

The totals of the selected values for each frequency is in the form of E_{ni}^2. This should be plotted on linear graph paper as shown below:



HA-2600 Total Equivalent Input Noise Squared

Since a noise figure is needed for the frequency of 1KHz to 24KHz, it is necessary to calculate the effective bandwidth of the circuit. With AV = 60db the upper 3db point is approximately 24KHz. The product of 1.57 (24KHz) is 37.7KHz and is the effective bandwidth of the circuit.

The shaded area under the curve is approximately 45 x 10^{-12} Volts^2; the total equivalent input noise is $\sqrt{E_{ni}^2}$ or 6.7 microvolts, and the total output noise for the selected bandwidth is $\sqrt{E_{ni}^2}$ x (closed loop gain) or 6.7 millivolts RMS.

Actual Measurements For Comparison

The circuit shown below was used to actually measure the broadband noise of the HA-2600 for the selected bandwidth:

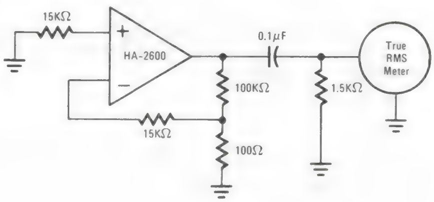


Figure 3
A Typical Test Circuit for Broadband Noise Measurements

The frequencies below the f_1 point of the bandwidth selected are filtered out by the RC network on the output of HA-2600. The measurement of the broadband noise is observed on the true RMS voltmeter. The measured output noise of the circuit is 4.7 microvolts RMS as compared to the calculated value of 6.7 microvolts RMS.

Acquiring the Data For Calculations

Spot noise values must be generated in order to make the output noise prediction. The effects of "Popcorn" noise have been excluded due to the type of measurement system.

The Quan-Tech Control Unit, model no. 2283 and Filter Unit, model no. 2181 were used to acquire spot noise voltage values expressed in ($V/\sqrt{Hz}$). The test system performs measurements from 10Hz by orders of magnitude to 100KHz with an effective bandwidth of 1Hz at each tested frequency.

Several source resistance (R_g) values were used in the measuring system to reveal the effects of R_g on each type of Harris' op amps and to obtain proper voltage noise values essential for current noise calculations.

A Discussion On "Popcorn" Noise

"Popcorn" noise was first discovered in early 709 type op amps. Essentially it is an abrupt step-like shift in offset voltage (or current) lasting for several milliseconds and having amplitude from less than one microvolt to several hundred microvolts. Occurance of the "pops" is quite random — an amplifier may exhibit several "pops" per second during one observation period and then remain "popless" for several minutes. Worst case conditions are usually at low temperatures with high values of R_g. Some amplifier designs and some manufacturer's products are notoriously bad in this respect. Although theories of the popcorn mechanism differ, it is known that devices with surface contamination of the semiconductor chip will be particularly bad "poppers". Advertising claims notwithstanding, the authors have never seen any manufacturer's op amp that was completely free of "popcorn". Some peak detector circuits have been developed to screen devices for low amplitude "pops", but 100% assurance is impossible because an infinite test time would be required. Some studies have shown that spot noise measurements at 10Hz and 100Hz, discarding units that are much higher than typical, is an effective screen for potentially high "popcorn" units.

The vast majority of Harris op amps will exhibit less than 3 μV peak-to-peak "popcorn". Screening can be performed, but it should be noted that the confidence level of the screen could be as low as 60%.

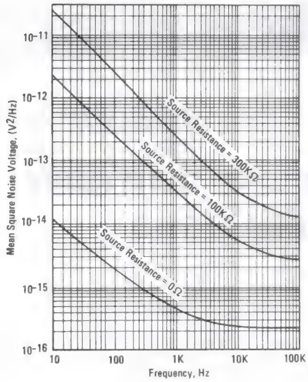
References

Fitchen, F.C. and Motchenbacker, C.D. Low Noise Electronic Design. New York: John Wiley and Sons, 1973.

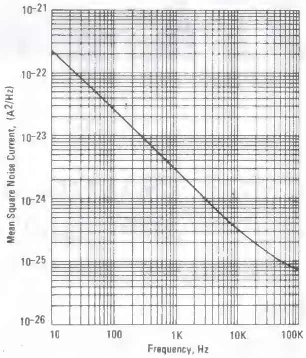
Instruction Manual, Model 2173C Transistor Noise Analyzer Control Unit. Quan-Tech, Division of KMS Industries. Whippany, New Jersey.

Typical Spot Noise Curves Unless Otherwise Noted: $V_S = \pm15V$, $T_A = +25^oC$

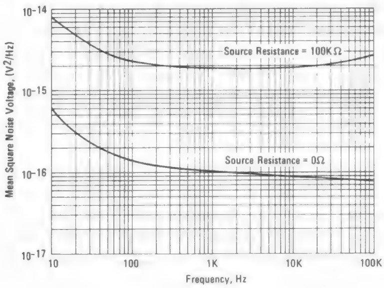
HA-2500/2510/2520 INPUT NOISE VOLTAGE



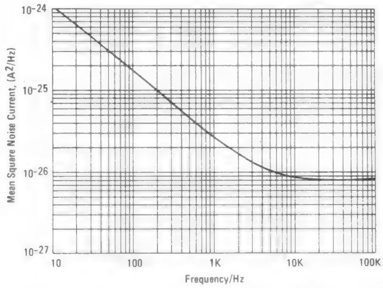
HA-2500/2510/2520 INPUT NOISE CURRENT



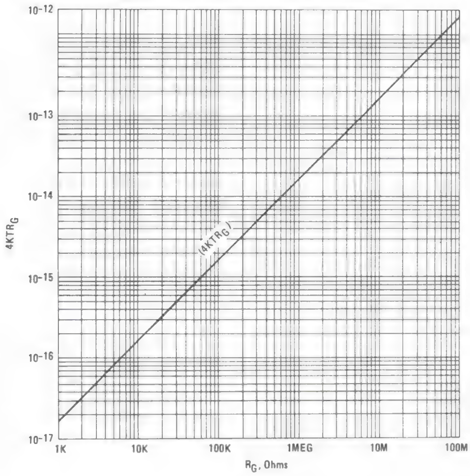
HA-4741 INPUT NOISE VOLTAGE



HA-4741 INPUT NOISE CURRENT



CURVE 12



10
APPLICATION NOTES

APP NOTE

FOR YOUR INFORMATION

No. 520

Harris Analog

CMOS ANALOG MULTIPLEXERS AND SWITCHES; APPLICATIONS CONSIDERATIONS

Don Jones and Al Little

Introduction

This article describes several important considerations for the use of CMOS analog multiplexers and switches. It includes selection criteria, parameter definitions, handling and design precautions, interfacing, typical applications, and special topics such as overvoltage protection and R.F. switching. Some other devices which perform analog switching functions are discussed as well.

Application Note 521 is also recommended for the analog multiplexer and switch user. It details the different CMOS processes used by various manufacturers, showing the performance trade-offs and failure modes which may be encountered with each.

Choosing the Right Device

A. Multiplexers: Protected or Unprotected?

Analog input signals which originate externally to a system can be destructive to a multiplexer for several reasons:

1. Analog signals may be present while the MUX power supplies are off.
2. The signal lines may receive induced voltage spikes from nearby sources.
3. Static electricity may be introduced on the signal lines by personnel or equipment.
4. Grounding problems are frequent; A. C. power line voltages at high impedance can appear on the signal lines. Signal lines can be accidentally shorted to other voltage sources.

Each of these situations are common in data acquisition, telemetry, and process control systems. In each case, a voltage at the multiplexer input exceeds the rail voltage. Without current limiting, this voltage will degrade or destroy the device.

Any conventional CMOS multiplexer can be protected against overvoltage destruction by external resistor-diode networks which limit input current to a safe level. Such networks are expensive, however, both in cost and in circuit board space. Another drawback is the output signal corruption that accompanies an overvoltage - regardless of which input is selected. This occurs due to parasitic bipolar transistors within the multiplexer which turn on during overvoltage. (Application Note 521 explains this mechanism in detail).

A few multiplexers feature built-in overvoltage protection, designed to eliminate the external networks. The protection capability varies widely among these devices, however. Some offer very slight advantages over ordinary multiplexers while others withstand wide voltage extremes. Unfortunately, nearly all suffer from the same output signal corruption problem described above.

Harris overvoltage protected multiplexers, HI-506A/507A/508A/509A, are an exception to this rule. During overvoltage, active protection circuitry automatically shuts off the parasitic transistor, thereby preventing output signal contamination. These devices will withstand a continuous voltage on any one input of ±20 Volts greater than either supply (this limitation is due only to temperature rise considerations at maximum ambient) and have withstood simulated static discharge conditions of greater than 4,500 Volts.

It should be emphasized that only the HI-506A through 509A (and exact equivalents from authorized alternate suppliers) will have this kind of protection necessary for inputs from the outside world. Certain CMOS process improvements, such as "floating body" and "buried layer" do help minimize one failure mode (latchup) but will still fail under excess voltage or current conditions prevalent in this type application.

A simplified equivalent circuit of the Harris internal protection network is shown in Figure 1.

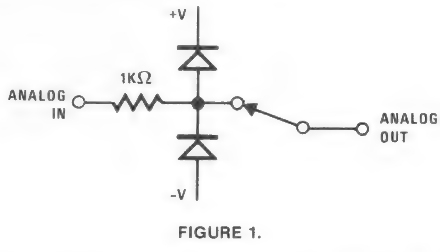


FIGURE 1.

This will help answer the question of what happens when the supplies are turned off, but input signals are present. If the supplies are shorted to ground, then the inputs will have about 1KΩ impedance to ground. If the supplies are open circuit, then the most positive and most negative inputs will act as supplies to the multiplexer.

In normal operating parameters, internally protected multiplexers have one difference from the unprotected versions-ON resistance is necessarily higher because of the added series current limiting resistor. However, to achieve the same degree of protection with conventional devices, the same resistance must be added externally, plus external diodes which would add to the effective leakage currents.

Conventional unprotected multiplexers are suitable for systems where the MUX inputs come from sources within the equipment, such as from op amps powered by the same $\pm$15 volt supplies. The HI-506/507/1818A/1828A are intended for this type system. They are entirely free of any latch-up tendency, which have plagued some other types, even in these more benign applications. They are also free of the performance compromises which have accompanied some attempts to cure the latch-up problem.

B. Which Switch To Switch To?

Harris furnishes a complete line of CMOS analog switches, including replacements for most of the available CMOS and JFET switches. All types feature rugged no-latch-up construction, uniform characteristics over the analog signal range, and excellent high frequency characteristics.

The HI-200 and HI-201 replace the popular, low cost DG200 and DG201 types dual and quad switches.

The HI-1800A is low leakage dual DPST switch with a versatile addressing scheme, allowing use of a single type for many different switching functions.

The HI-5040 through HI-5051 are low resistance types, offering one to four switches in virtually all combinations. These replace the HI-5040 series with significantly better performance, and with both 75 ohm and 30 ohm switches available in all configurations. These are also plug-in replacements for many of the DG180 and DG190 series of FET hybrid switches, offering the advantage of monolithic construction, but with slightly longer switching times.

The analog switches do not contain overvoltage protection on the analog inputs, although they will withstand inputs 2 or 4 volts greater than the supplies. External current limiting should be provided if higher overvoltages are anticipated, such as a resistor in series with the analog input of value: R(ohms)$\geq(V_{IN} - V_{SUPPLY}) \times 50$ where VIN is the maximum expected input voltage. All digital inputs do have overvolgate/static charge protection.

Data Sheet Definitions

A. Absolute Maximum Ratings

As with all semiconductors, these are maximum conditions which may be applied to a device (one at a time) without resulting in permanent damage. The device may, or may not, operate satisfactorily under these conditions - conditions listed under "Electrical Characteristics" are the only ones guaranteed for satisfactory operation.

B. V_S, Analog Signal Range

The input analog signal range over which reasonable accurate switching will take place. For supply voltages lower than nominal, V_S will be equal to the voltage span between the supplies. Note that other parameters such as R_{ON} and leakage currents are guaranteed over a smaller input range, and would tend to degrade towards the V_S limits. All Harris devices can withstand $+V_S$ applied at an input while $-V_S$ is applied to the output (or vice-versa) without switch breakdown - this is not true for some other manufacturers' devices.

C. R_{ON}, On Resistance

The effective series on-switch resistance measured from input to output under specified conditions. Note that R_{ON} changes with temperature (highest at high temperature) and to a lesser degree with signal voltage and current.

D. I_S(OFF), I_D(OFF), I_D(ON): Leakage Currents

Currents measured under conditions illustrated on the data sheet. Harris prefers to guarantee only worstcase high temperature leakages, because room temperature picoampere levels are virtually impossible to measure repeatable on available automated test equipment. Even under laboratory conditions, fixture and test equipment stray leakages may frequently exceed the device leakage. Leakages tend to double every 10^oC temperature rise, so it is reasonable to assume that the $+25^oC$ figure is about 0.001 times the $+125^oC$ measurement; however, in some cases there may be ohmic leakages, such as on the package surface, which would make the $+25^oC$ reading higher than calculated.

Each of these leakage figures is the algebraic sum of all currents at the point being measured: to each power supply, to ground, and through the switches; so the current direction cannot be predicted. In making an error analysis it should be assumed that all leakages are in the worst-case direction.

In most systems, I_D(ON) has the most effect, creating a voltage offset across the closed switch equal to $I_D(ON) \times R_{ON}$.

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APPLICATION NOTES

E. V_{AL}, V_{AH}; Input Thresholds

The lower and upper limits for the digital address input voltage at which the switching action takes place. All other parameters will be valid if all "0" addressd inputs are less than V_{AL} and all "1" inputs are greater than V_{AH}. Logic compatibility will be discussed in detail later in this paper.

F. I_A, Input Leakage Current

Current at a digital input, which may be in either direction. Digital inputs on Harris devices are similar to CMOS logic inputs; connection to MOS gates through resistor-diode protection networks. Unlike some other devices there is no DC negative resistance region which could create an oscillating condition.

G. T_A, T_{ON}, T_{OFF}; Access Time

The logic delay time plus output rise time to the 90% point of a full scale analog output swing. After this time the output will continue to rise, approaching the 100% point on an exponential curve determined by $R_{ON} \times C_D(OFF)$.

H. T_{OPEN}, Break-Before-Make Delay

The time delay between one switch turning OFF and another switch turning ON; both switches being commanded simultaneously. This prevents a momentary condition of both switches being ON, generally a very minor problem.

I. $C_S(OFF)$, $C_D(OFF)$, $C_D(ON)$ Input/Output Capacitance

Capacitance with respect to ground measured at the analog input/output terminals. $C_D(ON)$ is generally the sum of $C_S(OFF)$ and $C_D(OFF)$. $C_D(OFF)$ is usually the most important term as rise time/settling characteristics are determined by $R_{ON} \times C_D(OFF)$, as well as the high frequency transmission characteristics.

J. $C_{DS}(OFF)$, Drain to Source Capacitance

The equivalent capacitance shunting an open switch.

K. OFF Isolation

The proportion of a high frequency signal applied to an open switch input appearing at the output:

$$\text{off isolation} = 20 \log \frac{V_{IN}}{V_{OUT}}$$

This feedthrough is transmitted through $C_{DS}(OFF)$ to a load composed of $C_D(OFF)$ in parallel with the external load. The isolation generally decreases by 6dB/octave with increasing frequency.

L. C_A, Digital Input Capacitance

Capacitance to ground measured at digital input. This chiefly affects propagation delays when driven by CMOS logic.

M. P_D, Power Dissipation: I+, I-

Quiescent power dissipation, $P_D = (V+ \times I+) + (V- \times I-)$. This may be specified both operating and standby ("Enable" pin ON/OFF). Note that, as with all CMOS devices, dissipation increases with switching frequency; but that Harris devices exhibit much less of this effect.

Care And Feeding of Multiplexers And Switches

Dielectrically isolated CMOS ICs require no more care in handling and use than any other semiconductor - bipolar or otherwise. However, they are not indestructible, and reasonable common sense care should be taken.

In a laboratory breadboard, power should be shut off before inserting or removing any IC. It is especially important that supply lines have decoupling capacitors to ground permanently installed at the IC socket pins, as intermittent supply connections can create high voltage spikes through the inductance of a few feet of wire.

Because each of the major manufacturers of CMOS multiplexers and switches uses a radically different process, it is urged that units from all prospective suppliers be equally tested in breadboards and prototypes. It will be interesting to note which types survive best the hazards of a few weeks of breadboard testing.

Particular care of semiconductors during incoming inspection and installation is quite important, because the cost of reworking finished assemblies with even a small percentage of preventable failures can seriously erode profits. All equipment should be periodically inspected for proper grounding. With these devices, it is not usually necessary to shackle personnel to the nearest water pipe, if reasonable attention is paid to clothing and floor coverings; but be alert for periods of unusually high static electricity. If special lines are already set up for handling MOS devices, it wouldn't hurt to use them.

There are a few good rules for P.C. card layout:

1. Each card or removable subassembly should contain decoupling capacitors for each supply line to ground. This not only helps keep noise away from the analog lines, but gives good protection from static electricity damage when loose cards are handled.

2. When digital inputs come through a card connector, the pull-up resistor should be at the CMOS input. This forces current through the connector and prevents possible dry circuit conditions (see following discussion on digital interface).

3. All unused digital inputs must be tied to logic "0" (ground) or logic "1" (logic supply or device + supply) depending on truth table and action desired. Open inputs tend to oscillate between "0" and "1". It would also be best to ground any unused analog inputs/outputs and any uncommitted device pins.

Digital Interface

A. Reference Connection

HI-5040 thru HI-5051 and HI-1800A/1818A/1828A require a connection to the digital logic supply (+5V to +15V).

The HI-200/201/506A/507A have V_{REF} pins which are normally left open when driving from +5 volt logic (DTL or TTL), but may be connected to higher logic supplies (to +15V) to raise the threshold levels when driving from CMOS or HNIL. The HI-200/201 will have significantly lower power dissipation when V_{REF} is connected to a high level supply.

The HI-506/507/508A/509A do not have V_{REF} terminals, but will operate reliably with any logic supplied from +5 to +15 volts.

B. DTL/TTL Interface

One major difference found in comparisons of similar devices from different manufactures is the worst-case digital input high threshold (V_{AH} or V_{IH}). These range anywhere from +2V to +5V; and anything greater than +2.4V is obviously not compatible with worst-case TTL output levels. The fact is that no CMOS input is truly TTL compatible unless an external pull-up resistor is added. TTL output stages were not designed with CMOS loads in mind.

The experienced designer will always add a pull-up resistor from CMOS input to the +5 volt supply when driving from TTL/DTL:

1. Interchangeability: allows substitution of similar devices from several manufacturers.
2. Noise immunity: a TTL output in the "high" condition can be quite high impedance. Even when voltage noise immunity seems satisfactory, the line is quite susceptible to induced noise. The pull-up resistor will reduce the impedance while increasing voltage noise immunity.
3. Compatibility: one manufacturer does guarantee +2.0 volt minimum V_{AH}. However, this is accomplished with circuitry that is anything but TTL compatible: input current vs. voltage shows an abrupt positive then negative resistance region which is not the kind of load recommended for an emitter follower stage. A pull-up resistor will swamp out the negative resistance. Other CMOS inputs capacitively couple internal switching spikes to the input which could cause double-triggering without the pull-up resistor.
4. Reliability: it shouldn't happen with carefully processed ICs, but any possible long term degradation of CMOS devices usually involves threshold voltage shifts. The pull-up resistor will help maintain operation if input thresholds drift out of spec. On units without adequate input protection, the resistor will also help protect the device when a loose P.C. card is handled. Where the interface goes through a P.C. connector, the resistor will force current through the connector to break down any insulating film which otherwise might build up and cause erratic dry circuit operation.

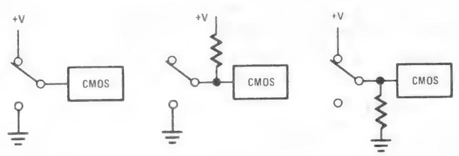
A 2K ohm resistor connected from the CMOS input to the +5 volt supply is adequate for any TTL type output. If power consumption is critical, open collector TTL/DTL should be used, allowing a higher value resistor - the voltage drop across the resistor is computed from the sum of specified "1" level leakage currents at the TTL output and CMOS input.

C. CMOS Interface

The digital input circuitry on all Harris devices is identical to series 4000 and 54C/74C logic inputs, and is compatible with CMOS logic with supplies between +5V and +15V without external pull-up resistors.

D. Electromechanical Interface

When driving inputs from mechanical switches or relays, either a pull-up or pull-down resistor must be connected at the CMOS input to clear the dry circuit and damp out any spikes, as illustrated in Figure 2, (b) and (c).



(a) POOR (b) GOOD (c) GOOD

FIGURE 2.

A Practical Multiplexer Application

Figure 3 illustrates a practical data acquisition system hookup using an analog multiplexer, a monolithic sample-and-hold and an A/D converter. The HA-2420/2425 sample-and-hold is a particularly good choice for this type application because it eliminates the need for a separate high impedance, high slew rate buffer amplifier. Its acquisition time is consistent with CMOS multiplexer settling times and most available A/D conversion times. Errors, after initial adjustment, are consistent with up to 12 bit absolute accuracy over a wide temperature range.

A. Accuracy

D.C. error sources include:

1. Multiplexer:
   a. input offset = R source x I_S(OFF)
   b. output offset = R(ON) x (I_D(ON) + I bias (S/H)
2. Sample-and-Hold
   a. input offset voltage
   b. charge injection; sample-to-hold offset
   c. gain error during "hold"
   d. drift during hold
3. A/D converter:
   a. linearity
   b. gain drift
   c. offset drift

Item 1(a) and (b), and 2(d) become significant only at very high temperatures. 2(a) and (b) are initially adjusted out with the offset adjustment pot on the S/H. 2(c) is usually adjusted out by A/D gain adjustment, but could also be removed by a voltage divider feedback on the S/H to give a slightly greater than unity gain during "sample". After initial adjustments, typical S/H errors are less than 0.5mV over 0°C to +75°C. Note that after adjustment, there may be an appreciable offset at the S/H output when switching from sample to hold. This is not a problem, since accuracy is required only during "hold", and the system is adjusted for this.

The largest system errors are usually 3(b) and (c), drifts with temperature and time. If two multiplexer channels can be dedicated for stable (+) and (-) reference voltage inputs, then the data processor can continuously calibrate the system, effectively removing all errors, except 1(a) and 3(a) which are usually negligible.

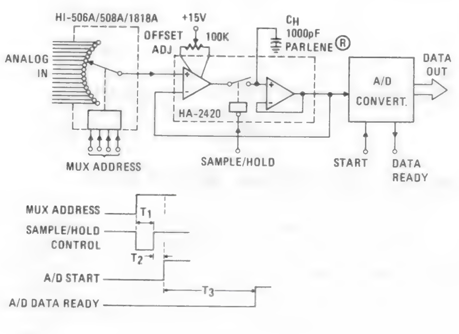


FIGURE 3.

B. Timing

The timing diagram in Figure 3 indicates the necessary system delays for each multiplexer address:

T_1 is the combined acquisition time for the multiplexer and S/H.
T_2 is the short interval required for the sample-to-hold transient to settle.
T_3 is the A/D conversion time.

The following table indicates minimum recommended timing for ±10 volt input range for acquisition/settling times to ½ LSB accuracy:

	T_1	T_2
10 bit:	6μs	1μs
12 bit:	12μs	2μs

The multiplexer, by itself, requires about 2μs and 9μs settling to 10 bit and 12 bit accuracy, respectively; but fortunately this can be concurrent with S/H acquisition time. This is longer than would be predicted by the R_{ON} C_D time constant; probably because of internal distributed capacitance, a rather long period is required to traverse the last few millivolts towards the final value.

It should be noted that impedance conditions at the multiplexer inputs can affect the necessary acquisition time. At the instant the multiplexer switches from one channel to a new one, there is appreciable current pulled through the new channel input in order to charge C_D from its old level to its new level. This can cause ringing on signal lines, or glitches at signal conditioning amplifier outputs which require longer periods to settle. It is best for signal conditioning amplifiers to be wide band types, such as HA-5170, so that their high frequency output impedance is low and recovery from load transients is fast; even though the signal to be measured is very low bandwidth.

The T_1 and T_2 times could be eliminated by alternating two S/H circuits, acquiring a new signal on the second while A/D conversion is taking place. The two S/H circuits would have inputs connected together, and outputs alternately connected to the A/D by an analog switch. Total time, then, would be T_3 plus the analog switch settling time.

If the MUX input channels are sequentially switched, each channel will be sampled at a rate of:

$$FS = \frac{1}{N(T_1 + T_2 + T_3)}$$

samples per second, where N is the number of channels. The frequency spectra of the input signals must then be no higher than $\frac{FS}{2}$.

In many systems, however, each channel carries a different maximum frequency of interest, and it may be desirable to depart from simple sequential scanning. Quickly varying signals, for example, could be addressed several times during a scanning period.

C. Adding Channels

For more than sixteen channels, several multiplexers may be tied together at the outputs, and addressed in parallel, but with only one "enabled" at a time. The MUX output offset will be increased, since I_D (OFF or ON) is additive. Also, output capacitance, C_D, is additive, creating increased access times.

These errors can be minimized in large systems by having several tiered levels of multiplexing; where the outputs of a number of MUXs are individually connected to the inputs of another MUX.

D. Differential Multiplexing

When low level analog signals must be conducted over a distance, it is generally better, from a noise pickup standpoint, to use a balanced transmission line carrying signals which are differential with respect to ground.

A dual multiplexer is used for this purpose, as shown in Figure 4. Two sample-and-hold circuits plus an op amp form a high impedance differential sample-and-hold with gain. At gains greater than 4, the minimum sampling time (T_1 in previous example) must be increased proportionately to gain to allow for overdamped settling characteristics.

When handling low level, or high impedance signals, consideration should be given to adding signal conditioning amplifiers at the signal sources, since this can often produce less troublesome, more accurate, lower cost systems.

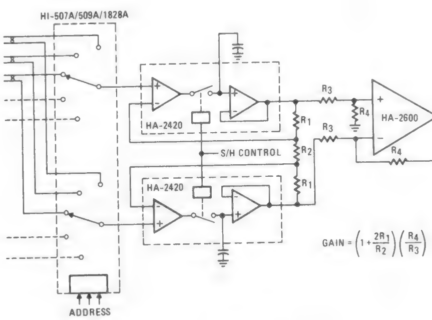


FIGURE 4.

E. Demultiplexing

Since the switches in a CMOS MUX conduct equally well in either direction, it is perfectly feasible to use it as a single input-selected multiple output switch. Figure 5 illustrates its use as a demultiplexer, with capacitors to hold the output signal between samples. When the address lines are synchronous with the address of the original multiplexer, the output lines will create the original inputs, except level changes will be in steps.

Overvoltage protection is not effective with signals injected at the normal MUX output, so an external network should be added, if necessary.

A more accurate demultiplexer could be constructed using the HA-2420/2425 sample-and-hold for each channel, connecting inputs together and sampling each channel sequentially.

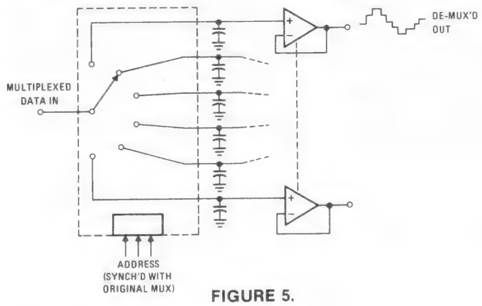


FIGURE 5.

Analog Switch Applications

A. High Current Switching

Analog switches are sometimes required to conduct appreciable amounts of current, either continuous, or instantaneous - such as charging or discharging a capacitor. For best reliability, it is recommended that instantaneous current be limited to less than 80mA peak and that average power over any 100 millisecond period be limited to $I2R_{ON} \leq$ (absolute maximum derated power-quiescent power). Note that R_{ON} increases at high current levels, which is characteristic of any FET switch. Switching elements may be connected in parallel to reduce R_{ON}.

B. Op Amp Switching Applications

When analog switches are used either to select an op amp input, or to change op amp gain, minor circuit rearrangements can frequently enhance accuracy. In Figure 6(a), R_{ON} of the input selector switch adds to R_1, reducing gain and allowing gain to change with temperature. By switching into a noninverting amplifier (b), gain change becomes negligible. Similarly, in a gain switching circuit, R_{ON} is part of the gain determining network in (c), but has negligible effect in (d).

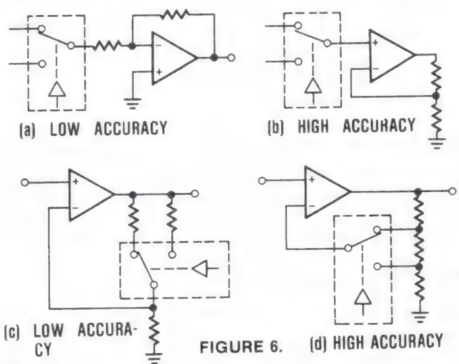


FIGURE 6.

C. Switching Spikes And Charge Injection

Transient effects when turning a switch off or on are of concern in certain applications. Short duration spikes are generated (Figure 7(a)) as a result of capacitive coupling between digital signals and the analog output. These have the effect of creating an acquisition time interval during which the output level is invalid even when little or no steady state level change is involved. The total net energy (charge injection) coupled to the analog circuit is of concern when switching the voltage on a capacitor, since the injected charge will change the capacitor voltage at the instant the switch is opened (Figure 7(b)).

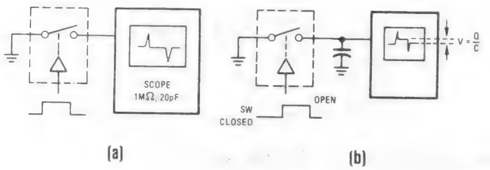


FIGURE 7.

Charge injection is measured in picocoulombs; the voltage transferred to the capacitor computed by

$$V = \frac{\text{Charge (pC)}}{\text{Capacitance (pF)}}$$

Both of these effects are, in general, considerably less for CMOS switches than for equivalent resistance JFET or PMOS devices, since the gate drive signals for the two switching transistors are of opposite polarity. However, complete cancellation is not possible, since the N and P channel switches do not receive gate signals quite simulaneously, and their geometrics are necessarily different to achieve the desired D.C. resistance match.

In applications where transients create a problem, it is frequently possible to minimize the effect by cancellation in a differential circuit, similar to Figure 8.

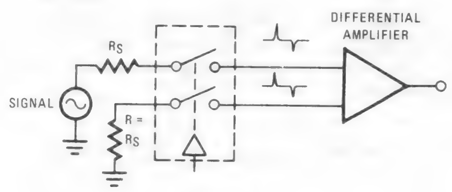


FIGURE 8.

Among the Harris analog switches, the HI-201 is the best from the transient standpoint, having turn-on spikes of about 100mV peak, 50ns width at the 50% point, and charge injection at turn-off of about 20 picocoulombs. Transients of the HI-5040 series are several times higher.

D. High Frequency Switching

When considering a switching element for R.F. or video type information, two factors must be watched: attenuation vs. frequency characteristics of an ON switch, and feedthrough vs. frequency characteristics of the OFF switch. Optimizing the first characteristic requires a low $R_{ON} \times C_D$ product, and the second a low value of C_{DS} (OFF).

One approach is to use the 30 ohm switch types of the HI-5040 series.

Figure 9 illustrates three circuit configurations; (a) is a simple series switch, (b) is a series-shunt configuration to reduce feedthrough, and (c) is a SPDT selector configuration with series-shunt elements. A 1K ohm load is illustrated, which might be the input impedance of a buffer amplifier; a lower load resistance would improve the response characteristics, but would create greater losses in the switch and would tend to distort high level signals.

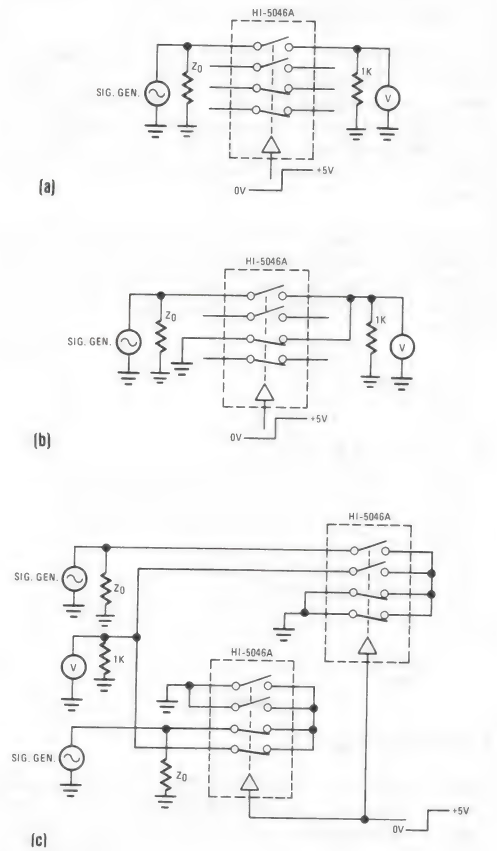


FIGURE 9.

Figure 10 shows ON and OFF frequency response for each of the above configurations. Arbitrarily, we will define useful frequency response as the region where ON losses are less than -3dB and OFF isolation is greater than -40dB.

The simple configuration (a) has excellent ON response, but OFF isolation limits the useful range to about 1MHz (the data sheet indicates -80dB isolation at 100kHz, but this is measured with 100 ohms load, which acounts for the 20dB difference).

The circuit in (b) shows a good improvement in isolation produced by the low impedance of the shunt switch. The useful range is about 10MHz; which could also be achieved in a simple SPDT 2-switch selector if source impedances are very low.

The selector switch in (c) has excellent characteristics, both ON and OFF curves indicating 40MHz useful response. Additional switches connected to the same point would reduce the ON response because of added shunt capacitance; but this could be eliminated by feeding separate summing amplifier inputs.

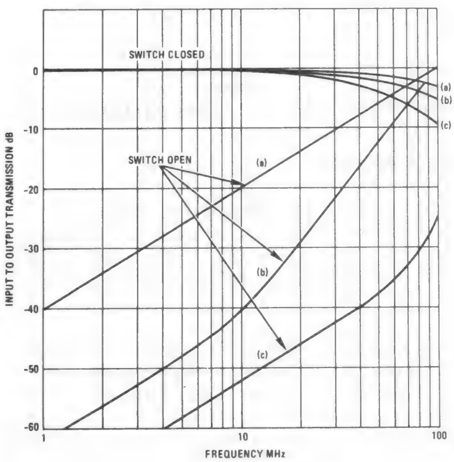


FIGURE 10.

For many applications, a better approach is to use the HI-524 monolithic wideband CMOS multiplexer. This device utilizes a series-shunt multiple switching network to achieve low crosstalk without sacrificing or compromising other operational parameters. As shown in Figure 11, each channel comprises three CMOS FET switch gates, with two in series and the third shunted to ground. The two series switches ensure both a high off isolation and low feed-through capacitance. The shunt grounding switch, closed automatically by the control logic when its corresponding series pair are open, shunts nonselected channels to ground, thus minimizing cross talk. With this circuit topology, crosstalk is typically -60dB at 10MHz.

A buffer amplifier is used with the HI-524 for high frequency applications, due to its higher ON resistance, and should offer sufficient bandwidth and slew rate to avoid degradation of the anticipated signals. For video switching, the HA-5033 and HA-2542 offer good performance plus ±100mA output current for driving coaxial cables. For general wideband applications, the HA-2541 offers

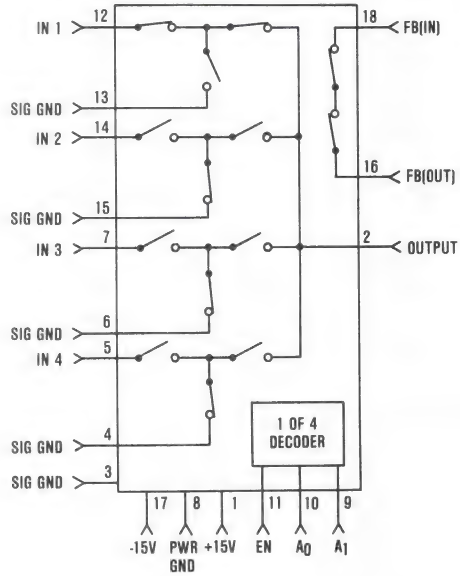


FIGURE 11.

the convenience of unity gain stability plus 90ns settling (to ±0.1%) and ±10V output swing. Also, the HI-524 includes a feedback resistance for use with the HA-2541. This resistance matches and tracks the channel ON resistance, to minimize offset voltage due to the buffer's bias currents.

Careful layout is, of course, important for high frequency switching applications to avoid feedthrough paths or excessive load capacitance.

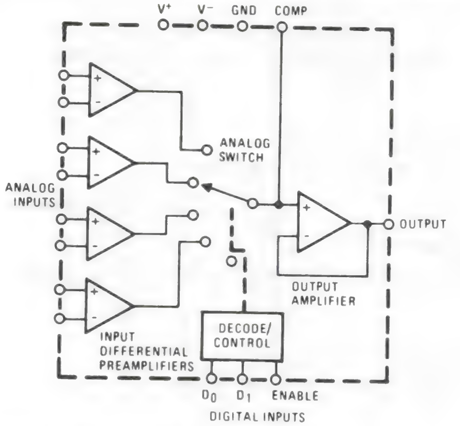
Alternatives to CMOS Switches and Multiplexers

CMOS devices are excellent in many applications. However, there are some other devices which merit consideration in certain analog switching circuits where they may improve performance, reduce parts count, or be more economical.

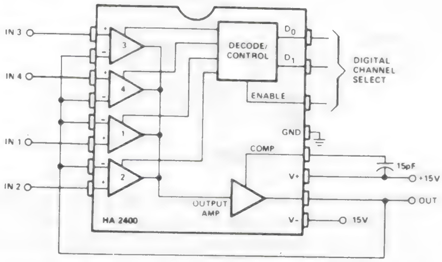
A. The PRAM, Programmable Amplifier

The HA-2400/2405 is a unique monolithic bipolar circuit which combines analog switching with high performance operational amplifiers. It basically consists of four op amp type input stages, any one of which is connected to a single output by bipolar switches controlled through a TTL compatible address decoder. In a single package, it contains the equivalent of 5 op amps plus a 4 channel multiplexer. It has literally hundreds of applications in signal selection and programmable signal conditioning.

Figure 12 illustrates a four channel multiplexer. Connections from the output to each input stage are always the same as a comparable op amp circuit; the +1 gain connection is illustrated.



(a) FUNCTIONAL DIAGRAM



(b) ANALOG MULTIPLEXER WITH BUFFERED INPUT AND OUTPUT

FIGURE 12.

Advantages over a comparable CMOS multiplexer circuit areas follows:

1. High input impedance (10^{12} ohnms), low output impedance (<0.1 ohm) means than ON resistance and leakage currents are no longer of concern. There is negligible transient loading of input lines.
2. Gain filtering, etc. can easily be added with feedback networks.
3. Fast acquistion (1.5μs).
4. Wide bandwidth (8MHz).
5. Superior feedthrough characteristics (-110dB at 10kHz, -60dB at 1MHz).

Disadvantages include:

1. Less accuracy for low level D.C. signals; the offset voltages of each input stage do not necessarily match or track each other.
2. Cannot be used in reverse as a demultiplexer.
3. Disabling the device (enable pin low) does not open the output line, or drive the output to zero. Adding channels may be accomplished by tying compensation pins together.

Figure 13 illustrates the PRAM used as a programmable gain amplifier. Any connection possible with op amps can be wired 4 ways to make programmable active filters, oscillators, etc., etc. Harris Application Note 514 shows many possibilities.

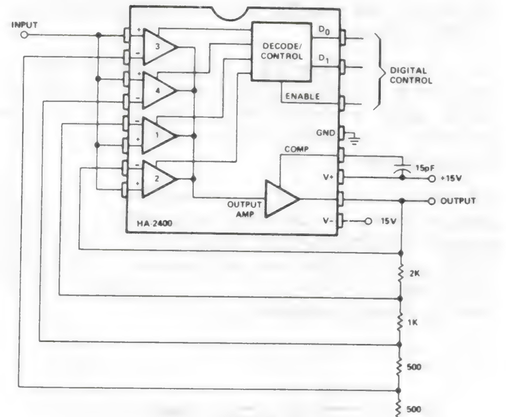


FIGURE 13.
AMPLIFIER, NONINVERTING PROGRAMMABLE GAIN

B. Sample-And-Hold

The sample-and-hold function has often been accomplished with separate analog switches and op amps. These designs always involve performance tradeoffs between acquisition time, charge injection, and droop rate.

The HA-2420/2425 monolithic sample-and-hold, illustrated previously in Figure 3 has many times better tradeoffs, usually at a lower total cost than the other approaches. The switching element is a complementary bipolar circuit with feedback which allows high charging currents (30mA), low charge injection (10pC), and ultra low OFF leakage current (5pA); a combination not approached in any other electronic switch. These factors make it also superior as an integrator reset switch, or as a precision peak detector as shown in Figure 14. Harris Application Note 517 illustrates many other applications.

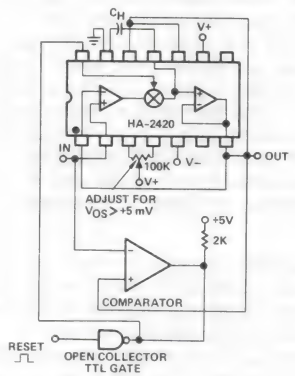


FIGURE 14.

APP NOTE

FOR YOUR INFORMATION

No. 521

Harris Analog

GETTING THE MOST OUT OF CMOS DEVICES FOR ANALOG SWITCHING JOBS

By: Ernie Thibodeaux
and Al Little

Introduction

CMOS analog switches and multiplexers are now widely used for a broad range of applications. They offer low power consumption, low on-resistance, and will conduct a signal in either direction. In addition, CMOS switch structures exhibit no DC offset voltage and can usually handle signals up to the supply rails.

Not all CMOS analog switches are alike, however. Different technologies are employed by different manufacturers. Some types, handicapped by inherent process limitations, can create significant problems for the user. Switches built with older types of junction isolation, for example, can literally self-destruct when a latch-up condition occurs. To prevent destruction, costly external protective circuits are needed, but the devices can still latch up unless the power is turned on and off in a set sequence. Switch circuits can also be destroyed by electrostatic discharge, input overvoltage spikes and power supply transients.

Newer types of technologies include latch-proof junction isolation (JI), floating-body junction isolation, and dielectric isolation (DI). Both JI techniques are conventional processes that have been slightly modified to alleviate the old problem of latch-up. However, both of these JI technologies still require costly external protection circuits to guard against burn-out in such applications as analog-signal multiplexing that interface them with the outside world. That is why JI devices are best suited for internal-switching applications where the electrical environment can be controlled. In contrast, the improved DI technology, by virtue of its construction, offers analog-switching devices suitable for many inside applications, as well as providing on-board analog protection for devices that interface with the other circuits. Happily, the smaller substrate area of the DI device delivers a better speed-power product than the JI technology.

The Basic CMOS Switch

The basic CMOS transistor (Figure 1) has parasitic junctions that are reverse-baised during normal operation. However, certain overvoltage conditions can forward-bias these junctions to cause high currents that could possibly destroy the devices.

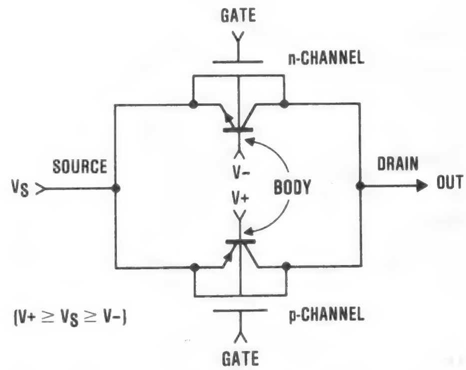


FIGURE 1. BAD

In the basic CMOS analog switch, the parasitic junctions are reversed-biased during normal operation. Large overvoltages, however, make them forward-biased and draw large currents.

The parasitic junctions are actually npn and pnp transistors that are normally reverse-biased by the applied body potentials. However, because many analog switches, and especially multiplexers, are connected to their analog sources through long lines, they are highly susceptible to externally induced voltage spikes. For example, these spikes, which can often exceed the p-channel body potential, V+, can inadvertently turn on a normally off switch through the parasitic pnp transistor (Figure 1).

The n-channel device is similarly affected when the parasitic npn transistor is turned on by a negative overvoltage. This action, commonly known as channel interaction, causes momentary channel-to-channel shorting, which introduces significant errors in the system. This intermittent condition is rarely isolated because it occurs only randomly.

One of the adverse effects of channel interaction is illustrated in Figure 2. Channel 1 of an analog multiplexer is selected when all other channels are off. Channel 16 receives an input-noise spike that momentarily exceeds the positive supply. The sequence causes channel 1 read-out to be +16V because of interaction with channel 16 just before initiating the hold command to the sample-and-hold device. To prevent this annoyance requires additional protective circuits that clamp each channel input to a voltage below the threshold of the parasitics to ensure that the channels remain inactive under any conditions.

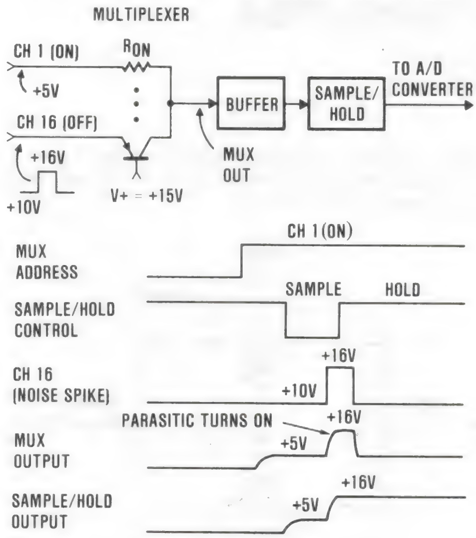


FIGURE 2. WORSE

With CMOS devices, noise spikes can cause channel interaction. In this multiplexer, although channel 1 is only one selected, noise spikes cause cross talk in channel 16, which affects reading.

A more serious condition exists when the substrates (p- or n-) lose their respective potentials to ground (Figure 3) -a condition that occurs when power to the device is turned off while the analog signals are still present. In this situation, the analog switch, which at that point represents a diode connected through the low impedance of the supply, draws high current from the analog source.

This current turns on the switch through its parasitics and shorts all channels to the output. These shorts can easily be catastrophic in multiplexer systems that have different power supplies for the analog source and the multiplexer switch. An error during troubleshooting or an inadvertent supply glitch can trigger this fault mode and destroy the whole system. Therefore, there is obviously much more to system reliability than having latch-proof CMOS devices.

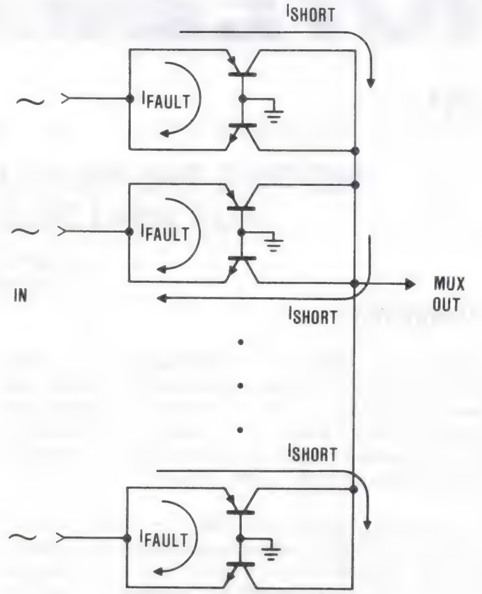


FIGURE 3. STILL WORSE

Most serious in CMOS swithes is losing substrate potential to ground. This condition, which happens when power is lost and the analog signal is present, causes very high currents.

Considering Latch-Proof JI Technology

The standard JI process has been modified by what is claimed to be latch-proof construction through control of the effective betas of the parasitic transistors. A cross section in Figure 4(a) shows the CMOS structure along with its parasitic transistors and the equivalent circuit in Figure 4(b) that gives rise to the silicon-controlled-rectifier latch-up problem.

Under any of the fault conditions previously mentioned, the npn and/or pnp can trigger this quasidual-gate SCR into a state of high conduction. If the transistor β product is 1 or greater, this configuration is sustained until either the device burns up or all sources of power are removed. By using a buried-layer configuration, as shown in the cross section, the β product is reduced to less than 1; eliminating the latch-up conditions.

Again, especially in multiplexer applications, the latch-free devices do not guarantee against destruction, and the JI multiplexer still requires costly discrete circuits around

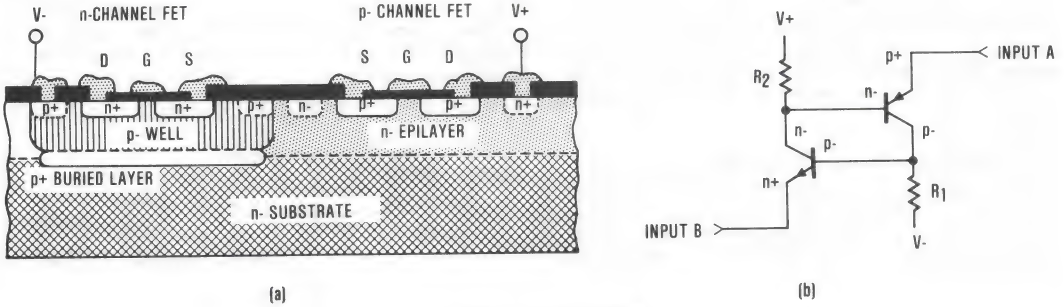


FIGURE 4. LATCH-PROOF.

Junction-Isolated devices are now made latch-proof with a buried-layer configuration (a), which keeps beta of parasitic transistor under unity. That kills chance for latch-up (b), which plagues devices built with older junction-isolation technology.

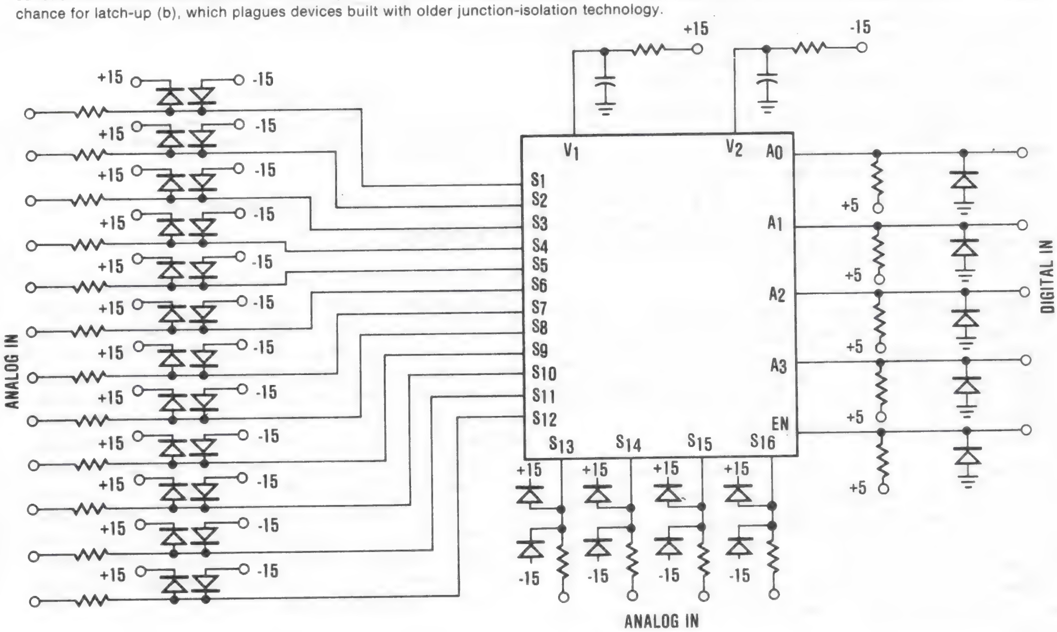


FIGURE 5. PROTECTION STILL NEEDED.

Although new JI devices won't latch up, they still can be destroyed by large currents. That's why typical JI multiplexers, like the one shown here, still need to be surrounded by external protective components, which drive up system costs.

the device, as shown in Figure 5. If an overvoltage exists, the resistor/diode circuit at each analog input limits the input voltage to the supply-voltage range to prevent the parasitic transistor action.

The resistors limit the overvoltage currents through the diodes. The diodes must have a low threshold voltage-much lower than the 0.6V silicon-junction threshold of the internal parasitic diodes-to ensure that the parasitics do not turn on.

A germanium diode offers a low threshold voltage, but its high leakage current makes it impractical, especially in 0.1% systems. Therefore, in most applications, more expensive low-leakage diodes are used.

For example, Schottky diodes meet the requirements but they are expensive. The total cost per multiplexer, including parts and labor, for the discrete protection circuit may well be double the initial purchase price of the device. Even then, its reliability will never approach that of an IC that has this protection already built in.

The Floating-Body JI Technology

Standard JI technology allows another approach to latch-proof device construction: a portion of the SCR continuity is broken by floating the "body" or substrate of the

n-channel switching device. A cross section of this process is similar to that in Figure 4(a), excluding the buried layer and the negative supply connection to the p- substrate, so that the dual-gate SCR is changed to a single-gate device that can only be triggered by the pnp parasitic. This, of course, reduces the latch-up probability by 50%.

To completely eliminate latch-up, as before, the β product of the transistors is reduced to less than 1. This accomplishment, certainly a significant improvement over the conventional process, offers greater reliability, but certain trade-offs must be made when the body of a MOSFET is floated.

Nominal source-to-drain breakdown voltages are reduced which limit the peak-to-peak signal range. Over-all breakdown is limited by the collector-emitter breakdown voltage, BV_{CEO}, of the non-parasitic transistor of the floating n-channel MOSFET. The breakdown voltage increases with the degree of reverse-bias potential applied to the substrate. With a floating body, BV_{CEO} is minimum, so particular care is necessasry when using these devices in configurations such as single-pole double-throw, dpst, and dpdt, where each side of the switch connects to opposite polarities. The peak-to-peak handling capability is specified at a minimum of 22V; therefore, 30V pk-pk cannot be switched with ±15V supplies, as it can with other CMOS devices.

What's more, the leakage currents of floating-body JI devices are higher than other types, simply because the ICEO of the floating base for the npn is much greater than ICBO of other devices having fixed reversed-biased body potentials. The increased leakage currents in spst switches may not be too significant.

However, in multiplexers that have the outputs of as many as 16 switches tied together in one IC, the total summation of currents can significantly affect system accuracy. For example, the specification for a worst-case 16-channel floating-body multiplexer is 10 microamperes, and the channel on resistance is 550 ohms. The DC offset error would be 5.5 millivolts, representing an accuracy to 0.055%.

Other 16-channel types specify worst-case parameters of 500 nanoamperes and channel resistance between 550 ohms and 2 kilohms. Their DC offset error is between 0.28mV and 1mV, respectively, allowing accuracy to 0.01% or better.

Finally, the effective off impedance of the floating-body switch is degraded by the floating-body technique. Off-isolation characteristics of a MOSFET are primarily determined by its source-to-drain capacitance. But with the base floating, the effective capacitance from emitter to collector is increased by the series combination of emitter-base and base-collector-junction capacitances (Figure 6a). This increase degrades the over-all off-isolation characteristics. For example, the off isolation for a typical floating-body channel at 1 megahertz that has R_L = 100 ohms is specified to be -54 decibels, which compares favorably with other types. However, at lower frequencies such as 1kHz, the isolation is only -62dB, compared to more than -110dB for improved devices. Capacitances C_1 and C_2 for them are shunted by the low AC impedance of the supply voltage (Figure 6b).

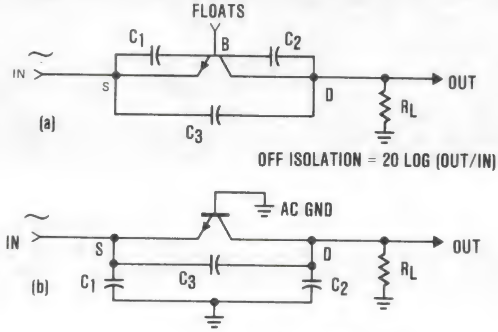


FIGURE 6. FLOATING BODIES.

Floating-body switches have degraded "off" impedance because total capacitance (a) combines two junction capacitances. In DI circuit (b), capacitances are shunted out.

The Linear Dielectric-Isolation Technology

The linear dielectric-isolation process requires no modifications to guard against latch-up. Its basic construciton ensures that the SCR configuration that causes latch-up can not exist. The functional cross section in Figure 7 reveals the silicon-dioxide isolation barrier fabricated between all parasitic transistors. This isolation allows each active element to be self-contained and independent with no interface junctions. At most, only three-layer structures are permitted for each tub, so that four-layer structures, or SCRs, are impossible. Also, since the DI technology requires no guard bands, junction capacitances, leakage currents, and size are minimized. The resulting increase in packing density per wafer, together with increased yields, enables these devices to be cost-competitive with other types.

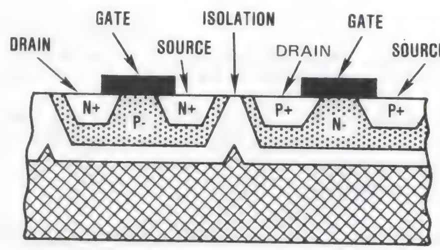


FIGURE 7. HOW DI DOES IT.

Dielectric isolation eliminates latch-up by a silicon-dioxide isolation barrier between devicees. This separates all active elements, eliminating interface junctions that cause parasitic SCRs.

In working with DI devices, the IC designer is not burdened with the fixed substrate potentials found in JI devices. He may let the substrate float, fix it to some

potential, or even modulate it. Figure 8 depicts a typical DI analog switch circuit that minimizes the variation of on resistance with the analog signal. Ordinarily, in conventional circuits, the body or substrate potentials of the n and p-channel devices are fixed and the source-to-body bias potentials vary with the analog input voltage. This change in body bias causes a wide variation of on resistance within the analog signal range. However, in the DI circuit, the bodies of P_1 and N_1 are connected together through N_3 during the on state. This allows the body to follow the input voltage providing a constant source-body bias and therefore a constant on resistance. During the offstate, the bodies of N_1 and P_1 are at their respective supply potentials through P_2 and N_2, thereby preserving high off isolation and low leakage currents.

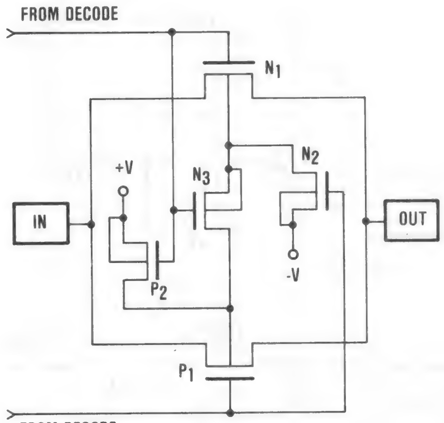


FIGURE 8. DI DOES IT.

In dielectrically isloated switches, on resistance modulation by the analog input is minimized by connecting N_1 and P_1 bodies together through N_3.

Designing a Foolproof CMOS Analog Multiplexer

In dielectrically isolated multiplexer circuits, protection can be provided on the chip primarily to eliminate channel interaction. This protection prevents normally off channels from being turned on by parasitics from other channels. And because this interaction is prevented, even worst-case power-supply faults cannot destroy the device. Moreover, since DI structures have no SCR effect, protection against latch-up and power-sequencing are not necessary. In short, DI multiplexers with built-in protection can withstand virtually any conceivable fault from the outside world.

The typical protected DI multiplexer (Figure 9) benefits from a combined bipolar/CMOS technology. The illustrated bipolar section is used to sense an analog over voltage condition and steer current away from the parasitic MOSFET junctions. Each of the switching devices, N_1 and P_1, has its own proteciton circuits. Devices P_3, D_6, D_7 and Q_6 protect P_1, while N_3, D_4, D_5 and Q_5 protect N_1. When the switch is off, the substrate of the p-channel FET, P_1, is connected to V+ through P_3 and diode D_7 for maximum isolation and low leakage currents in the off state. If the input voltage suddenly exceeds V+, the source-body junction, which would normally conduct, is instead clamped by transistor Q_6.

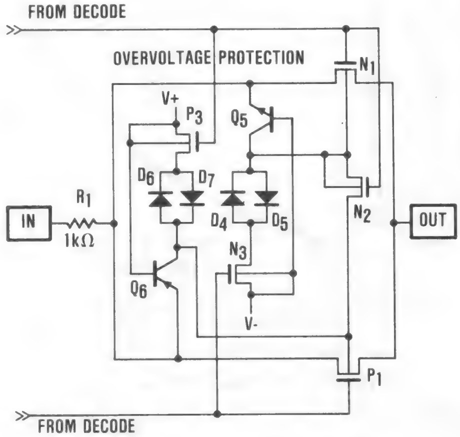


FIGURE 9. WINNING COMBINATION.

Combining bipolar and MOS technologies in the same multiplexer gives built-in protection. This circuit is typical for each channel in multiplexers HI-506A/07A/08A/09A and HI-546/47/48/49.

The base-emitter junction conducts to hold the source-body diode off with a saturation voltage VCE(SAT) of about 0.2V. Thus clamped, the switch is protected from the effects of overvoltage.

Clamp Q_6 always turns on before the forward-voltage drop of the source-body diode is exceeded because diode D6 requires an additional forward-voltage drop for conduction though the parasitic junciton. Moreover, resistor R_1 limits the current flowing through Q_6 when high overvoltages exist. Although R_1 adds to the total on-resistance of the channel, its associated error is insignificant, since most systems provide high-impedance buffering anyway. For negative overvoltages, N_1 is similarly protected. What's more, the protection circuit, rated at a continuous overvoltage of 35V, reveals a cross-talk current of only about 5nA (Figure 10).

When the switch is normally turned on, the substrates of N_1 and P_1 are connected together through N_2, which, as described before, results in a constant on resistance.

This condition represents an absolute error from channel interaction of only 6 microvolts ($R_{ON} \times 5nA$) - certainly negligible in most systems. In contrast, floating-body types have guarantees only that they won't be burned up by ±25V overvoltage. Their manufacturers do not make any claim against channel interaction. In fact, channel interaction occurs readily in these devices when the n- and p-channel thresholds are exceeded by an overvoltage.

10

APPLICATION NOTES

For example, the n-channel device, although floating, would be inadvertently turned on if the analog input exceeded the negative supply by its gate-to-source threshold, which is typically 1.5V.

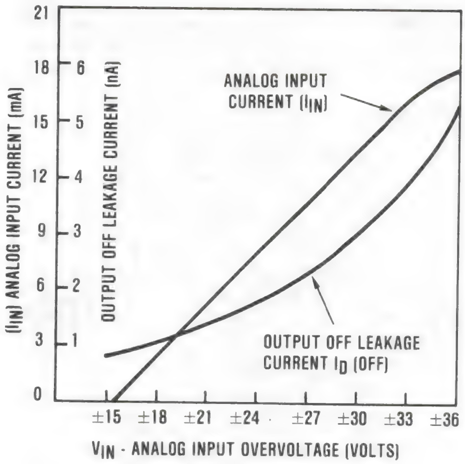


FIGURE 10. BLOCKING CROSS TALK.

DI switches have minimal cross-talk problems. An overvoltage of 33V produces a cross-talk current of only 5nA - an absolute error from channel interaction of only 6μV.

In addition to handling continuous input overvoltages, the **HI - 506 A / 546** series **multiplexers** also survive very large transient conditions. These devices typically withstand repeated static discharges well beyond 4,000 volts at any analog input. In fact, even the unprotected HI-506/507/508/509 units can withstand discharges beyond 3,000 volts, though they do not compare to the steady state and signal protection offered by the "A" series.

Adding Benefits

Additional DI benefits are passed on to the user in the design of the digital input-protection circuit shown in Figure 11. The fabrication of all components as isolated silicon islands eliminates any possibility of latch-up. The diodes switch fast and quickly discharge any static charge that may appear at the digital MOS input gates. Tests have shown that the digital inputs can typically withstand repeated discharges at the 2,000 volt level.

The DI technology enables a wide variety of active elements to be integrated on the same chip to provide maximum versatility. For example, in the transistor-transistor-logic/CMOS reference circuit shown in Figure 12, the bipolar technology enables realization of a simple zener reference circuit, consisting of resistor R_2 and transistors Q_1, Q_2, and Q_3.

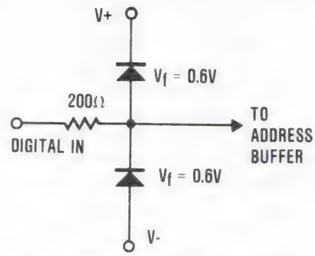


FIGURE 11. DIGITAL PROTECTION.

DI devices also protect digital inputs. For example, the diodes in this circuit quickly discharge any static charge that may appear on an MOS input gate.

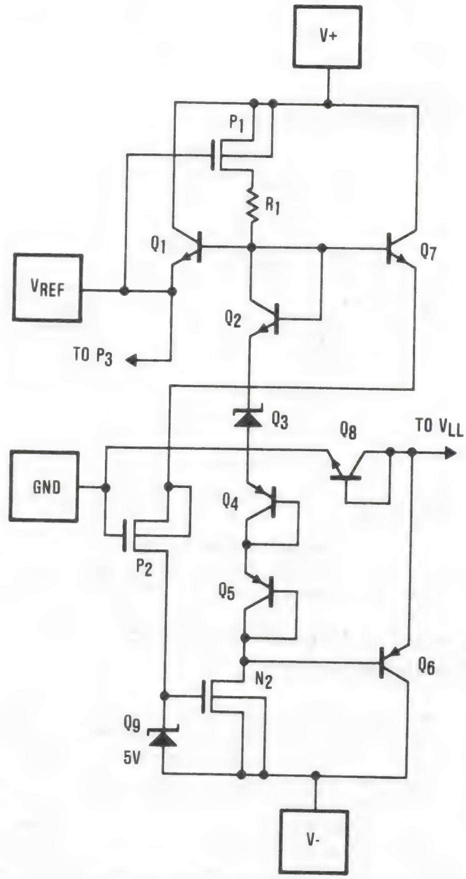


FIGURE 12. PACKING IT IN.

DI technology increases chip density of analog switch, allowing more circuit capability per package. For example, DI designs make possible this internal logic reference circuit in HI-200 and HI-201 switches.

The circuit develops a stable 5V reference for interfacing with TTL and eliminates the need for an additional 5V logic supply. Current for the zener (Q_3) is supplied through the normally on MOSFET, P_1, which can be easily turned off if not needed to minimize power consumption when interfacing with CMOS-logic circuits. P_1 turns off when V^+ or supply voltage V_{DD} is applied to the reference terminal V_{REF} to convert the ICs power consumption from bipolar to CMOS level. If power is not critical, V_{REF} can be left open to speed switching.

In high-speed data acquisition systems, the designer is concerned with both quiescent power and dynamic power consumption. If JI devices are used, the capacitance or leakage currents are so high they contribute a major portion of total power consumption. That situation is caused by the large-geometry parasitic junctions formed by the n- junction.

In contrast, the smaller substrate area of the DI device provides much less power drain. Dynamic-power consumption as a function of frequency for several 16-channel analog multiplexers ±15V supplies is shown in Figure 13. The DI device consumes only 100mW at 1MHz to yield the best speed-power product.

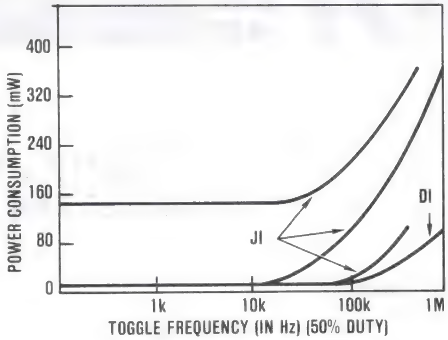


FIGURE 13. DI PERFORMS.

DI devices not only perform well, but do it with less power. Dynamic-power consumption data for commercial multiplexers shows DI device consuming only 100mW at 1MHz.

DIGITAL TO ANALOG CONVERTER TERMINOLOGY

By Dick Ti Tung

Introduction

In recent years the development and rapid reduction in cost of digital integrated circuits have resulted in an explosion in the applications of digital processing systems in the area of data acquisition and automatic process control. The need for a building block, such as the digital-to-analog converter (DAC), which interfaces the digital system with the analog world, is evident.

The purpose of digital-to-analog conversion is to produce a unique but consistent analog quantity, voltage or current, for a given digital input code. The most commonly used input digital code to a DAC is the natural binary number. A natural binary number is represented as

$$N = A_n 2^n + A_{n-1} 2^{n-1} + \ldots + A_1 2^1 + A_0 2^0 + A_{-1} 2^{-1} + \ldots + A_{-n} 2^{-n}$$

where the coefficients A_i (for $n \geqslant i \geqslant -n$) assume the values of "0" or "1" and is called a "bit". The left half portion of the binary number N

$$A_n 2^n + A_{n-1} 2^{n-1} + \ldots + A_1 2^1 + A_0 2^0$$

constitutes the integer part of the number N, whereas the right portion

$$A_{-1} 2^{-1} + A_{-2} 2^{-2} + \ldots + A_{-n} 2^{-n}$$

constitutes the fractional part of the number N. The bit that carries the greatest weight (left most bit) is called the most significant bit, or MSB. Similarly, the bit with the smallest weight (right most bit) is called the least significant bit, or LSB.

The analog output of a n-bit binary DAC is related to its binary number in the following manner:

$$E_o = FS(A_{-1} 2^{-1} + A_{-2} 2^{-2} + \ldots + A_{-n} 2^{-n})$$

where the term FS is defined as the nominal Full-Scale output of the DAC and it is known as the unreachable Full-Scale. It is easy to see that the actual Full-Scale output of the DAC, E_{FS}, with all the input bits "1" is

$$E_{FS} = FS(2^{-1} + 2^{-2} + \ldots + 2^{-n}) = FS(1-2^{-n}).$$

The term $FS(1/2^n)$ is the smallest output level that the DAC can resolve and it is known as the 1 LSB output level change. It is universal practice that the input code of a DAC is written in the form of binary integer with the fractional nature of the corresponding number understood.

As an example, the transfer function of an ideal 3-bit binary DAC is plotted as shown in Figure 1. Since a 3-bit DAC has only 8 discrete input codes which correspond to 8 different output levels (ranging from zero to 7/8 FS), no other output levels can exist and it is plotted as a bar graph. The line that connects the Zero and FS is called the Gain Curve.

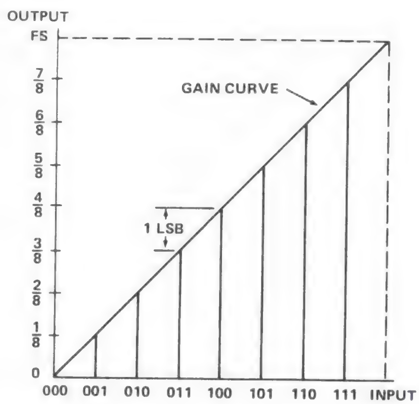


Figure 1 – Ideal Transfer Function Straight Binary (Unipolar)

There are two other input codings associated with binary DACs known as Bipolar codes, which are offset binary and two's complement binary codes. The offset binary code is obtained by offsetting the binary code such that the half-scale code, 10 . . . 0, becomes zero. And the two's complement code is achieved by inverting the MSB of the offset binary

code such that it is mathematically consistent with computer arithmetic. The transfer functions for the 3-bit DAC with offset binary input code and two's complement input code are plotted as shown in Figure 2 and Figure 3, respectively. (The +FS and -FS limits are used for easy interpretation of Bipolar operations. They are not confined by the previous definition of FS.)

In practical DACs, the zero output level may not be exactly zero (offset error), the range from zero to FS may not be exactly as specified (gain error), the differences in output levels may not be changing uniformly (nonlinearity), and so on. In selecting a DAC for a given application, some characteristics may have to be weighted more than the others. An understanding of some of the terms and characteristics involved in D/A conversion is helpful in choosing the correct part.

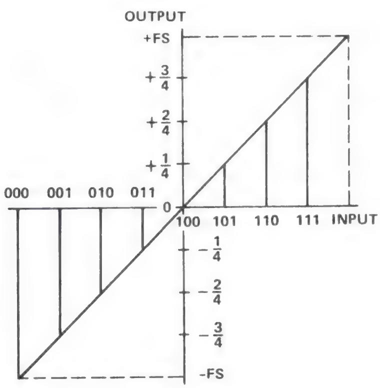


Figure 2 — Ideal Transfer Function Offset Binary (Bipolar)

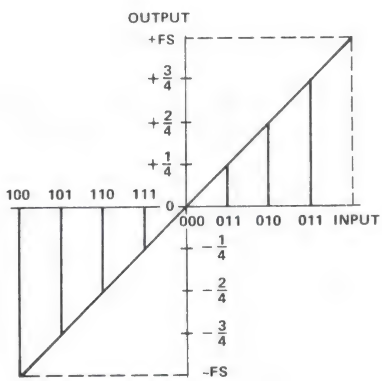


Figure 3 — Ideal Transfer Function Two's Complement (Bipolar)

Terminology

Least Significant Bit (LSB) — The digital input bit carrying the lowest numerical weight ($1/2^n$); or the analog output level shift associated with this bit ($FSR/2^n$) which is the smallest possible analog output step.

Most Significant Bit (MSB) — The digital input bit carrying the highest numerical weight (1/2); or the analog output level shift associated with this bit. In a binary DAC the MSB creates a 1/2 FSR output level shift.

Resolution — An indication of the number of possible analog output levels a DAC will produce. Usually, it is expressed as the number of input bits. For example, a 12-bit binary DAC will have $2^{12} = 4096$ possible output levels (including zero) and it has a resolution of 12 bits.

Absolute Accuracy — A measure of the deviation of the analog output level from the ideal value under any input combination. Accuracy can be expressed as a percentage of full scale range, a number of bits (n bits accuracy means a magnitude of $1/2^n$ FSR possible error may exist), or a fraction of the LSB (if a DAC with n-bit resolution has 1/2 LSB accuracy the magnitude of the possible error is $1/2(1/2^n FSR)$). Accuracy may be of the same, higher, or lower order of magnitude as the resolution. Possible error in individual bit weight may be cumulative with combination of bits and may change due to temperature variations. Usually, the accuracy of a DAC is expressed in terms of nonlinearity, differential nonlinearity, and zero and gain drift due to temperature variations.

Nonlinearity (linearity error) — A measure of the deviation of the analog output level from an ideal straight line transfer curve drawn between zero and full scale (commonly referred as endpoint linearity).

Differential Nonlinearity — A measure of the deviation between the actual output level change from the ideal (1 LSB) output level change for a one bit change in input code. A differential nonlinearity of ±1 LSB or less guarantees monotonicity; that is the output always increases for an increasing input.

Gain Drift — A measure of the change in full scale analog output, with all bits 1's, over the specified temperature range expressed in parts per million of full scale range per ^oC (PPM of FSR/^oC). It is measured with respect to +25^oC at high (T_H) and low (T_L) temperature, and it is specified the larger of the two representing worst case drift.

Offset Drift (Unipolar or Bipolar) — A measure of the change in analog output, with all bits 0's, over the specified temperature range expressed in parts per million of full scale range per ^oC (PPM of FSR/^oC). It is measured with respect to +25^oC at high (T_H) and low (T_L) temperature, and it is specified the larger of the two representing worst case drift.

Settling Time – The total time measured from a digital input change to the time the analog output reaches its new value within a specified error band. Usually, the settling time is specified for a DAC to settle for a Full-Scale code change (00 . . . 0 to 11 . . . 1 or 11 . . . 1 to 00 . . .0) to within $^{+}1/2$ LSB of its final value.

Compliance – Compliance voltage is the maximum output voltage range that can be tolerated and still maintain the specified accuracy.

The effects of gain error, offset error, nonlinearity, and differential nonlinearity on the transfer functions are plotted, respectively, as shown in Figure 4, 5, 6, & 7. A conversion chart which shows the number of bits and its resolution is given in Table 1.

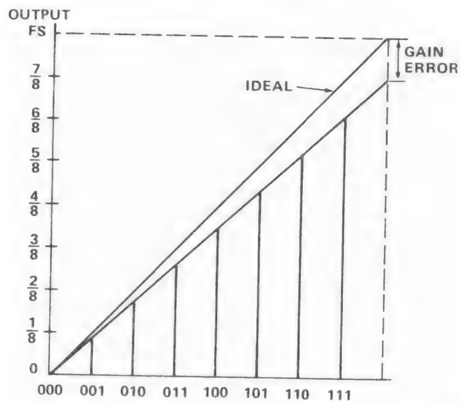


Figure 4 – Gain Error

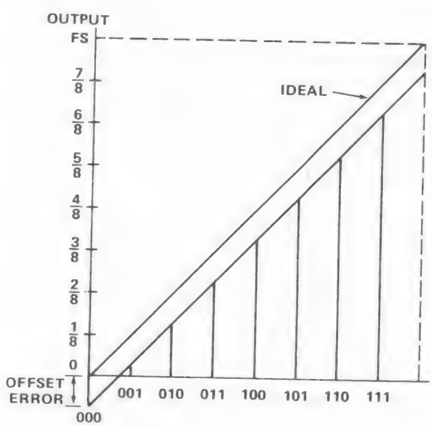


Figure 5 – Offset Error

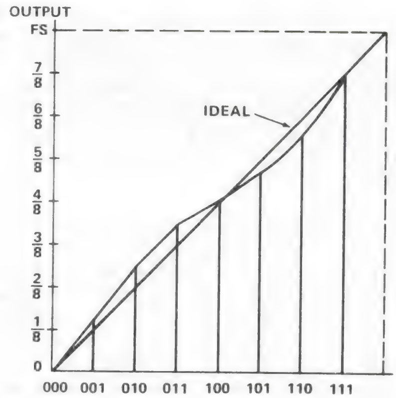


Figure 6 – Linearity Error

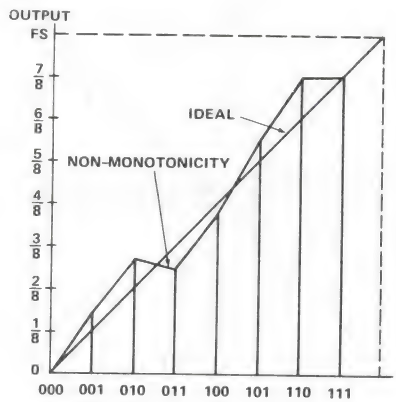


Figure 7 – Differential Linearity Error (Non-Monotonicity)

Table 1 – Conversion Chart

# OF BITS	LSB	RESOLUTION		TEMPCO PPM/°C – 1 LSB DRIFT OVER	
		%	PPM	0°C ⩽ TA ⩽ 75°C	-55°C ⩽ TA ⩽ 125°C
6	FS/64	1.5620	15,625	208.3	86.8
7	FS/128	0.7812	7.812	104.2	43.4
8	FS/256	0.3906	3,906	52.1	21.7
9	FS/512	0.1953	1,953	26.0	10.9
10	FS/1024	0.0977	977	13.0	5.4
11	FS/2048	0.0488	488	6.5	2.7
12	FS/4096	0.0244	244	3.3	1.4
13	FS/8192	0.0122	122	1.6	0.68
14	FS/16384	0.00610	61	0.8	0.34
15	FS/32768	0.00305	31	0.4	0.17
16	FS/65536	0.00153	15	0.2	0.08

DIGITAL TO ANALOG CONVERTER HIGH SPEED ADC APPLICATIONS

By Dick Ti Tung and Tom Westenburg

Analog-To-Digital Converter (ADC)

The uses of high speed DACs in CRT display, industrial process control, signal regeneration, etc., are well established. Perhaps one of the most important applications is to use the DAC in high speed ADC design. There are two types of ADC design where high speed and high resolution DACs are essential.

TRACKING ADC OR SERVO TYPE ADC

The tracking ADC is very efficient in monitoring one analog signal continuously, converting it into a sequence of digital codes representing the analog signal in real time.

Functionally, the analog input is compared with the output of a DAC, with the digital input of the DAC being driven by a counter. After the ADC is turned on, the counter increments until the DAC output crosses the analog input value. The counter will then, running up or down, drive the DAC 1 LSB at a time to track the input signal. The counter state represents the digital equivalent of the input signal.

In Figure 1, the analog input is fed into the span resistor of a DAC. The analog input voltage range is selectable in the same way as the output voltage range of the DAC. The net current flow through the ladder termination resistance, i.e.2kΩ for HI-562A produces an error voltage at the DAC output. This error voltage is compared with 1/2 LSB by a comparator. When the error voltage is within ± 1/2 LSB range, the Q output of the comparators are both low, which stops the counter and gives a data ready signal to indicate that the digital output is correct. If the error exceeds the ±1/2 LSB range, the counter is enabled and driven in an up or down direction depending on the polarity of the error voltage.

Since the digital output changes state only when there is a significant change in the analog input, the data ready signal is then very useful in adaptive systems or computer systems for efficient data transfer. When monitoring a slowly varying input, it is necessary to read the digital output only after a change has taken place. The data ready signal could be used to trigger a flip-flop to indicate the condition and reset it after read-out.

The main disadvantage of the tracking ADC is that the time required to initially acquire a signal, for a 12 bit ADC, could be up to 4096 clock periods. The input signal usually must be filtered so that its rate of change does not exceed the tracking range of the ADC (1 LSB per clock period).

SUCCESSIVE-APPROXIMATION ADC

Perhaps the most widely used technique for a high speed analog-to-digital converter design is the successive approximation method. Ideal for interfacing with computers, this type is capable of both high speed and high resolution, and the conversion time is fixed and independent of the magnitude of the input voltage.

Figure 2 shows a block diagram of a successive-approximation ADC. When a negative going start conversion pulse is applied to the ADC, the internal registers of the successive approximation register (SAR) are set to low except for the MSB, which is set to high. This turns on the MSB of the DAC. The FS output current of the DAC is compared with the current fed through the span resistor by the analog input. The net current flow through the ladder termination resistance produces an error voltage at the DAC output. This error voltage is then compared with a fixed reference by a comparator to determine whether the analog input is greater or less than the present state of the DAC. The result of the comparison is clocked into the SAR at the rising edge of the clock. The MSB of the SAR will be set to high if the analog input is greater; otherwise, it will be set to low. At the same time, the second bit of the SAR is set to high with the remaining bits at their previous states. During the second clock period, the sum of the result of the first choice and the weight of the second bit is compared with the analog input. The second bit is set to high or low in the same manner as the MSB, and so on, until the LSB is updated.

During this conversion time, the output of a status flip-flop is set to high, indicating that a conversion is taking place. It will return to low at the end of conversion to signify that the output state of the SAR represents the digital equivalent of the input analog voltage.

It is easy to see that in any successive-approximation ADC application, the analog input should remain reasonably constant during the conversion to avoid erroneous results. This is usually accomplished by using a sample-and-hold circuit in the analog line.

However with the new digital error correction circuitry incorporated in the HI-774A the input can vary. During the first portion of the conversion the input can move up to +0.78%/-0.76% of FSR and remain 12-bits accurate. This error correction window allows the user to start a conversion before the input has completely settled.

Data Acquisition System

The typical data acquisition system is depicted in Figure 3. The HI-506 multiplexer is used as an analog input selector. Which is controlled by a binary counter to address the appropriate channel. The HA-5330 is a high speed sample and hold. Sample Hold Control is tied to the status (STS) output of the HI-774A, so that whenever a conversion is in process the S/H is in the hold mode. A conversion is initiated by the clock input going low, and when the clock goes high the mux address changes. The mux will be acquiring the next channel while the ADC is converting the present input, held by the S/H. The clock low time should be between 225ns and 6.5μs, with the period greater than 8.5μs. With this timing R/C will be high at the end of a conversion so the output data will be valid ~100ns before STS goes low. This allows STS to clock the data into the storage register. The register address will be offset by one, if this is a problem then a 4-bit latch can be added to the input of the storage register. With a 100KHz clock rate each channel will be read every 160μs.

This 16-channel data acquisition system is applicable to industrial process control, and multi-channel panel display. It can also interface with an intelligent terminal, such as a micro-computer system, to provide multi-channel data conversion function. The offset error and gain error of the data acquisition system over the operating temperature range can be easily compensated by proper programming.

By the same token, a 15-channel data acquisition system with offset correction could be easily incorporated as shown in Figure 4. Consider the case that one of the analog input channels is dedicated to sense the ground level, and its binary equivalent is stored in latch register B in its complementary form to establish a ground reference in real time. All the other analog input channels will then be converted and stored in register A, one at a time. The binary adder will perform the binary subtraction in less than 1μs for the given pair of A and B. This, in fact, eliminates the offset error of the ADC, offset error of the S/H circuit, and excess droop of the S/H due to temperature variation.

This circuit is easy to implement and is especially useful when an intelligent terminal is not available. To expand this concept one step further, the gain error of the system due to temperature variations could also be eliminated if a binary multiplier is used to correct the gain facter in real time.

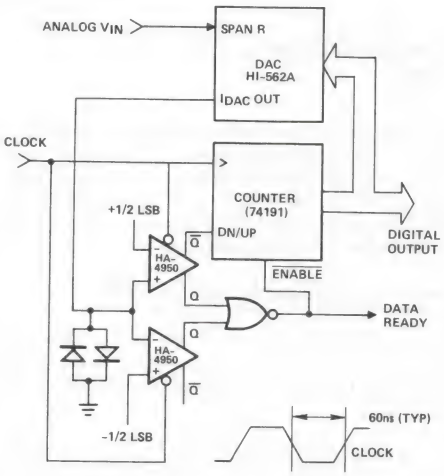


Figure 1. Tracking ADC

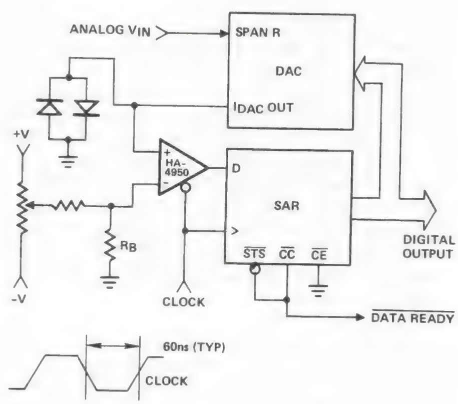


Figure 2. Successive-Approximation ADC

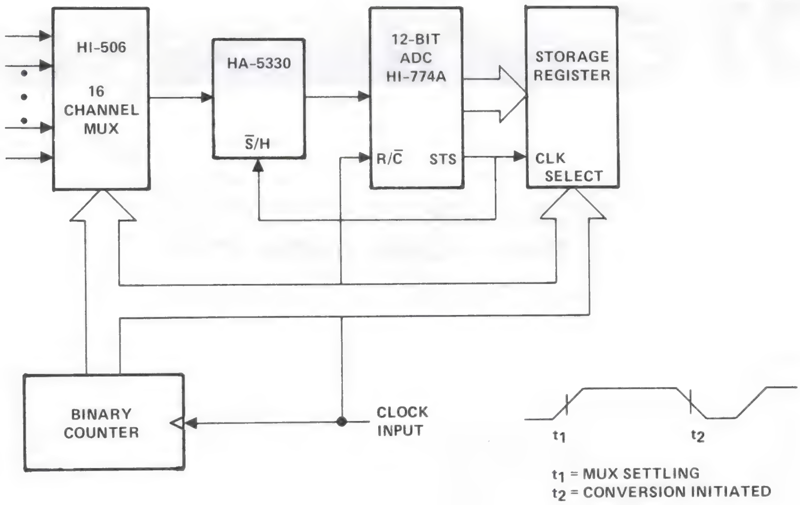


Figure 3. 16 Channel Data Acquisition System

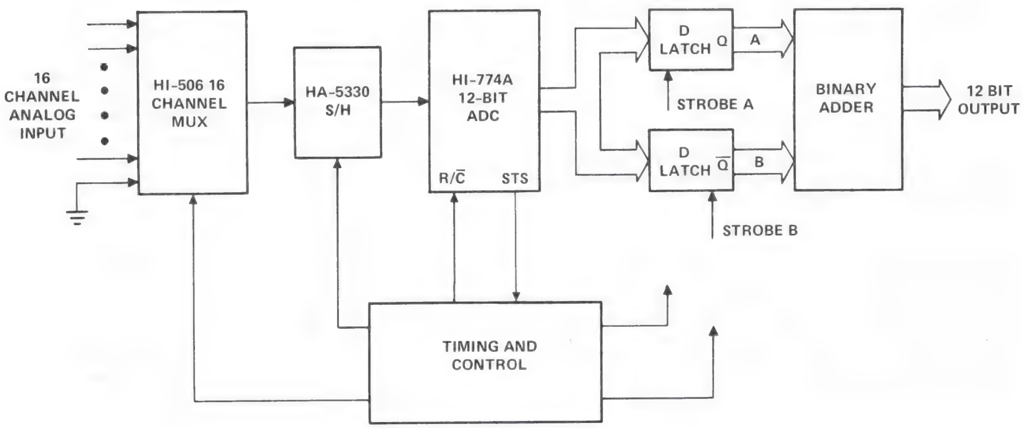


Figure 4. 15 Channel Data Acquisition System with Offset Correction

10
APPLICATION
NOTES

APP NOTE

FOR YOUR INFORMATION

No. 525

Harris Analog

HA-5190/5195 FAST SETTLING OPERATIONAL AMPLIFIER

By G. Cotreau, D. Jones, R. Whitehead

Introduction

The military temperature range HA-5190 and its commercial temperature equivalent, HA-5195, are monolithic operational amplifiers featuring ±200V/μs slew rate, 150MHz gain-bandwidth-product, and 70ns settling time. Similar performance has previously been available only in more costly modular and hybrid amplifiers, which require much higher bandwidth and slew rate to achieve the same settling time as HA-5190/5195. Since it exhibits a classical -6dB/octave rolloff over most of its frequency range, remarkably smooth output wave forms are generated by HA-5190 when reasonable care is employed.

Applications for this op amp include pulse, RF, and video amplifiers, wave form generators, high speed data acquisition and instrumentation circuits.

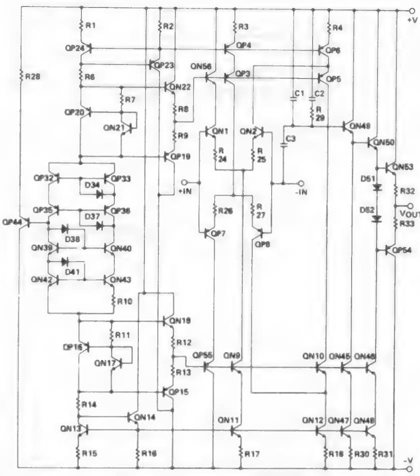


Figure 1. HA-5190/5195 Schematic.

Inside the HA-5190/5195

Figure 1 shows the schematic of the HA-5190/5195 design. The schematic can be simplified to show the AC signal path as shown in Figure 2.

The input stage consists of two symmetrical differential transistor pairs. The signal path for positive going signals is Q_1, Q_2, and Q_3, while negative going signals pass through Q_4, Q_5, and Q_6. The signal then goes through the output stage (represented by the voltage follower symbol) consisting of one PNP and two NPN emitter followers.

In Figure 2, the compensation network is C_1, C_2, C_3, and R_{29}. This network makes the amplifier system appear as second-order critically damped. The scheme produces the dominant pole plus two zeros. The zeros are positioned to cancel the effects of undesired poles developed by the F_t of the transistors.

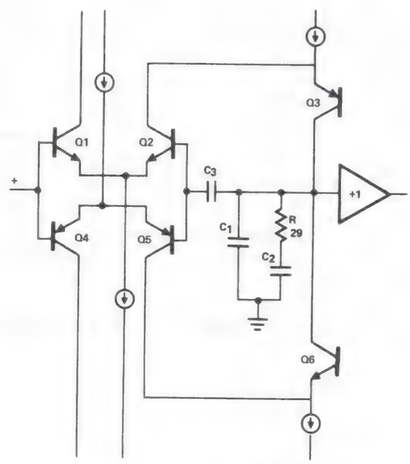


Figure 2. Simplified HA-5190 Schematic.

Considerations For Prototyping

When using the HA-5190, high frequency layout techniques are recommened for bread-boarding. The device should be mounted through a ground plan and all No Connect (NC) Pins should be tied to this plane for pin isolation. If an IC socket is to be used, Teflon types are recommended. Feedback components should be mounted between Teflon insulated standoffs located as close as possible to the device pins.

The input impedance characteristic of the HA-5190 is such that the closed loop performance (DC and AC) will depend on both the feedback component ratio and the actual impedance presented to each amplifier input. For best high frequency performance, resistor values for feedback networks should be limited to a maximum of 5K ohms (preferably less than 1K ohm). Film type resistors are recommended. Power supply decoupling with ceramic capacitors from the device supply pins to ground is essential.

It is recommended that optimum circuit values for a particular application be developed through experimentation using amplifiers from several production runs. The PC artwork in the vicinity of the HA-5190 should be prototyped early to determine any sensitivites to layout.

OPERATION AT ELEVATED TEMPERATURES

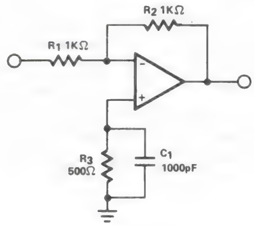
HA-5190/5195 may be used without a heat sink up to +75°C, ambient. Above this temperature, the power derating is 9.6mW/°C for the 14 Lead Ceramic DIP. THERMALLOY Model 6007 or AAVID Model 5602B are recommended. For the 12 Lead To-8 Metal Can, derate at 11.5mW/°C and recommended heat sinks are THERMALLOY Model's 2240A or 2268B.

FREQUENCY COMPENSATION

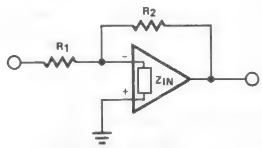
HA-5190/5195 is stable in standard DC amplifier configurations with closed loop gains exceeding +5 or -4. At these or higher gains, optimum AC performance can be achieved by keeping network resistor values as low as is practical.

Quite simple circuitry, as illustrated in Figure 3, gives excellent performance for lower closed loop gains. The compensation schemes use the amplifier's differential input impedance to reduce both the input and feedback signals thereby raising the effective noise gain approximately 14dB to a stable point on the frequency response curve.

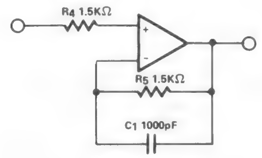
Inverting and non-inverting unity gain connections for HA-5190 are shown in Figure 3 (a) and (c). R_3 and R_5 serve only to balance DC voltage offsets due to input bias current, and may be replaced with a short for AC applications. C_1 is not neccessary for stability, but helps reduce overshoot and smooth the frequency response. Settling time or frequency response can be optimized (about 30MHz small signal bandwidth is practical) by fine tuning component values.



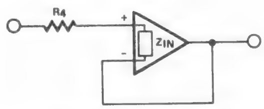
(a) Gain = -1



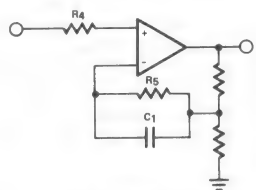
(b) Stabilization using Z_{IN}.



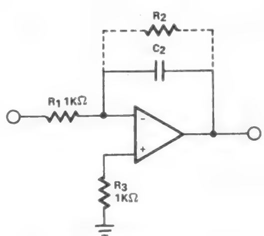
(c) Gain = +1



(d) Stabilization using Z_{IN}.



(e) Non-inverting gain stage.



(f) Integrator

Figure 3. Compensation recommended when $1 + \frac{R_2}{R_1} < 5$.

For closed loop gains between 1 and 5, reducing R_1 in Figure 3 (a) and (e) will raise the gain with minimum effect on bandwidth. However, in the inverting configuration, R_1 determines the input impedance, and it may be more practical to raise R_2 at the expense of bandwidth. In Figure 3 (e), R_4 and R_5 may be reduced as gain is increased and removed entirely at gains greater than +4.

For applications requiring 100% feedback at high frequencies, such as integrators and low pass filters, HA-5190/5195's compensation scheme should be thoroughly evaluated through experimentation. The circuit in Figure 3 (f) is quite stable, using the two 1K ohm resistors.

Suggested Methods For Performance Enhancement

To avoid compromising AC performance, the HA-5190 design does not include provisions for internal offset adjustment.

The circuits in Figure 4 (a) and (b) show two possible schemes for offset voltage adjustment.

Figure 5 (a) and (b) uses the inherent qualities of the FET to reduce input bias currents by several orders of magnitude and raise input impedance to thousands of megohms. Both circuits are shown in the unity gain follower mode. Circuit gain can be implemented using normal feedback techniques. To optimize for speed, care should be taken in layout. Experimental results yielded slew rates of approximately 130V/μs.

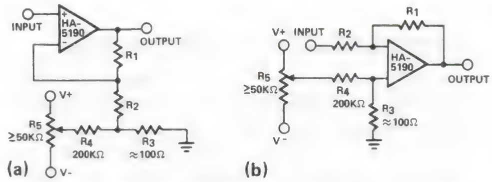
Figure 5 (c) illustrates a composite inverting amplifier which greatly reduces DC errors due to the HA-5190 input bias current and gain, while retaining superior settling time. The 0 dB frequency of the integrator section approximates the open loop low frequency pole (~2.5kHz) of the HA-5190. This circuit might also be connected as a current-to-voltage amplifier for use with a high accuracy, high speed DAC.

Figure 6 shows a composite amplifier scheme for boosting output current drive of the HA-5190/5195. The circuit gain (shown A_V = 5) can be adjusted using normal feedback systems. HA-5190 used in conjunction with HA-5033 can drive 50 ohm coaxial cable, with proper termination to 250MHz.

Applications

INTRODUCTION

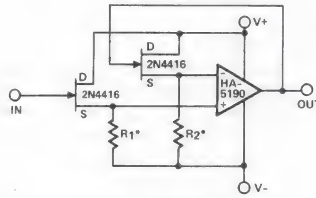
HA-5190/5195 represents an ideal building block for high speed, precision data acquisition systems and for video pulse amplification. Although this amplifier can be used in a wide variety of other applications, the ones to be discussed show where it can be used most advantageously.



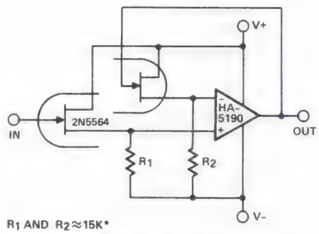
RANGE OF ADJUSTMENT FOR BOTH NON-INVERTING (LEFT) AND INVERTING AMPLIFIERS (RIGHT) DETERMINED BY PRODUCT OF V_{SUPPLY} AND R_3/R_4 RATIO.

$$A_V = 1 + \frac{R_1}{R_2 + R_3}$$

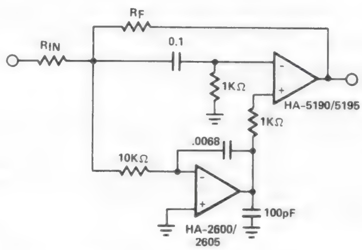
Figure 4. Offset Nulling.



(a) * VALUES SHOULD BE DETERMINED EXPERIMENTALLY FOR OPTIMIZED PERFORMANCE.



(b) R_1 AND $R_2 \approx 15K^*$
INPUT FETS ARE MATCHED PAIR 2N5564



(c)

Figure 5. Reducing Input Bias Currents.

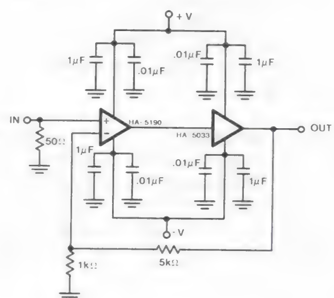


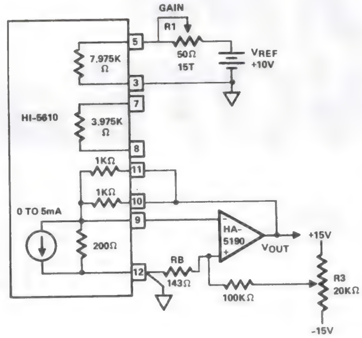
Figure 6. Boosting Output Current.

Application 1 Fast DAC Output Buffer

The circuit at right illustrates the HA-5190's usefulness as a high speed DAC buffer.

The amplifier operates as a current-to-voltage converter/output buffer to the HI-5610 which is a precision 10 bit DAC with output current settling time less than 100ns. The voltage divider on the non-inverting input serves to null any DC errors introduced into the system. The amplifier maximizes speed of the system since its dynamic performance exceeds that of the DAC.

Application 1



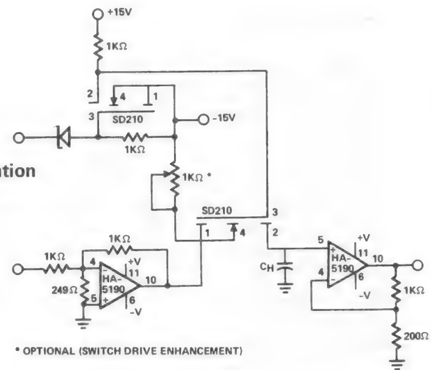
Application 2 High Speed Sample/Hold

Sample/Hold circuits are used in many areas of data acquisition systems such as de-glitchers for D/A converters and input stages for successive approximation A/D converters.

The circuit at right uses the speed and drive capability of the HA-5190 coupled with two high speed DMOS FET switches.

The input amplifier is allowed to operate at a gain of -5 although the overall circuit gain is unity. Acquisition times of less than 100ns to 0.1% of a 1 volt input step are possible. Drift current can be appreciably reduced by using FET input buffers on the output stage of the Sample/Hold.

Application 2

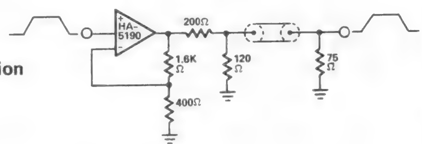


Application 3 Video Pulse Amplifier/75 ohm Coaxial Driver

HA-5190/5195 is also well suited for video pulse applications. The circuit at right could be found in various types of video broadcasting equipment where 75 ohm systems are commonly employed.

HA-5190 can drive the 75 ohm coaxial cable with signals up to 2.5 volts peak-to-peak without the need for current boosting. In this circuit the overall gain of the circuit is approximately unity because of the impedance matching network.

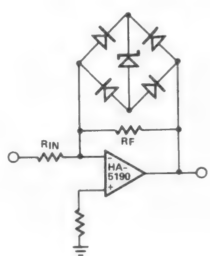
Application 3



Application 4 Output Limiter

HA-5190 is rated for ± 5 volt output swing, and saturates at ± 7 volts. As with most op amps, recovery from output saturation is slow compared to the amplifier's normal response time; so some form of limiting, either of the input signal or in the feedback path, is desirable if saturation might occur. The circuit above illustrates a feedback limiter, where gain is reduced if the output exceeds ± (Vz + 2Vf). A 5 volt zener with a sharp knee characteristic is recommended.

Application 4



VIDEO APPLICATIONS HA-5190/5195

By L. E. Garner

Introduction

Offering superior performance in video and RF circuits, the HA-5190/5195 family can be used effectively in the design of television broadcast studio equipment, test instruments, and monitoring or surveillance TV systems. A very high 200V/μs slew rate, a full power bandwidth of 6.5MHz, and a fast settling time of only 70ns (typ) are but three of the unique characteristics which make these devices ideal for critical wideband video and RF applications. Other features include true differential operation, excellent stability with gains $\geq$5, and complete freedom from latch up, the latter a result of the exclusive HARRIS dielectric isolation process combined with optimized chip design and layout.

The op amp family can be used, typically, as studio tape head, test instrument, and video camera preamplifiers, as buffers, as broadcast relay link repeaters, as coaxial line drivers, and as cable or industrial system video repeater and bridging amplifiers. Extremely versatile, the devices can be operated effectively in AGC and dc gain controlled configurations as well as in fixed gain designs, and are fully capable of driving low impedance loads.

When used in standard video amplifier configurations, the HA-5190/5195 devices easily meet or exceed the performance tolerance specifications of applicable current FCC (NTSC) composite TV signal standards as well as the requirements of EIA Tentative Standard RS-170A.

Video Performance

The overall color video performance of the HA 5190/5195 family was confirmed by checking a number of standard devices. Tests were made to determine both video response and signal/noise ratio under typical operating conditions. The basic video amplifier circuit illustrated in Figure 1 was used for the tests, with the actual procedures abstracted from those described in EIA Standard RS-250-B. The general test setup is shown in Figure 2.

VIDEO RESPONSE TESTS

Referring to Figure 1, the test video amplifier comprised an HA5190/5195 op amp, BNC coaxial input jack J1, input level control R1 shunted by impedance matching resistor R2, input series stabilization resistor R3, gain control network R4-Rgain, series output limiting resistor Rs, and BNC coaxial output jack J2. Operational power was supplied by a well regulated and filtered dual line operated power supply.

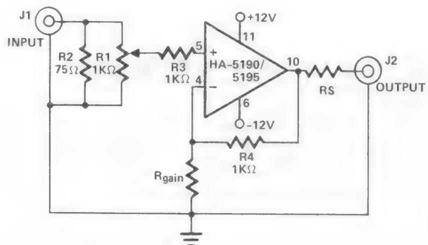


Figure 1–Test Video Amplifier

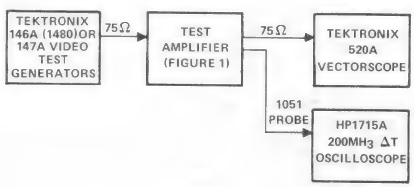


Figure 2–Video Response Test Setup

Initially, standard NTSC and EIA ramp and timing test signals were applied using the Tektronix Models 146A (1480) and 147A video test generators. Amplifier performance was observed and measured at various levels with a Tektronix 520A Vectorscope and HP Model 1715A 200MHz delta time Oscilloscope Three of the RS-250-B specified test waveforms used are illustrated in Figure 3, including the (a) ramp linearity, (b) 12.5T and 2T sine-squared pulse and bar, and (c) multiburst signals. With the test signal level maintained at 1.0V p-p, level control R1 was adjusted as needed to establish a 1.0V p-p output signal (at J2) for each gain value. The Vectorscope was used to measure color differential phase and gain, with the Oscilloscope used to check for distortion of the 2T, 12.5T, multiburst and color bar signals. The average test results are summarized in Table A. All measured values were well within applicable specifications.

Table A - Summary of Test Results

NOMINAL GAIN	R_{gain}	R_s	DIFF ϕ	DIFF GAIN	2T	12.5T	MULTI	COLOR BARS
1	∞	0	-0.2°	-0.5%	UNM*	UNM*	FLAT	UNM*
2	1k	75Ω	-0.15°	≈0	UNM*	UNM*	FLAT	UNM*
5	251Ω	200Ω	-0.2°	≈0	UNM*	UNM*	FLAT	UNM*
10	110Ω	200Ω	-0.4°	-0.5%	UNM*	UNM*	FLAT	UNM*

*UNM : UNMEASURABLE DISTORTION

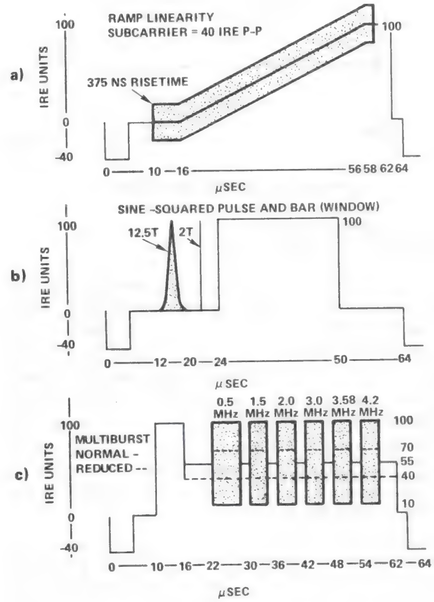


Figure 3—Video Test Signal Waveforms

S/N RATIO

Signal/noise (S/N) ratio measurements were made using the same basic amplifier configuration, but with Rgain fixed at 251Ω, ±1%, and Rs at 200Ω ±5%. The dc power supply terminals were bypassed with a 100 μ F tantalum capacitor. A Tektronix 147A NTSC Test Signal Generator was used as a signal source, with output measurements made using a Rhode & Schwartz Video Noise Meter, as diagrammed in Figure 4. The Tektronix 147A was set to deliver a flat field signal at 50 IRE units, with the R&S Video Noise Meter adjusted as follows: (a) 10kHz High pass, (b) Video Bandpass, (c) Subcarrier Trap OFF, (d) Internal Sync, (e) Tilt & Sag Comp OFF.

Under the specified conditions and with level control R1 adjusted to deliver a 1.0V p-p signal at J2, the measured p-p signal/RMS noise ratio averaged 68dB, or well over the minimum value required by applicable standards.

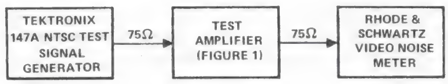


Figure 4—S/N Ratio Test Setup

General Considerations

Since the HA-5190/5195 devices do not require special treatment, optimum video performance can be achieved by observing standard high frequency design and wiring practices. However, the following suggestions, abstracted in part from HARRIS Application Note 525, should prove helpful when developing practical designs.

POWER SUPPLY REQUIREMENTS

A well-regulated, well-filtered dual dc power source is required for best operation, for the op amps draw moderate currents during normal operation. Although not essential in all applications, it is recommended that the power supply lines be decoupled using 0.01 μ F ceramic capacitors to circuit ground, with the capacitors located as near to the amplifier terminals as possible to minimize lead inductances. For optimum performance and operation at specified parameters, the dc power supply should furnish not less than ±10V dc, with higher source voltages (±15V, typically) preferred.

TEMPERATURE CONSIDERATIONS

The HA-5190/5195 devices can be used without heat sinks at ambient temperatures up to 75°C. Under these conditions, the internally generated heat stabilizes device operation and ensures relative immunity

to external temperature variations. At ambients above 75°C, however, the 14 Lead Cerdip devices should be derated 9.6mW/°C, with a suitable heat sink, such as a THERMALLOY Model 6007, or AAVID Model 5602B. To provide adequate heat dissipation. For the 12 Lead To-8 Metal Can derate at 11.5mW/°C and recommended heat sinks are THERMALLOY's 2240 or 2268B. Application Note 556 also suggest safe operating area conditions.

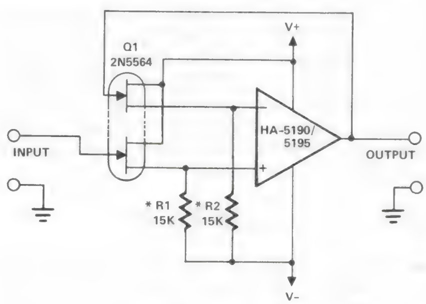
Under some conditions, the internally generated heat can affect other components. Therefore, avoid mounting temperature sensitive devices or components near or directly adjacent to the op amps.

DESIGN HINTS

Except for their exceptional performance specifications, the HA-5190/5195 devices are essentially standard op amps and may be treated as such by the video equipment or system designer. Thus, conventional design techniques may be used when developing specific circuit configurations, as long as maximum ratings are observed and adequate compensation is made for device operational characteristics. For example, the closed loop performance (dc and ac) at gains$\geq$5 depends on both the feedback component ratio and the actual impedance at each amplifier input. Since the devices offer a comparatively low input impedance, feedback network resistor values should be 5kΩ or less (preferably, less than 1kΩ) for optimum high frequency performance.

If the intended video application requires a high input impedance, a FETpreamp stage may be added ahead of the HA-5190/5195 op amp, as shown in Figure 5. Full details and an additional FET input circuit are provided in HARRIS Semiconductor Application Note 525.

Where used, a FET preamp not only raises the effective input impedance from (approximately) 10kΩ to thousands of megohms, but also reduces the input bias current requirement by several orders of magnitude. There is, of course, a trade-off in frequency response, with a FET input stage reducing the effective overall slew rate from 200V/μs to 130V/μs (typically). However, the full power bandwidth with a FET input is more than adequate for all low to mid level video applications.



*Approximate Values

Figure 5– FET Input Circuit

Some video applications may require output currents which exceed the maximum capabilities of the HA-5190/5195 devices. In these cases, the HA-5190/5195 op amps can be teamed with high performance current boosters such as, for example, the HA-5033. A typical cascaded op amp/booster circuit is illustrated in Figure 6. Since the current booster, a unity gain device, has a typical slew rate and bandwidth (Slew Rate = 1300V/ μs FPBW = 65MHz) far grater than that of the op amp, the overall frequency performance of the composite amplifier is essentially that of the op amp alone.

To compensate for manufacturing tolerances and ensure optimum performance, the fixed component values used in specific designs should be finalized empirically, using active devices from several production runs.

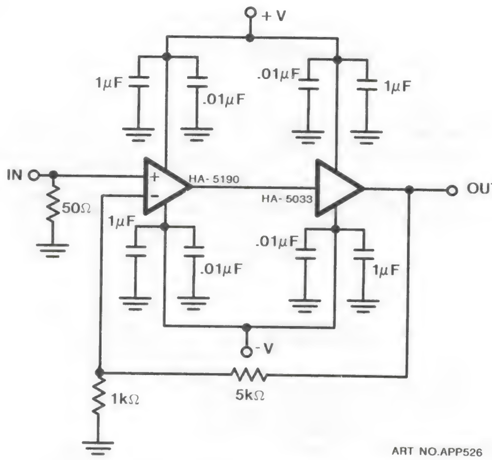


Figure 6—Boosting Output Current

PROTOTYPING TIPS

In accordance with standard engineering practice, new circuit designs should be breadboarded to verify overall operation. Afterwards, a number of preproduction prototypes identical to the planned production design should be assembled and tested using active devices from several production runs. These prototype tests permit optimization of component values and determination of circuit sensitivities to layout and component positioning. Preliminary environmental tests, if required, also may be made using the prototypes.

If IC sockets are used, Teflon types are preferred to minimize distributed capacitances. For the same reason, feedback components should be mounted between Teflon insulated standoffs located as close as practicable to the device pins or socket terminals. For maximum stability, film type resistors are recommended for the feedback networks.

Signal carrying leads should be kept short and direct, of course, to minimize both lead inductances and distributed capacitances. The devices should be mounted through a ground plane. If this is impracticable, single point grounding should be used to avoid ground loops.

Typical Applications

The test circuit given in Figure 1 may be used as a general purpose video amplifier, although minor changes in component values may be needed to optimize operation for specific requirements. Additional practical circuits are illustrated in Figures 7 and 8.

RF AGC AMPLIFIER

Designed and checked as a buffer for the head preamp of a studio video tape recorder, the circuit shown in Figure 7 functions as a wide band adjustable AGC amplifier. With an effective bandwidth of approximately 10 MHz, it is capable of handling RF input signal frequencies from 3.2 to 10MHz at levels ranging from 40mV up to 3V p-p.

AGC action is achieved by using opto coupler/isolator OCI as part of the gain control feedback loop. In operation, the positive peaks of the amplified output signal drive the OCI LED into a conducting state. Since the resistance of the OCI photosensitive element is inversely proportional to light intensity, the higher the signal level, the lower the feedback resistance to the op amp inverting input and hence the greater the negative feedback, thereby lowering stage gain. Any changes in gain occur smoothly because the inherent memory characteristic of the photoresistor acts to integrate the peak signal inputs. In practice, the stage gain is adjusted automatically to a point where the output signal positive peaks are approximately one diode drop above ground.

GAIN SET control R5 applies a fixed dc bias to the op amp non-inverting input, thus establishing the steady-state zero input signal current through the OCI LED and determining the signal level at which AGC action begins. In experimental tests under large signal conditions (i.e., E_{IN} = 3V p-p), a GAIN SET value of -0.26V provided unity gain, while a value of -1.55V yielded on A_V of 2.7 , with a flat response to 5.0MHz at both levels. Under small signal conditions (i.e., E_{IN} = 40mV), gains from 8 to 50 could be achieved as the GAIN SET value was adjusted from 0.65V to -80mV. At A_V = 8, the frequency response was flat to 5MHz, while at A_V = 80, the response was limited to that of the HA-5190/5195.

The effective AGC range depends on a number of factors, including individual device characteristics, the nature of the RF drive signal, the initial setting for R5, et al. Theoretically, however, the AGC range can be as high as 4000:1 for a perfect op amp, for the OCI photoresistor can vary in value from 1 Megohm with the LED dark to 250Ω with the LED full on.

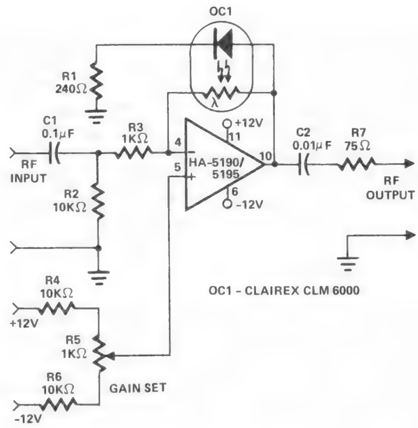


Figure 7–RF AGC Amplifier

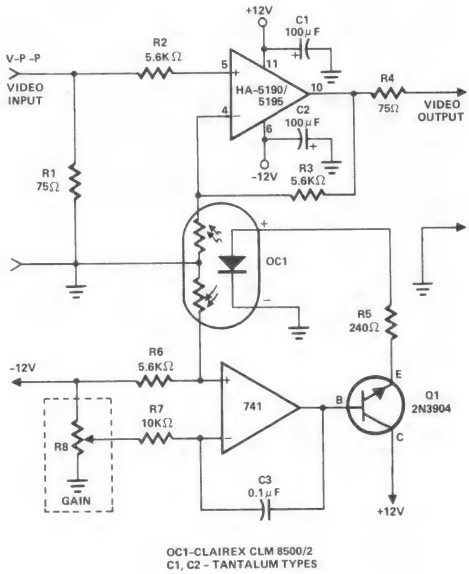


Figure 8—DC Gain Controlled Video Amplifier (Analog Multiplier)

DC GAIN CONTROLLED VIDEO AMPLIFIER

Suitable for use in virtually any application requiring a variable gain wideband or video amplifier, the circuit illustrated in Figure 8 employs a cascaded op amp integrator and transistor buffer (Q1) to drive the amplifier gain control element. Except for a simple modification, the HA-5190/5195 stage is connected as a conventional non-inverting operational amplifier, and includes input and output impedance matching resistors R1 and R4, respectively, series stabilization resistor R2, and power supply bypass capacitors C1 and C2. The circuit differs from standard designs in that the gain control network includes a photoresistor, part of OCI.

Referring to the schematic diagram, opto coupler/isolator OCI contains two matched photoresistors, both activated by a common LED. The effective resistances offered by these devices is inversely proportional to the light emitted by the LED. The greater the current through the LED, then, the more intense its light emission, and the lower the effective values of the photoresistors. One photoresistor is part (with R3) of the HA-5190/5195 gain network, while the other forms a voltage-divider with R6 to control the bias applied to the integrator non-inverting terminal.

In operation, the dc voltage supplied by GAIN control R8 is applied to the integrator inverting input terminal through input resistor R7. Depending on the relative magnitude of the control voltage, the integrator output will either charge or discharge C3. This change in output, amplified by Q1, controls the current supplied to the OCI LED through series limiting resistor R5. This action continues until the voltage applied to the integrator non-inverting input by the R6-photoresistor voltage divider matches the control voltage applied by R8 to the inverting input. At the same time, of course, the ratio of the R3-photoresistor gain network is changing, adjusting the op amp stage gain. As the control (R8) voltage is readjusted, the OCI photo-resistances track these changes, automatically readjusting the op amp gain in accordances with the new control voltage setting.

In experimental tests with typical devices, the amplifier gain could be varied from 12dB to 2dB as the dc control voltage was changed from 5.0 to 10.5Volts. Typical plots of stage gain (A_V) versus control voltage (V) are shown in Figure 9.

Since all temperature sensitive components are inside the integrator feedback loop, the circuit is quite stable with respect to changes in the ambient temperature.

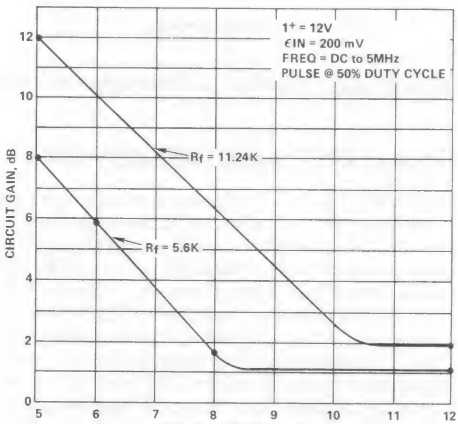


Figure 9 - Plot Of AGC Circuit Gain Versus Control Voltage

ACKNOWLEDGEMENTS

A. J. Carl Cooper of HARRIS CVS (Consolidated Video Systems), 1255 E. Arques Ave., Sunnyvale, CA. 94086, developed the basic circuits described herein and, in addition, devised and executed the initial evaluation and performance tests.

B. Richard Whitehead and Robert Junkins of HARRIS SEMICONDUCTOR, P.O. Box 883, Melbourne, Fla. 32901, carried out additional confirmation tests of circuit performance and made other significant contributions to this publication.

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1. HA-5190/5195 Wideband, Fast Settling Operational Amplifiers (Harris data brochure)

2. Application Note 525 - HA-5190/5195 Fast Settling Operational Amplifier. January 1988.

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4. EIA STANDARD RS5-250-B - Electrical Performance Standards for Television Relay Facilities.

ANALOG SWITCH APPLICATIONS IN A/D DATA CONVERSION SYSTEMS

By Richard Whitehead

Introduction

A choice of three approaches is available when implementing a data conversion system: 1). "build-from-scratch", 2) buy sub-systems and configure a system, or 3) purchase a pre-engineered system which meets the requirements. Also, as a matter of economics, the users of sensor-based data acquisition systems make it common practice to ensure a maximum number of elements are shared in the system. An invaluable tool used in this process is the analog switch or multiplexer. The purpose of this article is to focus attention on those parts of the system which require analog switches and to emphasize the importance of relative operating parameters.

Basic System Configurations

A/D data conversion systems can be categorized into two general groups: 1) low level signal conversion (analog signals below 1 volt) and 2) high level signal conversion (analog signals above 1 volt). Within these categories, four basic data conversion configurations are illustrated to point out the advantages of using analog switches.

Conditioning the analog signals prior to multiplexing (Figure 1A) is the most popular system arrangement and is both efficient and capable of high performance This configuration, which shares the level signals. Figure 1B represents a more austere approach resulting in lower cost and decreased performance. This type is useful in less demanding applications such as processing high level signals. To process multichannel, single event information such as wind tunnel or seismographic measurements the arrangement shown in Figure 1C is most likely to be used. This configuration represents a more expensive, less efficient approach due to the decreased number of shared elements. Figure 1D shows the elimination of the analog multiplexer and sample and hold circuits. By moving the multiplexing task to the digital domain, slower and lower cost A/D converters can be used.

Types Of Analog Switches

The most commonly used types of analog switches found in today's data conversion systems are: reed relay, JFET, and CMOS. Reed relays offer low ON and high OFF resistance and are capable of handling very high voltages, but have slow speeds. JFET switches have lower OFF leakage current and are capable of very high speeds. CMOS switches, which are the most popular and widely used in multiplexer applications, have low OFF leakage currents, good speed, and stable ON resistance under varying input signal conditions.

Selecting The Proper CMOS Analog Switch

The data conversion system error budget should be used to narrow the field of CMOS analog switches suitable for the application. Primarily, the speed of the switch must be consistent with the systems's sample rate requirements without introducing unacceptable transfer error. Significant dynamic errors inherent to CMOS analog switches are OFF channel leakage current and a settling time value dictated by the device's ON resistance and its inherent capacitance. Figure 2 shows the equivalent of a CMOS analog switch giving all of the inherent and distributed properties which may become the source of unwanted system errors.

Other system restrictions may further narrow the field of candidates suitable to performing the switching task. These restrictions could include, low power budget, hostile environment, cost, alternate sourcing, and package density. It's possible that all of

these restrictions could occur, and this situation mat influence the user to seek a compromise solution to his problem.

Fortunately, CMOS analog switches consume very little power and only the most demanding power budget would feel the strain of their power requirements. If the poerating environment of the device includes high voltage spikes, excessive noise pickup, and/or power supply interruptions, the selection should be narrowed to the internally protected analog multiplexers such as the HARRIS HI-506A/507A or the HI-546/547. These multiplexers come with guaranteed overvoltage specifications which engance the reliability of the data conversion system. They also insure output signal integrity while an overvoltage condition occurs on an unselected channel. It should also be ensured that the CMOS analog switch selected does not exhibit any inherent latch-up tendencies. The Harris dielectrically isolated CMOS analog switches offer latch free operation.

To some users the proper CMOS analog switch selection may become complicated leading to possible alternate solutions. An example of such a situation could be in high speed data conversion system where the settling time constraint placed on the multiplexer results in an unacceptable time penalty (Figure 3A). Figure 3B shows an alternate and practical solution to this problem. The two tiered multiplexing scheme may reduce the errors caused by leakage currents and settling time by an order of magnitude. Another practical solution would be to select an analog signal processor such as the HARRIS HY-9590/9591 shown in Figures 4A and 4B. These devices facilitate user application and reduce engineering time thereby reducing overall cost.

Other Uses For CMOS Analog Switches

Attention has been focused on the selection of CMOS analog multiplexers used to increase efficiency of data conversion systems through shared elements. But the versatile CMOS switch is not limited to only that function. Obviously they can be used in sample and hold circuits, with important parameters being switching speed, OFF leakage current, and charge transfer. Analog switches such as the HARRIS HI-200/201 and HI-300 series may be used in sample and hold circuits and also in auto-zeroing circuits for integrating type data converters (Figure 5).

Figure 6 shows the CMOS analog switch used to program the gain of an instrumentation amplifier.

Highlights

In A/D data conversion systems analog switches are mainly used as multi-channel multiplexers to increase system efficiency through shared elements.

CMOS analog switches are the most widely used in data conversion systems.

When selecting the proper CMOS analog switch, look for low OFF leakage current, good settling time, latch free operation, and stable ON resistance under varying analog signal input conditions.

If the environment is hostile, select from the internally protected CMOS analog multiplexers.

Where an alternate solution is required, attempt to ensure your solution is the most practical with respect to your error budget.

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Kaufman, Milton and Seidman, Arthur H. Handbook of Electronic Calculations. New York: McGraw-Hill Book Company, 1979.

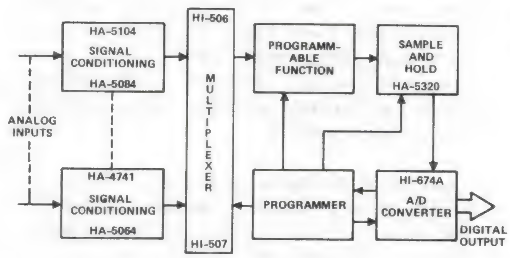


Figure 1A – Multiplexed. Signal Conditioning for Low Level Inputs

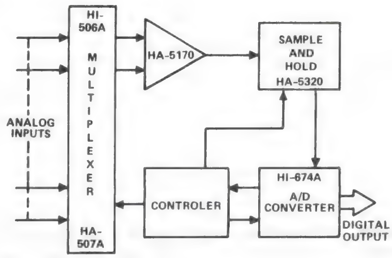


Figure 1B – Multiplexed, High Level Inputs

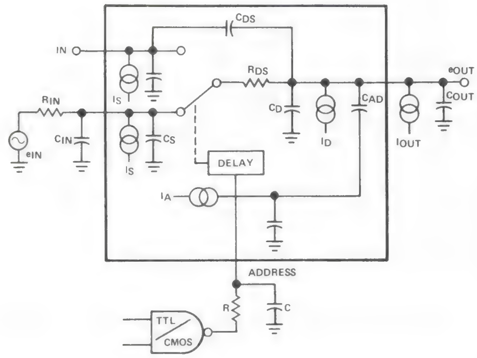


Figure 2 – Equivalent CMOS ANALOG SWITCH
DC Offset Error = $R_{DS} \times I_D$
Settling Time Determined by $R_{DS} \times C_D$

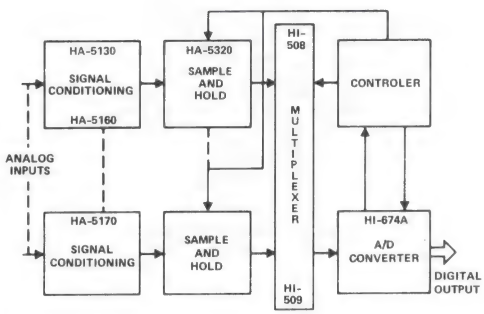


Figure 1C – Multiplexed, Sample / Hold Outputs

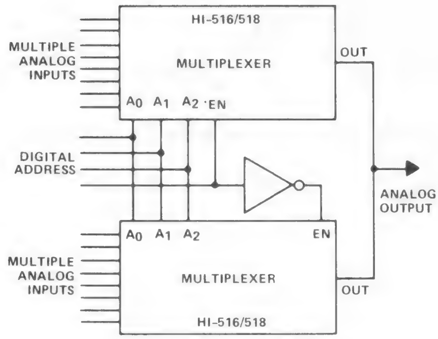


Figure 3A – Cascaded Multiplexers: Output Leakage Currents and Output Capacitance Increase Errors

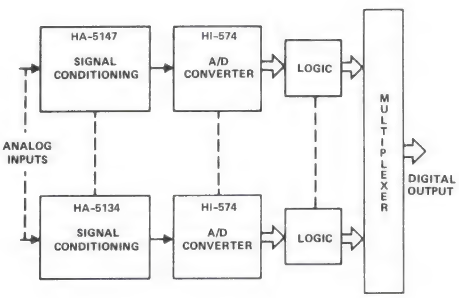


Figure 1D - Drgrtally Multiplexed A/D Outputs

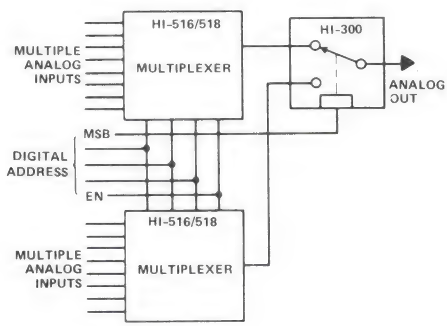


Figure 3B – Cascaded Multiplexers Two - Tiered Method: Errors Reduced Through Shared Switch

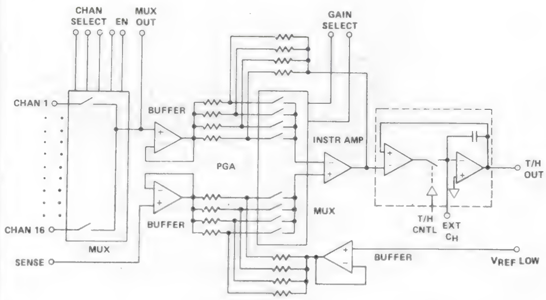


Figure 4B - Programmable DAQ Front-End (Single - Ended)

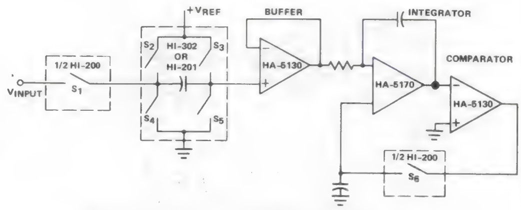


Figure 5. This autozero integrating converter uses six analog switches — S_1 through S_6. Zero correction occurs when S_3, S_4 and S_6 are "on". Integration occurs with S_1 closed. Integrate-reference takes place when S_2 or S_5 is "on".

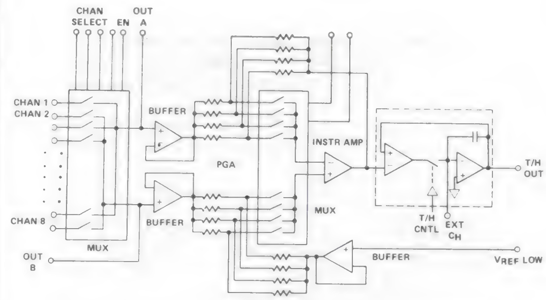


Figure 4A - Programmable DAQ Front-End (Differential)

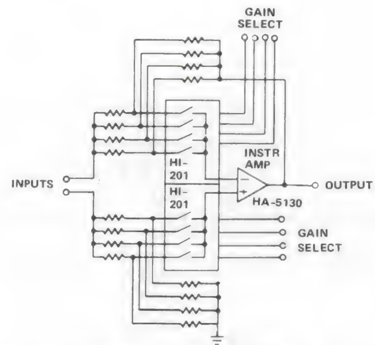


Figure 6 – Programmable Gain Instrumentation Amplifier

APP NOTE

FOR YOUR INFORMATION

No. 532

Harris Analog

COMMON QUESTIONS CONCERNING CMOS ANALOG SWITCHES

By Carl Wolfe

Introduction

The following information is a direct result of a significant amount of time spent in response to questions from users of HARRIS analog switches. Among the variety of questions are a few which seem to be asked more frequently than others. Over the next few pages, these questions are discussed with the hope that the answers will be helpful to the users and potential users of HARRIS analog switches. Some questions are technical in nature while others are simply questions on interpretation of the HARRIS Analog Data Book.

Power Supply Considerations

The first two questions are similar questions and the explanation will apply to both:

QUESTION #1: If the power supplies are off, will the switch be open? (Present a high impedance to the input signal)

QUESTION #2: If the power supplies are off, can an input signal be applied?

Both of these questions refer to an overvoltage condition when the supplies are off and an input signal is applied. A common misunderstanding is that the switch will be open and block the signal when actually the opposite occurs.

What is meant by the power supplies being off? Does it refer to the supplies being shorted to ground or does it imply they are open circuited?

If the power supplies go to ground, the input signal will pass through the switch and appear at the output. The explanation for this can be seen in Figure 1, which is a simplified CMOS switch cell. This switch cell consists of two enhancement type field effect transistors, one N-channel and one P-channel. An enhancement type of device is a FET which is normally off without some potential (gate voltage) to turn it on. A P-channel FET requires a negative potential (gate to source voltage) to turn it on and an N-channel FET requires a positive potential (gate to source). Contained in the physical structure of the FETS are parasitic transitors which are shown in Figure 1 as diodes from the source and drain to the body potentials of the devices. These diodes or parasitic junctions are normally reversed biased. If those junctions are forward biased, a fault condition exists where the signal is passed through the parasitic transitor. This is what occurs if the power supplies go to ground. Depending on the polarity of the input signal, either the N or P channel FET parasitics will be forward biased and the signal passed through the switch.

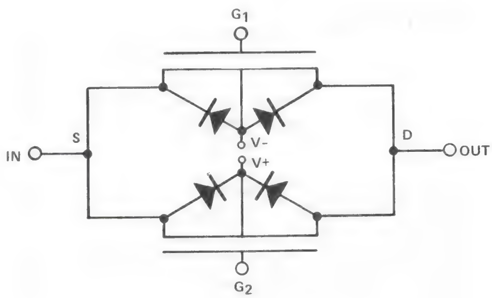


Figure 1. Basic CMOS Transmission Gate

Having the signal pass through the switch may be acceptable in some applications, but most likely it is not. An example would be user who was switching various voltages (transducers) as shown in Figure 2. If the supplies go to ground and these signals pass through the switch, the input voltage sources could easily be shorted.

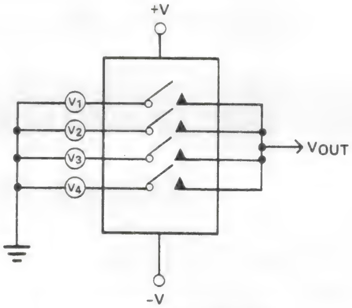


Figure 2. Switching Multiple Inputs

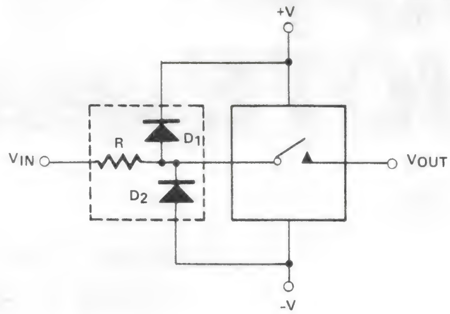


Figure 3. Protection for Each Analog Input

Another situation occurs if the power supplies are open circuited where the most positive and negative input signals will provide power to the switch. In this case, the signals being used for power will be passed to the output, but the remaining switches with inputs less than those used for supply will operate properly.

Input Overvoltage Protection

There is a possibilty the switch will be damaged if exposed to excessive current levels during an overvoltage condition. A second overvoltage condition is the case where the input signals exceed the existing power supply levels. Neither of these situations are recommended and the following questions are similar to those frequently asked.

QUESTION #3: Can an input greater than the supplies be applied?

QUESTION #4: In my application, there is a possibility that the switch will lose power and the input signal will still be applied. Is there a way to protect the switch if this situation occurs?

Referring to Figure 1 once again, if the input signal exceeds the supply by an amount greater than the breakdown voltage of the parasitic junction, the normally reversed biased junction will come forward biased. These forward biased junctions will pass the input signals to the output and possibly short out the input voltage sources.

The most common form of protection circuit for these types of overvoltage conditions is the resistor-diode network at the input of the switch as shown in Figure 3.

This circuit protects the device if the supplies go to ground or if the input exceeds the supply. If either of these situations occur the diodes will be forward biased and current path to ground will exist. This will protect the switch from excessive current levels. The primary purpose of the resistor is to limit the current through the diode.

Another advantage of using diode protection is that it prevents the input signal from passing to the output. This is a result of the input being clamped to the breakdown voltage of the protection diodes. If this breakdown voltage is less than the threshold voltage (turn on voltage) of the parasitic diodes, the parasitic transistor will remain reverse biased and the signal will not pass through the switch.

There are some disadvantages to the user with this type of protection. One would be the economics involved with using external protection for each analog input. This could present a cost problem if a large number of channels were involved. Another concern would be the current limiting resistors which adds to the on resistance of the switch contributing to the overall system error. A further possible source of error is current leakage in the diodes. It is recommended that low leakage diodes, such as schottkey diodes be used.

The protection circuit just discussed is not used to protect the switch from latch up. The HARRIS switches are constructed using the dielectric isolation process and the four layer SCR found in JI technology does not exist. This circuit is intended to protect the device from high current levels which result from the forward biasing of the parasitic transistors which are inherent in all FET structures.

If for some reason the resistor-diode protection circuit cannot be used there are other possibilities. The following method may help to avoid the extra cost of protecting each input. In this method, since the supplies are open circuited, the most positive and most negative signal will power-up the chip and any input with signals less than those being used for power will operate properly. However, this method can only be used if the outputs are not common and a user can afford to have at least two signals pass to the output.

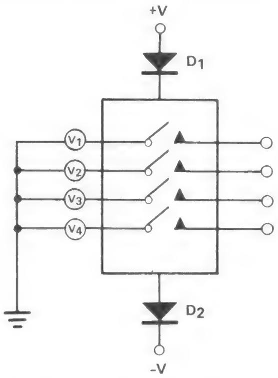


Figure 4. Powering the Switch With the Input Signals

Another alternative does not involve protection circuitry, but instead takes advantage of CMOS technology. An example would be a user who has ±15V supplies and needs to switch a +18V signal as shown in Figure 5. This appears to be an overvoltage condition since the input exceeds the supply. But rather than protect the device, the user can shift the supplies to +20V, -10V. Now the input signal is within the supply level and the switch should work properly. In certain applications the supply voltages can be adjusted in order to pass a larger range of input signals.

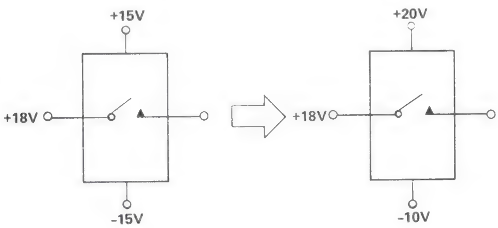


Figure 5. Varying the Supplies to Meet the V_{IN} < V Supply Requirements

Single Supply Operation

Single supply operation is a topic which is discussed frequently and the following are examples of typical questions.

QUESTION #5: Can the switch be operated at a single power supply?

QUESTION #6: What is the minimum power supply possible?

Usually engineers with critical power requirements request single supply operation. An example would be battery operated applications such as portable equipment. In these cases the designer is limited to single supply, low supply or both.

Trade-offs exist with single supply operation that should be pointed out to the user. An example is the HI-300 series of switches which has the capability of operating with a single +5 volt supply. The performance of the switch will vary, however, as the supply voltage varies. So, for the HI-300 series, as supply voltage decreases, the on resistance and the switching times increase. A 300 series switch with a single +5 volt supply will have higher on resistance and slower switching speeds than the same device at ±15 volts or even a single +15 volt supply. This represents a change in both DC and AC performance. Even though the switch may now meet the users power requirements at single supply, the question is whether it will still meet the performance requirements.

The explanation for these variations can be found in the FET devices composing the switch cell itself. The variation in on resistance is due to the fact that the channel impedance of FET is dependent on the gate - source bias. Since the gate voltage is determined by the supply voltage, it can be concluded that the on resistance is a function of the supply voltage.

The fact that the on resistance varies with supply voltage directly relates to the slower switching times, since the higher on resistance will reduce the available current needed to charge the internal capacitance of the switch. Lower changing current relates directly to slower switching times.

Questions About Harris Switches

Many of the questions asked about switches could apply to any CMOS switch manufacturer's products. But some questions are unique to both the Harris product line and data catalog. The following are examples of some of the more common questions concerning the Harris Analog Data Catalog.

QUESTION #7: What is the difference between the VL and VR pins on the HI-5043 and V_{REF} pins on the HI-201 ?

The device pins mentioned above have their own individual functions even though they are all associated wth the logic reference circuits of their respective designs. For the HI-201, the V_{REF} pin is the terminal which establishes the logic threshold levels for which the switch will change state. Although it is normally left open when driving from +5V logic (DTL or TTL), it can be connected to a higher supply in order to raise the switching threshold levels when driving from CMOS Logic greater than 5 volts. The V_{REF} pin enables the user to change from TTL to CMOS Logic.

The reference circuit of the HI-50XX series of switches is different from the HI-201, which accounts for the V_R and V_L pins. Even though the V_R terminal is brought out on the package, it is recommended that this pin be grounded. This terminal establishes the ground for the internal ref-

erence circuit. The V_L pin performs a similar function to the V_{REF} pin on the HI-201. It is normally connected to 5 volts for TTL logic but can be tied to a higher supply for CMOS levels. This effectively raises the switching thresholds to accomodate the higher CMOS level.

The next question is easily the most frequently asked question about HARRIS HI-50XX series of switches.

QUESTION #8: Are the switch functions shown on the data sheet a result of the logic address being HIGH or LOW ?

Actually, the answer to the question is printed at the top of the data sheet page,depicting switch functions "switch states are for a logic 1 input". Therefore, the address is in the HIGH state for the switch functions shown on that page.

Some other areas which are often questioned on the data sheets are the maximum ratings and performance between channels of the switches. The following questions are typical:

QUESTION #9: Will the switch operate at the absolute maximum ratings?

The topic of absolute maximum ratings does create some confusion. Basically, the contents of the Electrical characteristic table are the guaranteed parameters. The switch may operate with conditions other than those recommended, but are not guaranteed parameters. Anything above absolute maximum ratings may permanently damage the device.

Problems sometime arise when a customer tests some parts at conditions other than those which are guaranteed. If the parts work, the user may go ahead and design around these conditions. But there is a good possibility the next batch of switches may not perform in the same manner. The user must be aware that anything outside the guaranteed limits is a user's risk and susceptable to variations in manufacturing.

QUESTION #10: What is the variation in "on" resistance between channels on the switch?

There are two causes for these variation. One cause is process variation which is due to variables in manufacturing. This can create variation between channels on the same unit. The second reason is lot variation which can cause differences in performance from unit to unit. After all variations are taken into account, a good "rule of thumb" is ±10% tolerance on typical parameter values. So if a device has a typical on resistance of 50Ω , a user could expect a $\pm 5\Omega$ variation.

APP NOTE
FOR YOUR INFORMATION
No. 534
Harris Analog

ADDITIONAL INFORMATION ON THE HI-300 SERIES SWITCH

By Carl Wolfe

Introduction

The introduction of the HI-300 series of CMOS analog switches is the latest addition to the HARRIS switch family and gives the designer a viable second source to the Siliconix DG 300 series analog switch.

This family of monolithic, dielectrically isolated, CMOS analog switches consists of twelve products, the HI-300 thru HI-307 and the HI-381 thru HI-390 are designed for TTL level compatibility (logic "0" = .8V, logic "1" = 4.0V). The HI-304 thru HI-307 are CMOS compatible (logic "0" = 3.5V, logic "1" =11V).

The HI-300 series features low and nearly constant on resistance over analog signal range, low leakage and minimal power dissipation.

Improved Performance

An understanding of what a designer would consider important in an analog switch is useful in order to illustrate the advantage of the HI-300 series. Although any parameter could be considered important for a particular application, there are certain parameters considered to be most critical for the majority of applications. These parameters are:

- "on" Resistance (Ron)
- leakage current (I_{SOFF}, I_{DOFF}, I_{DON})
- switching speed (ton, toff)
- power supply current (I+, I-)

These parameters are important because the majority of designs require either high accuracy, speed, or low power dissipation.

ON RESISTANCE

In high accuracy systems, such as data acquisition systems, the designer would be concerned with minimizing errors caused by "on" resistance and leakage currents. An inverting programmable gain amplifier shown in Figure 1 will help illustrate the need for low on resistance and leakage current in high accuracy systems.

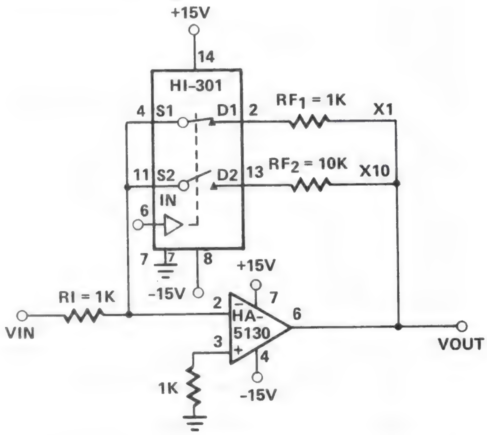


Figure 1 — Inverting Programmable Gain Amplifier

Ideally, the voltage gain of this inverting amplifier would be, $A_V = -(R_F/R_I)$. But when using a switch to program the gain, its characteristics must be taken into account and the amplifier gain equation must be modified to $A_V = -(R_F + R_{ON}/R_I)$. The higher the on resistance of the switch, the greater the gain error. Variations in the on resistance of the switch will also effect the gain error.

LEAKAGE CURRENT

Another source of error occurs in the switch "off" state, where leakage current causes offset voltage errors. In Figure 1 , leakage current flowing through the feedback resistor creates an output voltage error equivalent to the expression, $V_o = R_F \times I_{DOFF}$.

SWITCHING SPEED

A designer concerned with switching times would

obviously be sensitive to the ton and toff specifications. A low value of "on" resistance is also important, since this resistance increases the RC time constants and can slow the circuits overall performance.

POWER SUPPLY REQUIREMENTS

The last critical parameter would be power consumption. There are certain applications where power supply currents are the primary concern of the designer. Examples would be portable or battery operated equipment.

The majority of switch applications require critical performance in one or more of the areas just discussed. The HI-300 series offers improved performance in each of these areas. The following tables compare the HI-300 series with existing HARRIS switches. Table 1 contains maximum specifications for T = 125°C and Table 2 consists of typical values at T = 25°C.

+125°C Maximum Specifications

SWITCH TYPE	RON	I LEAKAGE	I SUPPLY	tON	tOFF
HI-200	125Ω	500nA	2mA	500ns	500ns
HI-5040	75Ω	500nA	.3mA	1.000ns	500ns
HI-300	75Ω	100nA	.1mA	300ns	250ns

Table 1 — Switch Comparisons at T=125°C

+25°C Typical Specifications

SWITCH TYPE	RON	I LEAKAGE	I SUPPLY	tON	tOFF
HI-200	55Ω	1nA	.5mA	240ns	330ns
HI-5040	25Ω	.8nA	.3mA	370ns	280ns
HI-300	30Ω	.1nA	.23μA	210ns	160ns

Table 2 — Switch Comparisons at T=25°C

From these tables it should be clear that the HI-300 series offers improved performance to the designer.

Inside The HI-300

Figure 2 shows the schematic of the digital input and driver stages of the HI-300. The purpose of this stage is to take the logic level signals and condition them to drive the gates of the FET switch cells.

The HI-300 series has a digital input protection circuit consisting of a 200Ω series resistor and clamping diodes, D1 and D2, to the supplies.

These diodes will quickly discharge any static charge which might appear at the digital inputs.

The F. E. T. Devices N1 thru N5 and P1 thru P5 form the input buffer and level shifter which establishes the proper voltages to drive the switch cell. N6, N7, P6, and P7 form the output buffers which isolate the level shifter from the capacitive load of the switch cell.

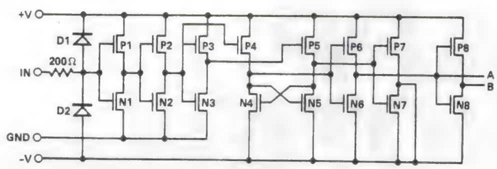


Figure 2 — Partial Schematic

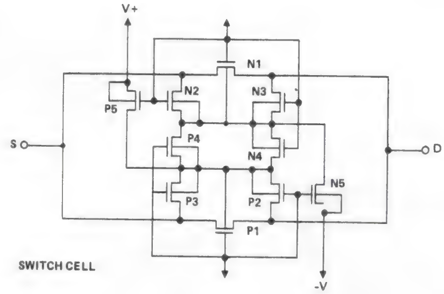


Figure 3 — Schematic

The switch cell shown in Figure 3 is based on the FET devices N1 and P1. The remaining devices, N2 thru P5 serve various functions, such as reducing leakage current, minimizing on resistance variations and minimizing charge injection.

Additional Performance Characteristics

(A) SINGLE SUPPLY OPERATION

The HI-300 series has the capability of single supply operation. These switches can operate to a minimum supply of +5 volts, although designers must be aware of the trade off which exists at these levels. The trade off is the performance of the switch will vary as the supply level varies. Examples of these performance variations are increased on resistance and slower switching times. So, a HI-300 series switch with a single five volt supply will have higher on resistance and slower switching speeds then the same device at ±15 volts or even a single +15 volt supply.

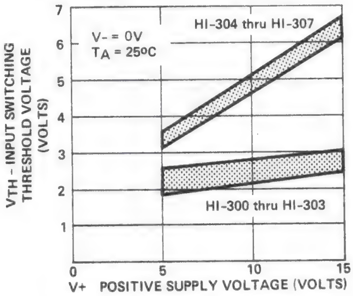
The explanation for these variations can be found in the F.E.T. devices composing the switch cell itself. The variation in on resistance is due to the fact that the channel impedance of the FET is dependent on the gate-source bias. Since the gate voltage is determined by the supply voltage, it can be concluded that the on resistance is a function of the supply voltage.

The fact that the on resistance varies with supply voltage directly relates to the slower switching times. The higher resistance reduces the available current

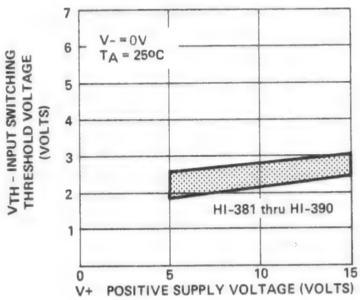
needed to charge the internal capacitances of the switch. Lower charging current directly relates to the slower switching times.

The explanations, just given, along with the following typical curves of the HI-300 single supply operation, should aid the designer in applying the HI-300 series in single supply applications.

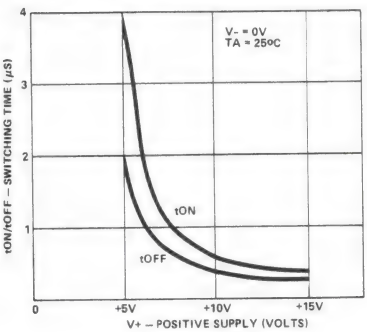
INPUT SWITCHING THRESHOLD VS. POSITIVE SUPPLY VOLTAGE HI-300 THRU HI-307



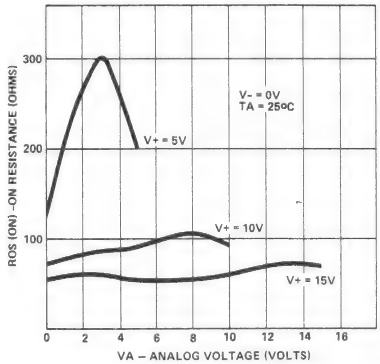
INPUT SWITCHING THRESHOLD VS. POSITIVE SUPPLY VOLTAGE HI-381 THRU HI-390



SWITCHING TIME VS. V+ - POSITIVE SUPPLY VOLTAGE



RDS(ON) VS. ANALOG AND POSITIVE SUPPLY VOLTAGE WITH V- = 0V



B) CHARGE INJECTION

The charge injection of a switch is a critical parameter for certain applications, such as small signal switching or sample and hold circuits.

For the case of small signal switching, unwanted switching spikes result from this transferred charge causing system errors. These spikes are created when the transitions of the gate voltage are capacitively coupled to the output through the gate to source and gate to drain capacitances, as shown in Figure 4. The magnitude of these switching spikes will depend on the values of the load and source impedances, the value of the gate voltage and the size of the internal capacitances of the switch.

For the sample and hold circuit, shown in Figure 5, a common problem is sample to hold offset error. It is caused by the same mechanisms discussed for the small signal application, but in this case the charge is transferred to the hold capacitor and an offset voltage is created. The voltage is determined by the following relationship. $V = Q/C_H$.

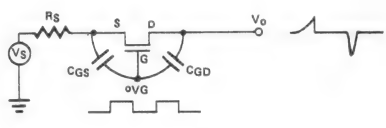


Figure 4 – Charge Transfer

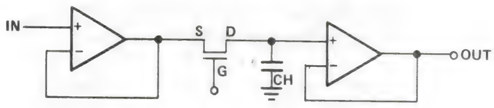


Figure 5 — Sample and Hold

Charge injection can create problems in the type of applications just described. A typical curve of the HI-300 series charge injection performance is shown in Figure 6 as an aid to designing in these type of circuits.

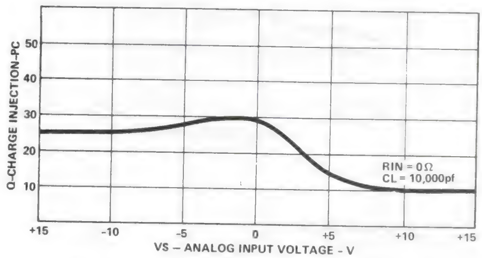


Figure 6 — Charge Injection vs. Input Voltage

Application Hints

A. POWER SUPPLY CONSIDERATIONS

The HI-300 series analog inputs do not feature overvoltage protection. External protection circuitry would be necessary if the switches were subjected to possibly destructive situations.

An example could be an overvoltage condition where the power supplies to the switch go down while an analog input signal is still present. A common misunderstanding is that the switch will be open and block the input signal, when actually the opposite occurs.

If the power supplies go to ground, the input signal will pass through the switch and appear at the output. The explanation for this can be seen in Figure 7, which is a simplified CMOS switch cell. This switch cell consists of two enhancement type field effect transistors, one N-channel and one P-channel. An enhancement type of device is a FET which is normally off without some potential (gate voltage) to turn it on. A P-channel FET requires a negative potential (gate to source voltage) to turn it on an N-channel FET requires a positive potential (gate to source). Contained in the physical structure of the FETS are parasitic transistors which are shown in Figure 7 as diodes from the source and drain to the body potentials of the devices. These diodes or parasitic junctions are normally reversed biased. If those junctions are forward biased, a fault condition exists where the signal is passed through the parasitic transistor. This is what occurs if the power supplies go to ground. Depending on the polarity of the input signal, either the N or P channel FET parasitics will be forward biased and the signal passed through the switch.

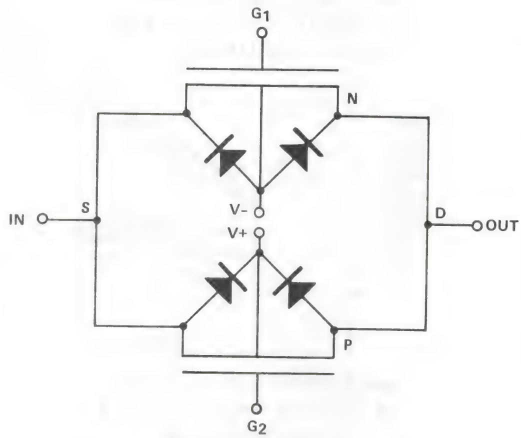


Figure 7 — Basic CMOS Transmission Gate

Another situation occurs if the power supplies are open circuited, the most positive and negative input signals will provide power to the switch. In this case, the signals being used for power will be passed to the output, but the remaining switches with input signals less than those used for supply will operate properly.

A second overvoltage condition is the case where the input signals exceed the existing power supply levels. Referring to Figure 7, if the input signal exceeds the supply by an amount greater than the breakdown voltage of the parasitic junction, the normally reversed biased junction will become forward biased. These forward biased junctions will pass the input signals to the output and possibly short out the input voltage sources.

The most common form of protection circuit for these types of overvoltage conditions is the resistor-diode network at the input of the switch as shown in Figure 8. This circuit protects the device if the supplies go to ground or if the input exceeds the supply. If either of these situations occur, the diodes will be forward biased and a current path to ground will exist. This protects the switch from excessive current levels. The primary purpose of the resistor is to limit the current through the diodes.

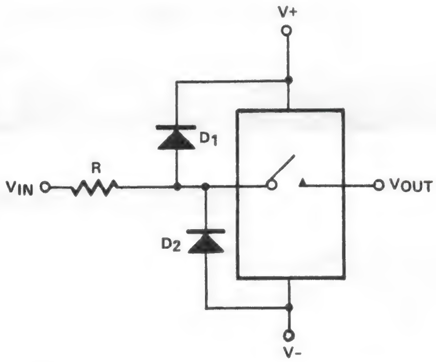


Figure 8 — Protection for Each Analog Input

Another advantage of using diode protection is that it prevents the signal from passing to the output. This is a result of the input being clamped to the breakdown voltage of the protection diodes. If this breakdown voltage is less than the threshold voltage (turn on voltage) of the parasitic diodes, the parasitic transistor will remain reversed biased and the signal will not pass through the switch.

The protection network may introduce unwanted error into the circuit in the form of leakage current and increased on resistance. It is recommended that low leakage diodes be used, such as Schottkey diodes. If the switch is looking into a high impedance, such as the input operational amplifier, the error introduces by the increased on resistance will be negligible.

The protection circuit just discussed is not used to prevent the switch from latch up. The HI-300 series switch is constructed using the HARRIS dielectric isolation process and the four layer SCR found in JI technology does not exist. This circuit is intended to protect the device from high current levels which result from the forward biasing of the parasitic transistors which are inherent in all FETS.

An alternative to protection circuits takes advantage of CMOS technology. Assume an overvoltage condition exists where the input exceeds supply. Rather than use external components to protect the device, it may be possible to shift the supplies in order to accomodate the input signal. An example would be an application with ±15 volt supplies, but attempting to switch a +18 volt input signal. A possible solution would be to shift the supplies to V+ = +20V and V− = -10V and now the input signal is within the existing supplies. In some applications the supply voltage can be adjusted in order to pass larger input signals.

Acknowledgement

A. Engineering staff of Harris Semiconductor, P.O. Box 883, Melbourne, FL 32901, particularly Frank Cooper, whose useful comments contributed to this publication.

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APP NOTE

FOR YOUR INFORMATION

No. 535

Harris Analog

DESIGN CONSIDERATIONS FOR A DATA ACQUISITION SYSTEM (DAS)

By Tarlton Fleming

Introduction

This is a collection of guidelines for the design of a data acquisition system. Its purpose is to supplement the more methodical block-by-block discussions available in numerous other papers and application notes. Emphasis in this note is on the less easily quantifiable happenings "between the blocks", rather than a description of the block components and their error contributions. This latter information may be found in the Bibilography under "General".

A data acquisition system is defined to include all the components needed to generate the electrical analogs of various physical variables, transmit these signals to a central location and digitize the information for entry into a digital computer. Among these components are transducers, amplifiers, filters, multiplexers, sample/holds and analog-to-digital converters. The system also includes all signal paths tying these functions together.

Several system architectures will be considered, followed by a general discussion aimed at the designer who must choose hardware for a given application. Topics include:

- Data Acquisition System Architecture
- Signal Conditioning
- Transducers
- Single-Ended vs. Differential Signal Paths
- Low-Level Signals
- Filters
- Programmable Gain Amplifier
- Sampling Rate
- Computer Interface

Data Acquisition System Architecture

At present the most widely used DAS configuration is that shown in Fig. 1. It handles a moderate number of analog channels, feeding into a common multiplexer, programmable gain amplifier (if required), track/hold amplifier and A-D converter.

A more specialized and expensive variation is to place a Track/Hold in each channel as shown in Fig. 2. Switching all channels to HOLD simultaneously produces a "snapshot" view which preserves the phase relation of signals in all channels. This information is important in seismic studies and vibration analyses.

The DAS system of Fig. 3 offers many advantages, but is not yet practical except for slowly changing channel data. Low frequency signals allow dedication of a slow but accurate integrating type A-D converter for each channel. The channel filters often included to reduce aliasing errors and noise are not necessary, since aliasing is not a problem with low bandwidth signals. The integrating converter suppresses wideband noise by averaging it about the instantaneous signal level. Also, the converter's integration period may be chosen to provide almost complete rejection of a specific interference frequency such as 60 Hz. Digital outputs from the converters are then digitally multiplexed.

The system shown in Fig. 3 has an inherent advantage over the other two systems, having eliminated both the track/hold and the analog multiplexer with their many error contributions. The disadvantage, of course, is cost. Fig. 3 would become the system of choice in many more applications, if a significant reduction should occur in the price of successive - approximation A-D converters.

A small RAM may be added at the converter's output in any of these systems, to buffer the computer and offload its involvement with individual conversions. Timing and control may be arranged to scan all channels repeatedly, and continuously update a RAM location for each channel. The computer is then free to look at a recent reading for any channel, at any time.

Further discussion will center on Fig. 1, both in the single-ended version shown, and in the differential version.

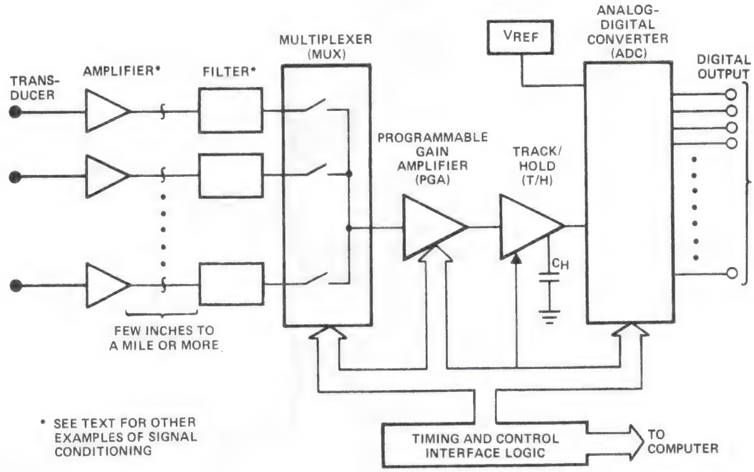

FIGURE 1. Typical Data Acquisition System

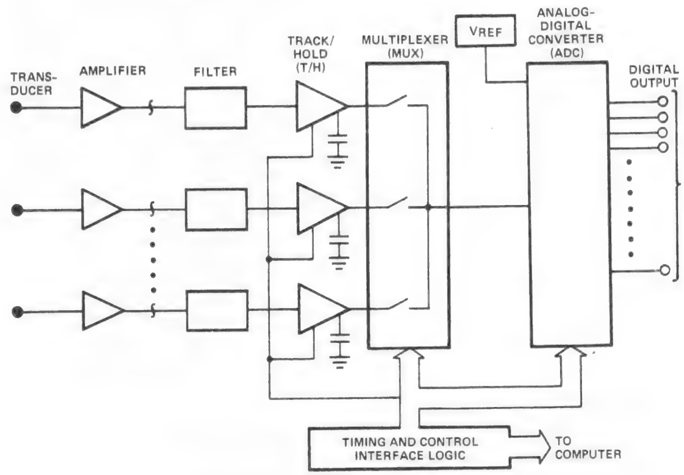

FIGURE 2. DAS System For Simultaneous Sampling Of All Channels

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APPLICATION NOTES

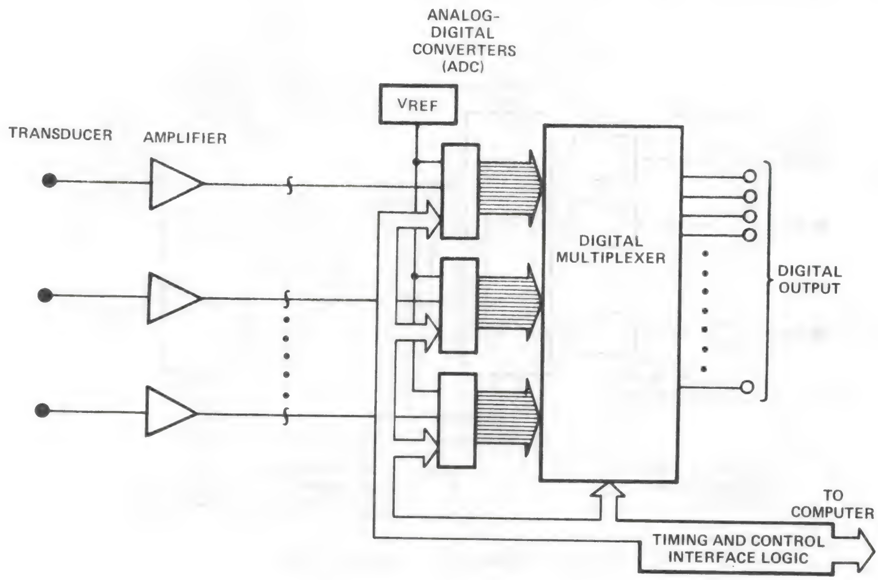


FIGURE 3. High Accuracy, Multi-Converter DAS System

Signal Conditioning

Signal conditioning refers to all the operations performed on a transducer signal up to (and including) digitization by the A-D converter. Standard among these operations are multiplexing, programmable gain, and Track/Hold. Others may be added as required:

- Transducer excitation
- Amplification
- Filtering
- Calibration
- Linearization
- Voltage to current conversion (4 to 20 mA; 10 to 50 mA)
- rms to dc conversion
- Logarithmic signal compression
- Common mode rejection

For highest signal-to-noise ratio all signal conditioning should be performed near the transducer, with the exception of common mode rejection and filtering. Filters should be located near the multiplexer input. Besides minimizing alias errors originating in the high end of the transducer's output spectrum, filters suppress wideband noise picked up on signal lines to the transducer.

Transducers

The first item in the signal path of a DAS is the transducer. This device usually transforms energy from one form to another, producing an electrical analog of the physical variables to be monitored or measured. Transducers are based on a variety of physical principles but most produce a voltage as output. Some yield an intermediate variable such as resistance or capacitance, which is transformed to voltage by an applied electrical excitation (carrier frequency, dc voltage, current source).

Often, several types of transducers are available to sense a given quantity. When selecting a voltage output transducer, remember that a low source resistance is desirable, both to minimize noise and to reduce loading by the next "block" in the signal path. Provision on the transducer for a convenient method of signal calibration will be welcome, once a system is in operation. Also, a center tap on the transducer allows better interface to a balanced line if low level signals are to be transmitted.

Several questions arise at this point:

- Should the signal path be single-ended or differential?
- Should the signal be transmitted at low level (100 mV) or high level?
- What type of conductor should be used for signal transmission?

Answers to these and other questions are covered in the following Sections.

Signal-Ended vs. Differential Signal Paths

Consider the transducer output. A high level signal (100 mV to 10 V) is easier to handle than low level. Is a common mode signal present? If not, is it likely to be acquired as "pickup" during transmission? This is likely if the cable is routed near fluorescent lights, motors or other electrical machinery. If common mode voltage is not expected, then an economical single-ended connection is possible, with a single wire per channel and a common return. (see Fig. 4). High level signals, short distance and controlled conditions will ensure good performance with this arrangement.

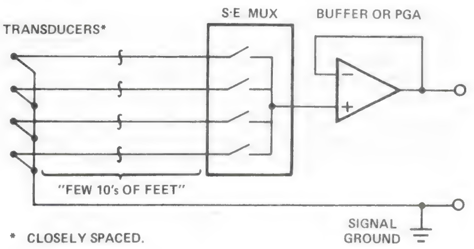


FIGURE 4. Single-ended Data Paths

Low level signals require special treatment. Whether high or low level, the presence of common mode voltage calls for a differential signal path. The most widely used solution is an unshielded, twisted pair of wires, good for 1000 feet or so with a bandwidth of 100 KHz. As a minimum then, two wires per channel feed into a differential amplifier or multiplexer, buffered by a full or pseudo-differential amplifier to reject the unwanted common mode voltage (see Fig. 5).

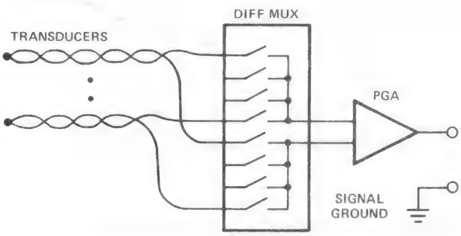


FIGURE 5. Differential Data Paths

For the case in which the transducer output is a low level voltage, the choice is whether to transmit it as is, or to boost the level by adding an amplifier. The amplifier will provide low source impedance as well as gain; two valuable forms of signal conditioning. However, providing power to a remote amplifier can be difficult. Even if a supply is available at the remote site, the voltage between two widely separated commons presents a problem. If the sum of signal plus common mode voltage does not exceed the input range of either the multiplexer or buffer amplifier, Fig. 5 can be used.

A more expensive approach is required for higher common mode voltages. One reliable technique is the "flying capacitor" multiplexer of Fig. 6, using reed relay switches. This works well for thermocouples bonded to machinery and riding on hundreds of volts relative to DAS ground, but in some applications the reed relay's 1 ms response time can be a limitation.

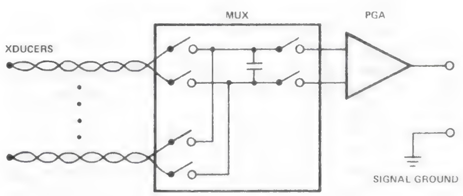


FIGURE 6. "Flying Capacitor" multiplexer using reed relay switches for high CMV signals.

Isolation amplifiers can handle higher voltages and higher bandwidths than the system of Fig. 6. For example, magnetically isolated amplifiers are rated at 2KV and up with a small signal bandwidth of approximately 2 KHz. One of these per channel is expensive, but in addition to common mode rejection it can solve the problem of supplying power at the remote transducer. Isolation amplifier models are available which include $\pm 15V$ terminals, referenced to the floating front-end of the amplifier. This power can provide transducer excitation and supply an amplifier or other signal conditioning circuitry.

For higher bandwidth data, optically isolated isolation amplifiers are available with $f_{-3dB} = 15KHz$ and 2KV isolation. These amplifiers do not provide the external supply terminals to power transducer circuitry.

Low Level Signals

The main concern with signals below 100mV is that noise, offset voltage, and other aberrations can represent a large percentage error. A shielded, differential signal path is essential for transmitting these signals, especially to maintain a noise level below 50μV rms.

Most transducer outputs are low level and low bandwidth as well. Since shielding precautions to be described are intended to produce an acceptable signal to noise ratio, filters may not be necessary. Otherwise, active filters with their relatively large dc errors should not be used for low level signals. Passive filters on the other hand, are restricted to two or three poles as a practical limit, which in turn restricts the allowable signal bandwidth for a given accuracy (see the Section titled Filters).

The transmission cable carrying the transducer signal is critical in a low level system. It should be as short as practical and rigidly supported. Signal conductors should be tightly twisted for minimum enclosed area, to guard against pickup of electromagnetic interference, and the twisted pair should be shielded against capacitively coupled (electrostatic) interference. A braided wire shield may be satisfactory, but a lapped foil shield is better since it allows only one tenth as much leakage capacitance to ground per foot.

A key requirement for the transmission cable is that it present a balanced line to sources of noise interference. This means an equal series impedance in each conductor plus an equally distributed impedance from each conductor to ground. The result should be signals equal in magnitude but opposite in phase at any transverse plane. Noise will be coupled in-phase to both conductors and rejected as common mode voltage. Again, any such noise will be directly proportional to the source impedance driving the line. An isolation or instrumentation amplifier may be used to terminate the line, providing high input impedance, common-mode rejection, conversion from a differential to single-ended signal path, and a buffer for the ON resistance of the following multiplexer.

Coaxial cable is not suitable for low-level signals because the two conductors (center and shield) are unbalanced. Also, ground loops are produced if the shield is grounded at both ends by standard BNC connectors. If coax must be used, carry the signal on the center conductors of two equal-length cables whose shields are terminated only at the transducer end. As a general rule, terminate (ground) the shield at one end only, preferably at the end with greatest noise interference. This is usually the transducer end for both high and low level signals.

Printed circuit traces and short lengths of wire can add substantial error to a signal even after it has traveled hundreds of feet and arrived on a circuit board. Here, the small voltage drops due to current flow through connections of a few milliohms must be considered, especially to meet an accuracy requirement of 12-bits or more.

The table of Fig. 7 is a useful collection of data for calculating the effect of these short connections. (Proximity to a ground plane will lower the values for inductance.)

WIRE GAGE	EQUIVALENT WIDTH OF P.C. CONDUCTOR (2 OZ. Cu.)	DC RESISTANCE PER FOOT	INDUCTANCE PER FOOT	IMPEDANCE PER FOOT	
				AT 60Hz	AT 10KHz
18	0.47"	0.0064Ω	0.36μH	0.0064Ω	0.0235Ω
20	0.30"	0.0102Ω	0.37μH	0.0102Ω	0.0254Ω
22	0.19"	0.0161Ω	0.38μH	0.0161Ω	0.0288Ω
24	0.12"	0.0257Ω	0.40μH	0.0257Ω	0.0345Ω
26	0.075"	0.041Ω	0.42μH	0.041Ω	0.0488Ω
28	0.047"	0.066Ω	0.45μH	0.066Ω	0.0718Ω
30	0.029"	0.105Ω	0.49μH	0.105Ω	0.110Ω
32	0.018"	0.168Ω	0.53μH	0.168Ω	0.171Ω

FIGURE 7. Impedance of Electrical Connections, +20° C

As an example, suppose the ADC in Fig. 1 has 12-bit resolution, and the system accuracy is to be ± ½ LSB (± 1.2mV). The interface logic might draw 100 mA from the + 5V supply. Flowing through six inches of #24 wire, this current produces a drop of 1.28mV; more than the entire error budget. Obviously, this digital current must not be routed through any portion of the analog ground return network.

Filters

The presampling or anti-aliasing filters shown in Fig. 1 are normally required with high-level signals of significant bandwidth, especially if the signal is to be reconstructed by a digital-to-analog converter after processing. If low level signals require a passive filter, the differential configuration of Fig. 8 preserves some degree of impedance balance on the line.

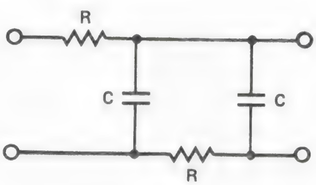
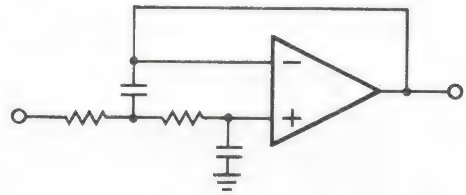


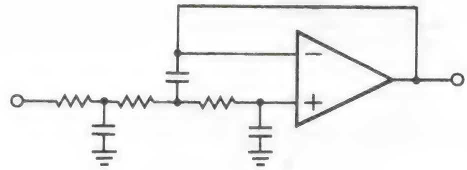
FIGURE 8. A Passive, Two Pole, Low Pass, Differential Input Filter

A low-pass Butterworth response is best for the channel bandlimiting filter in most data acquisition systems. The Butterworth filter output decreases monotonically with frequency, though this attenuation is very slight within the passband. Other filter types produce ripple in the passband, whose amplitude degrades accuracy unless expensive, high tolerance components are used.

Butterworth is not the most linear phase response, and if signal group delay is critical an elliptic (Bessel) filter should be chosen. Again, however, Butterworth fits most applications. A given number of poles may be had by cascading the two and three pole sections shown in Fig. 9. Either reference under "Filters" in the Bibliography gives a systematic procedure for calculating R and C values in terms of a given cutoff frequency. See the Section on "Sampling Rate" for the poles vs. accuracy requirement.



a. TWO POLE SECTION



b. THREE POLE SECTION

FIGURE 9. Butterworth Low-Pass Filters

Programmable Gain Amplifier (PGA)

Unless the ratio of highest to lowest signals anticipated on any channel is ≤ 2, some form of programmable gain amplification is desirable between the multiplexer and A-D converter. Without this variable gain block, the MSB's are idled one after another as input level decreases. Although the resolution of an n-bit converter remains a constant $FS/2^n$ by definition, resolution referred to the input level is decreasing (FS = Full Scale).

Considering resolution as referred to the input level, a 12-bit converter digitizes an input of .06FS to only 8 bits. The full 12-bit resolution applies only for $V_{IN} \geq FS/2$. Therefore to fully utilize the converter, gain should be added as necessary before each conversion, to meet the condition $FS/2 \leq V_{IN} \leq FS$. Then the amount of gain introduced by the PGA is noted by the computer to keep track of the actual input value.

Three other services are performed by the PGA:

1. Buffering: Prevents a loading effect due to the multiplexer's ON resistance.

2. Differential to Single-Ended Conversion: Necessary for the majority of Track (or Sample) /Holds and A-D converters.

3. Common Mode Rejection (CMR). When connected to the output of a differential multiplexer, the PGA's differential input rejects the common mode voltage accumulated by a signal transmission cable. Fig. 10 shows a subtractor or "pseudo-differential" PGA suitable for wideband signals with low common mode content. In this circuit, CMR is limited by precision of the "K" ratio and variations in the channel source impedance.

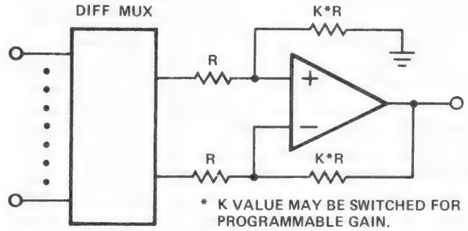


FIGURE 10. Subtractor or Pseudo-Differential PGA

Fig. 11 is the full differential PGA, necessary for low-level, high common mode signals. This version offers the highest gain accuracy and for high gain, the best CMR.

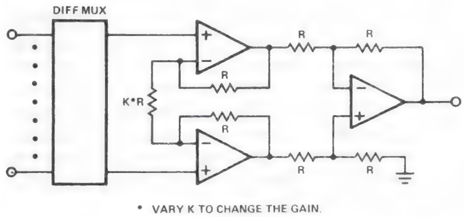


FIGURE 11. Full Differential PGA

The PGA normally precedes the Track/Hold, since the PGA would amplify any error introduced by that device. This order must be reversed to implement an auto-range capability, because the signal voltage must be held at the PGA input for the duration of an auto-range subroutine by the computer. Such an algorithm consists of:

- Set PGA gain
- Trigger a conversion
- Note RESULT
- Iterate until (FS/2 ≤ RESULT ≤ FS)

Sampling Rate

Throughput rate for a DAS may be defined as the maximum number of digital samples per second that it can produce without exceeding its specified limit for accuracy. The system may run at a lower speed to avoid generating redundant and useless data; but if a waveform of significant bandwidth is to be reconstructed from the digital samples, then "the higher the better" is generally the rule for sampling rate.

The required rate is often higher than one would suppose. For example, using the criteria of data bandwidth alone, a very low sample rate is required for the slowly changing voltage outputs from a solar panel. Once per minute for each channel might be enough. With 60 channels though, the rate required is once per second. In addition, one might require a maximum of one second for notice of failure on any channel, boosting the required sample rate to 60 samples per second. In this manner low bandwidth channels may require a high speed DAS, according to the relationship:

System Sample Rate = (Highest Channel Rate) X (Number of Channels)

Also, a very high sample rate is required to preserve the high frequency content of a transient event on a single channel. The most commonly encountered requirement though, is a multichannel DAS (see Fig. 1) with a modest bandwidth on each channel. For example, each data source might be an accelerometer with an output ranging through several hundred Hertz.

Notice that the low and high bandwidth signals just described cannot be handled efficiently with the same system. A sample rate high enough for the highest bandwidth channel will oversample the lower bandwidth channels, generating unnecessary data. High and low bandwidth data are best handled by separate multiplexer/converter systems.

Presampling filters are essential to ensure accuracy in the sequence of digital samples representing a given channel. Since the multiplexer is a sampler (as is the Sample/Hold and A-D Converter) this means a separate filter dedicated to each channel preceding the multiplexer. A single filter following the multiplexer would do the job, but its modest response time would form a bottleneck restricting the sample rate. Guidelines are needed then, to relate a given level of accuracy to data bandwidth, filter cutoff frequency, and number of filter poles.

As mentioned earlier, a filter limits the error due to alias frequencies by restricting the bandwidth of both signal and noise. Either acting alone or in concert may cause error, since alias frequencies arise in several ways:

1. Overlap of the signal spectrum and the lower sideband associated with the sampling frequency f_S.
2. Overlap of the upper and lower sidebands associated with any two consecutive harmonics of f_S.
3. Overlap of any sideband with wideband noise from the data channel.

A band-reject filter would control case 1, but a low-pass type is needed to handle cases 2 and 3 as well. Again, the Butterworth response is preferred in most applications, but it does offer increasing phase shift and gain error for frequencies approaching the cutoff (-3dB) frequency. This cutoff should be set no higher than necessary for acceptable gain error in the highest signal components. A higher cutoff will only include unnecessary noise bandwidth.

Finally, for a given accuracy specification such as ± ½ LSB, a tradeoff may be made between the sample rate and number of poles. These poles usually come from the filter, but the number may include any pole(s) inherent in the transducer, provided they occur at an acceptable location relative to the cutoff frequency.

Fig. 12 shows aliasing error due to the signal spectrum alone vs sampling rate for different numbers of poles. The horizontal axis is normalized to Sampling Frequency/Cutoff Frequency. Notice that a 2-pole filter requires a sampling frequency 30 times the filter cutoff frequency, just to obtain 1% accuracy. For ± ½ LSB error in a 12-bit system (±.01%), a 5-pole filter requires sampling at 11 times the cutoff frequency. Remember, Fig. 12 applies only to the signal spectrum. Noise will cause some additional aliasing error.

Clearly, Nyquist's Sampling Theorem is not a practical guide for sampling rate in real applications. Actual (as opposed to hypothetical) filters cannot bandlimit a signal sufficiently to permit the theoretical minimum of two samples per cycle of highest signal frequency.

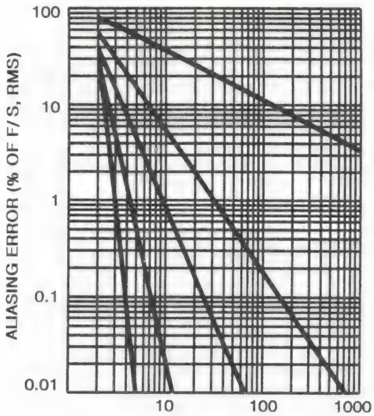


FIGURE 12. Effect of Filter Poles on Aliasing Error

Computer Interface

The typical DAS we have described (Fig. 1) requires several control signals:

- Multiplexer Channel Address
- PGA Gain Address
- Track/Hold Control
- A-D Converter
  - -Start Convert
  - -MSB Invert
  - -Short Cycle
  - -Unipolar/Bipolar
  - -Output Byte Enable
  - -Conversion Interrupt, etc.

This control can be provided directly by the computer, but some portion of these signals is usually supplied by an intermediate block of control logic. For monitoring predictable channel data, the DAS can repeatedly scan through its channels, trigger the converter, and notify the computer when each data sample is ready. This independent operation can be accomplished by a clock and counter arrangement to supply channel and gain addresses, plus a dual "one shot" multivibrator (74123) to gate the Start Convert and Track/Hold functions.

To handle a sudden change in data level or other unexpected event, the computer must be able to random access any channel or PGA gain. Provision is made to write this information to the DAS via the computer's data or address bus, using appropriate address decoders and latches.

When processing higher bandwidth signals, one error source to be minimized is the Track/Hold's aperture delay uncertainty, or jitter. The logic which generates the T/H control signal needs close attention, since jitter in this waveform adds to that specified for the device itself.

Finally, the DAS output consists of a serial stream of parallel digital words from the converter, synchronized with the converter's status signal indicating when the data is valid. Techniques for passing this data to the computer include direct memory access (DMA), memory mapping, and mapping via a dedicated I/O port, all with or without an external interrupt of the processor.

DMA is most efficient for the high speed transfer of large volumes of data. This can proceed by program request, resulting in the movement of a block of data to a designated sequence of memory locations, at a speed limited only by the memory cycle time. As an alternative, hardware can be configured to allow transfer of a data word during every non-memory machine cycle. This allows an almost continuous output of data from the DAS. The transfers are asynchronous and unsolicited by the program with only a slight increase in software execution time.

For less demanding data rates the choice is between an I/O or memory mapped interface. The former is best for small systems. For example, the 8085 microprocessor can control up to eight I/O devices without external address decoding. Addition of decoders expands the field from 8 to 256 peripherals.

There is a range of applications for which the choice of I/O or memory mapping is not clear, but memory mapping becomes attractive with increasing system complexity. The memory reference instructions available with this approach simplify programming and speed execution. A further increase in throughput is obtained by use of the processor's interrupt system, allowing the main program to proceed while an analog-to-digital conversion is in progress.

Memory mapping plus interrupt is very effective; however, the software overhead associated with service of an interrupt-driven I/O interface results in a diminishing advantage as the required throughput rate increases. Again, DMA offers the advantage for high data rates.

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APP NOTE

FOR YOUR INFORMATION

No. 538

Harris Analog

MONOLITHIC SAMPLE/HOLD COMBINES SPEED AND PRECISION

By Tarlton Fleming

Introduction

A new Sample-Hold amplifier from Harris Semiconductor offers the best combination of speed and accuracy available in a monolithic device. It was developed for moderate to high speed applications-and particularly as an input for successive-approximation A/D converters which perform a precise conversion in 30 microseconds or less. This second-generation design includes a 100pF MOS hold capacitor, and offers a 1.0 microsecond acquisition time along with high accuracy over the commercial and military temperature ranges.

This new product, the HA-5320, can track a signal indefinitely (like an op amp) while in the sample mode. At the instant a digital HOLD command is applied the corresponding signal level is held and maintained at the output. The ratio of sample (track) to hold time is set by the user, according to the duty cycle of his digital control signal.

Comparision With Earlier Design

The HA-5320 retains the versatility of its predecessor, the popular HA-2420. That is, both have the uncommitted differential inputs of an op amp, allowing their Sample-Hold function to be combined with many conventional op amp circuits. Their circuit designs are different, though, producing significant differences in performance. These are best illustrated by describing the new device in contrast with older HA-2420. Table 1 summarizes the electrical characteristics of each, based on a 100pF hold capacitor.

Both IC's are packaged in a 14 pin DIP and operate on ±15V supplies. The hold capacitor connections differ as shown in Figure 1. Otherwise, the pinouts are compatible to this extent: Either device will operate in an existing HA-2420 socket if pin 6 is grounded, preferably to the system signal ground.

The HA-5320 delivers optimum performance when used as intended – relying on the internal 100pF hold capacitor alone. At +75°C this capacitor allows only 19μV of droop in 15μs. The Droop Rate is proportional to Drift Current, which increases with temperature (Figure 3). Droop may be reduced by adding external cpacitance C_H as shown in Figure 1B. This extra capacitance will reduce the bandwidth (Figure 5) and affect other parameters as shown in Figure 4. Also, a capacitor of value $0.1C_H$ should be added at pin 8 to reduce output noise in the Hold mode. Whether operating with additional hold capacitance or not, an HA-5320 offers a considerable improvement in accuracy over the HA-2420. Particularly welcome is the elimination of variation in "pedestal" error with input voltage. Further, the residual pedestal error may be nulled to zero, yielding great accuracy at a given temperature.

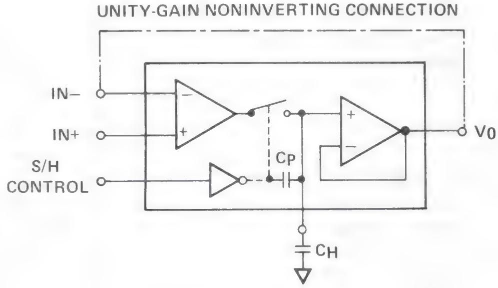


Figure 1A. HA-2420 Diagram

Test Conditions: $V_{PS} = \pm15V$; $V_{AL} = 0.8V$ (Sample); $V_{AL} = 2.0V$ (Hold); $C_H = 100pF$

(Room Temp R = +25°C; Full Temp. F is -55°C to +125°C)

PARAMETERS	TEMP.	HA-5320 MIN	HA-5320 TYP	HA-5320 MAX	HA-2420 MIN	HA-2420 TYP	HA-2420 MAX	UNITS
Input Characteristics								
Offset Voltage	R		0.2	0.5		2		mV
	F			2.0			6	mV
Bias Current	R		70	200		40		nA
	F			200			400	nA
Offset Current	R		30	100		10		nA
	F			100			100	nA
Common Mode Range	F	±10			±10			V
CMRR	R	-80	-90		-80	-90		dB
Transfer Characteristics								
Large Signal Voltage Gain	R	1×10^6	2×10^6			50K		V/V
Feedthrough Attentuation, 100KHz	F	76	80			76		dB
Gain Bandwidth Product	R		2.0			2.8		MHz
Output Characteristics								
Voltage	F	±10			±10			V
Current	R	±10			±15			mA
Full Power Bandwidth	R		600			100		KHz
Transient Response								
Rise Time	R		100			50	75	nS
Overshoot	R		15			25	40	%
Slew Rate	R		45		5	7		V/S
Digital Input Characteristics								
Voltage High (V_{AH})	F	2.0			2.0			V
Voltage Low (V_{AL})	F			0.8			0.8	V
Current (V_{AL} = 0V)	F			-4			-800	μA
Current (V_{AH} = 5V)	F			100			20K	nA
Sample/Hold Characteristics								
Acquisition Time, to ±0.1% FS	R		0.8			2.5		μS
±0.01% FS	R		1.0			3		μS
Aperture Time	R		25			30		ns
Effective Aperture Delay Time	R		-25			30		ns
Aperture Uncertainty	R		0.25			5		ns
Drift Current	R		8			5	50	pA
	F		1.7			1.8	10	nA
Pedestal Error	R		1.0			9		mV
Power Supply Characteristics								
Positive Voltage	F	14.5	15	16		15		V
Negative Voltage	F	-14.5	-15	-16		-15		V
Positive Current	R		11	13		8.5	12.5	mA
Negative Current	R		-11	-13		-8.5	-12.5	mA
PSRR	F	-65	-75		-80	-90		dB

Table 1. Electrical Characteristics HA-5320 vs. HA-2420.

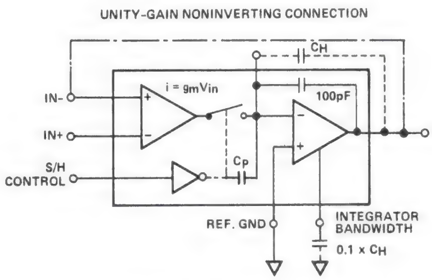


Figure 1B. HA-5320 Diagram

Understanding Pedestal Error

When a S/H amplifier is switched from Sample to Hold, its output voltage rarely matches the ideal value one would expect from a perfect device. Instead, it differs by a small ΔV of a few millivolts, even with a DC input applied. Called "Sample to hold offset" or "pedestal", this error has a predictable polarity and magnitude for given conditions.

In general, this error is affected by magnitude of the input voltage, magnitude of the digital control level V_{AH}, rise time of the logic transition, size of the hold capacitor and temperature. Most troublesome of these is the variation of pedestal with input voltage, and this effect has been completely eliminated in the HA-5320.

Pedestal error is caused by the injection of charge onto the hold capacitor from a digital input, through small values of parasitic capacitance. Injection can come directly from the S/H control input or from the internal switch action. In Figure 1A and 1B, the capacitance of a base-collector junction in the switching circuit is represented as Cp, which varies with base-collector voltage for the transistor. That voltage is constant for the HA-5320, since Cp connects to a virtual ground. Therefore, charge injection and the resulting pedestal error are not affected by changes in V_{IN}. (For the HA-2420 in Figure 1A, Cp varies with V_{IN} and produces a varying pedestal.)

Another source of injected charge is the S/H control signal. This coupling is virtually zero within the HA-5320 chip, but a packaged unit exhibits about one millivolt change in pedestal per volt change in TTL level. However, compensation in the chip has been adjusted for zero pedestal at the nominal TTL level of 3.5V.

Null the Pedestal

This may be accomplished by introducing an equal and opposite voltage at the output, using the Offset Adjust terminals as shown in Figure 2. Since pedestal error does not change with V_{IN}, it may be treated as a simple offset. Use of the Offset Adjust shifts the pedestal error to the Sample Mode though, which may cause problems in a few applications.

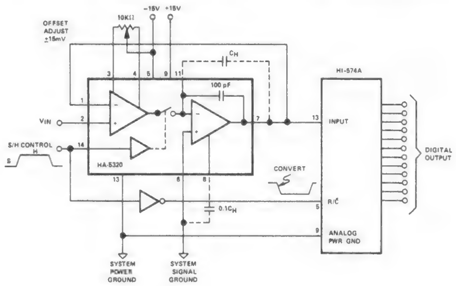
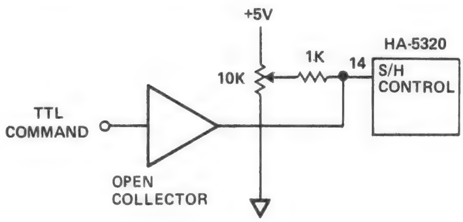


Figure 2. Signal Processing System

For these, one may make use of the relation between pedestal magnitude and the digital input level.

As mentioned earlier, the pedestal changes about one mV per volt of change in the digital "1" level, or V_{AH}. For small systems simply adjust V_{AH} until the pedestal is eliminated. In larger systems, the same adjustment may be made locally:



Understanding Droop Error

"Droop" is a change in output voltage vs. time while in the hold mode, caused by a flow of leakage current from the hold capacitor. For the HA-5320, this change is quite linear with time. The leakage current includes "off" leakage from the bipolar switch and bias current into the inverting input of the output integrator. The switch output consists of the joined collectors of two "off" transistors, NPN and PNP. These are tied to a JFET gate at the integrator input, so the hold capacitor looks at three leakage components, each of which doubles every 10°C. Ideally, these sum to zero and maintain a net zero leakage into the hold capacitor with changes in temperature. Effort has been made to achieve this. The JFET also produces less output noise than does the MOSFET used in the HA-2420.

An externally-supplied hold capacitor may provide other avenues for leakage current, but of course the HA-5320 does not require an external capacitor. Its 100pF internal hold capacitor is a guaranteed and factory-tested component. This eliminates the uncertainty associated with a user supplied com-

ponent, and also eliminates the selection, purchase, stocking, test and assembly of high quality hold capacitors.

The typical leakage (called "drift") current varies with temperature as shown in Figure 3. Then, droop error is directly related to drift current by the relation

$$V_{DROOP} = \frac{I_{DRIFT}\,\Delta t_H}{C_H}$$

where t_H is time in the hold mode. Using C_H=100pF and Δt_H = 25 μs, typical droop error may be calculated for a given temperature:

$$V_{DROOP} = \begin{array}{l} 1.25\,\mu V\ @ +\ 25^oC \\ 23.0\ \ \mu V\ @ +\ 75^oC \\ 425.0\ \ \mu V\ @ +125^oC \end{array}$$

This shows a typical droop error of less than 1/5 LSB in 12 bits at +125^{o}C, for one of the major applications targeted for this device (input to a successive-approximation A/D converter with 25μ s conversion time.)

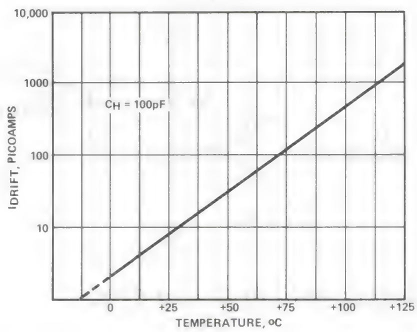


Figure 3. Hold Mode Drift Current v.s. Temperature

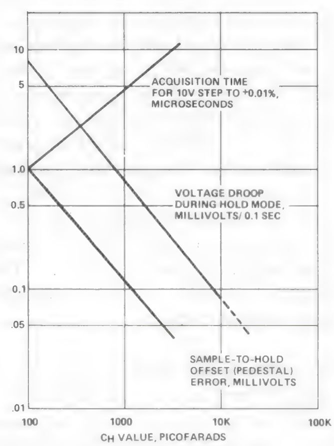


Figure 4. Typical Sample-and-Hold Performance v.s. Hold Capacitance

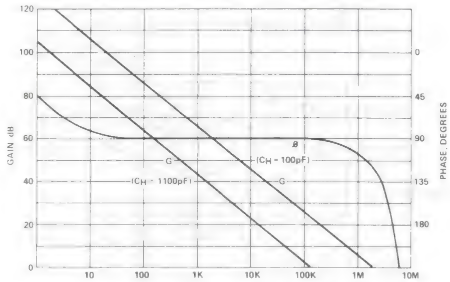


Figure 5. Open Loop Gain and Phase Response

Output Current

Up to ±20mA may flow without damage, but the guaranteed limit for normal operation is ±10mA. The design does not include short circuit protection; consequently output impedance remains low with increasing frequency. This is an advantage in Figure 2, where the S/H output sees step changes in load current as a conversion proceeds. The HA-5320 is able to absorb these current changes with only a small and brief (5mV, 100nS) perturbation in its output voltage. A higher output impedance would extend this transient toward the moment of decision by the converter's comparator, producing a degradation in digital output accuracy.

With power applied, avoid a momentary short of the HA-5320 output to any fixed potential such as ground or either supply.

Signal Processing Considerations

An analog signal may be digitized by a Sample/Hold-AD converter system such as the one shown in Figure 2. If required, the analog signal may then be reconstructed from that sequence of digital samples, using a D/A converter. One might ask, how does the sample/hold alone constrain this sampling process? That is, how high a frequency can be digitized to a given level of accuracy?

The HA-5320 imposes three types of limit on the highest signal frequency applied at its input. First, the analog channel in the Sample mode has a 2MHz small signal BW, and a 600KHz Full Power BW (20 Vpp input). Next, Aperture Uncertainty Time contributes a trade-off between accuracy and frequency. Finally, Acquisition Time places a ceiling on the maximum sample rate obtainable with a given A/D converter, according to:

$$\text{MAX SR} = \frac{1}{t_{ACQ} + t_{CONV}}$$

where t_{CONV} is the A/D converter's conversion time. (Input frequency must not exceed one half the Sample rate, unless the application is tolerant of "alias" errors).

For example, the typical HA-5320 Acquisition Time for a 10V step is:

Temp	Acquisition Time, t_{ACQ} ±0.1%	±0.01%
+25°C	0.8µs	1.0µs
+125°C	0.9µs	1.1µs

Thus a 25µs converter could generate approximately $(1\mu s + 25\mu s)^{-1}$ = 38,460 samples per second, allowing input frequencies as high as 19.23 KHz under ideal conditions (a low noise signal source with abrupt bandlimiting).

In most applications though, a low pass "antialiasing" filter is required to bandlimit the HA-5320 input. This filter controls "alias" error by reducing the amplitude of all signals and noise at and above the Nyquist frequency (SR/2). A given accuracy requirement translates to a minimum attenuation at the Nyquist frequency, which is accomplished by increasing the sample rate and/or the filter complexity(# poles). Twelve bit (±1/2 LSB) accuracy for example, calls for a 5 pole filter and sampling at 11X the highest signal frequency of interest. Using 38.46KHz for Sample Rate, this limits the input frequency to 3500Hz (SR/11). If this seems low, bear in mind that 12 bits ±1/2LSB is a tight specification.

The HA-5320's Aperture Uncertainty Time also imposes a limit on input frequency, independent of that due to filter poles and sample rate. The relation is

$$f_{max} = \frac{1}{2^{n+1} \pi t_{AU}}$$

where t_{AU} is the aperture uncertainty and f_{max} is the highest frequency that can be sampled to ±1/2 LSB accuracy at n-bit resolution. Typical t_{AU} is 270ps for the HA-5320, leading to 143.9 KHz for f_{max} at 12 bits. That makes the HA-5320 compatible with some of the fastest 12 bit converters available today. Also, since f_{max} increases for lower resolution, the frequency limit based on aliasing will be encountered first in nearly all applications.

Another parameter of concern is feedthrough. After sampling a signal and holding it, how much of that signal will couple to the output and appear superimposed on the DC level there? At 100KHz, the answer is 1mVpp at the output, due to 10Vpp at the input. At 10KHz, the feedthrough is still -80dB indicating the coupling path is resistive over this range.

At lower frequencies, the feedthrough is less (better) than this, since the HA-5320 is designed for relatively short hold periods. For example, the 3500Hz limit mentioned above for a 12 bit, 25µs converter requires 285µs to complete one cycle. The HA-5320 will see only a small fraction of this input cycle during each hold period.

Op Amp Properties

Both the HA-5320 and HA-2420 behave like op amps in the sample mode, and may be treated as such-that is, external feedback may be connected to form filters, integrators, inverting and non-inverting amplifiers with gain, etc. This versatility is in contrast to many other designs in which the inverting input is internally connected, committing the device to the noninverting unity gain configuration.

Referring to Figure 1, it may be noted that the HA-5320 is even more like an op amp that the HA-2420. Where the HA-2420 input stage is a voltage amplifier (actually an op amp by itself), the HA-5320 input stage is a transconductance amplifier, producing an output current $g_m V_{IN}$. Also, the HA-5320 output stage is an integrator, analogous to the 2nd stage of a classical op amp. The hold capacitor corresponds to the op amp's compensation capacitor, through here the analogy falters. Like the op amp though, closed loop gain-bandwidth product for the HA-5320 may be predicted from the expression g_m/C_H.

Fabrication of the HA-5320 features the Harris high frequency dielectric isolation (DI) process, with front-diffused collectors and P-channel JFET's. This approach has yielded DC input characteristics which compare well with those of premium monolithic op amps. Typical Offset Voltage is 200µV at +25°C and only 2mV at +125°. Offset Current is guaranteed less than 100nA at +125°C, or half the value of Bias Current at that temperature. Common Mode Rejection is guaranteed 80dB minimum over the ±10V range, with 90dB typical.

The HA-5320 is very stable in the noninverting unity gain connection. Typical phase margin is 60° at an open loop unity gain frequency of about 2MHz.

As mentioned earlier, the addition of external hold capacitance has a direct affect on bandwidth. For example, adding 1000pF increases C_H from 100pF to 1100pF. As a result, the 2MHz unity gain bandwidth shrinks to (100/1100) 2MHz = 182KHz. This means more time must be allowed for acquisition for a new sample, but not in the same ratio: Acquisition Time to .01% increases from 1.0µs to only 8.7µs.

Figure 6 shows the response to a 10 volt step in the sample mode. The asymmetry from rise to fall time for slew rate and overshoot is common to all units.

Figure 7 shows some Sample/Hold characteristics for a small signal (10mVpp) input. The Sample to Hold settling time is less than 200ns-higher gain and sweep speed resolve this to about 160ns. Notice

the final overshoot is less than .01% (one millivolt). This response is the same for any signal level. Also, slew rate is proportional to the magnitude of an input step, yielding a fairly constant value for slewing time, regardless of the distance slewed. This produces about one microsecond of acquisition time for any step change exceeding small signal conditions. For the small signal input of Figure 7, however, acquistion time is about 400ns (no slewing).

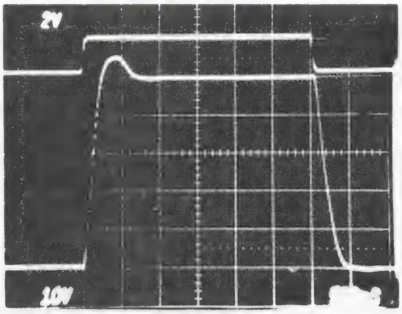


Figure 6. Step Response

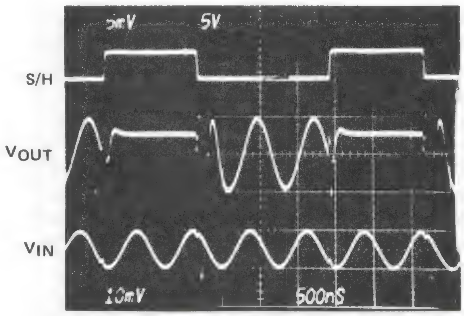


Figure 7. Small Signal Transient Response

Applications

A/D CONVERTER INPUT

An important application has been presented in Figure 2, in which the HA-5320 serves to reduce the aperture time of an A/D converter. More directly, the Sample/Hold "freezes" an instantaneous value of V_{IN} and holds it constant during the analog to digital conversion. In Table 2, f_{max} without a Sample/Hold is relatively low, since aperture time equals the HI-574A conversion time. Adding the HA-5320 substitues a much smaller aperture, which could allow an input frequency over 100KHz, but a lower limit is imposed by alias error effects. This limit depends on various conditions in the application, so the values listed for f_{max} (using the HA-5320) are only representative.

REQUIRED	HI-5712 CONVERSION TIME, MAX.	f_{MAX} (Vin) WITHOUT SAMPLE/HOLD	USING THE HA-5320: MAXIMUM SAMPLING RATE	f_{MAX} (Vin)	Min. # POLES, ANTI-ALIASING FILTER
8 BITS ±1/2LSB	7μS	88.8Hz	111KHz	24.8KHz	8
10 BITS ±1/2LSB	8.5μS	18.3Hz	95KHz	6.2KHz	3
12 BITS ±1/2LSB	10μS	3.9Hz	83KHz	1.5KHz	3

Table 2. Accuracy v.s. Maximum Input Frequency f_{max}

PEAK DETECTOR

An analog signal requires about 100ns to propagate through the HA-5320. For time varying signals, this assures a voltage difference between input and output. Also, the voltage changes polarity when the signal slope changes polarity (passes a peak). This behavior makes possible a Sample-Hold peak detector, by adding a comparator to detect the polarity changes.

In Figure 8 the exclusive NOR gate allows a reset function which forces the HA-5320 to the sample mode. The connections shown detect positive peaks; the comparator inputs may be reversed to detect negative peaks. Also, offset must be introduced to provide enough step in voltage to trip the comparator after passing a peak.

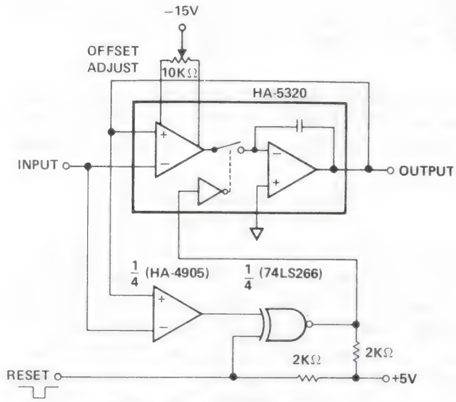


Figure 8. Positive Peak Detector

This circuit works well from below 100Hz up to the frequency at which slew rate limiting occurs. It captures the amplitude of voltage pulses, provided the pulse duration is sufficient for slewing to the top of the pulse.

The author wishes to thank design engineer Paul Hernandez and senior technician Roger O'Brien for their technical support.

HA-5170 PRECISION LOW NOISE JFET INPUT OPERATIONAL AMPLIFIER

By J. S. Prentice and R. W. Leath

Introduction

The HA-5170 is a precision, JFET input, operational amplifier which features low noise (12 nV/$\sqrt{Hz}$ at 1kHz), low offset voltage (100 μ V), low offset voltage drift (3 μ V/°C), and low bias currents (20pA). Complementing these excellent input characteristics are dynamic performance characteristics never before available from precision operational amplifiers. An 8V/μs slew rate, 5MHz bandwidth and fast settling times less than 1.5 μs (settling to 0.01%) make the HA-5170 well suited for fast, precision A/D or D/A converter designs, precision sample and holds, precision integrators, or transducer signal amplifier designs.

Inside the HA-5170

The Harris technology has two important advantages. First, a unique ion implant process produces JFET's with excellent matching and low 1/f noise. Second, the JFET's are in their own dielectrically isolated islands which completely eliminates the largest gate current component — the island to substrate leakage.

The HA-5170 has two voltage gain stages. The first consists of a differential JFET pair with resistor loads which develops a gain of 10. The second is a complete bipolar op amp with a gain of 30K. The absence of active loads in the first stage insures that the offset voltage, offset voltage drift and noise voltage result exclusively from the input JFET pair.

When it comes to building low noise JFET componets, bigger is better. The JFET input noise voltage, both the 1/f and white componets, is inversely proportional to the square root of the gate area. Likewise, the input noise voltage due to the drain load resistors is inversely proportional to the square root of the resistance value. The JFET's "weigh in" at a whooping 110 mil^2 gate area with the resistors at 14kΩ. This results in typical noise voltages of 12nV/$\sqrt{Hz}$ at 1kHz, 25nV/$\sqrt{Hz}$ at 10Hz and 1 μ V p-p over the 0.1 to 10Hz frequency band.

Trimming the offset voltage of a JFET op amp usually degrades the offset voltage temperature coefficient, so a trim scheme that simultaneously nulls both the offset voltage and offset voltage temperature drift was developed. The dominant JFET mismatches arise from mismatches in the channel height and doping profiles, not photolithography errors. It is not surprising that the V_P mismatches correlate with the I_{DSS} mismatches.

The amplifier offset voltage is given by

$$V_{OS} = \Delta V_P \left(1 - \sqrt{\frac{I_{DS}}{I_{DSS}}}\right) + \frac{V_P}{2}\sqrt{\frac{I_{DS}}{I_{DSS}}}\left(\frac{\Delta I_{DSS}}{I_{DSS}} - \frac{\Delta I_{DS}}{I_{DS}}\right)$$

In this circuit, the mismatch of the drain load resistor sets the JFET drain current mismatch.

$$\frac{\Delta I_{DS}}{I_{DS}} = -\frac{\Delta R}{R}$$

Thus, the offset voltage can be zeroed by trimming the load resistors. Since V_P has a large positive temperature coefficient, the offset voltage drift is normally degraded. By making the loads from composite resistors, thin film resistors in series with diffused resistors, the temperature coefficient of the Δ R/R ratio can be set to cancel both the trimming induced drift and also the JFET mismatch induce drift. This makes the HA-5170 the first JFET op amp in which trimming the offset voltage simultaneously trims the offset temperature drift. Furthermore, the offset voltage drift is reduced to even lower values when the offset voltage is nulled externally with an offset adjustment pot. The 5170 has a typical offset voltage of 100 μ V, offset drift of 3 μ V/°C (without external offset nulling), and warm-up drift of only 20μV.

The excellent dc performance of the HA-5170 is complemented with dynamic A.C. performance never before available from precision operational amplifiers. The 8V/μs slew rate and 5MHz bandwidth allow the designer to extend precision instrumentation applications in both speed and bandwidth. The fast settling time of the HA-5170 (typically less than

$1.5\mu s$, settling to 0.01%) also makes it well suited for fast precision A/D and D/A converter designs.

Applications

Several applications which utilize the design features and excellent performance of the HA-5170 are described below.

Single Op Amp Instumentation Amplifier

The HA-5170 may be used as a single op amp instrumentation amplifier because of a unique design feature which places the offset adjust terminals at the juncture of two differential gain stages. The instrumentation amplifier, as shown in Fig. 1, is very simple and provides good performance features such as low noise, low offset voltage, low offset voltage drift and high input impedance at low cost.

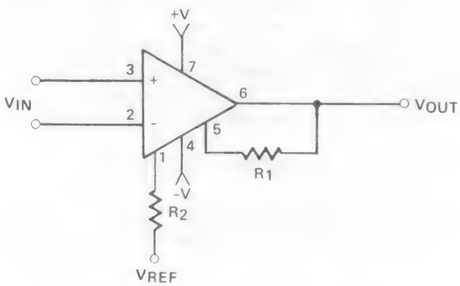


Figure 1. Single Op Amp Instrumentation Amplifier

The gain of the first differential stage is internally fixed at a gain approximately equal to 12. A feedback resistor R_1 connected between the output (Pin 6) and the balance pin (Pin 5) will close the loop around the second differential stage and set its gain. The closed loop gain of the instrumentation amplifier varies directly with the value of R_1 and is approximately

$$A_{VCL} = 12.5\ V/V/k\Omega$$

The minimum gain which can be applied is about 125 ($R_1 = R_2 = 10k\Omega$) because the current into pins 1 or 5 must be limited to 4mA.

The second resistor (R_2, which is connected between Pin 1 and a reference voltage) is used to establish a reference voltage level for the output. This reference voltage may be placed at ground potential or may be variable for use as offset adjustment. The resistor R_2 should also be matched with R_1 in order to maintain high common mode and power supply rejection ratios. Standard 1% tolerance resistors will typically provide 90dB rejection ratios.

The two inputs of the HA-5170, pins 2 and 3, may now be used as high impedance, true differential inputs with a common mode range of $-V_{supply}+3V$ to $+V_{supply}+0.1V$. If resistor values $R_1 = R_2 = 16k\Omega$ are used, for example, this circuit will provide a closed loop gain of 200 with a 3dB bandwidth of 20kHz and a THD $< 0.5\%$ ($V_{out} = 2V_{p-p}$). The gain linearity is typically better than 0.2%. However, the gain also changes about 0.2%/V with both common mode and power supply voltages. The gain T.C. is around 450ppm/°C but this can be reduced to less than 200ppm/°C just by using carbon film resistors which normally have negative T.C.'s (approximately 260ppm/°C for $16k\Omega$ resistors). Of course using resistors which have negative T.C.'s near 450ppm/°C will cancel gain T.C.'s altogether. If a variable gain is desired, a trim pot (in addition to R_1 and R_2) may be placed between the offset adjust pins. Resistors R_1 and R_2 and the maximum value of the trim pot will set the minimum gain. As the resistance of the trim pot is decreased, the gain will increase proportionally to the inverse of the trim pot resistance. This relationship of gain and trim pot resistance is shown in Fig. 2.

This circuit also maintains all the HA-5170's excellent A.C. and D.C. characteristics such as low offset voltage, low offset voltage drift, low noise, and high gain.

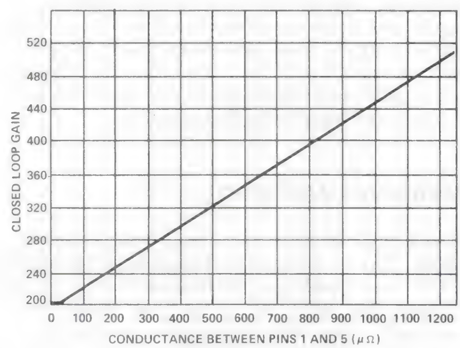


Figure 2. Closed Loop Gain Vs. Conductance Of Trimpot

Sine Wave Oscillator

The instrumentation amplifier circuit described above can be easily modified to produce a low distortion sine wave oscillator with voltage controlled amplitude as shown in Fig. 3. The small changes in gain of the instrumentation amplifier that occur with changes in common mode voltage has been exploited here to provide oscillator amplitude control with a voltage source. Another unique feature of this circuit is that is does not require any of the nonlinear components that most other sine wave oscillators require.

The phase lead network, which consist of R_3, R_4, and C_1, cancel the phase lag through the amplifier and oscillation occurs at the frequency where the product of amplifier gain and voltage feedback ex-

actly equals one. The amplifier gain is expressed as

$$A_V = \frac{A}{(1 + j\omega/\omega_o)}$$

where A is the dc gain (about 125 for $R_1 = R_2 = 10k\Omega$), ω_o is the bandwidth (about 200K rad/s) and ω is the frequency of oscillation. The voltage feedback is expressed as

$$\frac{j\omega C_1 R_4}{[1 + j\omega C_1 (R_3 + R_4)]}$$

For their product to be equal to one, both of the following must be true:

$$\omega = \frac{\omega_o}{[C_1 (R_3 + R_4)]}$$

$$AC_1R_4 = C_1(R_3 + R_4) + \frac{1}{\omega_o}$$

The oscillation amplitude is stabilized at the point where the loop gain is equal to one by the small gain nonlinearity of the instrumentation amplifier.

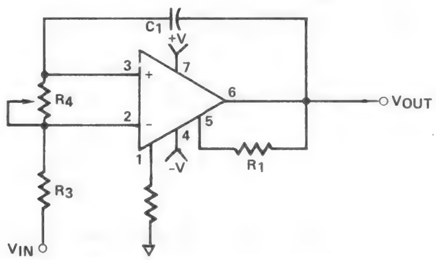


Figure 3. Sine Wave Oscillator With Voltage Controlled Amplititude

This operating point and initial amplitude is set by the resistor divider network of R_3 and trim pot R_4 ($R_4 \ll R_3$). The amplitude can then be varied by applying a common mode voltage (V_{IN}) through R_3. Positive common mode voltages increase amplitude by decreasing gain non-linearity while negative common mode voltages decrease amplitude. A typical curve of amplitude versus common mode voltage is shown in Figure 4. The gain non-linearity of the instrumentation amplifier is small, however, and distortion less than 0.5% can be obtained over a 100Hz to 100kHz range.

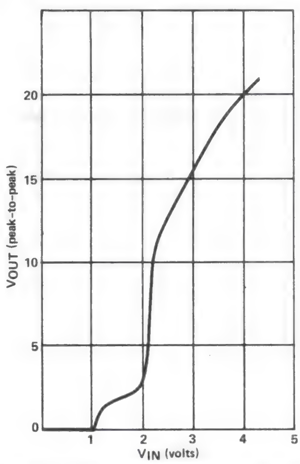


Figure 4. Oscillation Amplitude Vs. V_{IN}

Frequencies down to 10Hz can be achieved by lowering ω_o with a capacitor in parallel with R_1.

High Impedance Transducers

The HA-5170 is well suited as a preamplifier for high impedance transducers, such as photo diodes and hydrophones, because of its high input impedance and low current noise. Fig. 5 shows a photo diode preamplifier circuit whose output voltage is approximately the photo diode current times the value of R_1. When no light is present, the output of the HA-5170 is

$$V_O = I_{ND} R_1 + I_N R_1 + V_{NR} + V_N$$

where I_{ND} = Shot noise of diode
I_N = Noise current of Op Amp
V_{NR} = Noise voltage of resistor
V_N = Noise voltage of Op Amp

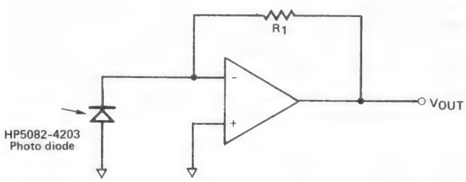


Figure 5. Photodiode Preamplifier

The signal to noise ratio is maximized when the rms sum of op amp and resistor noise current sources is equal to or lower than the noise current of the photo diode. Noise voltage sources are converted to noise current sources by dividing by R_1. The noise current of the photo diode may be approximated by the shot noise formula $2qI_d$, where I_d is the dark current, and is in the range of 10^{-13} to 10^{-14} A/$\sqrt{Hz}$, depending upon the choice of photo diodes. The rms sum of the three sources is approximately 4×10^{-14} A/$\sqrt{Hz}$ at 1kHz, assuming $R_1 = 20M\Omega$. This rms summation is approximately the same magnitude as the noise current of the photo diode with the dominant noise source being the resistor noise (about 2.9×10^{-14} A/$\sqrt{Hz}$). If a bipolar op amp were used instead of the HA-5170, the noise current (typ. 4×10^{-13} A/$\sqrt{Hz}$) would be much higher than the noise current of the photo diode. The response time of the photo diode can be improved by applying 5 to 20 volts of reverse bias but the increased speed is achieved at the expense of higher shot noise.

A resistor equal to the feedback resistor could be inserted between the non-inverting input and ground to reduce offset voltage. This is usually not necessary since the output offset voltage would only be 600μV for a 20MΩ resistor.

Fig. 6 shows a hydrophone preamplifier with a 100Hz to 100kHz bandwith and a gain of 100. Since hydrophone impedance is capacitive, it should be bypassed with a large bleeder resistor to shunt the bias currents to ground.

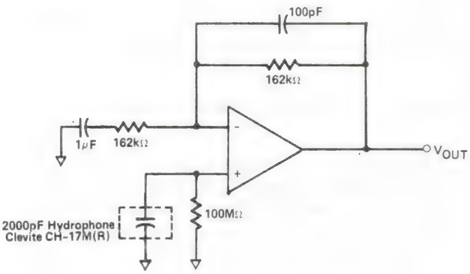


Figure 6. Hydrophone Preamplifier

Current Source/Sink and Current Sense Circuits

The HA-5170 can be used as a well regulated, two terminal, constant current source or sink, as shown in Fig. 7, or as a current sense amplifier, as shown in Fig. 8. These circuits take advantage of FET inputs' capability to accept a common mode voltage up to 0.1V above the positive supply.

The current from the constant current source consists of amplifier supply current and load current through R_2, both of which pass through the sense resistor R_1. The amplifier output will sink just enough current to cause the IR drop across R_1 to equal the amplifier offset voltage. This offset voltage may be adjusted by the trim pot R_3 and typically has a minimum adjustment range of 6mV. Smaller offset voltages give better power supply rejection ratios and usually give better results. The amplifier supply current, typ. 1.8mA, sets the minimum constant current while the amplifier short circuit protection limits the maximum to 15mA. Current regulation better than 0.08%/V and temperature variations better than 0.08%/°C can be achieved with this design.

Two operating constraints should be observed for best results. The resistor R_1 should be selected so that the amplifier output voltage remains at least 1.3V from either supply pin and the total voltage across pins 4 and 7 should be at least 12V but not over 40V.

The HA-5170 may also be used as a simple current sense amplifier in power supply applications. In this circuit, the power supply current develops a small voltage drop across the sense resisitor (R_S in Fig. 8) and the ammeter will display a current which is equal to $I_s \times \frac{R_s}{R_1}$. Of course the HA-5170 could also be placed in an open loop (comparator) configuration in which case the output would "trip" when the IR drop across R_s exceeds the offset voltage. This "trip" point can be controlled by an offset adjust trim pot connected as shown. The low noise, low offset voltage, and low bias current characteristics of the HA-5170 provide accurate measurement of supply current with very few components and can operate over a supply range of 7 to 40V.

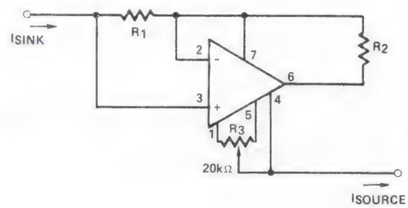


Figure 7. Two Terminal Constant Current Source/Sink

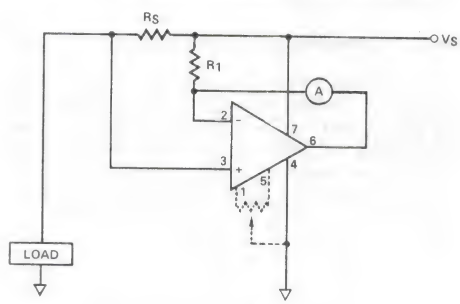


Figure 8. Current Sense Amplifier

APP NOTE

FOR YOUR INFORMATION

No. 541

Harris Analog

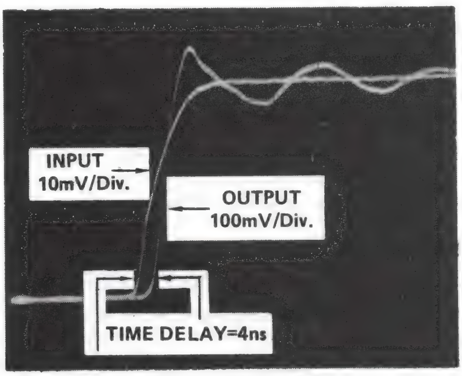
USING HA-2539 OR HA-2540 VERY HIGH SLEW RATE, WIDEBAND OPERATIONAL AMPLIFIERS

By: Richard Whitehead

Introduction

With the superior dynamic performance available from the HA-2539 and HA-2540, a wide variety of applications can be "idealized". From high fidelity audio to television broadcast and receiving equipment these operational amplifiers can be used to provide increased system capabilities. Employing the Harris High Frequency Dielectric Isolation Process, the HA-2539 with true differential input devices offer 600V/µs slew rate coupled with 600MHz gain bandwidth product. These outstanding AC parameters in conjunction with an excellent time delay of 4ns (see photo), standardize HA-2539 in critical wideband video and RF applications.

The HA-2540 is very similiar in design with the HA-2539, except for the addition of some small internal compensation (approximately 7pF). It offers a 400V/µs slew rate and a 400MHz gain-bandwidth product. The pinout of the HA-2540 uses the familiar 14 lead DIP pinout of other Harris wideband amplifiers.



HA-2539 TRANSIENT RESPONSE WAVEFORMS

Prototyping With HA-2539 or HA-2540

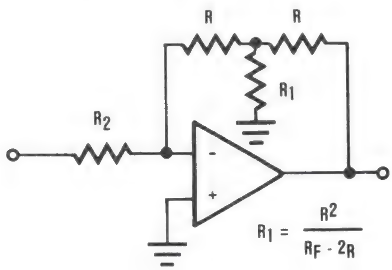
Being a "true" operational amplifier, HA-2539 or HA-2540 may be "designed in" using conventional high frequency amplifier techniques. Quality I.C. sockets may be used, but for maximized dynamic performance it is suggested these devices be mounted through a ground plane. External components should have minimal lead lengths and perferably connected directly to the device pins. Metal film or metal oxide resistors are recommended for feedback components. If direct connection is not possible, Teflon insulated standoffs should be used with locations as close as possible to device pins. Power supply decoupling with .001µF ceramic capacitors from the device supply pins to ground is essential. Alternatively, filter connectors such as Erie 1201-052 are suggested for optimum decoupling.

For best high frequency performance, feedback resistor values should be restricted to minimal values. Values below 5KΩ are recommended to reduce possibilities of introducing unwanted poles into the applications transfer function. Figure 1 indicates how high values for closed loop gain can be implemented, while maintaining feedback element values. This method is called "T network" feedback and values for the resistors can be derived from the following expression.

$$R_1 = \frac{R2}{R_f - 2R}$$

Where:

Rf is the value of feedback resistance to be reduced and R is a value preselected by the designer.



WHERE R IS PRESELECTED AND R_F
IS DESIRED FEEDBACK RESISTOR VALUE

FIGURE 1. KEEPING FEEDBACK VALUES LOW

The HA-2539 and HA-2540 may be used without heat sinks up to +75°C ambient. Power derating above this temperature is 9.6mW/°C and heat sinking is recommended. Thermalloy model 6007, Unitrack CPU 1017, or AAVID 5602B heat sinks are suggested for temperatures up to+125°C ambient. Also refer to Application Note 556 for further Safe-Operating-Area information.

General Operating Considerations

Dynamic performance of the HA-2539 and HA-2540 were maximized through the exclusion of output short circuit protection and internal offset voltage adjustment circuitry.

Although these amplifiers can withstand momentary short circuits to ground, it is recommended that some output current limiting network be used, if the operating environment is hostile. Figure 2 shows a suggested method for output terminal protection.

Offset voltage adjustment may be accomplished by the suggested methods shown in Figure 3 (a) and (b).

As with many wideband, high speed devices, recovery from output saturation can be in the order of microseconds. HA-2539 and HA-2540's saturation recovery from its positive rail is of the classical variety where voltage charges on the "body" capacitance of output devices must discharge before normal operation can be resumed. Recovery from the negative rail is similar to the positive rail recovery except during saturation small signal oscillation may occur. This oscillation is due mainly to a regenerative signal coupled back to the input during saturation.

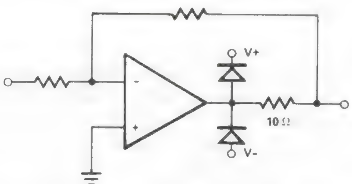
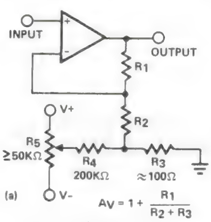
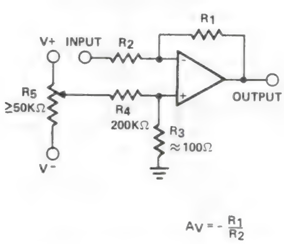


FIGURE 2. OUTPUT PROTECTION FROM FAULT CONDITIONS FOR HA-2539 & HA-2540



3a.



3b.

FIGURE 3. OFFSET NULLING FOR HA-2539 AND HA-2540

Range of Adjustment for Both Non-Inverting (Top) and Inverting Amplifiers (Bottom) Determined by Product of V_{SUPPLY} and R_3/R_4 Ratio.

General Applications

FREQUENCY COMPENSATION

HA-2539 and HA-2540 are stable in standard operational amplifier circuits with closed loop gains exceeding +10 or -9. Keeping the network resistor values and source resistance as low as practical in these configurations should optimize the dynamic performance.

Circuit configurations shown in Figure 4 may be used to stabilize the HA-2539 or HA-2540 at closed loop gains less than specified. Figure 4(a) employs capacitance to over damp the amplifiers' response. Stable operation to gains of 5 are practical. Figure 4(b) utilizes the amplifier's differential input impedance to reduce input and feedback signals thereby raising noise gain to a stable point on the response curve. Gains of -3 are practical.

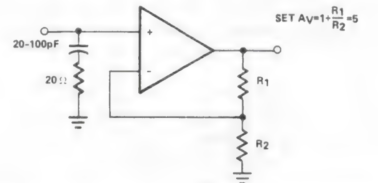


FIGURE 4a. COMPENSATION BY OVERDAMPING

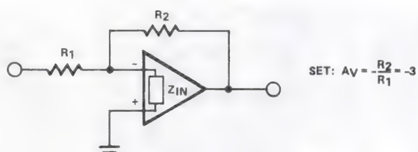


FIGURE 4b. STABILIZATION USING Z_{IN}

Reducing DC Errors

A composite amplifier scheme may be used to reduce errors due to offset voltage and bias current. Figure 5 shows HA-2539 and HA-5170 in a composite configuration which greatly reduces DC errors without compromising the high speed, wideband characteristics of HA-2539. The HA-2540 could also be used, but with slightly lower speeds and bandwidth response.

The HA-2539 amplifies signals above 40KHz which are fed forward via C_2 and R_2. Resistors R_4 and R_5 set the voltage gain at -10. The slew rate of this circuit was measured at 350V/μs. Settling time to a 0.1% level for a 10V output step is under 150ns and the gain bandwidth product is 300MHz.

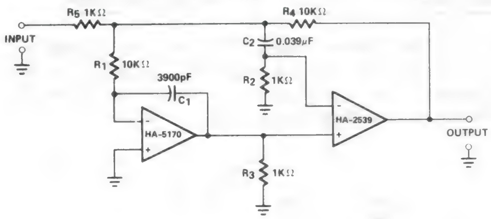


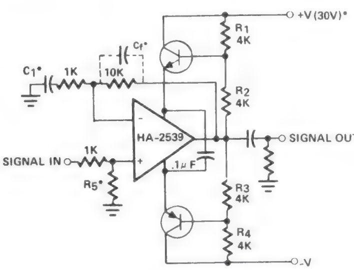
FIGURE 5. COMPOSITE AMPLIFIER

The HA-5170 amplifies signals below 40KHz, as set by C_1 and R_1, and controls the DC input characteristics such as offset voltage, drift, and bias currents of the composite amplifier. Therefore, it has an offset voltage of 100μV, drift of 2μV/^{o}C and bias currents in the 20pA range. The offset voltage may be externally nulled by connecting a 20K pot to pins 1 and 5 with the wiper tied to the negative supply. The DC gains of the HA-5170 and HA-2539 are cascaded, which means that the DC gain of the composite amplifier is well over 160dB.

The excellent AC and DC performance of this composite amplifier is complemented by its low noise performance, 0.5μVrms from 0.1Hz to 100Hz, and makes it very useful in high speed data acquisition systems.

Boosting Output Power and Increasing Output Signal Swing

Figure 6 shows a cost effective method for increasing output voltage swing or boosting power of the HA-2539 or HA-2540 while adapting the device to supply rails which exceed the absolute maximum ratings. The supply rail values are limited only by the breakdown voltages of the transistors used, provided R_1 through R_4, are set to limit the voltage at the device supply pins to nominal supply voltages (±15V). Transistor selection should be limited to high f_T (greater than 60MHz) types such as MPS-A06 and MPS-A56. Physical layout properties may necessitate the use of phase lead compensation, in which case C_F may be added. It has unmeasurable distortion and very low noise within the audio band.



*NOTES:

1. Used for experimental purposes. $C_1 \approx$ 3pF.
2. C_1 is optional (.001μF → .01μF ceramic).
3. R_5 is optional as can be utilized to reduce input signal amplitude and/or balance input conditions R_5 = 500Ω to 1KΩ.

FIGURE 6. BOOTSTRAPPING FOR MORE OUTPUT POWER AND VOLTAGE SWING

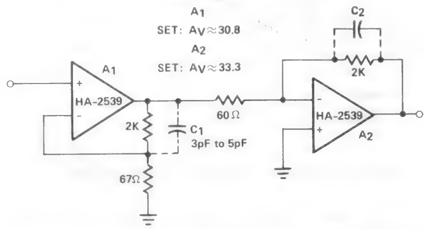
Applications

INTRODUCTION

HA-2539 and HA-2540 may be utilized in a wide variety of applications ranging from active filters to video pulse amplification. However, the applications to follow were selected to show where this can be used most advantageously.

APPLICATION 1: CASCADED AMPLIFIER

Cascaded amplifier sections are used to extend bandwidth and increase gain. Using two HA-2539 devices, this circuit is capable of 60dB gain at 20MHz.



APPLICATION 1. CASCADED AMPLIFIER SECTION

APPLICATION 2: VIDEO GAIN BLOCK

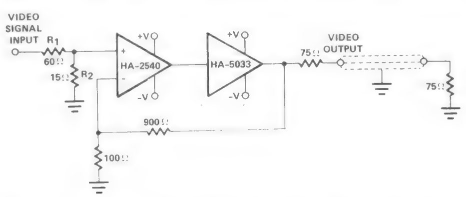
Video drivers and gain blocks used in color video systems are most always required to have outstanding differential phase and differential gain specifications. These requirements historically have eliminated the use of operational amplifiers and favor large discrete amplifiers which can be tailored to minimize systems errors.

This configuration utilizes the wide bandwidth and speed of HA-2540 plus the output capability of HA-5033. Stabilization circuitry is avoided by operating HA-2540 at a closed loop gain of 10 while maintaining an overall block gain of unity. However, gain of the block may be varied using the equation:

$$\frac{V_{OUT}}{V_{IN}} = 5 \frac{R_2}{(R_1 + R_2)}$$

where $R_1 + R_2 = 75\Omega$

A maximum block gain of 3 is recommended to prevent signal distortion.

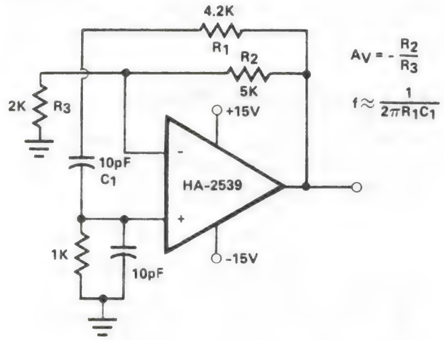


APPLICATION 2. VIDEO GAIN BLOCK HA-2539 & HA-2540

The circuit in Application 2 was tested for differential phase and differential gain using a Tektronix 520A vector scope and a Tektronix 146 video signal generator. Both differential phase and differential gain were too small to be measured.

APPLICATION 3: HIGH FREQUENCY OSCILLATOR

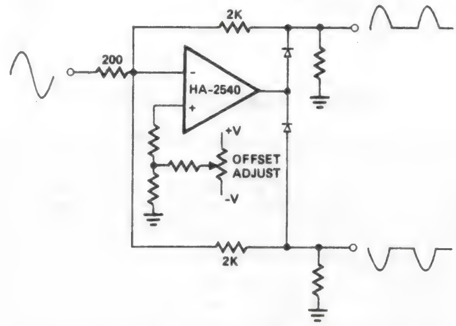
Intended primarily as a building block for a QRP transmitter, this 20MHz oscillator delivered a "clean" $6V_{p-p}$ signal into a 100Ω load.



APPLICATION 3. 20MHz OSCILLATOR

APPLICATION 4: WIDEBAND SIGNAL SPLITTER

With one HA-2539 or HA-2540 and two low capacitance switching diodes, signals exceeding 10MHz can be separated. This circuit is most useful for full wave rectification, AM detectors or sync generation.



APPLICATION 4. WIDEBAND SIGNAL SPLITTER

Acknowledgments

A. Terry D. Hass of Solitron, Inc., Stuart, FL. developed and tested video gain block.

B. Ron Jasinski of Sound Studio Services, 3208 Cahuenga Blvd. West, Los Angeles, CA. 90068 developed and tested bootstrapped output scheme.

C. Russ W. Leath of Harris Semiconductor developed and tested composite amplifier circuit.

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Application Note 525 — HA-5190/5195 Fast Settling Operational Amplifier May 1979.

Tobey, Braeme, and Huelsman. Operational Amplifiers Design and Applications. New York: McGraw-Hill Company, 1971.

Application Note 552 — HA-2542 "T Network" Schematic

Application Note 556 — Thermal Safe-Operating-Areas For High Current Op Amps

APP NOTE
FOR YOUR INFORMATION

No. 543
Harris Analog

NEW HIGH SPEED SWITCH OFFERS SUB-50ns SWITCHING TIMES

By Carl Wolfe

Introduction

An ideal CMOS analog switch would exhibit such characteristics as zero resistance when turned on, infinite resistance when turned off, zero power consumption, and zero switching time. Unfortunately, such a device is usually found as an example in a college textbook. The real world offers tradeoffs and imperfections which prevent the realization of the ideal. The integrated circuit designer works within these limits and attempts to optimize device performance by utilizing new technologies and improving circuit design. The development of a new high speed analog switch required the use of both of these techniques to achieve its performance. (See Appendix I: "Inside the HI-201HS").

The HARRIS HI-201HS is the industry's first sub-50ns monolithic analog switch and along with fast switching speed, offers improved performance and pin compatibility with industry standard 201's (Fig. 1). This article will discuss the technology, performance, and applications for this product.

Improve Those Existing Designs

The application circuits which follow are examples of typical applications and illustrate how the HI-201HS can improve existing applications where standard 201's are presently being used.

The first example is a high speed multiplexer shown in Fig. 2. The analog multiplexer is a circuit which switches a number of analog inputs to a single output and is used heavily in data conversion and avionic applications. This function can be easily achieved with the HI-201HS by tieing the outputs together and selecting the appropriate analog input. The HI-201HS is an excellent choice for this application since its low on resistance and leakage current will reduce system error, and its high speed is unmatched by any other monolithic analog switch. Since the output capacitance is additive, the RC time constant of the load will increase when the outputs are made common.

The next application is a high speed sample and hold which takes advantage of the improved performance of the HI-201HS and the precision F.E.T. input of the HA-5160 high slew rate amplifier. A sample and hold circuit or track and hold as it is sometimes called, has two operating modes. In one mode the switch is closed and the capacitor charges to the input voltage. The second mode occurs when the switch is opened and the capacitor holds this charge for a specified period of time.

The speed of a sample and hold circuit is directly related to the switching device used and the output amplifier. This characteristic of a sample and hold circuit is called the acquisition time. It is defined as the time required following a "sample" command, for the output to reach its final value. The acquisition time includes the switch delay time, the time constant of the switch on resistance and hold capacitor ($T = R_{ON}\,C_{HOLD}$), and the slew and settling times of the output amplifier.

The photographs shown in Fig. 3 illustrate the improvement in the acquisition time possible by using the HI-201HS. The first photograph represents the sample/hold circuit using a standard 201 switch and an HA-5100 operational amplifier. The first waveform is the "Sample" voltage (V_A). The second waveform is the voltage on the hold capacitor (V_1). And the third waveform is the output of the amplifier (V_2).

The second photograph is the same circuit with a HI-201HS and on HA-5160 op amp. Comparison of the photographs shows the HI-201HS has significantly reduced the switch delay time and the high slew rate of the 5160 amplifier has also contributed to the reduced acquisition time.

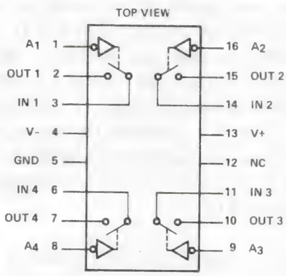
A source of error in this circuit is a d. c. offset which is called sample to hold offset error. This error is

primarily due to the charge injection (Q) of the switch and is related to the hold capacitance by the following expression,

$$\text{offset error } (V_O) = \frac{\text{charge transfer (Q).}}{C_H}$$

The reduced charge injection of the HI-201HS (typically 10 pc) will result in immediate reduction of this error.

Using analog switches with operational amplifiers is common in circuit design. An example is shown in Figure 4 which is an integrator with start/reset capability.

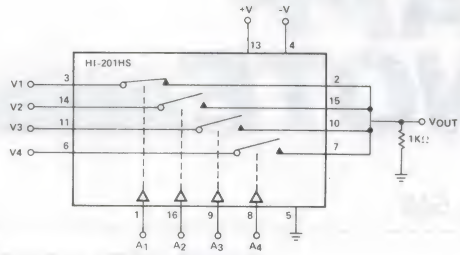


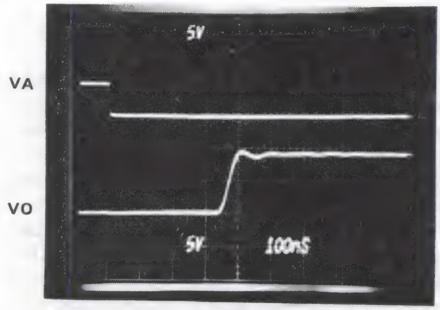
LOGIC	SWITCH
$0 - V_{AL} \leq .8V$	ON
$1 - V_{AH} \geq 2.4V$	OFF

TYPICAL SPECIFICATIONS (±15V Supply)

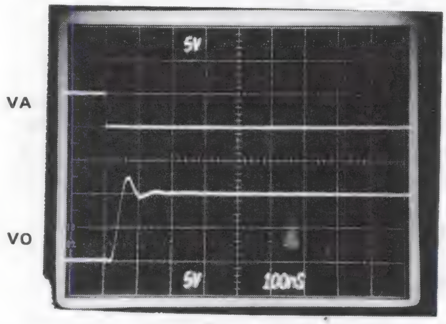
Analog Signal Range	±15V
On Resistance	30Ω
Off Leakage	.3nA
Switch On Time	30ns
Power Dissipation	120mW

Figure 1. Typical Pinout and Specifications – The HI-201HS is pin compatible with standard 201's and offers improved performance. Specifications given are typical values at T_A = 25°C.





(a)



(b)

Figure 2. High Speed Analog Multiplexer: (a) circuit response using the standard 201 (T_{access} = 400ns) (b) circuit response using HI-201HS (t_{access} = 50ns). The access time is defined as total time required to activate an "off" switch to the "on" state. Access time is normally measured from the initiation of the digital input pulse (V_A) to the 90% point of the output transition.

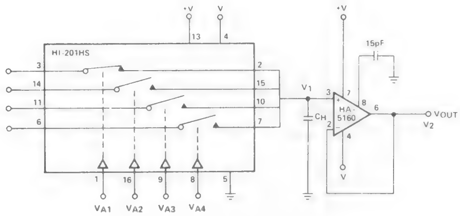


Figure 3A. High Speed Sample and Hold: The basic sample and hold samples the input voltage when the switch is closed and the capacitor holds the voltage when the switch is open. The speed of the switching element affects the speed of the sample and hold.

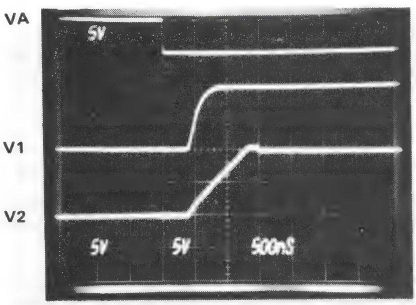


Figure 3B. Circuit response to a "Sample" command using a standard 201 and an HA-5100 operational amplifier (Acquisition time = 1.5μs)

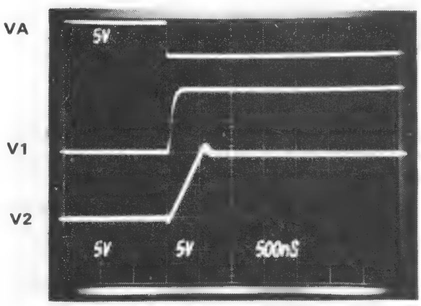


Figure 3C. Circuit response using an HI-201HS and HA-5160: HI-201HS significantly reduces switch delay time. (Acquisition time = 500ns)

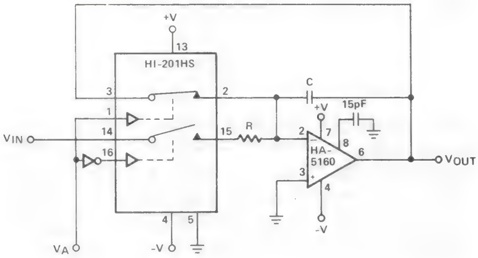


Figure 4A. Integrator with Start/Reset: A low logic input pulse disconnects the integrator from the analog input and discharges the capacitor. When the logic input changes to a high state, integrator is activated.

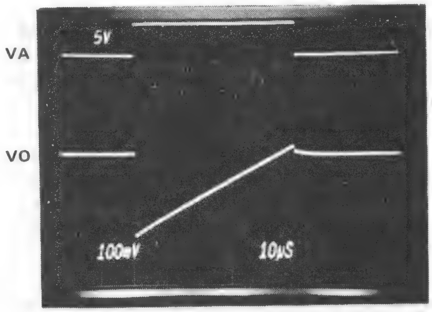


Figure 4B. Low Level Integration— Circuit response using standard 201 switch.

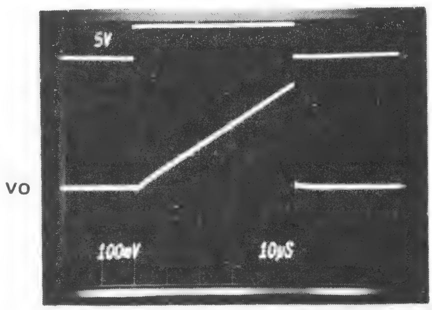


Figure 4C. Low level integration—Circuit response illustrates improved charge injection of the HI-201HS.

The switch is used to apply the input signal and to reset the integrator. Applying a low logic level removes the input signal and the capacitor is discharged. When a logic level high is present, the input signal is integrated with a rate of change equal to

$$dvo/dt = \frac{i_f}{C_f} = \frac{-V_i}{R_1 C_f}$$

The reduced on resistance, leakage current, and charge injection of the HI-201HS will improve the performance of this circuit and an example of this improved peformance can be seen in the photographs in Figure 4. These photographs illustrate the reduced charge injection which the 201HS offers. The component values are R_1 = 1MΩ , C = 150pF and V_{IN} = -1V. With these values, the amplifier will integrate the input signal with a slope of 6.6mv/μ s. For a 50 μs time period, the amplifier will integrate to a magnitude of ≈ 300mV. The photographs of the test results indicate this to be true, but it should be apparent that the two photographs are quite different. The first photograph represents the amplifier output using a standard 201 as the reset switch. The second photograph is the same circuit with a 201HS.

The offset error in the first photograph is due to the charge injection of the switch. Using the expression Q = V x C and knowing the standard 201 has a typical charge transfer of 30pc, this offset can be calculated. V = Q/C = 30pc/150pf=200mV.

Other examples of combining switches and amplifiers are shown in figures 5 and 6. In both these applications the switch is used to tailor the amplifiers performance. Figure 5 is a low pass filter with a selectable break frequency.

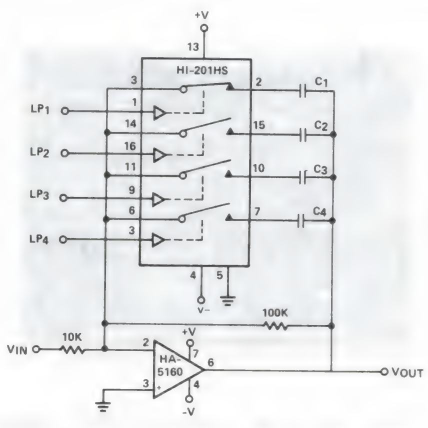


Figure 5. Low Pass Filter with Selectable Break Frequency— Switch selection places various values of capacitance in parallel with the feedback resistor. The value of the capacitor determines the break frequency. The break frequency is that frequency at which the signal begins attenuation.

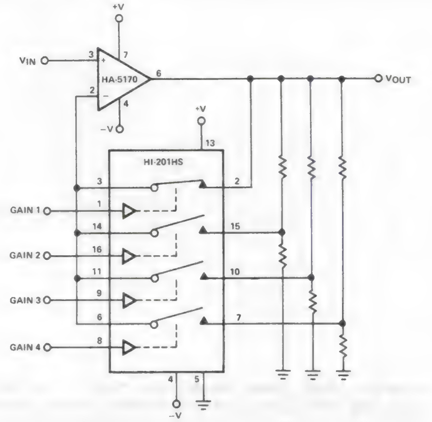


Figure 6. Amplifier with Programmable Gain— Switch selection activates a new voltage gain which is determined by the resistive feedback.

Depending on which switch is selected, a particular cutoff frequency is introduced by the expression,

$$F_C = \frac{1}{2\pi R\, C_x}$$

A programmable gain amplifier is shown in Figure 6. Similar in function to the filter application, the gain of the amplifier is determined by selection of a switch.

When using switches with other components it is important that a switch be selected which introduces a minimal amount of error to the circuit. Operational amplifier gain error due to high on resistance or offset voltages due to excessive leakage current and charge injection are examples of potential error created by the switch. The previous applications have demonstrated that the 201HS offers improved performance by minimizing circuit error and increasing system speed.

On The Drawing Board

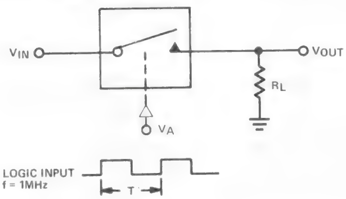
Since the introduction of the HI-201HS switch, many engineers have expressed an interest in using this new product. Although much of their work is in a preliminary stage and they do not want to divulge exact details on their designs, the following information is intended to give you an idea of how other engineers are considering using the HI-201HS.

The majority of the engineers are interested in taking advantage of the products fast switching speed. One particular engineering group is investigating replacement of DMOS (double-diffused MOS) transistors with the HI-201HS.

The DMOS transistor is capable of extremely fast switching speeds (1ns) and until now, switches

fabricated using CMOS technology have not been fast enough to be considered. But the HI-201HS is attractive since it offers unprecedented switching speed along with the established benefits of CMOS technology. Such benefits include a wider analog signal range capability and lower operating power requirements.

A common application for analog switches is time division multiplexing, where many signals are processed on a single channel. High speed switching allows higher information capacity on the channel, since the switching speeds of an analog switch are directly related to the maximum switch activation frequency. The faster a switch can turn on and off, the higher the possible switching frequency. An example of this relationship is shown in Figure 7. If a switch is activated at a frequency of 1MHz, it must turn on and off within a 500ns time period. Since the HI-201HS has a maximum on and off times of 50ns, and can turn on and off within a 100ns time period, it theoretically possible that it can be activated at a 5MHz frequency rate. This improved capability is making the HI-201HS an attractive component to design engineers requiring high frequency data processing. Conversations with engineers indicates that possible applications are computer graphics and visual display circuit designs.



$$T = 1/f$$
$$T = 1/10^6$$
$$T = 10^{-6}\ \text{sec} = 1\ \mu s$$
$$\frac{T}{2} = 500\text{ns}$$

Figure 7. High Frequency Switching — HI-201HS fast switching times allow it to transfer data at a higher rate of frequency.

Another area where the HI-201HS is generating interest is in the area of medical electronics. This is a growing field and improvements are continously being made as products become available much of the medical equipment being designed requires both high speed and accuracy.

Medical test equipment is primarily used to transmit or receive information from the patient. An example where both these functions are used is in the area of ultrasound. Ultrasound testing requires that a signal be transmitted to the patient and the return signal is then amplified and displayed or recorded. The 201HS is being considered for the use in such an application and would be used to control the transmission and reception of these signals.

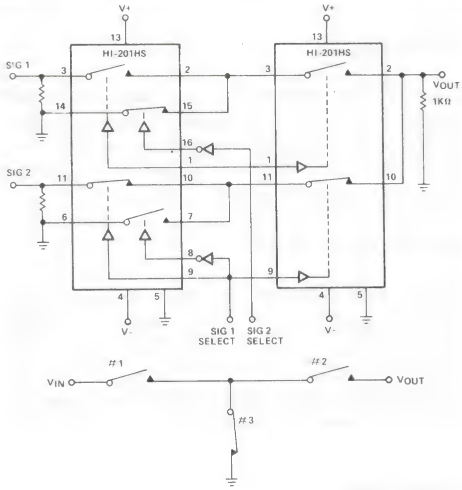


Figure 8. Video Switching with Improved Isolation— Improved high frequency off state performance is obtained by using a T-Switch configuration. When two series switches are off, the third switch is shorted to ground.

The designers are not only interested in fast switching speed, but also in low on resistance. This is an important aspect of the switch since many of the electrical signals in medical electronics are of a small magnitude. An example is patient monitoring equipment which converts physiological parameters into electrical signals. If these low level electrical signals require switching before amplification, a low on resistance switch is essential to minimize the voltage drop across the switch itself. The low on resistance of the HI-201HS enables it to be used in applications using signals of smaller magnitude.

Video circuit design involves the control of high frequency signals. Applications which require the switching of these high frequency signals are usually limited by the off isolation and crosstalk performance of the switch. Off isolation is defined as the amount of feedthrough of an applied signal through an off switch. Crosstalk is the amount of cross coupling of an "off" channel to the output of an "on" channel. Both of these switch characteristics will degrade as the frequency of the input signal increases.

The HI-201HS has some improvement over the standard 201 in these areas but the configuration shown in Figure 8 is being used by designers to improve the isolation capabilities of CMOS analog switches. This configuration is known as "T" switching since the three switches used for passing the signal could be thought of in the shape of the letter T. The simplified figure shows that when switches # 1 and # 2 are off, switch # 3 is tied to ground. When switches #1 and #2 are on, #3 is off. This improves isolation by having two channels in series off and any feedthrough is fed to ground.

Conclusion

The HARRIS HI-201HS is the fastest monolithic CMOS analog switch available. It offers improved performance for existing designs and should be considered for use in any application where switching speed is an important criteria.

ACKNOWLEDGEMENTS

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Appendix I–INSIDE THE HI-201HS

The HI-201 is a TTL compatible quad CMOS analog switch which features switching times under 50ns and a typical "on" resistance of 35Ω. The fast switching times are achieved through a combination of process and circuit design techniques. The HI-201HS is fabricated using a dielectric isolation process with complementary PNP and NPN bipolar transistors and polysilicon-gate CMOS. The use of bi-technology process enabled a unique circuit called a D. C. Static Level Shifter to be designed.

The typical CMOS analog switch consists of a switch cell which is driven by a level shifter. The level shifter converts a single logic input into two complementary outputs which drive the gates of the CMOS switch cell (Fig. A). The switch cell represents a capacitive load to the level shifter, so fast switching times require large drive currents to charge these capacitances quickly. The D. C. Static level shifter circuit (Fig. B) provides large drive currents only when switching and dissipates little power in a quiescent condition.

The D. C. static level shifter achieves high switching speeds through the use of a unique bipolar input stage and a network of switching and holding MOS transistors. Devices MN5, MP5, MN9 MP9 are the switching transistors and MN6, MP6, MN10, MP10 are the holding transistors. The major advantage of the bipolar input transistors is that its transconductance (g_m) is much higher than that possible with F. E. T. transistors.

To understand the level shifter operation, consider a change of logic input from low state to high. Initially V_A is low, $Q = Q_1 = Q' = -15V$ and $\overline{Q} = \overline{Q}_1 = \overline{Q'} = 15V$. VB is at ground and QN2, QP2 are off. When V_A goes high, QN2, QP2 turn on, which slew the gates of switching devices MN5, MP5 with a current $I = (V_A - 2V_{BE})/R$. The switching devices overcome the holding devices, MN10, MP10 and switch the internal nodes Q_1, and $\overline{Q}_1$. CMOS buffers I_{11}, I_{13} provide large drive currents to the switch cell, while inverters I_{12}, I_{14} provide delayed feedback signals. The feedback signals turn off holding devices MN10, MP10 while turning on holding devices MN6, MP6. The feedback also turns on QN2, QP2 by means of MN1, MP1. These feedback signals have returned the level shifter to a static condition by turning the bipolar input stage and MOS switching transistors off.

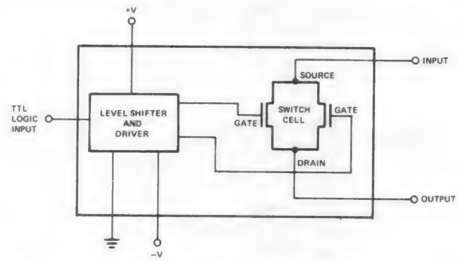


Figure A. Simplified I. C. Analog Switch Operation—Level Shifter converts logic input into drive signal for CMOS switch cell.

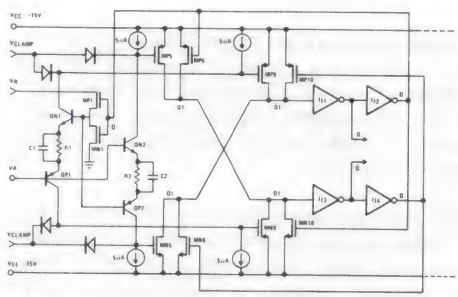


Figure B. Simplified D. C. Static Level Shifter — The level shifter consists of a unique bipolar input stage and a network of switching and holding devices.

Similar operation occurs when V_A goes from high to low, bipolar transistors QN1, QP1 turn on MN9, MP9. The feedback resets the holding devices and turns off the bipolar input stage.

Appendix II-HI-201HS vs. STANDARD 201

The use of a dual technology process and a creative design improves the performance of this analog switch. The following table illustrates the results of this combination by comparing the specification of the HI-201HS with the standard 201.

It should be apparent from Table 1 the substantial improvement in switching speeds offered by the HI-201HS. But since the switch "off" time of the high speed switch is measured differently from the standard 201, a brief discussion of test methods will avoid any confusion.

Figure A is a typical switching time test circuit for an analog switch. The "on" time is measured from the logic input to the 90% point of the output.

The "off" time can be measured from the logic input to either the 90% or 10% point of the output. This variation in the "off" time test point is due to the dependence of the measurement on the load. The dominant component of the switch "off" time is an exponential RC time constant determined by the values of the load resistance and capacitance. The "off" time of the HI-201HS is measured to the 90% point. The RC time constant due to load is excluded from this measurement. The photograph included in Figure A is a typical HI-201HS switching time response.

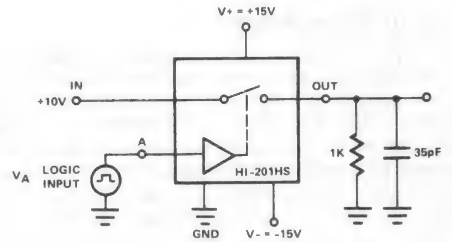
The remainder of table one compares other critical specifications of CMOS analog switches. The HI-201HS is not only a high speed switch but also offers improved performance in other areas. The parameters of "on" resistance, leakage current, and charge injection can all contribute unwanted errors to system level applications. With the improvements shown in these areas, the HI-201HS offers potential improvement in system accuracy for a wide variety of applications. and since the HI-201HS is pin compatible with existing 201's, the high speed version can be plugged into existing designs for immediate improvement in performance.

The HI-201HS is an improvement over the standard 201 in many areas, but some trade-offs still exist. One such trade-off was the power dissipation of the product. In order to meet the high speed criteria, larger internal currents are needed which in turn demand increased supply current. But this apparent shortcoming is more than offset by the products performance.

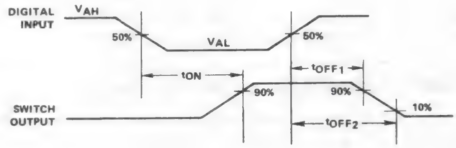
Parameter	Temperature	HARRIS HI-201HS	HARRIS HI-201
Switching Speed			
t_{ON}	25°	50ns	500ns
t_{OFF}	25°	50ns	500ns
ON Resistance	125°	75Ω	125Ω
Leakage Current			
I_{SOFF}	125°	100nA	500nA
I_{DOFF}	125°	100nA	500nA
Charge Injection			
Q	25°	10pc (typ)	30pc (typ)
Power Dissipation			
Pd	125°	240mw	60mw

Table 1. Specification Comparison: Improved performance of HI-201HS over standard 201's (all values are maximums unless stated otherwise).

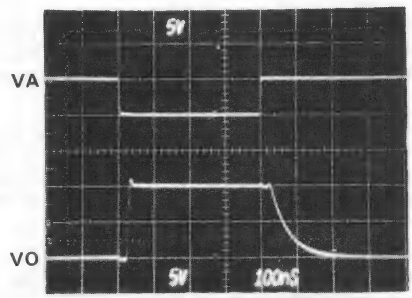
SWITCHING TEST CIRCUIT (t_{ON}, t_{OFF})



(a)



(b)



(c)

Figure A. Switching Time Test Circuit: (a) Switching test circuit, (b) Switching waveforms, (c) Typical HI-201HS response.

10

APPLICATION NOTES

APP NOTE

FOR YOUR INFORMATION

No. 544 February 1988

Harris Analog

MICROPOWER OP AMP FAMILY HA-5141/42/44 AND HA-5151/52/54

Russell Leath and Richard Whitehead

Introduction

Offering the best speed power product of any low power operational amplifier available, the HA-514X/515X can be effectively utilized in a wide variety of portable system applications. The features available from this family of devices can be easily incorporated into dictation equipment, medical monitoring systems, remote electronic sensors and other system designs.

Low or Micropower?

Actually, the HA-5141/42/44 operational amplifiers are micropower devices. That is, they consume microwatts of power (250μW typ.) as opposed to low power devices which consume 1 to 10mW. This exceptionally low power consumption however does not compromise the speed and flexibility of this family of amplifiers. Table 1 lists the speed/power relationships of some amplifiers in this class. The industry standard 741 was listed to show that HA-5141 has more speed for a fraction of the power consumed. A brief discussion concerning how the HA-514X/515X achieves this unique relationship can be found in the inset below.

For highest speed for power consumed, HA-5141 is a factor of 10 better than the nearest device, and the HA-5151 is six times better than the HA-5141.

Part Number	Power Dissipation	Slew Rate	Full Power Bandwidth	Gain Bandwidth
HA-5141	250μW	1.5V/μs	60KHz	400KHz
RC4132	250μW	0.13V/μs	5.5KHz	150KHz
OP-20	275μW	0.02V/μs	0.9KHz	100KHz
HA-5151	1000μW	4.5V/μs	95KHz	1300KHz
LM1OC	2000μW	0.11V/μs	5.5KHz	80KHz
LM741	8000μW	0.7V/μs	20KHz	1500KHz

TABLE 1. SPEED/POWER RELATIONSHIPS

Dual or Single Supply

Enhancing the micropower consumption and speed capabilities of the HA-514X/515X is its ability to operate over a wide range of supplies. It can be operated in double supply mode from $\pm$15V down to $\pm$1.5V or in single mode from +30V down to +3V. The quiescent supply current remains nearly constant over the entire supply range making it most suitable for operation in battery powered systems. The HA-514X family requires only 60μA/amp, and the HA-515X family requires only 200μA/amp for typical quiescent operation.

Making the Most of Micro Amps

To achieve high slew rate while requiring only microamps to operate, the HA-514X/515X designs utilizes a current amplifying front end. As can be seen in the simplified schematic under zero signal conditions, current source I_1 flows through D_1 and P_1 while I_2 flows through D_2 and P_2. This flow sets up a DC bias current of I_1 and I_2 through N_1 and N_2. This bias current is slightly higher with the HA-515X family and therefore allow a faster response time.

Under small signal conditions, the cross coupling of N_1 to P_2 and N_2 to P_1 establishes small signal currents i_1 and i_2 through collectors of N_1 to P_2 and N_2 and P_1 respectively. This differential current (i_1-i_2) is similar to a standard differential pair and is given by;

$$i_1 - i_2 = gm \text{ where } gm = f\ (hib)$$

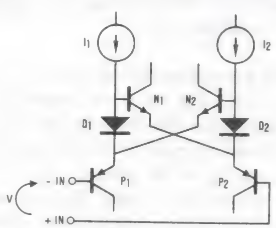
However, under large signal inputs and unlike the standard differential pair, the maximum differential current is not limited by the DC biasing current sources. The maximum slewing current is limited only by the β of N_1 and is orders of magnitude larger than the DC biasing current.

For a standard differential pair under large signal conditions the differential current is given by;

$$i_1 - i_2 = I_1 \tanh V \text{ and } i_1 - i_{2max} = 2I_1$$

But for the HA-514X/515X the large signal differential current is; $i_1 - i_2 = I_1(e^{v/vt} - e^{-v/vt})$

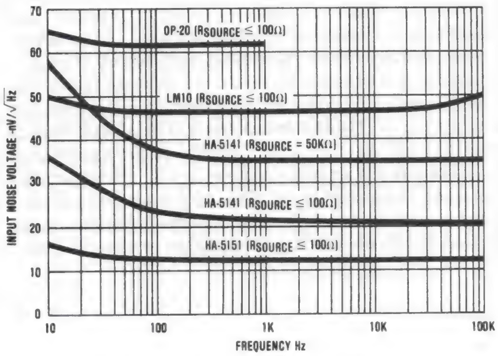
and i_1-i_2 increases exponentially until limited by β_{N1}. The HA-514X/515X design utilizes two gain stages which allows for high DC gain at lower collector impedance levels. These lower impedance levels permit unstacked device design which allows for lower operating voltage levels.



HA-514X/515X CURRENT AMPLIFYING FRONT END

Noise Parameters Also Attractive

With rugged bipolar construction combined with the dielectric isolation technology, the HA-514X/515X design maintains noise characteristics comparable to amplifiers requiring much higher supply currents. The noise curves compare the HA-514X/515X with other amplifiers in its class. It is readily observed that the HA-5141 has lower noise components even with higher source impedances. With typical noise values of $23nV/\sqrt{Hz}$ and $0.03pA/\sqrt{Hz}$ at 1KHz this device family is very "user friendly" to the portable system designer. As shown, the HA-5151 has even lower noise.



NOISE CURVES COMPARING HA-5151 WITH OTHER AMPLIFIERS

Other Useful Qualities

When operated in single supply mode this family of amplifiers is capable of output voltage swings from 0V to V(+) -1 Volt while sourcing 3mA output current. Their common range under single supply conditions is 0V to V(+) -1V. These qualities coupled with 60KHz full power bandwidth and 0.4MHz small signal bandwidth further widens the application range of the HA-5141/42/44. The HA-5151/52/54 is even more versatile with 1.3MHz small signal bandwidth and 95KHz full power bandwidth.

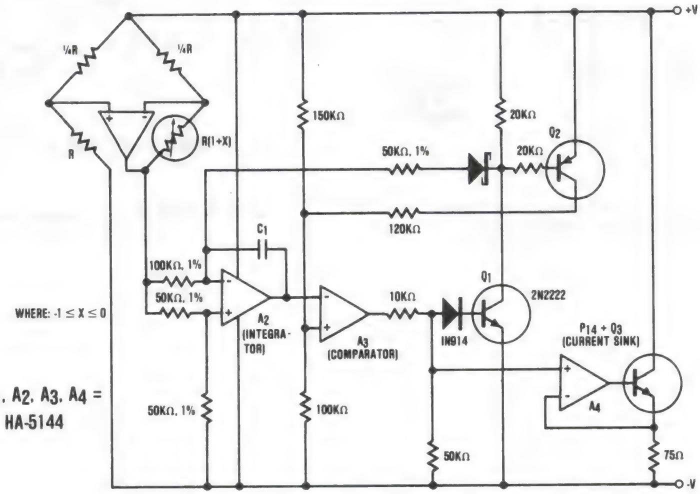
Applications

The flexibility and inherent qualities of the HA-514X/515X are most suitable for battery operated and/or low voltage systems such as remote electronic sensors or solar operated designs. The following applications are just a few of the many possibilities which can best utilize this amplifier's capabilities.

APPLICATION 1—REMOTE SENSOR LOOP TRANSMITTER

This circuit shows amplifier A_1 as a sensor amplifier in abridge configuration. Amplifiers A_2 and A_3 are configured as a voltage to frequency converter and A_4 is used as the transmitter. This entire sensor/transmitter can be powered directly from a 4 to 20mA current loop.

The bridge configuration produces a linear output with respect to the changes in resistance of the sensor. The voltage at the output of A_1 causes the integrator output A_2 to ramp down until it crosses the comparator threshold voltage of A_3. A_3 turns on Q_1 and Q_2. Q_1 causes the output of A_2 to ramp up at a rate nearly equal to its negative slope while Q_2 provides hysteresis for the comparator. In addition, Q_1 and Q_2 help eliminate changes in power supply (loop) voltage. Amplifier A_4 and Q_3 are configured as a constant current sink which turns on when the comparator goes "high". The resulting increase in loop current transmits the frequency of the V to F converter back to the control circuitry.



A1, A2, A3, A4 = ¼ HA-5144

REMOTE SENSOR — CURRENT LOOP TRANSMITTER

APPLICATION 2—CHARGE POOL POWER SUPPLY

It is usually desirable to have the remote transmitter of a 4 to 20mA current loop system powered directly from the transmission line. In some cases this is not possible due to high power requirements set by the remote sensor/-transmitter system. In these cases an alternative to the separate power supply is still possible. If the remote transmitter can be operated in a pulsed mode where it is active only long enough to perform its function, then a charge pool power supply can still allow the transmitter to be powered directly by the current loop. In this circuit a constant current I_1 is supplied to the charge pool capacitor (CP) by the HA-5141 (where I_1 = 3mA). The voltage V_1 continues to rise until the output of the HA-5141 approaches +Vs or the optional voltage limiting provides by Z_2. The LM2931 voltage regulator supplies the transmitter with a stable +5V supply from the charge collected by CP. Available power supply current is determined by the duration, allowable voltage droop on Cp, and required repetition rate. Example: If V_1 is allowed to droop 4.4V and the duration of operation is 1msec, the available power supply current is approximately

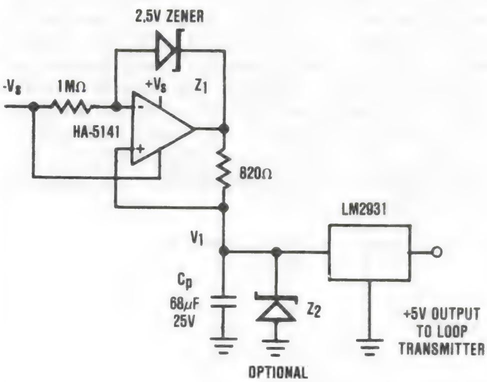
$$I_{ps} = C_p \frac{dV1}{dt} = 68\mu F \bullet \frac{4.4V}{1msec} = 30mA.$$

The repetition rate of operation is determined by the time required for the 3mA constant current source to restore V_1 to its previous value. In this example:

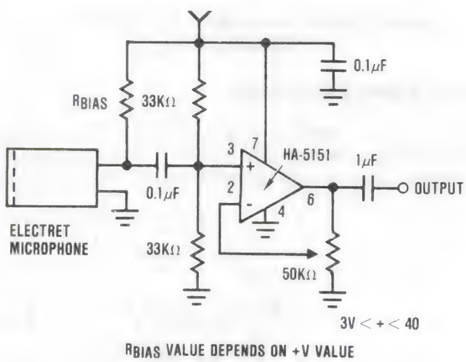
$$t = 68\mu F \bullet \frac{4.4V}{3mA} = 100msec \text{ is required.}$$

APPLICATION 3—LOW POWER MICROPHONE AMPLIFIER

The HA-515X op amp is very well suited for use in audio applications which require high gain, bandwidth and speed at low voltages and with low power consumption. Requirements such as these are usually found in battery, telephone line or solar powered circuits. The circuit below shows how the HA-5151 may be used to amplify the audio signal from an Electret microphone. This circuit may be operated with a single power supply voltage as low as 3V or as high as 40V and can provide over 25dB of gain over the audio frequency range. The 4.5V/μsec slew rate and low noise of the HA-5151 provides low distortion operation while only consuming about 200μA of supply current.



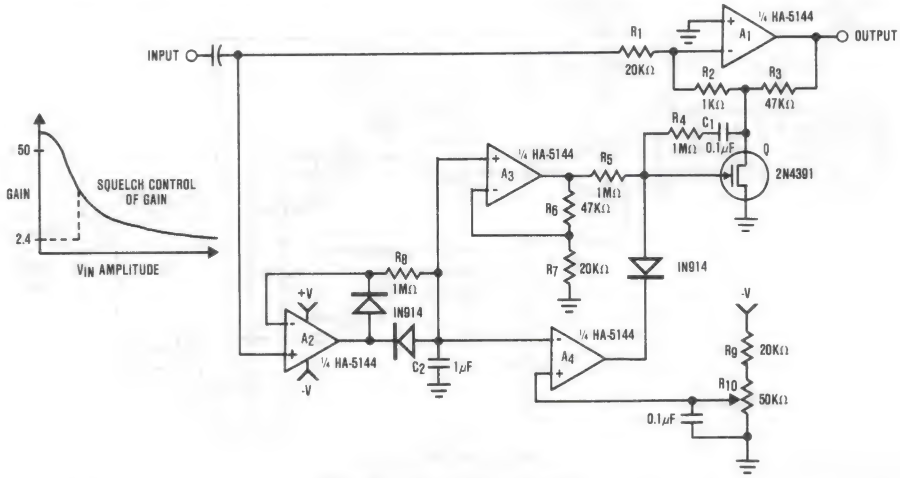
CHARGE POOL POWER SUPPLY FOR PULSED LOAD 4-20mA LOOP TRANSMITTER



LOW POWER MICROPHONE AMPLIFIER

APPLICATION 4—AGC WITH SQUELCH CONTROL

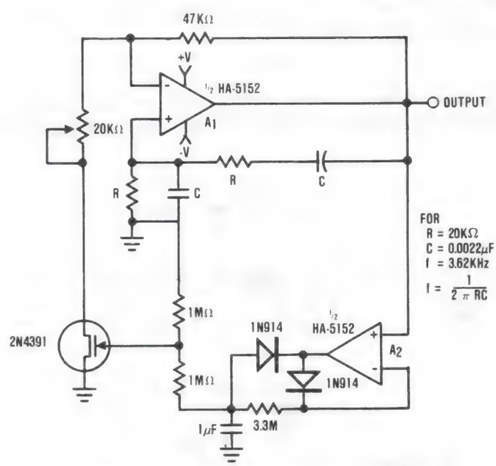
Automatic gain control is a very useful feature in a number of audio amplifier circuits such as tape recorders, telephone speaker phones, communication systems and P.A. systems. The circuits shown below consists of a HA-5144 quad op amp and a FET transistor used as a voltage controlled resistor to implement an A.G.C. circuit with squelch control. The squelch function helps eliminate noise in communications systems when no signal is present and allows remote hands free operation of tape recorder systems. Amplifier A_1 is placed in an inverting gain T configuration in order to provide a fairly wide gain range and to keep the signal level across the FET small. The small signal level across the FET and the addition of resistors R_5 and R_6 help reduce nonlinearities and distortion. Amplifier A_2 acts as a negative peak detector to keep track of signal amplitude. Amplifier A_3 may be used to amplify this peak signal if the cutoff voltage of the FET is higher than desired. Amplifier A_4 acts as a comparator in the squelch control section of the circuit. When the signal level falls below the voltage set by R10 the gate of the FET is pulled low turning it off completely and reducing the gain to 2.4. The output A_4 may also be used as a control signal in applications such as a hands free tape recorder system.



AGC WITH SQUELCH CONTROL

APPLICATION 5—LOW VOLTAGE WEIN BRIDGE OSCILLATOR

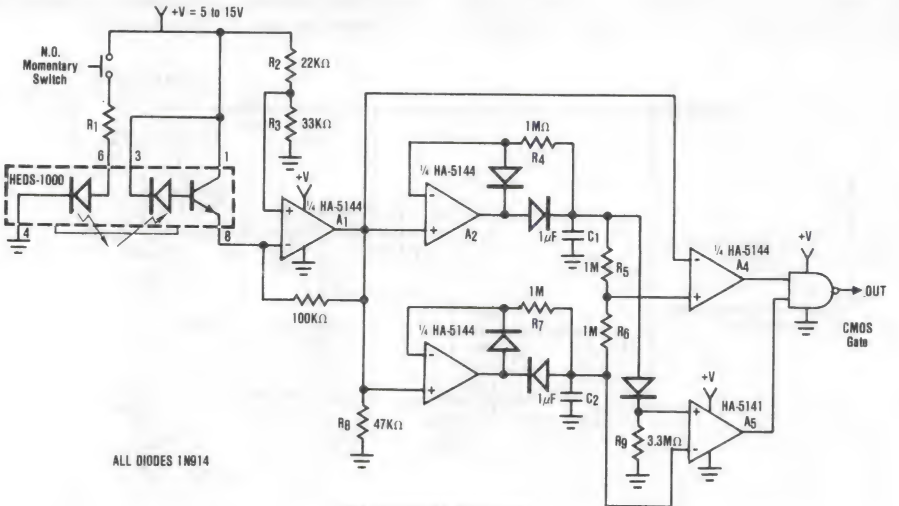
The circuit shown to the right utilizes a HA-5152 dual op amp and FET to produce a low voltage, low power Wein Bridge sine wave oscillator. Resistors R and capacitors C control the frequency of oscillation while the FET, used as a voltage controlled resistor, maintains the gain of A_1 at exactly 3 to sustain oscillation. The 20K pot may be used to vary the signal amplitude. The HA-5152 has the capability to operate down to ±1.5V supplies and this circuit will produce a low distortion sine wave output while drawing only 400μA of supply current.



LOW VOLTAGE WEIN BRIDGE OSCILLATOR

APPLICATION 6—BAR CODE SCANNER

The circuit shown below illustrates a method of interfacing a HEDS-1000 emitter-detector pair with a HA-5144 for use as a bar code scanner circuit. The HA-5144 is used as an amplifier system which converts the bar and space widths of the printed bar code into a pulse width modulated digital signal. Amplifier A_1 is used to amplify the current output of the detector. The output of A_1 is passed to two precision peak detector circuits which detect the positive and negative peaks of the received signal. Amplifier A_4 is used as a comparator whose reference is maintained at the midpoint of the peak to peak signal by resistors R_5 and R_6. This provides a more accurate edge detection and less ambiguity in bar width. Amplifier A_5 is used as an optional noise gate which only allows data to pass through the gate when the peak to peak modulation signal is larger than 1 diode drop. This circuit is operated by a single supply voltage with low power consumption which makes it ideal for battery operated data entry systems.



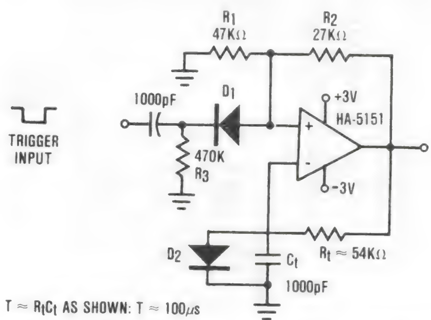
BAR CODE SCANNER

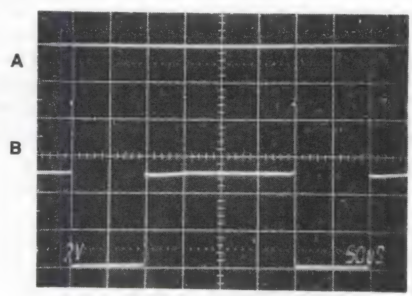
APPLICATION 7—MONOSTABLE MULTIVIBRATOR

The circuit below illustrates the usefulness of the HA-5151 as a battery powered monostable. In this circuit the ratio is set to .632, which allows the time constant equation to be reduced to:

$$T = R_tC_t$$

D_2 is used to force the output to a defined state by clampinng the negative input at +0.6V. Triggering is set by C_1, R_3, and D_2. An applied trigger pulls the positive input below the clamp voltage (+0.6V) which causes the output to change state. This state is held because the negative input cannot "follow" the change due to $R_t \bullet C_t$. As can be seen in the photograph, this particular circuit has a output pulse width set at approximately 100μs. Use of potentiometers for R_t and varible capacitors for C_t will allow for a wide variation in T.





SCALE: VERTICAL, A = 1V/DIV B = 2V/DIV
HORIZONTAL = 50μs/DIV

MONOSTABLE MULTIVIBRATOR

APPLICATION 8—AC COUPLED DYNAMIC AMPLIFIER

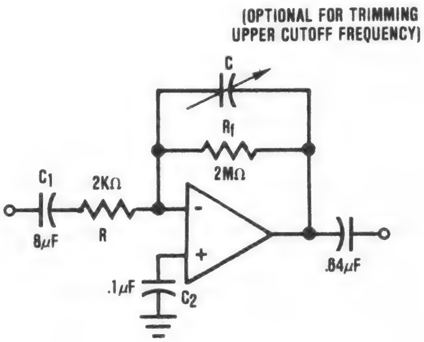
The circuit shown below is yet another of the many ways to utilize the advantages of HA-5141/42/44. This circuit would be most useful for biomedical instrumentation and acts as a bandpass filter with gain. Low frequency cutoff is set at 10Hz while the high frequency break point is given by the open loop roll off characteristic of the HA-5141/42/44. In this case, the A_{VCL} = -60dB where the rolloff occurs at approximately 300Hz. This corner frequency may be trimmed by inserting a capacitor in parallel with R_f.

Acknowledgements

A. Russell Leath of Georgia Institute of Technology — Engineering Experiment Station, Atlanta, GA., developed an evaluated the circuits in this Application Note.

B. Don Jones, Jon Dutra, and David Graen, Harris Semiconductor, Analog Division, Field Application Engineers provided inputs leading to the development of the circuits in this Application Note.

C. Gerry Cotreau, Harris Semiconductor, Analog Division, provided inputs involving operation of HA-514X/HA-5151X devices.



A.C. COUPLED DYNAMIC AMPLIFIER (A_{VCL} = -1000)

APP NOTE

FOR YOUR INFORMATION

No. 546

Harris Analog

A METHOD OF CALCULATING HA-2625 GAIN BANDWIDTH PRODUCT vs. TEMPERATURE

By: Carl Wolfe and John Prentice

Introduction

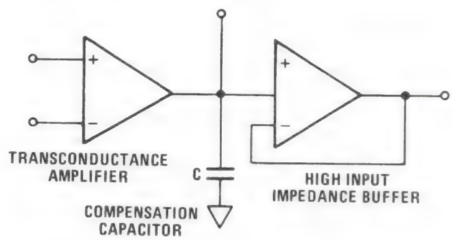
The job of the analog circuit designer would be simplified if all designs were intended to operate at a constant temperature. But since this is usually not the case, the majority of designs require that I.C. performance with respect to temperature be considered.

A common request for analog designers using the HA-2625 operational amplifier is information on the Gain Bandwidth Product (GBP) vs. Temperature. The GBP is defined as the product of the amplifier gain and bandwidth at a specified frequency. Knowledge of this operational amplifier characteristic with temperature provides insight into the amplifier's open loop frequency response variation with temperature.

The following information describes a method of calculating HA-2625 GBP vs. Temperature.

Procedure for Computing Gain Bandwidth Product

A simplified configuration of the HA-2625 op amp is shown in Figure 1. The gain of this operational amplifier over its intermediate frequency range can be expressed by Equation 1.



BENEFITS

- MORE TEMPERATURE-STABLE THAN MILLER INTEGRATOR TYPES
- AVAILABILITY OF HIGH IMPEDANCE INPUT FOR OUTPUT LIMITING

FIGURE 1. TYPICAL HARRIS OP AMP CONFIGURATION

$$A_V = \frac{g_m}{2\pi f C_C} \qquad (1)$$

$$\theta_V = \theta_{gm} - 90^o$$

where,

A_V = magnitude of voltage gain

θ_V = phase of voltage gain (-90^o due to C_C phase shift)

g_m = transconductance magnitude of op amp input stage

θ_{gm} = transconductance phase

f = bandwidth

C_C = compensation capacitance (includes internal and external capacitance)

Rewriting Equation 1, the GBP can be expressed as a function of transconductance.

$$GBP = A_V f = \frac{g_m}{2\pi C_C} \qquad (2)$$

Transconductance magnitude/phase characteristics vs. frequency and temperature are shown in curves 1 through 8. The GBP vs. temperature can be calculated by using Equation 2 and the given transconductance data.

As an example, let's calculate the variation of GBP over the temperature range of +25^{o}C to +75^{o}C. The operating frequency is given to be 100KHz and the external compensation capacitor is 50pF.

Before applying equation 2, both the transconductance magnitude and compensation capacitance values must be determined. Referring to curve 2, the transconductance magnitude for an ambient temperature of +25^{o}C and an operating frequency of 100KHz is 3.2×10^{-3} mmho.

The compensation capacitance value represents total capacitance. Therefore, in addition to the external capacitor component value, C_C should include an internal device capacitance of 3pF plus 5pF to account for fixture capacitance.

So by using values of $g_m = 3.2 \times 10^{-3}$ mmho and C_C = 50 + 2 + 5 = 57pF, the GBP is computed as follows:

$$GBP = \frac{3.2 \times 10^{-3}}{2\pi\,(57 \times 10^{-12})} = 8.94\text{MHz}$$

Next, the transconductance gain at +75°C (Curve 4) is determined to be 2.85×10^{-3} and, by applying Equation 2 once again, the calculation is:

$$GBP = \frac{2.85 \times 10^{-3}}{2\pi\,(57 \times 10^{-12})} = 7.96\text{MHz}$$

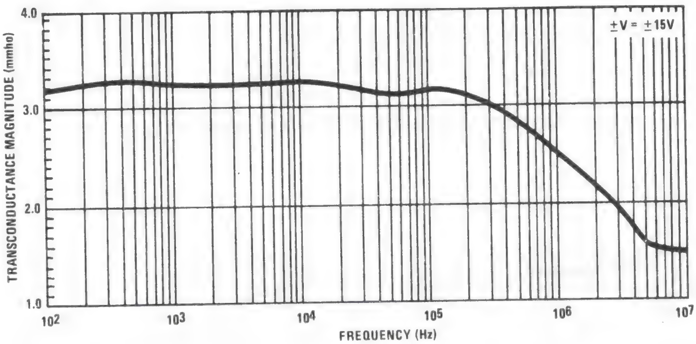
The variation of GBP vs. temperature for this example is:

$$\frac{8.94 - 7.96}{8.94} = 10.9\%$$

The above method applies only for the intermediate frequencies of the op amp since the gain becomes load dependent at both frequency extremes. This is due to the impedance of the op amp output stage being less than that of C_C at very high or very low frequencies.

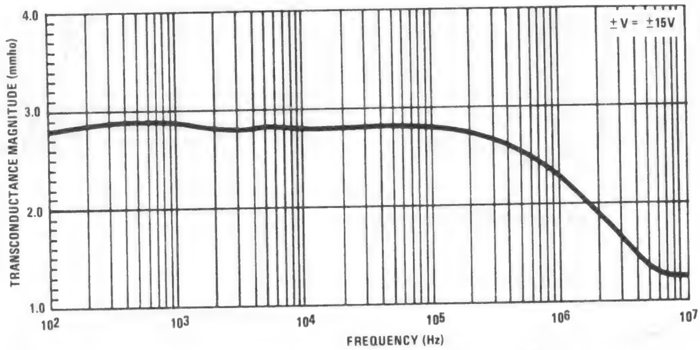
Finally, the transconductance curves provided are based on experimental data and should be considered as typical.

Curve 1



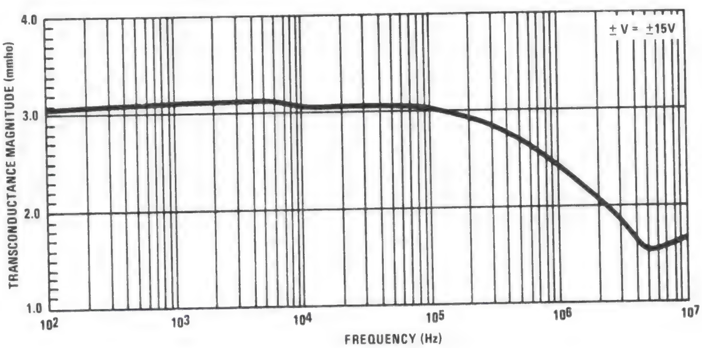
TRANSCONDUCTANCE MAGNITUDE vs. FREQUENCY T_A = 0°C

Curve 2



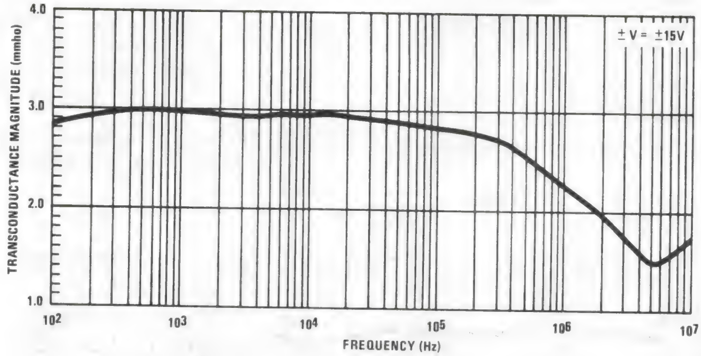
TRANSCONDUCTANCE MAGNITUDE vs. FREQUENCY T_A = +25°C

Curve 3



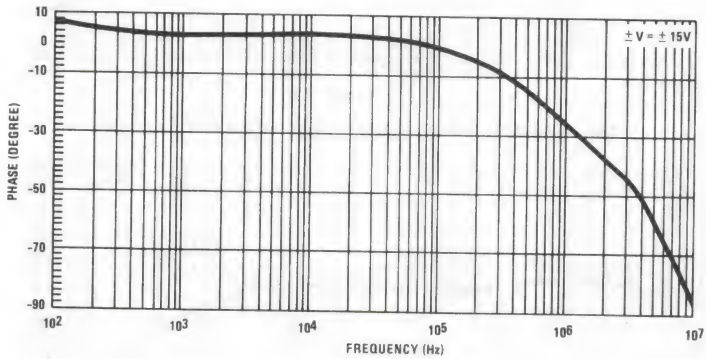
TRANSCONDUCTANCE MAGNITUDE vs. FREQUENCY T_A = +50°C

Curve 4



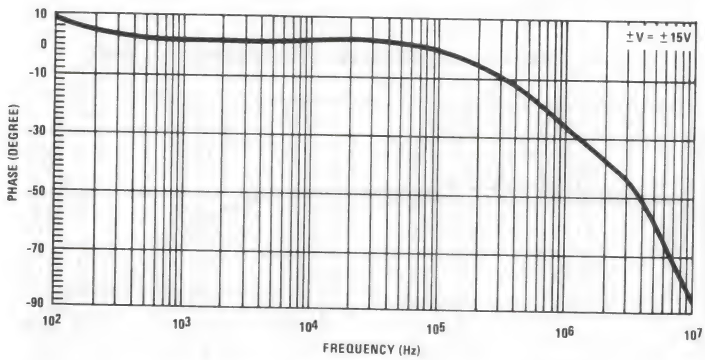
TRANSCONDUCTANCE MAGNITUDE vs. FREQUENCY T_A = +75°C

Curve 5



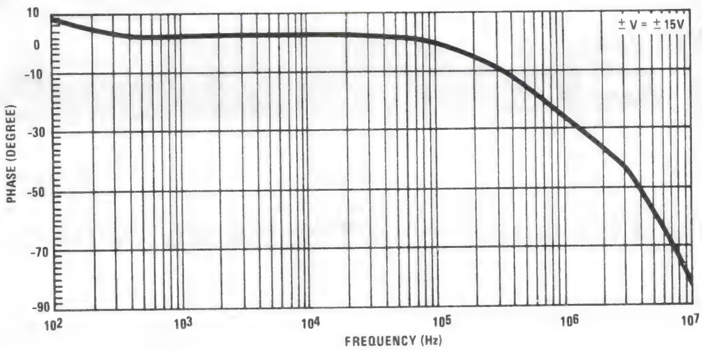
TRANSCONDUCTANCE PHASE vs. FREQUENCY T_A = 0°C

Curve 6



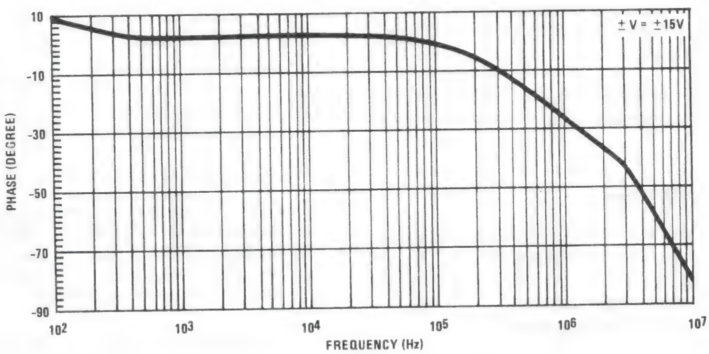
TRANSCONDUCTANCE PHASE vs. FREQUENCY T_A = +25°C

Curve 7



TRANSCONDUCTANCE PHASE vs. FREQUENCY T_A = +50°C

Curve 8



TRANSCONDUCTANCE PHASE vs. FREQUENCY T_A = +75°C

APP NOTE

FOR YOUR INFORMATION

No. 548

Harris Analog

A DESIGNERS GUIDE FOR THE HA-5033 VIDEO BUFFER

Carl Wolfe

Introduction

Harris Semiconductor is an industry leader in the high speed, wideband, monolithic operational amplifier market. Due to the high performance of Harris products, designers in the more specialized areas of electronics have shown interest in utilizing these products in their applications. One such area is video design. In an effort to address this market, Harris has introduced the HA-5033 video buffer.

This paper will discuss the HA-5033 design and provide additional performance characteristics not shown in the data sheet.

HA-5033 Description

The HA-5033 is a unity gain monolithic I.C. designed for any application requiring a fast wideband buffer. A voltage follower by design, this product is optimized for high speed 50Ω and 75Ω coaxial cable driver applications common in color video systems.

Critical performance characteristics are summarized in Table 1. Outstanding differential phase/gain characteristics combined with an output current capability of ±100mA makes the HA-5033 an excellent choice for the line driver applications required in video circuit design.

PARAMETER	MIN	TYP	MAX	UNITS
Input Offset Voltage			15	mV
Input Bias Current			35	μA
Differential Phase		.1		degree
Differential Gain		.1		%
Slew Rate (±15V)	1000			V/μS
Output Current		±100		mA
Bandwidth (small signal)		250		MHz
Bandwidth (V_{IN} = 1 V_{RMS})		65		MHz
Supply Current			20	mA

TABLE 1. HA-5033 SPECIFICATIONS: T_A = +25°C; $\pm V_{SUPPLY}$ = ±12V (UNLESS OTHERWISE SHOWN)

Other features, which include a minimum slew rate of 1000V/μs, make the HA-5033 useful in high speed A/D data conversion and sample/hold circuits.

The HA-5033 is offered in two package configurations, the T0-8 metal can and the 8 pin epoxy Mini-Dip. The pinouts for each package are illustrated in Figure 1.

TOP VIEWS

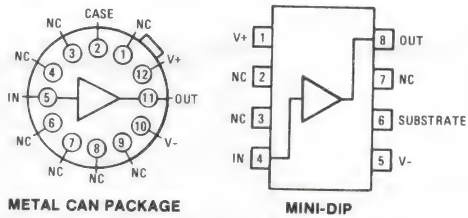


FIGURE 1. HA-5033 PINOUTS: T0-8 METAL CAN-PIN COMPATIBLE WITH THE LH0033 HYBRID. 8 PIN MINI-DIP - FABRICATED USING A COPPER LEAD FRAME. ADVANTAGES INCLUDE EXCELLENT THERMAL CHARACTERISTICS AND BOARD SPACE SAVINGS.

The high performance of this product (summarized in Table 1) is the result of the Harris High Frequency Dielectric Isolation Process. A major feature of this process is that it provides both PNP and NPN high frequency transistors which make wide bandwidth designs, such as the HA-5033, practical.

A Closer Look

Most manufacturer's data sheets provide a schematic diagram and depending upon the complexity of the product, this schematic may be comprehensive or possibly a simplified version. Schematics are a visual means of presenting information, ranging from reliability data, such as transistor counts, to circuit information for circuit analysis or computer simulation. But the most important reason for the schematic is to communicate to the customer the internal structure of the product and therefore, some insight into its operation.

At first glance, a schematic may appear as nothing more than a collection of resistors and transistors. But upon closer examination, particular areas of operation should become evident. Using the HA-5033 as an example (Figure 2), it will be shown that the HA-5033 consists of a signal path, bias network, and performance optimization circuitry.

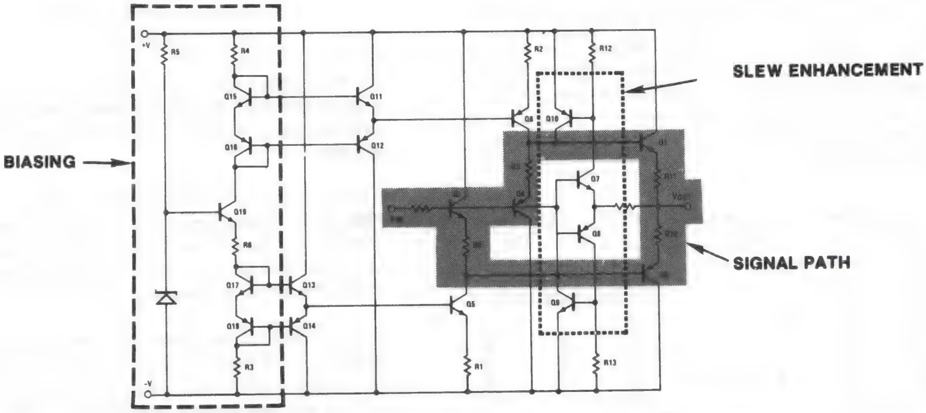


FIGURE 2. HA-5033 SCHEMATIC: VIDEO BUFFER DESIGN CONSISTS OF THREE OPERATING AREAS; SIGNAL PATH, BIAS NETWORK AND PERFORMANCE OPTIMIZATION CIRCUITRY.

Signal buffering is accomplished by cascading two emitter followers. In order to achieve symmetrical positive and negative output drive capability, two pairs are paralleled. The first pair consists of Q1 and Q4 for positive drive while the second pair Q2, Q3, provide negative drive. The emitter resistors of Q1, Q2 ensure stability with respect to load resistance, enhance differential phase/gain performance, and stabilize the quiescent operating point. This signal path has been high-lighted on the schematic.

The bias circuitry consists primarily of the diode-biasing located on the left portion of the schematic along with transistors Q5, Q6. This circuitry ensures the designed performance of the other active elements.

The performance optimization circuits are a slew enhancement circuit and a bias network buffer circuit. The transistors Q7, Q8, Q9 and Q10 are for slew enhancement. If the input voltage exceeds the output by one V_{BE}, Q7 will turn on Q10, which in turn provides extra base drive to Q1. Similary, Q9 will supply extra base drive to Q2.

Transistors Q11, Q12, Q13 and Q14 prevent high frequency or transient signals from affecting the bias circuitry. This prevents C_{CB} multiplication of current sources Q5 and Q6, which also improves differential gain/phase performance.

Note that output current limiting was not designed into the HA-5033. If there is a possiblity of the output being shorted to ground or the supplies, external current limiting will be necessary.

Any designer interested in using the HA-5033 should be aware of a characteristic related to output transistor operation. As the data sheet performance curves (reproduced in Figure 3) show, the output swing is a function of frequency. These curves show the point at

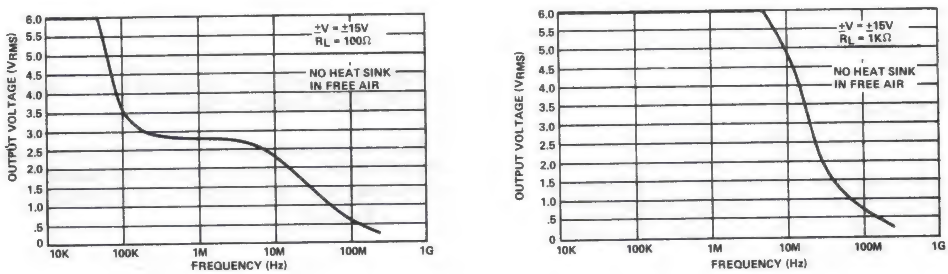
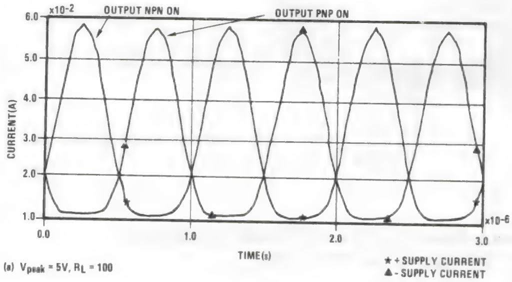


FIGURE 3. OUTPUT SWING VS. FREQUENCY PERFORMANCE CURVES: CURVES SHOW POINT OF OBSERVABLE DISTORTION FOR GIVEN FREQUENCY. OPERATION BEYOND THE CURVES SHOWN WILL APPROACH CONDITIONS WHERE OUTPUT TRANSISTORS ARE SIMULTANEOUSLY ON. THE RESULTING INCREASE IN CHIP TEMPERATURE WILL LEAD TO THERMAL RUNAWAY.

which observable distortion occurs for a given frequency. However, if the signal amplitude, signal frequency or both are increased beyond the curves shown, thermal "runaway" will occur. This is due to both the NPN and PNP output transistors approaching a condition of being simultaneously on. This condition has been computer simulated and the results are shown in Figure 4.



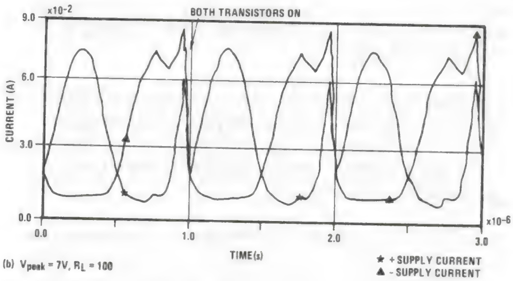


FIGURE 4. OUTPUT TRANSISTOR COMPUTER SIMULATION RESULTS

This condition occurs if the frequency of the analog signed does not allow sufficient time for the output PNP transistor to turn off. The frequency which causes this "push-push" output stage can be determined by using the following relationship,

$$\text{Full Power Bandwidth (FPB)} = \frac{SR}{2\pi V_p}$$

Where:
SR = Slew Rate
V_p = Analog Signal Peak Voltage

Therefore, the designer can determine the approximate frequency of thermal runaway by supplying the peak analog voltage and measuring the buffer slew rate for a particular application.

For example, the slew rate for the HA-5033 with a load of R_L = 1K ohm and C_L = 1000pFwas measured to be 83 V/μS. The FPB for a 5V peak analog signal was calculated,

$$FPB = \frac{83V/\mu S}{2\pi(5V)} = 2.6MHz$$

So the estimated frequency of thermal runaway for the given conditions is 2.6MHz. Measurements in the lab resulted in a thermal runaway frequency equal to 2.5MHz.

Although the FPB relationship gives the designer a method of estimating the frequency of thermal runaway, it is recommended that the HA-5033 be operated to the left of the curves shown in Figure 3. Heat sinking the buffer will not prevent this condition from occuring.

The purpose of heat sinking a semiconductor is to maintain the device junction temperature below a specified maximum limit. This is a thermal problem and can be evaluated using the thermal analog of Ohms Law illustrated in Figure 5.

Where:
P_{dmax} = Power Dissipated ($P_{DC} + P_{AC}$), Watts
T_j = Maximum Junction Temperature, ^oC
T_a = Ambient Temperature, ^oC
$\theta_{j\text{-}c}$ = Junction to Case Thermal Resistance, $^oC/W$
$\theta_{c\text{-}s}$ = Case to Heat Sink Thermal Resistance, $^oC/W$
$\theta_{s\text{-}a}$ = Heat Sink to Ambient Thermal Resistance, -C/W

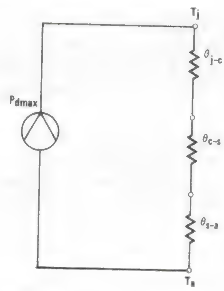


FIGURE 5. THERMAL ANALOG OF OHMS LAW: SEMICONDUCTOR /HEAT SINK SYSTEM

In this thermal system, current is replaced by power, voltage by temperature, and electrical resistance by thermal resistance. By using Figure 5, the following expression is derived,

$$P_{dmax} = \frac{T_{jmax} - T_A}{\theta_{j\text{-}c} + \theta_{c\text{-}s} + \theta_{s\text{-}a}}$$

This expression allows the designer to determine the maximum power dissipation of a semiconductor/heat sink system.

The expression for the semiconductor in free air is,

$$P_{dmax} = \frac{T_{jmax} - T_A}{\theta_{j-a}}$$

In order to make use of these expressions, the following information is required. θ_{j-c} and T_{jmax}, from the semiconductor manufacturer and θ_{c-s} and θ_{s-a}, from the heat sink manufacturer.

For the Harris HA-5033, the maximum junction temperature is $T_{jmax} = 200^oC$. The thermal impedances for the HA-5033 in the T0-8 metal can package are $\theta_{j-c} = 31^oC/W$ and $\theta_{j-a} = 99^oC/W$. The epoxy mini-dip thermal impedances are $\theta_{j-c} = 27^oC/W$ and $\theta_{j-a} = 90^oC/W$.

Recommended heat sinks for the HA-5033 in the T0-8 metal can package are the Thermalloy 2240A[1] and IERC-UP-T08-51CB[2] (base), IERC-UP-C7 (top). Thermal impedances are $\theta_{s-a} = 27^oC/W$ and $\theta_{s-a} = 10^oC/W$, respectively. θ_{c-s} is dependent upon the type of insulator or thermal joint compound used. Both products are two piece heat sinks, but differ in design.

By using the given product information and supplying an operating ambient temperature, the designer can determine the maximum power the system will dissipate and not exceed the maximum junction temperature.

For example, Figure 6 shows the maximum power dissipation for the HA-5033 in a T0-8 metal can package to be 1.75W at 25oC.

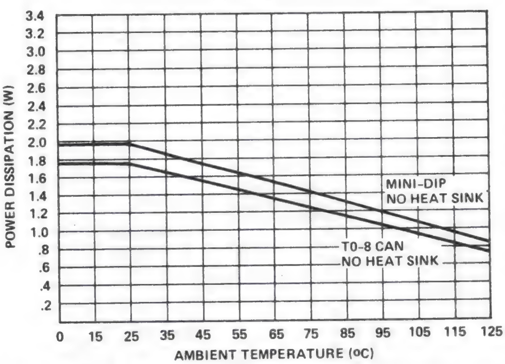


FIGURE 6. HA-5033 MAXIMUM POWER DISSIPATION VS AMBIENT TEMPERATURE: FREE AIR

The maximum power dissipation of the HA-5033/2240A heat sink system is calculated to be,

$$P_{dmax} = \frac{200-25}{31 + 27} = 3.01W$$

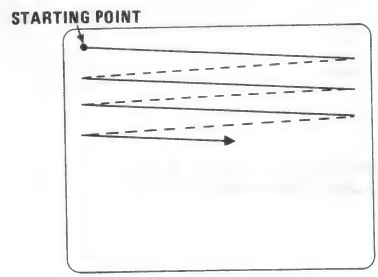
Therefore, the HA-5033 used with the Thermalloy 2240A can dissipate 3.0W at 25oC and not exceed the maximum junction temperature of 200oC.

The power dissipation limits shown in Figure 6 and those determined with the heat sink apply for both quiescent and load related power. Therefore,

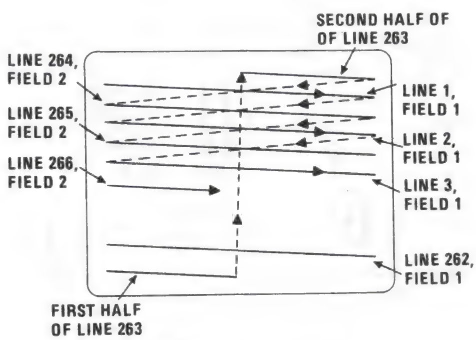
$$P_{dmax} > P_{DC} + P_{AC}$$
$$P_{DC} = (+V)(+I) + (-V)(-I)$$
$$P_{AC} = (1/T)\int_0^T v(t)\, i(t)\, dt$$

Video Performance

The images which appear on your television picture tube are created by a process called scanning[3]. Scanning is a method of recreating the optical image of a scene one line at a time. Referring to Figure 7a, an electron beam moves or "scans" from left to right and quickly returns to a position below its starting spot. This process continues until the bottom of the picture is reached and the beam returns to the original top left hand position. This method is called sequential scanning.



SEQUENTIAL SCANNING



INTERLACED SCANNING

FIGURE 7. SCANNING SEQUENCE

10

APPLICATION NOTES

Incorporated into present television broadcast standards is a technique called interlaced scanning. Interlaced scanning recreates the scene by providing two half scans. As shown in Figure 7b, the first scan traces out the odd numbered lines, the second scan fills in the even numbered lines. This technique avoids the flicker problem and excessive bandwidths required for similar picture definition using sequential scanning.

The United States NTSC (National Television Systems Committee) broadcast standard is a 525 line standard. Each scan consists of 262½ lines. The first scan is known as field one, the second, field two. Therefore, the complete picture consists of two fields.

The first 21 lines of each field are blank. Those lines are left open and are not used to broadcast video information. Instead, these lines contain other important information, such as sync pulses, data transmission, and test signals. The test signals contained in these lines are called the Vertical Interval Test Signals (VITS)[4,5], which allows real-time monitoring of the television broadcast signal quality. These test signals were used to evaluate the video performance of the HA-5033.

Four test signals are commonly used in the vertical interval. They are the multiburst, color bar, composite and vertical interval reference. These test signals are shown in Figures 8 through 11.

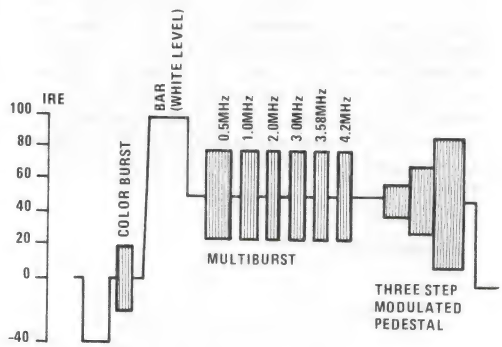


FIGURE 8. MULTIBURST SIGNAL (FIELD 1, LINE 17) ALLOWS FREQUENCY RESPONSE CHECKS

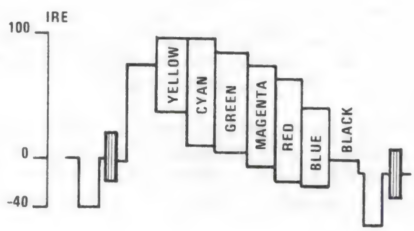


FIGURE 9. COLOR BAR (FIELD 2, LINE 17) ENABLES MONITORING OF COLOR TRANSMISSION QUALITY

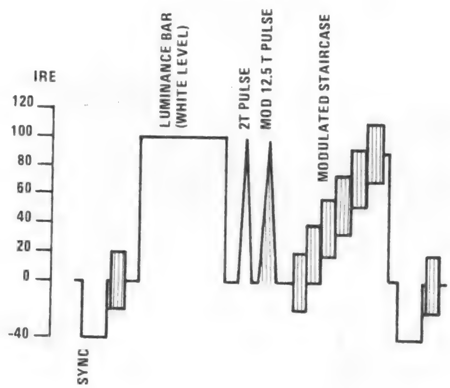


FIGURE 10. COMPOSITE SIGNAL (FIELD 1, AND 2, LINE 18) DESIGNED FOR GAIN AND TIME DELAY TESTS

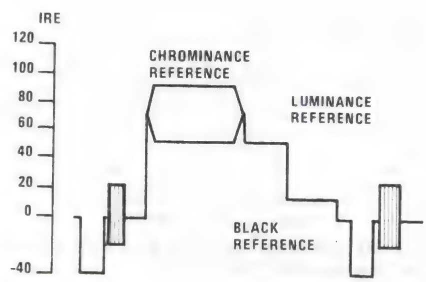


FIGURE 11. VERTICAL INTERVAL REFERENCE SIGNAL (FIELD 1 AND 2, LINE 19) PROVIDES COLOR AND GAIN REFERENCES

Each test signal was created to allow various distortions to be measured without interfering with the normal video transmission. These signal distortions which exist in television systems are defined as linear or non-linear. Non-linear distortion, such as differential phase and gain, vary with the amplitude of the picture signal. Linear distortions, usually dependent upon frequency response, are independent of signal level. For example, the multiburst test signal is very useful for frequency response checks, where as the composite signal contains signals for checking gain error.

Determining the HA-5033's performance level with respect to the NTSC standard required the definition of a measurement method. Test equipment was needed that would produce the necessary NTSC test signals and also monitor the device under test performance. The test configuration, shown in Figure 12 consisted of a Tektronix 149A NTSC[6] generator and Marconi TF 2914A video analyzer[7].

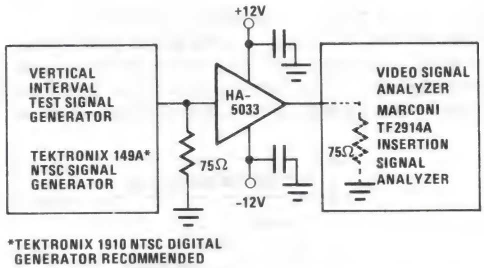


FIGURE 12. HA-5033 NTSC PERFORMANCE TEST CONFIGURATION

The TF 2914A has the capability of measuring 24 separate video parameters. Other advantages include direct readout and much more accuracy than possible using scope methods. Table 2 lists the video parameters tested on the HA-5033 along with the particular VITS utilized by the TF 2914A.

VIDEO PARAMETER	VERTICAL INTERVAL TEST SIGNAL USED
Luminance Bar Amplitude	Luminance Bar, Composite Signal (Fig. 10)
Sync Amplitude	Sync Pulse, Composite Signal (Fig. 10)
2T Pulse to Bar Ratio	2T Pulse/Luminance Bar, Composite Signal (Fig. 10)
Chrominance to Luminance Gain Inequality	Chrominance Component Amplitude of the 12.5T Pulse and Luminance Bar Amplitude, Composite Signal (Fig. 10)
Chrominance to Luminance Delay	Time Difference of Chrominance and Luminance Components of the 12.5T Pulse, Composite Signal (Fig. 10)
Luminance Non-Linearity	Largest and Smallest Step Amplitude of the Modulated Step Staircase, Composite Signal (Fig. 10)
Signal to Noise Ratio	Luminance Bar Level to Noise Voltage, Composite Signal (Fig. 10)
Chrominance to Luminance Crosstalk	Chrominance Component of 3 Step Modulated Pedestal and Luminance Bar, Multiburst Signal (Fig. 8)
Low Frequency Error	Amplitude of Low Frequency Signals
Bar Tilt	Difference of Luminance Bar Amplitude, Composite Signal (Fig. 10)
2T K Factor	2T Pulse, Composite Signal (Fig. 10)
Differential Gain	Amplitude Deviation of Modulated Step Staircase, Composite Signal (Fig. 10)
Differential Phase	Phase Deviation of Modulated Step Staircase, Composite Signal (Fig. 10)
Flag	Luminance Amplitude, Multiburst Signal (Fig. 8)
Multiburst 1-6	Amplitude of Each Frequency Burst, Multiburst Signal (Fig. 8)
Color Reference Burst Amplitude	Color Burst Amplitude, Multiburst Signal (Fig. 8)

TABLE 2. TF 2914A VIDEO MEASUREMENT PARAMETERS REFERRED TO VERTICAL INTERVAL TEST SIGNALS

Since the TF 2914A measurement includes any inaccuracies of the NTSC signal generator, a "delta" measurement was neccesary. The NTSC generator was connected directly to the analyzer and the results recorded. Next, the HA-5033 was inserted and the results recorded. The difference between the two readings was considered the actual HA-5033 performance. Table 3 lists the video performance results of the HA-5033.

VIDEO PARAMETER	HA-5033	UNITS
Luminance Bar Amplitude	93.6	IRE*
Sync Amplitude	37.5	IRE
2T Pulse to Bar Ratio	99.9	IRE
Chrominance to Luminance Gain Inequality	99.9	IRE
Chrominance to Luminance Delay	1.5	nS
Luminance Non-Linearity	0.1	%
Signal-to-Noise Ratio	66	db
Chrominance to Luminance Crosstalk	51.6	IRE
Low Frequency Error	0.3	mv
Bar Tilt	0.3	IRE
2T K Factor	0.1	K
Differential Gain	0.1	%
Differential Phase	0.1	degree
Flag	99.5	IRE
Multiburst 1 Amplitude	49.2	IRE
Multiburst 2 Amplitude	49.3	IRE
Multiburst 3 Amplitude	51.0	IRE
Multiburst 4 Amplitude	50.4	IRE
Multiburst 5 Amplitude	49.7	IRE
Multiburst 6 Amplitude	50.0	IRE
Color Reference Burst Amplitude	40.4	IRE

TABLE 3. HA-5033 NTSC VIDEO PERFORMANCE

* IEEE Standard 205-1958 defines the levels of television video signal in terms of IRE units. 100 IRE units = 0.714V, P-P

Applying The HA-5033

The most important consideration when designing with the HA-5033 is layout. The wide bandwidth of the buffer necessitates that high frequency layout procedures be followed. Recommended procedures include the use of a ground plane, minimization of all lead lengths, avoiding sockets, and proper power supply decoupling.

Standard practice in RF/Video layout is the use of a ground plane. A ground plane minimizes distributed circuit capacitance and inductance which degrade high frequency performance. The ground plane can also incorporate the metal case of the HA-5033, since pin #2 is internally tied to package. This feature allows the user to make contact between the ground plane and the package which extends shielding, provides additional heat sinking and eliminates the use of a socket. IC sockets contribute bandwidth limiting interlead capacitance and should be avoided.

For the epoxy mini-dip, additional heatsinking can be derived from soldering the no connection pins #2, 3, and 7 to the ground plane. Also, pin #6 can be tied to either supply, grounded or left open. But to optimize device performance and improve isolation, it is recommended that this pin be grounded.

Another method of enhancing device performance is power supply decoupling. For the HA-5033, it is recommended that the positive and negative power supplies be bypassed with capacitors to ground. Ceramic capacitors ranging in value from .01 to .1 μF will minimize high frequency variations in supply voltage. Solid tantalum capacitors 1μF or larger will optimize low frequency performance. It is also recommended that the bypass capacitors be connected as close to the HA-5033 as possible, preferably directly to the supply pins.

Finally, keeping all lead lengths as short as possible will minimize distributed capacitance and reduce board space. It is essential that the guidelines dis-

cussed above be followed to avoid marginal performance.

Another consideration when applying the HA-5033 is load capacitance. Although the HA-5033 is designed to handle load capacitance values up to .01μF, it has a worst case stability region in the area of 50pF. The computer simulation of the HA-5033 frequency response in Figure 13 illustrates the gain peaking which occurs in the 150MHz region.

There are three suggested methods of dealing with this particular characteristic of the HA-5033. Isolating the load capacitance from the buffer output is the object of the first method. This is accomplished by placing a series resistor between the output and the load.

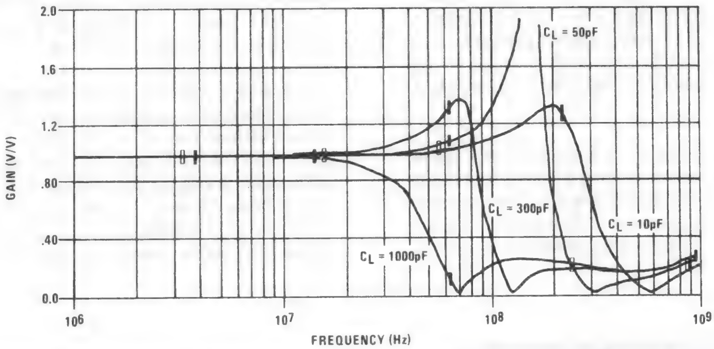


FIGURE 13. COMPUTER SIMULATION OF HA- 5033 GAIN CHARACTERISTICS VS FREQUENCY AND LOAD CAPACITANCE

A second technique utilizes the HA-5033 frequency response with respect to load capacitance. Referring once again to Figure 13, notice that the gain peaking is removed with additional load capacitance. This is the basis of method two, adding additional load capacitance to approach a region of stability.

A drawback to adding more load capacitance is that the buffer's dynamic characteristic will degrade and bandwidth performance will be less than data sheet specifications. The third method solves this trade-off by using a "bootstrap" technique of adding capacitance from input to output. This method achieves stability without sacrificing performance.

An explanation of why adding capacitance will stabilize the HA-5033 can be found in the Y parameter data shown in Figure 14. The expression for the buffer gain in terms of Y parameter is:

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{-Y_{21}}{Y_{22} + Y_L}$$

Y_{21} = Forward Transmittance
Y_{22} = Output Admittance
Y_L = Load Admittance

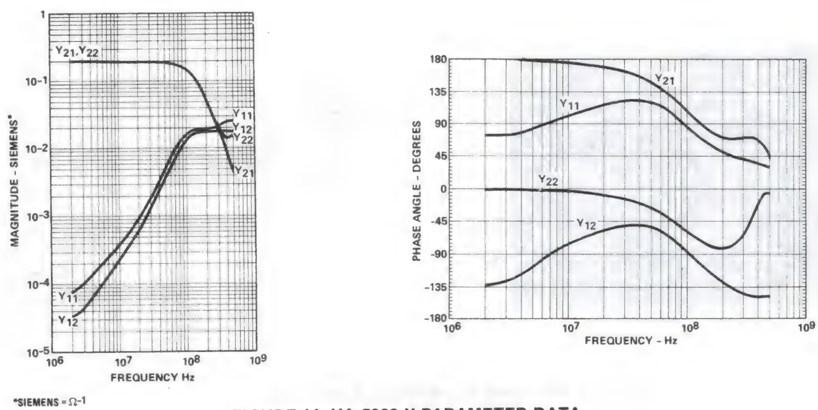


FIGURE 14. HA-5033 Y PARAMETER DATA

Notice that the load admittance, Y_{22}, phase becomes inductive ($-jY_L = -90^o$) at high frequency. So if the load, Y_L, is capacitive ($+jY_C = +90^o$) and the sum of $Y_{22} + Y_L$ become small, peaking occurs. Adding additional capacitance changes the effective phase angle and peaking can be reduced.

Using the HA-5033 as the analog input buffer of a flash converter is an example of application where the suggested stabilization methods are useful. Although its been stressed to keep all distributed capacitance to a minimum to optimize device operation, the load which a flash converter presents to the buffer represents a greater concern.

Flash or parallel converters are a special case, since the analog input circuit must drive a non-linear input impedance[8]. This non-linearity is due to the potential input impedance changes of the 255 parallel comparators which comprise the converter analog input. In addition to the non-linearity, the input capacitance of these converters tends to be relatively large, 100-300pF.

Example of the various stabilization methods tested with the TWR 1007 8 bit video flash converter are shown in Figure 15. Figure 15a illustrates the series resistor method. 15b is the load capacitance method and 15c is the bootstrap method. Photographs of the experimental results show the analog input sampling convert signal (pin 30), the MSB digital output (D1 pin 40), and the buffer output (converter input).

It is recommended that a complete evaluation for each method be conducted to determine the optimum component values. The value of the series resistor will depend upon the input capacitance of the particular converter used. A suggested starting value is 50ohms. With the capacitance methods, the distributed capacitance of the layout will affect component values. These experimental results were obtained using C = 240pf.

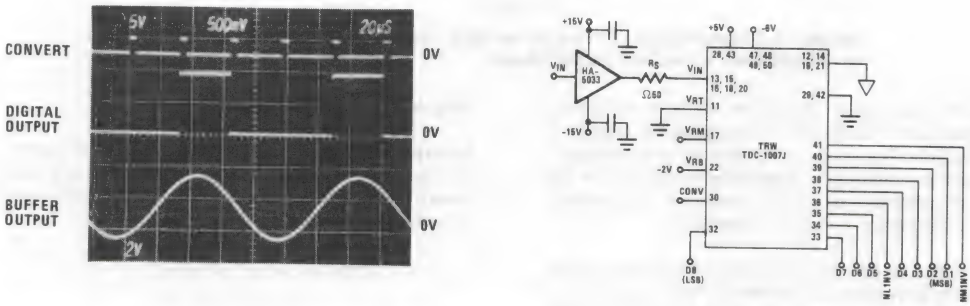


FIGURE 15a. ENHANCING 5033 PERFORMANCE IN FLASH CONVERTER APPLICATIONS: SERIES RESISTOR METHOD

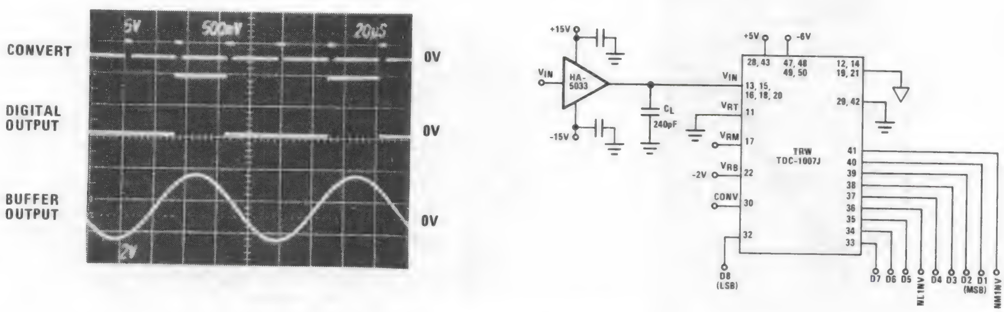


FIGURE 15b. LOAD CAPACITANCE METHOD

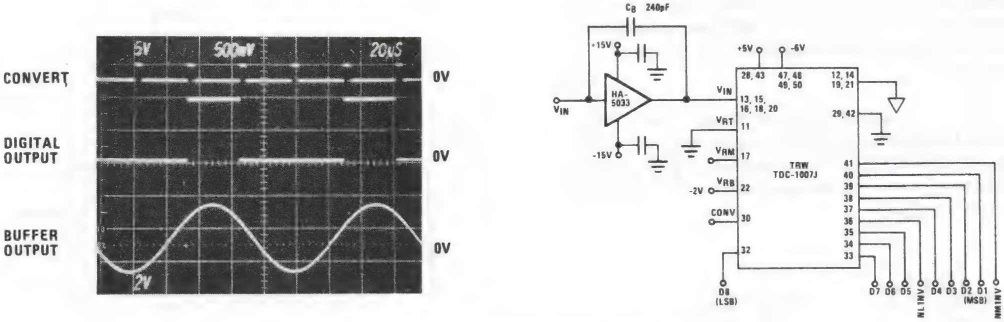
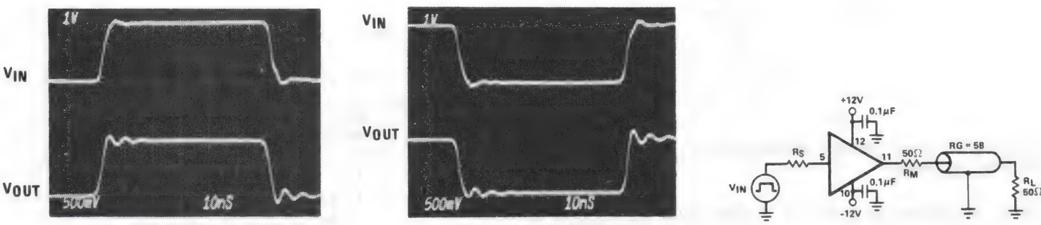


FIGURE 15c. BOOTSTRAP CAPACITANCE METHOD

The signal levels in most video applications are 1V p-p or less. Although the HA-5033 was shown with ±15V power supplies in the converter applications, lower power supplies will accommodate these video signal levels. For example, at ±5V power supplies, the HA-5033 can swing ±2V into a 75 ohm load.

The HA-5033 is an excellent high speed line device capable of driving 50 ohm and 75 ohm coaxial cable.

These type of drive requirements are common in video circuit design. Figures 15 and 16 illustrate two typical application examples. Figure 15 is an example of a 50 ohm system using the HA-5033 alone. R_m matches the buffer output impedance to the cables characteristic impedance. Depending upon the response required, this resistor may not be necessary. If used, the output voltage will be one half the input voltage.



POSITIVE PULSE RESPONSE
$T_A = 25^oC$
$R_S = 50\Omega$
$R_M = R_L = 50\Omega$
$V_0 = V_{IN}\left(\frac{R_L}{R_L + R_M}\right) = ½\,V_{IN}$

NEGATIVE PULSE RESPONSE
$T_A = 25^oC$
$R_S = 50\Omega$
$R_M = R_L = 50\Omega$
$V_0 = V_{IN}\left(\frac{R_L}{R_L + R_M}\right) = ½\,V_{IN}$

FIGURE 15. VIDEO COAXIAL LINE DRIVER - 50 OHM SYSTEM

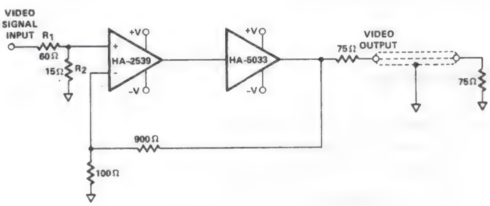


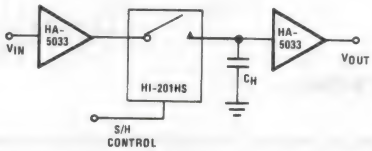
FIGURE 16. VIDEO GAIN BLOCK

Figure 16 illustrates the use of the buffer within the feedback loop of an operational amplifier. This configuration provides additional output current capability for the HA-2539 op amp and gives the designer voltage gain control.

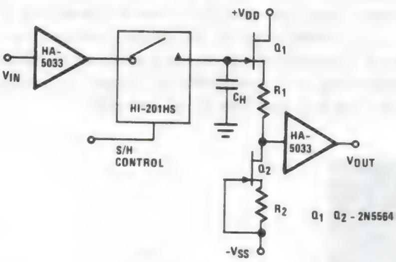
Another application which utilizes the HA-5033's output drive capability is the high speed sample and hold circuit shown in Figure 17. The input buffer provides drive current to the hold capacitor while the output buffer functions as a data line driver. The switching element in this application is the HI-201HS high speed CMOS switch which contributes it's own benefits to the application[9]. Depending upon the application requirements, using the HA-5033 as the output buffer in Figure

17a may not be acceptable. Lab tests have shown that the input bias current of the HA-5033 becomes a factor for low values of hold capacitance (< .01μF) during the hold mode.

A solution is to add a low bias current F.E.T. input stage, as shown in Figure 17b. Q1 acts as a voltage follower and Q2 is a current source. Matching Q1, Q2 and R1, R2 are important considerations in order to minimize offset voltages.



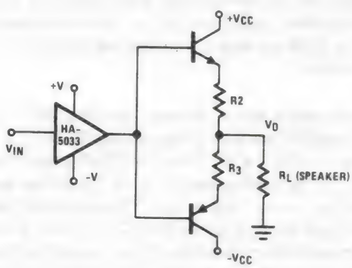
(a)



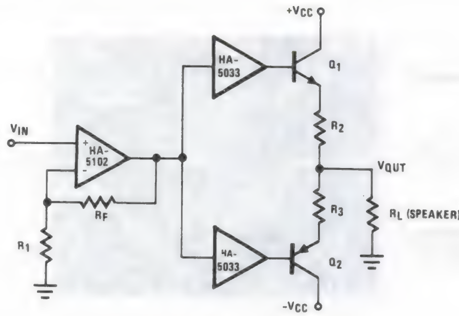
(b)

FIGURE 17a. HIGH SPEED SAMPLE/HOLD (b) MODIFIED OUTPUT BUFFER

When the drive capability of the HA-5033 is insufficient, consider adding an external output stage. Figure 18a illustrates an example where a push-pull complementary output stage has been added to the HA-5033. Although unable to drive the low impedances of speakers, typically 4-8 ohm, the buffer can be used to drive audio output transistors. A variation of this configuration is shown in Figure 18b, where separate buffers individually drive each transistor base. A low noise input stage is provided by the HA-5102.



(a)



(b)

FIGURE 18. AUDIO DRIVERS

A common method of achieving an audio oscillator circuit is to use a transistor or IC amplifier with LC or RC feedback. An alternative technique of generating sinusoidal waveforms, using the HA-5033, is shown in Figure 19. Crystal oscillators offer improved frequency stability over time and temperature. This particular oscillator configuration[10] produces an 18.18 MHz, 2.8V_{p-p} sinusoidal waveform into a 1K ohm load.

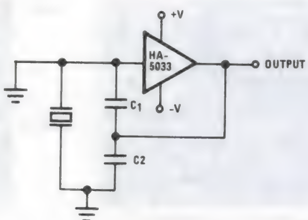


FIGURE 19. CRYSTAL OSCILLATOR: ±V = ±15V, C1 = 12pF, C2 = 39pF, 18MHz QUARTZ CRYSTAL

Conclusion

The HA-5033 is a high performance integrated circuit presently being utilized in a wide variety of applications. This paper has provided additional information to aid designers in applying the HA-5033 video buffer in future applications.

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2. Stu Rasmussen and Clifford B. Schrock "Television Operational Measurements, Video and RF for NTSC Systems" Tektronix, 1980.

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4. L. E. Weaver, Television Video Transmission Measurements, (London, Marconi Instruments, 1971).

5. F. F. Mazda, ed., Electronic Engineers Reference Book, 5th ed. (London Butterworth, 1982).

Acknowledgements

1. Technical contributions of John Prentice and Robert Junkins.

2. Sales and Technical Staff of Marconi Instruments.

APP NOTE

FOR YOUR INFORMATION

No. 550

Harris Analog

USING THE HA-2541

Alan W. Hansford

Introduction

In response to an industry wide need for a faster, unity gain stable, monolithic operational amplifier, Harris Semiconductor has designed and manufactured the HA-2541 device.

This fully differential op amp has an unprecedented set of dynamic parameters which should be most useful for demanding designs in video, data acquisition, robotics, and RF systems. These devices' capabilities may also be utilized when existing systems must be upgraded or modified for additional performance.

The HA-2541's outstanding features include 90ns settling time, 250V/μs slew rate, and 40MHz unity gain bandwidth, which until recently, could only be achieved through hybrid configurations.

The applications information which follows, points in the direction where a vast number of application circuits await the HA-2541.

Prototyping

As with any high performance device, care should be taken in prototyping so as not to undermine the performance characteristics of the HA-2541. Several simple do's and don'ts should avoid most design problems. Standard high frequency layout techniques are strongly recommended in order to gain the full benefit of the HA-2541's capabilities. The first is proper mounting of the HA-2541 through a ground plane. Since sockets tend to extend the lead length and increase parasitic capacitance, they are not recommended. If sockets must be used, Teflon types are preferred. The mounting of the feedback components should be as close as practical to the HA-2541 and on Teflon standoffs.

The wide bandwidth of the HA-2541 makes it prone to unwanted high frequency poles if large value feedback resistors are used (10K ohms). This calls for low value film type resistors. Actual component values may depend heavily on layout implementation. It is therefore suggested that early prototyping be done to verify the quality of operation and to optimize component values. Additionally, power supply decoupling as close to the power pins as possible, is recommended.

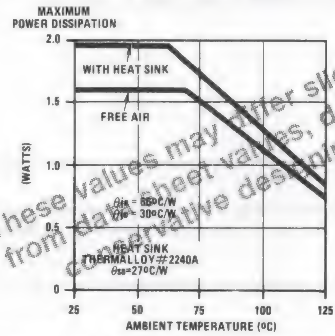
Thermal Considerations

(Also Refer to Application Note 556)

In order to achieve the 250V/μsec slew rate that the HA-2541 is capable of, a high quiescent power level was needed. This, along with the high output capacity of the HA-2541, means that the package must dissipate a large amount of heat.

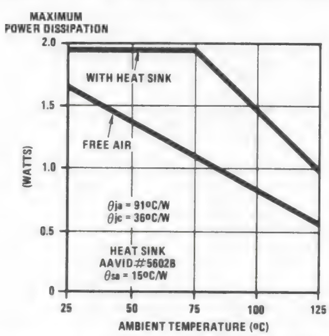
The device's junction temperature upper limit is 175°C. This places a restriction on the power output at elavated ambient temperatures. The charts below mark the acceptable region of operation with and without a heat sink (Thermalloy 2240A or 5602B are acceptable units and the ones used in the construction of the charts). The curves assume proper installation including the use of heat conductive compounds to facilitate the energy transfer.

CHART 1. TO-8 METAL CAN (HA2-2541-X)



NOTE: For maintaining maximum junction temperatures below +175°C, derate at 15.2mW/°C beyond +68°C ambient.

CHART 2. 14 PIN DIP PACKAGE (HA1-2541-X)



NOTE: For maintaining maximum junction temperatures below +175°C, derate at 11.0mW/°C beyond +25°C ambient.

Performance Enhancements

The HA-2541, like any other high performance device, has certain design features, which give the HA-2541 its excellent wideband performance. Although the HA-2541 has been laser trimmed to minimize offset voltage, an external potentiometer connection has been provided to reduce this even more. Figure 1 illustrates the suggested offset adjustment.

The input DC performance is improved by the use of balanced input impedances on the two input terminals of the device. Figure 2 illustrates this technique which greatly reduces any effects caused by the input offset currents.

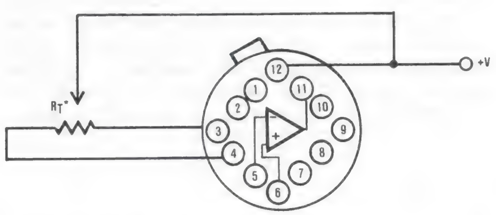
The input signal can be given even more isolation from the effects of input bias currents with the use of FET buffered inputs as shown in Figure 3. The reduction of the input bias currents is quite large, which makes the FET HA-2541 combination an excellent choice for low current applications such as atomic particle detectors (radiation counter circuitry).

Applications

The HA-2541 is a very versatile device with applications in nearly every area of its bandwidth. Perhaps one of the best ways to gain some familiarity with the part is by examining its use in some of the more straightforward applications. The Wein Bridge oscillator in Figure 4 is just such an application.

The HA-2541 is well suited for use as the heart of an oscillator circuit. In spite of the rudimentary diode limiting provided by R_3 - R_7 and D_1 & D_2, a good quality sine wave of 40MHz is readily attainable with an upper limit of 50MHz which exceeds the unity gain bandwidth of the HA-2541.

R_1C_1 and R_2C_2 provide the required regenerative feedback needed for adequate frequency stability. In theory the feedback network requires a gain of three to sustain oscillation. However, the practical gain needed is just over three and is provided for by R_8 and R_9.



*Offset Adjustment Range Is Approximately ± 8mV for RT = 5KΩ

FIGURE 1. SUGGESTED METHOD FOR NULLING V_{OS}

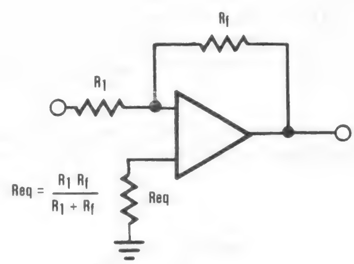
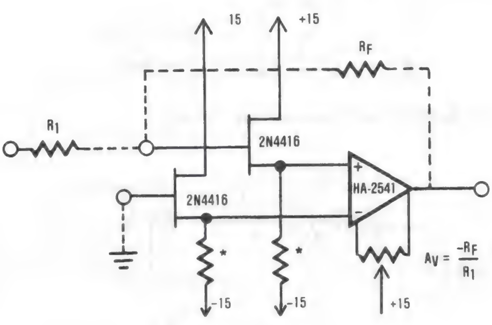


FIGURE 2. MINIMIZING THE EFFECTS OF OFFSET CURRENT



*Value should be determined experimentally for optimum performance.

FIGURE 3. BUFFERING THE HA-2541 INPUTS WITH FETS.

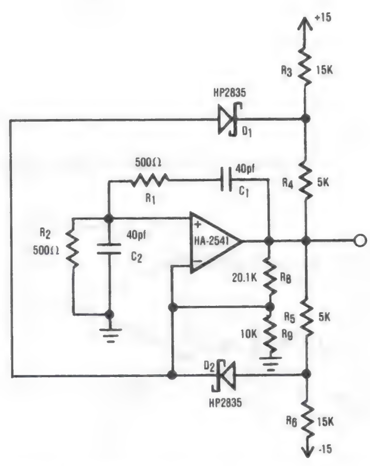


FIGURE 4. 40MHz WEIN BRIDGE OSCILLATOR

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APPLICATION NOTES

High power amplifiers and buffers are in use in a wide variety of applications. Many times the "high power" capability is needed to drive large capacitive loads as well as low value resistive loads. In both cases the final driver stage is usually a power transistor of some type, but because of their inherently low gain, several stages of pre-drivers are often required. The HA-2541, with its 10mA output rating, is powerful enough to drive a power transistor without additional stages of current amplification. This capability is well demonstrated with the high power buffer circuit in Figure 5.

The HA-2541 acts as the pre-driver to the output power transistor. Together, they form a unity gain buffer with the ability to drive three 50 ohm coaxial cables in parallel, each with a capacitance of 2000pF. The total combined load is 16.6 ohms and 6000pF capacitance.

Video

One of the primary uses of the HA-2541 is in the area of video applications. These applications include signal construction, synchronization addition and removal, as well as signal modification. A wide bandwidth device such as the HA-2541 is well suited for use in this class of amplifier. This, however, is a more involved group of applications than ordinary amplifier applications since video signals contain precise DC levels which must be retained.

The addition of a clamping circuit restores DC levels at the output of an amplifier stage. The simple form of the circuit is shown in Figure 6A with a capacitor and analog switch added to the inverting amplifier configuration. The switch closes during a certain portion of the incoming signal. This causes the capacitor to charge to a value which represents the 0V reference of the input waveform. The shorting action of the switch causes the output of the HA-2541 to go to 0V during the 0V reference of the input signal.

This simple amplifier/clamping circuit has several drawbacks. The largest is the drain on the holding capacitor by the input bias currents of the HA-2541, with the resulting change in the reference voltage. This condition is easily addressed with the use of an HA-5320 sample and hold. The low output impedance of the sample and hold can easily provide the required input bias current for the HA-2541 without draining the holding capacitor. The result is a constant DC reference between the scan lines of the video signal.

The second drawback of the simple amplifier/clamp results from the color synchronization information being transmitted along with the 0 Volt DC reference level. By closing the analog switch, the color burst is passed through the low impedance capacitor to ground and consequently lost. This situation is remedied by placing a 3.57MHz trap in series with the analog switch and holding capacitor. This will block the color burst signal and allow it to be passed to the output as an amplified signal. Figure 6B shows both the "trap" and the sample and hold reference additions to the simple amplifier with DC restore.

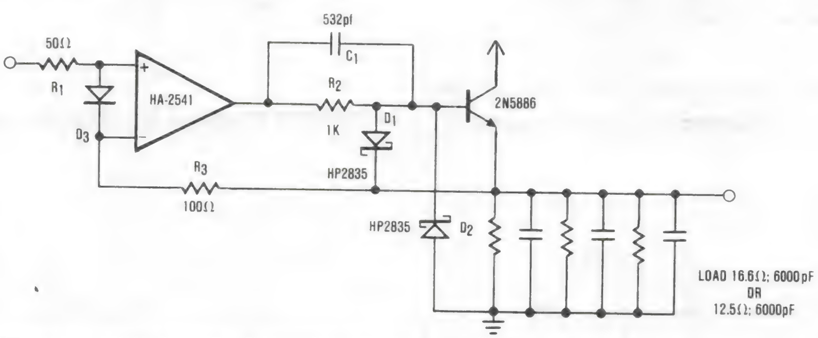

FIGURE 5. DRIVING POWER TRANSISTORS TO GAIN ADDITIONAL CURRENT BOOSTING

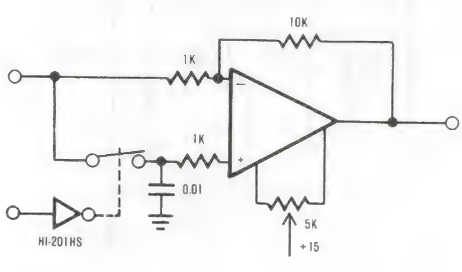

FIGURE 6A. SIMPLE DC RESTORER

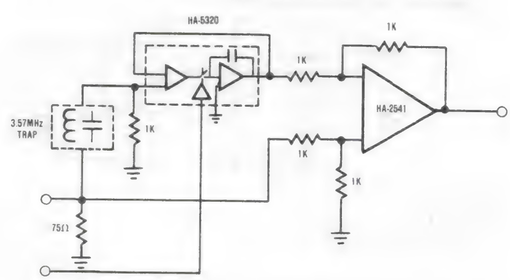

FIGURE 6B. IMPROVED VIDEO DC RESTORER

The amplifier designs to this point work with the full video signal or the "composite" signal. The HA-2541 has several applications one stage back, in the construction of the composite signal itself.

The composite video signal has several components which must be combined to create the final waveform. One that has already been used is the 0 volt reference and the color burst combination. Two others are the horizontal synchronization pulse and the video picture information.

The circuit in Figure 7 is a traditional summing amplifier configuration with the addition of the now familiar DC clamping circuit. The operation is quite simple in that each component (synchronization, color burst, picture information, etc.) of the composite video signal is applied to its own input terminal of the amplifier. These combine algebraically and form the composite signal at the output. The clamping circuit (if used) restores the 0 volt reference of the composite signal.

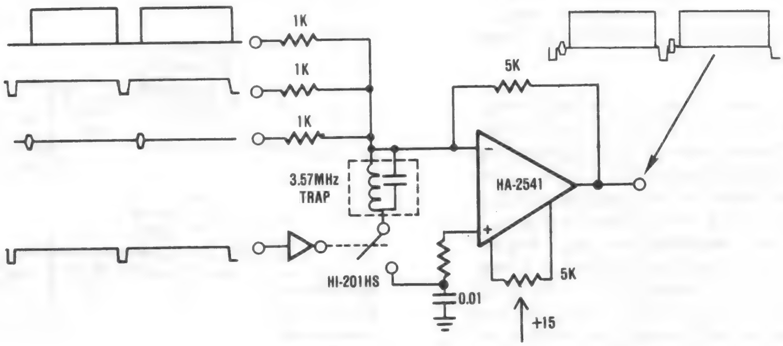

FIGURE 7. SUMMING AMPLIFIER FOR COMPOSITE VIDEO PLUS CLAMPING CIRCUIT

One drawback resulting from the algebraic addition of the input waveforms is the requirement that each input component exist only during the period that it is needed in the composite signal. An example of this is the color burst which can be present at its input terminal only during its portion of the composite signal since no gating circuitry is available.

The multiplexer circuit in Figure 8 can be used for video signal construction by gating each component through to the HA-2541 as it is required. The inherent channel separation of the multiplexer allows each component of the composite signal to be continuously present at the input. This has several important implications. The first is that the duration of each component of the signal is precisely controlled by a digital timing chain (which can be easily reproduced at remote locations with high precision). Second, the only analog signals needed are the color burst and the picture information. All reference signals such as the horizontal synchronization, the 0 volt reference, and the previously unmentioned vertical synchronization signals can be simulated with accurate DC references. These are gated, along with the other components, to form the composite video signal.

An extension of the multiplexed signal construction technique is a type of signal modification. When several cameras are used together without a common synchronization signal, they are not easily combined for special effects and switching. A solution to this problem would be to strip the synchronization pulses off of each of the incoming camera waveforms and apply a new common synchronization pulse. The new pulse will enable switching equipment to combine the separate signals for whatever effect is needed.

It should be noted that widely varying horizontal speeds may necessitate the use of analog delay chains with the synchronization technique. This will produce pictures of compatible quality and proportion (vertical speed is more constant and contains a dead zone for any differences, vertical retrace).

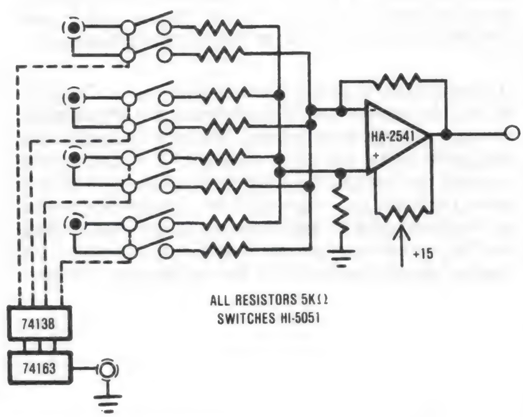

FIGURE 8. MULTIPLEXING WITH HA-2541

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APPLICATION NOTES

The multiplexer system used for video signal construction has other applications of interest. The concept of combining several channels into one can be reversed to form a demultiplexer, where the function is to take several combined channels and separate them into their original form. This type of application can be implemented to solve some well-known industrial problems.

The multiplexer/demultiplexer scheme is readily adapted to the industrial remote controller system where several sensors must communicate over transmission lines to the controller. With the multiplexer/demultiplexer configuration a very large number of sensors are able to communicate with the controller over extended distances through a single coaxial line.

The wide bandwidth of the HA-2541 coupled with its high output rating make it an excellent component of multiplexed data systems. Several schemes of signal switching can be used at the multiplexer end of the system. The HI-5051 switch is well suited for this application especially in the differential configuration shown in Figure 8. The charge injection due to switching channels in and out of the circuit is minimized in this differential mode. A reset pulse aligns the system synchronization and provides the basis for channel separation in the demultiplexer section. As the channels are sequentially placed at the HA-2541 input, they are transmitted to the demultiplexer circuit. In Figure 9 the HA-5320 sample and hold acts as a buffer for each channel and provide a reference source when the other channels are being addressed. Another plus in this demultiplexer circuit is the capability of "de-glitching" the information by simply shifting the clocking rate so as to place all channels in the hold mode during the presence of input spikes.

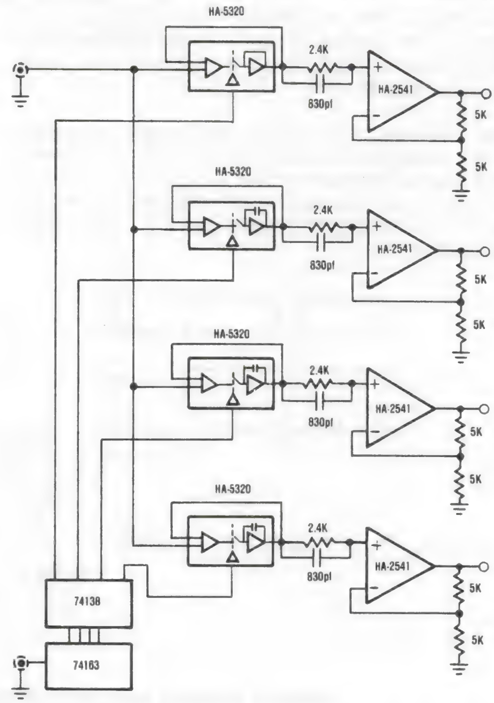

FIGURE 9. DEMULTIPLEXING WITH HA-2541

Write Amplifier

The recent proliferation of industrial and computerized equipment containing programmable memory has increased the need for reliable recording media. The magnetic tape medium is presently one of the most widely used methods. The primary component of any magnetic recording mechanism is the "write" mechanism. In support of this area the circuit of Figure 10 is presented.

The concept of the write generator is very basic. The digital input causes both a change in the output amplitude as well as a change in frequency. This type of operation is accomplished by altering the value of a resistor in the standard twin tee oscillator. An HI-201 analog switch was used to facilitate the switching action. The effect of the external components on the feedback network requires R_{6A} and R_{6B} to be much smaller than would normally have been expected when using the twin tee feedback scheme.

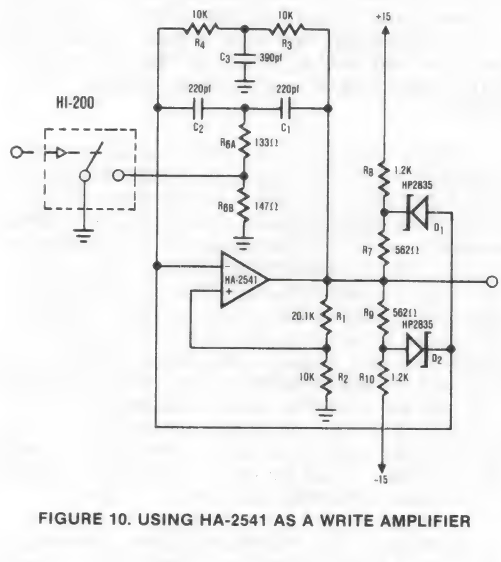

FIGURE 10. USING HA-2541 AS A WRITE AMPLIFIER

The output seen in the photograph of Figure 11 is limited with the aid of D_1, D_2 and R_4-R_7. This is aided by fixing the gain of the amplifier to just over three with R_8 and R_9.

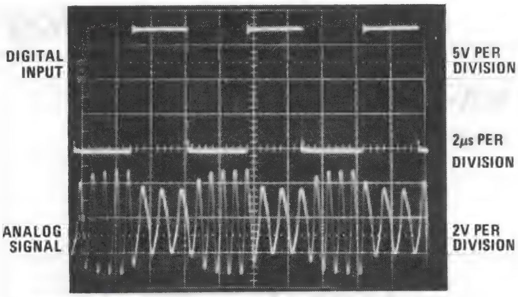

FIGURE 11. DIGITALLY CONTROLLED OUTPUT OF WRITE AMPLIFIERS

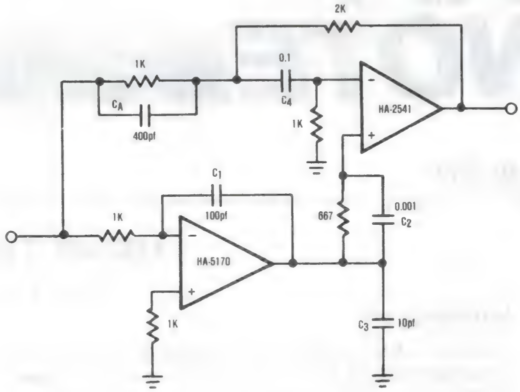

FIGURE 12. COMPOSITE AMPLIFIER

Composite Amplifier

The wide bandwidth of the HA-2541 can be used to extend the dynamic range of other useful but frequency limited amplifiers. The HA-5170 is an excellent example of this adaptation. The precision DC characteristic of the HA-5170 are augmented by the bandwidth of the HA-2541. This produces a composite amplifier which approximates the DC performance of the HA-5170 and the frequency range of the HA-2541.

The circuit in Figure 12 has been optimized for operation in the neighborhood of 15MHz. Optimization is quite simple and is accomplished largely through C_A. If a lower frequency region of operation is desired, an additional capacitor, C_2, will give greater flexibility in the choice of component values.

Programmable Amplifier

Often a circuit will be called upon to perform several functions. In these situations the variable gain configuration of Figure 13 may be quite useful. This programmable gain stage depends on CMOS analog switches to alter the amount of feedback and thereby the gain of the stage. Placement of the switching elements inside relatively low current area of the feedback loop, minimizes the effects of bias currents and switch resistance on the calculated gain of the stage. Voltage spikes may occur during the switching process, resulting in temporarily reduced gain because of the make-before-break operation of the switches. This can be minimized by providing a separate voltage divider network for each switched gain.

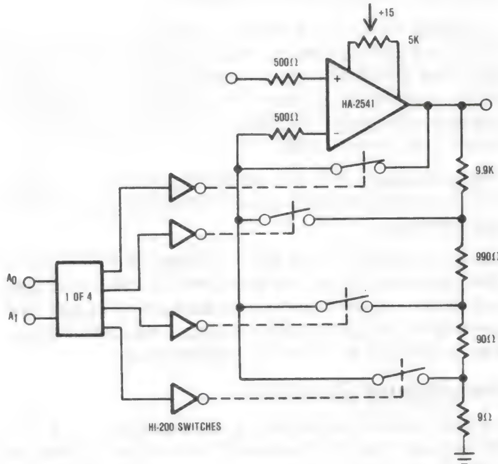

FIGURE 13. A GAIN PROGRAMMABLE HA-2541

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2. Thermalloy Semiconductor Accessories Catalog, Thermalloy Inc. Dallas, Texas.

3. Arthur B. Williams, "Designers Handbook of Integrated Circuits." (McGraw-Hill, 1984) pps. 1-10, 1-27.

APP NOTE

FOR YOUR INFORMATION

No. 552

Harris Analog

USING THE HA-2542

Richard A. Whitehead

Introduction

In the multi-faceted electronics industry, there are many circuit applications which require the capabilities of two or more types of operational amplifiers in the same location. To fulfill this need, design engineers are usually challenged with fabricating a discrete amplifier design or selecting an expensive hybrid amplifier which appears to be an "ALL-IN-ONE" type of amplifier.

The Harris HA-2542 is a state of the art monolithic device which also approaches the "ALL-IN-ONE" amplifier concept. This device features an outstanding set of AC parameters augmented by excellent output drive capability providing for suitable application in both high speed and high output drive circuits.

Offset voltage nulling and bandwidth controls add flexibility when the HA-2542 is used in performance-tailored applications.

Primarily intended to be used in balanced 50Ω and 75Ω coaxial cable systems as a driver, the HA-2542 could also be used as a power booster in audio systems as well as a power amp in power supply circuits. This device would also be suitable as a small DC motor driver.

Prototyping Guidelines

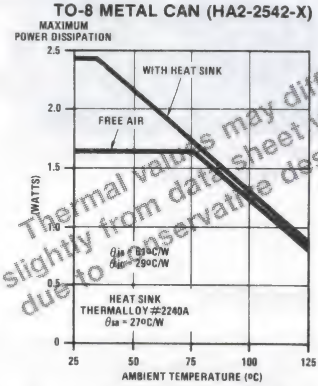
For best overall performance in any application, it is recommended that high frequency layout techniques be used. This should include: 1) mounting the device through a ground plane: 2) connecting unused pins to the ground plane: 3) mounting feedback components on Teflon standoffs and/or locating these components as close to the device as possible; 4) placing power supply decoupling capacitors from device supply pins to ground.

As a result of speed and bandwidth optimization, the HA-2542's case potential, when powered-up is equal to the V- potential. Therefore, contact with other circuitry or ground should be avoided.

Heat Sinking (Also Refer to Application Note 556)

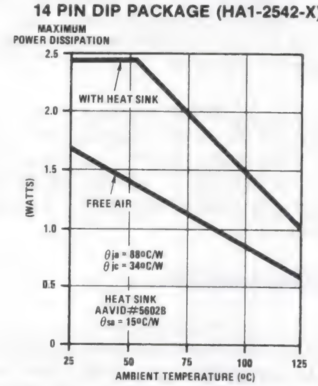
To drive heavy loads found in typical coaxial cable systems, the HA-2542 may require heat sinking to avoid exceeding its maximum junction temperature (+175°C). Figure 1 shows maximum power dissipation curves derived for the HA-2542 with and without the recommended heat sink. Should another type of heat sink be used, then the following expression should be used to determine maximum power dissipation.

TO-8 METAL CAN (HA2-2542-X)



NOTE: For maintaining maximum junction temperatures below +175°C, derate at 16.4mW/°C beyond +75°C ambient

14 PIN DIP PACKAGE (HA1-2542-X)



NOTE: For maintaining maximum junction temperatures below +175°C, derate at 11.4mW/°C beyond +25°C ambient.

FIGURE 1. HA-2542 MAXIMUM POWER DISSIPATION CURVES

$$P_{dmax} = \frac{T_{jmax} - T_A}{\theta_{j\text{-}c} + \theta_{c\text{-}s} + \theta_{s\text{-}a}}$$

Where: T_{jmax} = maximum junction temperature of the device

T_A = Ambient

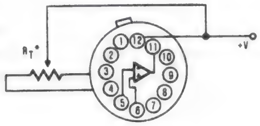
$\theta_{j\text{-}c}$ = Junction to case thermal resistance

$\theta_{c\text{-}s}$ = Case to heat sink thermal resistance

$\theta_{s\text{-}a}$ = Heat sink to ambient thermal resistance

Performance Enhancements

DC errors can be reduced and AC stability increased by recommended adjustments to the control points made available in the HA-2542 device. The suggested method for nulling the offset voltage of HA-2542 is shown in Figure 2, while Figure 3 suggests the method for controlling the bandwidth. Figure 4 shows normalized AC parameters versus compensation capacitance. Experimental results indicated that approximately 17pF was necessary to stabilize the HA-2542 for unity gain operation.



*OFFSET ADJUSTMENT RANGE IS APPROXIMATELY ±15mV FOR R_T = 5KΩ.

FIGURE 2. SUGGESTED OFFSET VOLTAGE ADJUSTMENT

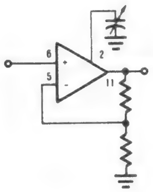


FIGURE 3. SUGGESTED METHOD FOR INCREASING AC STABILITY

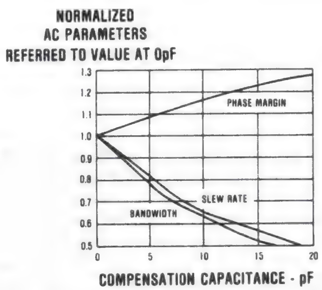
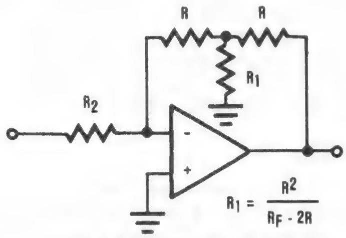


FIGURE 4. NORMALIZED AC PARAMETERS

For best high frequency performance, feedback resistor values should be restricted to minimal values. Values below 5KΩ are recommended to reduce possibilities of introducing unwanted poles into the application's transfer function. Figure 5 indicates how high values for closed loop gain can be implemented, while maintaining feedback element values. This method is called "T network" feedback and values for the resistors can be derived from the following expression.

$$R_1 = \frac{R^2}{R_f - 2R}$$

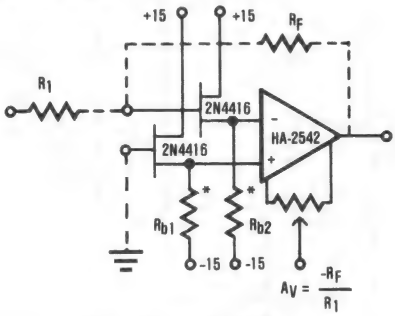
Where: R_f is the value of feedback resistance to be reduced and R is a value preselected by the designer.



WHERE R IS PRESELECTED AND R_F IS DESIRED FEEDBACK RESISTOR VALUE.

FIGURE 5. KEEPING FEEDBACK VALUES LOW

Utilizing some relatively familiar techniques, the input bias currents of the HA-2542 can be sharply reduced. Figure 6 employs discrete FETs to provide input bias currents in the pA range without appreciably diminishing the AC performance.



*R_{b1} AND R_{b2} SHOULD BE DETERMINED EXPERIMENTALLY FOR BEST RESULTS.

FIGURE 6. USING DISCRETE FETs TO REDUCE THE HA-2542's INPUT BIAS CURRENT

Composite amplifiers are hybrid "marriages" between precision and wideband operational amplifiers. Using the HA-2542 as the AC device in the composite amplifier shown in Figure 7 provides an additional dimension to its

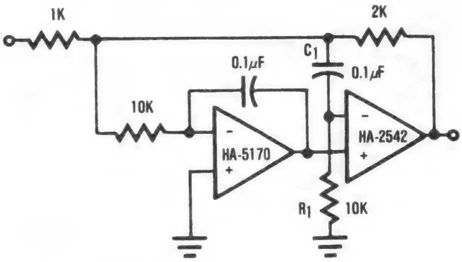


FIGURE 7. COMPOSITE AMPLIFIER CIRCUIT REDUCES DC ERRORS

10

APPLICATION NOTES

capabilities. Now, the hybrid represents a precision type, high speed, wideband, power amplifier.

In this circuit, high frequency amplification tasks are performed by the HA-2542 and are set by combination R_1-C_1. The HA-5170 acts as the DC amplifier providing precision type input parameters while cascading its DC gain with that of the HA-2542. This cascade of gains develops very high loop gain for the composite amplifier.

Applications

Most attractive to the video system designer is the HA-2542's combination of speed, bandwidth, and output drive capability. Augmenting these features are much desired differential gain and phase specifications of 0.1% and 0.2 degrees respectively. Previously these parameters could only be provided by hybrid or discrete component circuitry. A primary application which fully utilizes these features is the coaxial cable driver.

The configuration shown in Figure 8 represents a simple multi-channel security system. The HA-2542 is being operated at a closed loop gain of 2 and is driving a balanced coaxial line system which appears as a 50Ω load. The signal throughput from the multiplexer input to the coaxial outputs is 1. Experimental results showed that coaxial line lengths could exceed 100 feet without adversely affecting video signal quality.

HA-2542 is capable of $2V_{p-p}$ signals to 16MHz in this configuration. Resistor R_B is used to trim overall system gain to prevent color saturation if the cameras and monitors are color types. The controller to the multiplexer could be one of several variations including remote, remote wired, or automatically time sequenced.

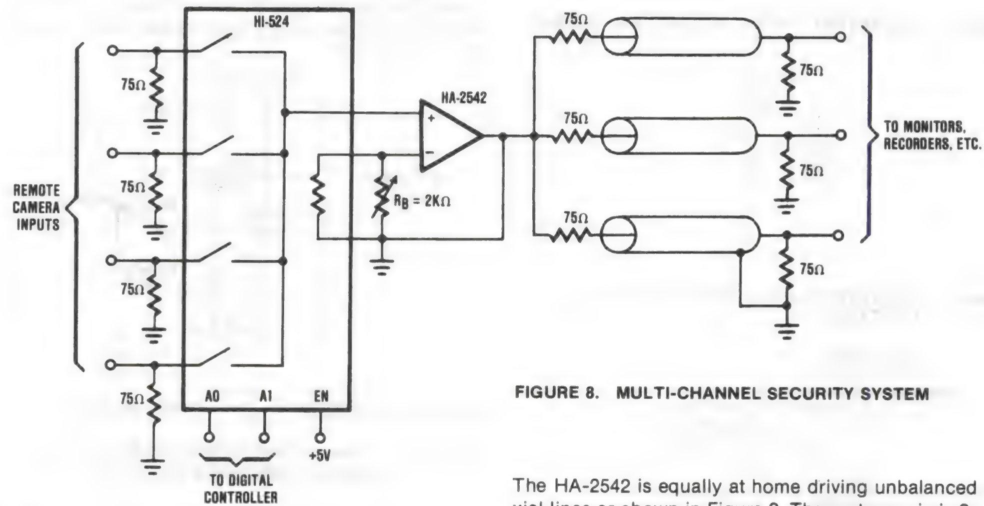


FIGURE 8. MULTI-CHANNEL SECURITY SYSTEM

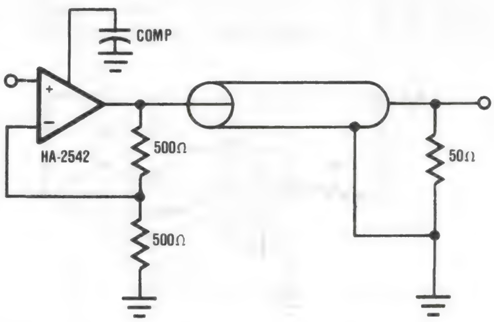


FIGURE 9. DRIVING UNBALANCED COAXIAL CABLES

The HA-2542 is equally at home driving unbalanced coxial lines as shown in Figure 9. The system gain is 2 and, depending on cable length, compensation capacitance may be necessary to provide additional stability. In this configuration, the HA-2542 can delivery $10V_{p-p}$ signals at frequencies above 8MHz. For this application, power requirements will usually necessitate the use of heat sinking for the HA-2542.

Another video type application requiring an op amp with excellent speed and output drive is the analog input driver of a flash converter circuit. Figure 10 shows the HA-2542 buffering the input of an 8-bit flash converter. Because of the heavy input capacitance (100pF - 300pF) and high number of individual internal comparator inputs (255), the impedance of the input is non-linear. A typical high speed op amp used in this configuration would exhibit oscillation tendencies regardless of compensation and isolation techniques used. The photograph shown in Figure 10 indicates that the HA-2542 is very stable in this application.

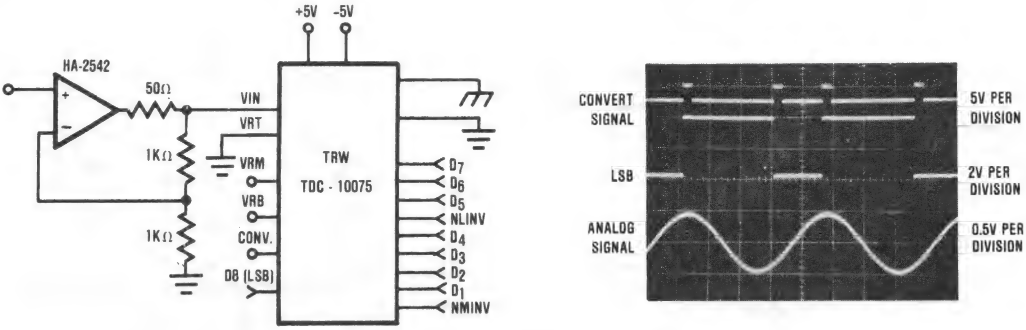


FIGURE 10. DRIVING THE NON-LINEAR INPUT IMPEDANCE OF FLASH CONVERTERS (ONE INPUT SHOWN)

Power Supply

The HA-2542 with its excellent output current could also be used as a power source in DC power supply systems. In Figure 11, a simplified digitally programmable power supply is shown which utilizes the high output current capabilities of the HA-2542. Combination R_1-R_2 sets the gain of the amplifier, while V_{REF} and the "weighted" resistor ladder permit the HI-201 to perform digital selection of the voltage to be used.

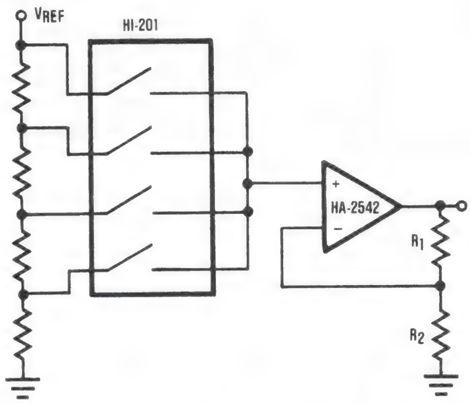


FIGURE 11. DIGITALLY PROGRAMMABLE POWER SUPPLY

Audio

In studio quality audio systems, the HA-2542 could be readily used in driver applications such as a speaker driver. Figure 12 shows a method which increases the power capability of a drive system for audio speakers. In this circuit two HA-2542s are used to operate on half cycles only, which greatly increases their power handling capability. "Bridging" the speaker as shown makes 200mA of output current available to drive the load. The HA-5102 is used as an AC coupled, low noise, pre-amplifier which drives the bridge circuit.

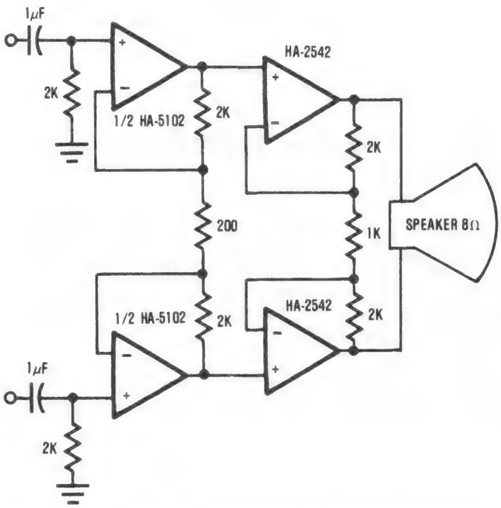


FIGURE 12. BRIDGE LOAD DRIVE FOR AUDIO CIRCUITS

Another variation of the bridged load type circuit is shown in Figure 13a. In this circuit the load voltage is increased by a factor of 4. The HA-2542s are connected in a manner such that the output voltages will be equal in amplitude and opposite in phase. This circuit can also be used to drive long lengths of twisted shielded pair cable.

Boosting Output Current

If the excellent output current of the HA-2542 requires boosting because of extreme loading, then the configuration shown in Figure 13b could be used. In this circuit, the HA-2542 drives the high power transistor stage and provides circuit gain. With the power transistors shown, the output drive is increased to several amps. Speed and power bandwidth have not been appreciably affected. Boosting the output current to these higher levels provides for additional implementation into DC motor drive or bridge transducer drive circuits.

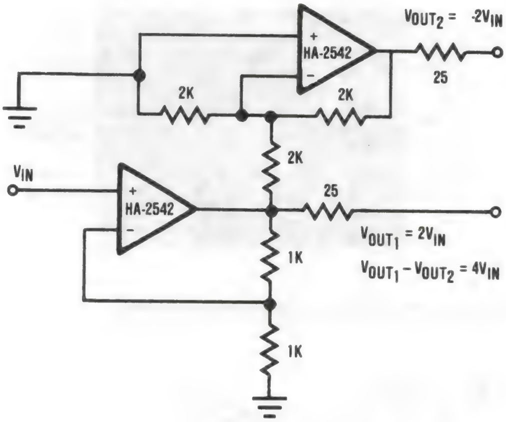


FIGURE 13A. DIFFERENTIAL CIRCUIT FOR LINE DRIVING

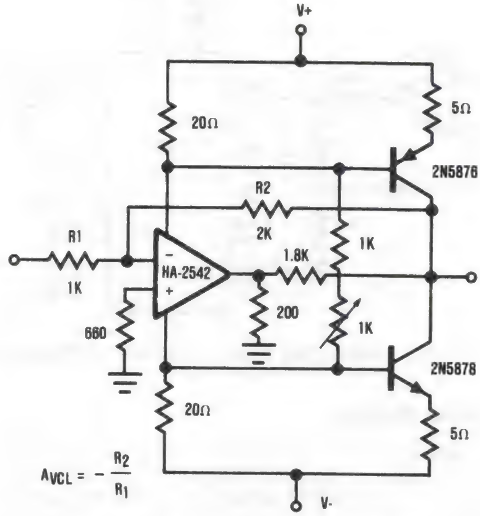


FIGURE 13B. DRIVER STAGE FOR HIGH POWER TRANSISTORS

The output drive capability of the HA-2542 is highly suitable for direct drive applications of small DC motors and, since it is an operational amplifier, it can also perform the function of motor speed control. This type of closed loop system can be found throughout the robotics and media recording industries.

The system shown in Figure 14 consists of the HA-2542, a small 12V DC motor, and a position encoder. During operation, the encoder causes a series of "constant width" pulses to charge C_1. The integrated pulses develop a reference voltage which is proportional to motor speed and is applied to the inverting input of HA-2542. The non-inverting input is held at a constant voltage which represents the desired motor speed. A difference between these two inputs will send a corrected drive signal to the motor which completes the speed control system loop.

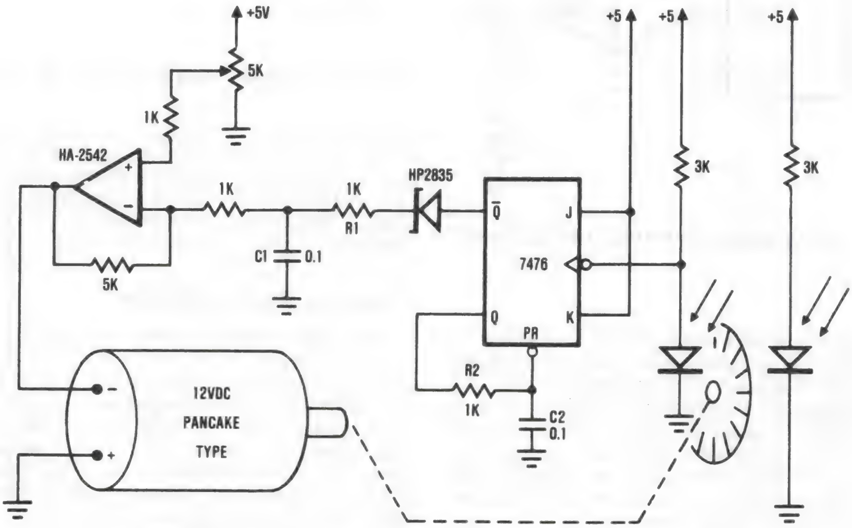


FIGURE 14. CONTROLLING DC MOTOR SPEED WITH HA-2542

No. 553

Harris Analog

HA-5147/37/27, ULTRA LOW NOISE AMPLIFIERS

By Alan Hansford

Introduction

Engineers interested in precision signal processing will find the HA-51X7, with its unique features, very interesting. Utilizing an advanced design with special device geometries, the HA-51X7 has moved the Harris dielectric process into a new arena of both speed and precision. Perhaps one of the most remarkable features of the HA-51X7 is its ultra low noise performance, which makes it the first monolithic amplifier to combine speed, precision, and ultra low noise operation (Figure 1).

To realize this device, intense attention was given to the "total" design from input to output (Figure 2).

The input stage consists of a cross-coupled differential pair which provides a very high CMRR (125dB) through the use of CASCODE circuits. Effective use of the bias current cancellation scheme also keeps the bias currents to a mere 10nA. With laser trimming of the load resistors R1 and R2, the offset voltage is kept below 25μV at 25°C. The entire input stage has been optimized for low noise operation and is largely responsible for the amplifier's ultra low noise voltage of 3.0nV/$\sqrt{\text{Hz}}$ @ 1KHz. Low frequency noise, on the other hand, is particularly important in DC applications and the HA-5147's 2.7Hz lower noise corner will prove quite beneficial for many users.

The loading on R1 and R2 is kept to a minimum through the use of emitter followers between the input stage and the second differential pair. C4 provides a feedforward path around the second stage at high frequencies and feeds into the level shifter and current mirror section. This portion of the design provides a differential to single-ended conversion and relies on C2 to tailor the rolloff of the second stage. Two vertically-constructed PNP transistors within the level shifter dramatically increase the frequency response of the amplifier compared to that of other construction techniques.

Emitter followers in the fourth stage reduce the capacitive loading effects of C1 by providing a separate driver for C1 and the output stage. The output stage here is a high speed buffer that employs complementary transistors as well as short circuit protection.

The high performance features of the HA-5147 have quite clearly moved this device closer to the "ideal" than any other amplifier in its class. Yet, with some simple external components, this device can be positioned even closer to the "ideal." An offset nulling potentiometer can reduce V_{OS} (Figure 3a), while the already hefty output stage (I_{out} = 20mAmin) can be boosted without reducing the excellent speed and bandwidth characteristics (Figure 3b).

	PRECISION HA-5137	HA-5147 PRECISION WIDEBAND	WIDEBAND HA-2620
V_{OS}	25μV	→ 25μV	4mV
V_{OS} DRIFT	1μV/mo.	→ 1μV/mo.	10μV/mo.
V_{OS} TEMPCO	0.2μV/C	→ 0.6μV/C	5μV/C
I_{bias}	±10nA	→ ±8nA	±1nA
I_{OS}	±7nA	→ ±10nA	±1nA
NOISE VOLTAGE	3.0nV/$\sqrt{\text{Hz}}$	→ 3.0nV/$\sqrt{\text{Hz}}$	16nV/$\sqrt{\text{Hz}}$
NOISE CURRENT	0.4pA/$\sqrt{\text{Hz}}$	→ 0.4pA/$\sqrt{\text{Hz}}$	1.6pA/$\sqrt{\text{Hz}}$
OPEN LOOP GAIN	1.8V/μV	→ 1.8V/μV	0.15V/μV
CMRR	126dB	→ 125dB	100dB
PSRR	120dB	→ 130dB	90dB
GAIN BANDWIDTH	63MHz	120MHz ←	100MHz
SLEW RATE	17V/μs	37V/μs ←	35V/μs
POWER BANDWIDTH	270KHz	560KHz ←	550KHz
POWER CONSUMPTION	90mW	85mW ←	90mW

FIGURE 1.
The HA-5147 combines the qualities of precision Op Amps with those of the wideband speed category.

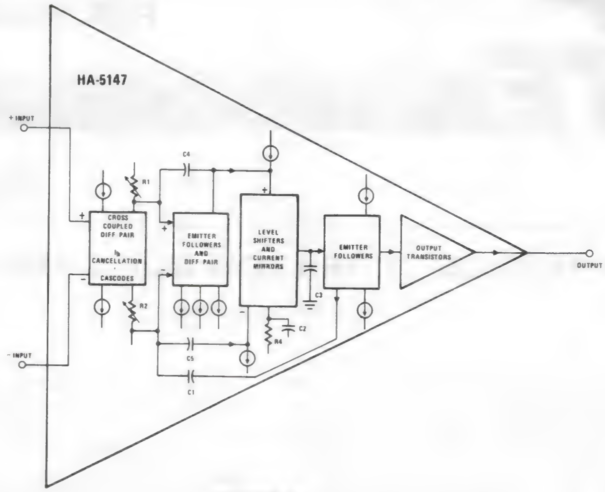


FIGURE 2.

Intense attention was given to the "total" design from inputs to output.

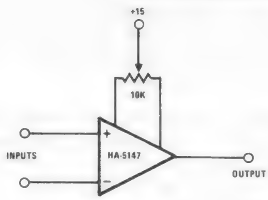


FIGURE 3a.

Nulling the HA-5147's offset voltage to 0 volts brings it closer to "ideal"

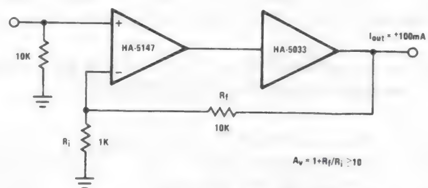


FIGURE 3b.

The HA-5147's output current can be boosted to ±100mA by using the HA-5033. AC performance is not affected.

Low Noise Design

Since the HA-51X7 is a very low noise operational amplifier, low noise design techniques must be used to make the most of this feature. There are two primary means of keeping noise down, one requires the amplifier inputs to look into low source resistances and the other requires bandwidth limiting by filtering. A short outline of noise prediction will be presented here to support these concepts.

Noise can be divided into several categories, which include thermal noise (white noise) and flicker noise (pink noise or 1/f noise). The feedback components are strongly dominated by thermal noise making thermal noise the most important of these from a system design standpoint (an exception to this are high gain DC amplifiers which require low 1/f noise as measured by the noise corner). Flicker noise is more a function of the amplifier construction quality, and system design variations are less effective in reducing this type of noise.

Noise is usually rated in one of two ways. The first is RMS voltage or current (a measure of peak-to-peak noise in a given bandwidth) and the second is by noise density spectrum in $V/\sqrt{Hz}$ and $A/\sqrt{Hz}$ (a measure of the spectral content of the noise in the frequency domain). The two rating schemes are related, with RMS noise levels generated from the integration of the noise density spectrum over a desired frequency bandwidth.

As an illustration of noise prediction, the noise density for the standard inverting amplifier configuration (Figure 4a) will be determined. The total noise is derived from the combination of several noise sources, only three of which are of any significance. These are the amplifier's noise voltage, the thermal noise of the feedback components, and the noise generated by the current noise of the amplifier within the feedback components.

The total noise is defined as the square root of the sum of the squares of the individual noise terms.

$$E_n = G\sqrt{(E_{amp})^2 + (E_{\substack{\text{feedback}\\\text{network}}})^2 + (E_{\substack{\text{current noise in}\\\text{feedback network}}})^2}$$

E_n = total noise

G = gain of stage

E_{amp} = amplifier noise voltage........$3.0nV/\sqrt{Hz}$ @ f > 1KHz

$$E_{\substack{\text{feedback}\\\text{network}}} = \sqrt{4KTR_{eq}}$$

where... $K = 1.381E-23$
$T = 300$
$R_{eq} = R \,||\, R_f$

$$E_{\substack{\text{current noise in}\\\text{feedback network}}} = I_{noise} R_{eq}$$

$I_{noise} = 0.4pA/\sqrt{Hz}$ @ f > 1KHz

or more specifically . . .

$$E_n = G\sqrt{(E_{amp})^2 + R_{eq}4KT + (I_{noise} R_{eq})^2}$$

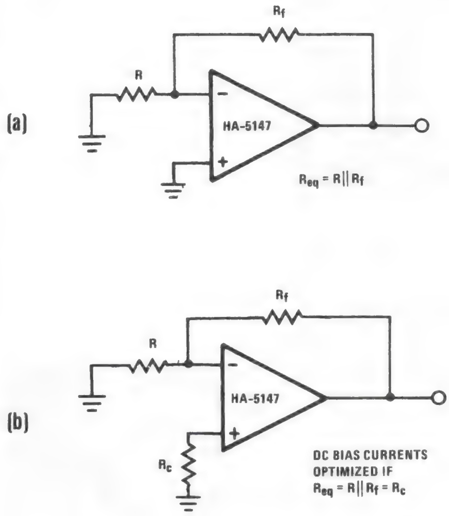


FIGURE 4. NOISE PREDICTION CIRCUITS

A reasonable estimate of noise levels can be generated with these two basic amplifier circuits.

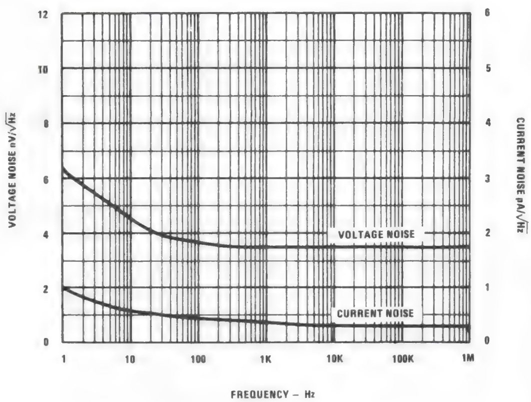


FIGURE 5. HA-5147 NOISE CHARACTERISTICS

The HA-5147's exceptional noise characteristics may be used to improve existing and new high quality audio systems. HA-5127 and HA-5137 have identical noise characteristics.

Both the amplifier noise voltage and noise current are constant above 1KHz and rise slightly for lower frequencies (Figure 5). The resistor thermal noise is derived from the parallel combination of the feedback network (R_{eq}) and several constants (4KT). The third noise term again uses the equivalent resistance of the feedback network (R_{eq}) as well as the current noise generated at the input terminals of the amplifier.

It should be evident from the above formula that extremely large values of R_{eq} (especially over 10Kohm) will dominate the noise density while low values for R_{eq} will yield to the amplifier's own noise characteristics. Note the asyptotic convergence of the noise voltages in Figures 3a-3c at low values of R_{eq}.

A second circuit (Figure 4b) balances the effects of input bias currents by placing a resistor R_C, equal to R_{eq}, between the non-inverting input and ground. While reducing DC errors, this configuration adds two additional terms to the noise formula.

$$E_n = G\sqrt{(E_{amp})^2 + R_{eq}4KT + (I_{noise}\,R_{eq})^2 + R_C\,4KT + (I_{noise}\,R_C)^2}$$

The original contributors to output noise remain as before and the additional terms represent the thermal contribution by R_C and the associated amplifier current noise seen through that resistor. To optimize DC design, $R_{in} \parallel R_f = R_{eq} = R_C$, therefore the noise density equation reduces to . . .

$$E_n = G\sqrt{(E_{amp})^2 + 2R_{eq}4KT + 2(I_{noise}\,R_{eq})^2}$$

Again the relationship between large values of R_{eq} and a high noise density spectrum remains.

RMS noise is derived in part as the integral of the noise density spectrum over a given bandwidth. Below is the complete expression . . .

$$E_{rms}\ (\text{from } f_0 \text{ to } f_1) = \sqrt{\int_{f_0}^{f_1} E_{\substack{\text{noise}\\\text{density}\\\text{spectrum}}}^{\,2}\,df}$$

The strict integration assuming E_n is constant works well for f_0 above ≈ 1KHz. Both the amplifier's noise voltage and the noise current increase for frequencies below 1KHz. This makes for difficult integration since complicated expressions for I_{noise} and E_{amp} must be generated. To avoid this problem, graphical integration techniques or sampled methods can be used with great success.

The curves in Figures 6a-6c illustrate the relationship between the RMS noise and R_{eq} for both amplifier designs. It should be apparent from the predicted RMS noise curves that increased bandwidth causes an increase in noise voltage. An interesting effect of this relationship is that only absolute bandwidth (f_1-f_0) is important. The general frequencies of interest (if they are above 1KHz) are irrelevant. More simply, 100Hz of bandwidth near 10KHz contains as much noise as 100Hz of bandwidth near 1MHz. This implies that bandwidth should be restricted with appropriate high and low pass filtering, if the lowest noise voltages are to be attained.

From the previous discussion, it is apparent that low noise designs require low resistor values. This is not to say that high gain should be avoided, just that low input and source resistance values are required for low noise opera-

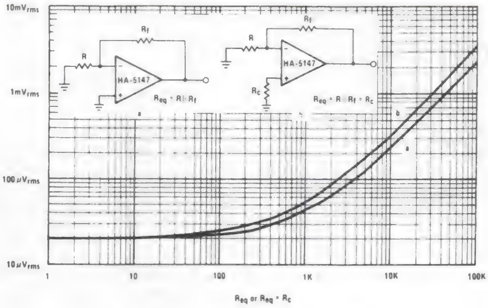


FIGURE 6a. PREDICTED NOISE

Predicted RMS noise at output for bandwidth of 10KHz - 500KHz for HA-5147.

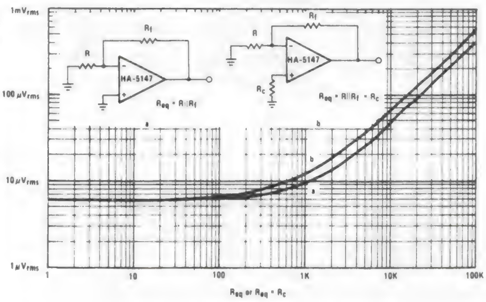


FIGURE 6b. PREDICTED NOISE

Predicted RMS noise at output for bandwidth of 20Hz - 20KHz for HA-5147.

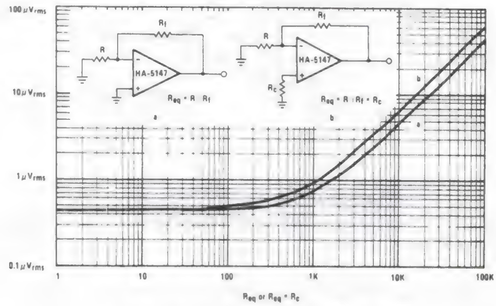


FIGURE 6c. PREDICTED NOISE

Predicted RMS noise at output for bandwidth of 10Hz - 100Hz for HA-5147.

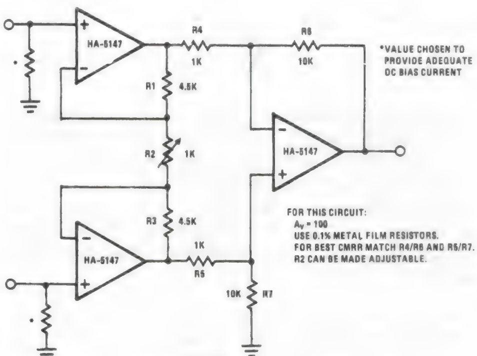


FIGURE 7. INSTRUMENTATION AMPLIFIER

Thanks to higher speed and more bandwidth, this standard three amplifier instrumentation amplifier will have 10MHz bandwidth and 550KHz power bandwidth.

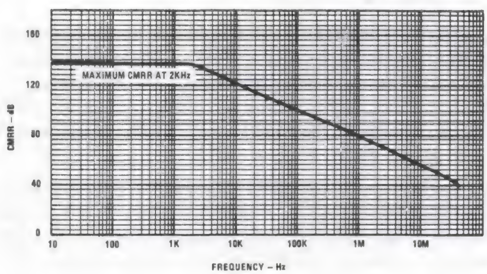


FIGURE 8. HA-5147 CMRR VS. FREQUENCY

The instrumentation amplifier's maximum CMRR can now be moved to much higher frequencies when using the HA-5147.

tion. Closer examination of the RMS noise formula will also show that limiting bandwith, with filtering, will also reduce noise levels. Additionally, metal film and wirewound resistors have lower excess noise (a component of resistor noise in addition to thermal noise) than carbon resistors and are therefore preferred.

Applications

Heavily used throughout the world of signal processing is the instrumentation amplifier and it is this particular circuit that can best utilize all of the features of the HA-5147. By using the HA-5147, the standard 3 amplifier instrumentation circuit (Figure 7) is now able to extend its bandwidth to 10MHz or its power bandwidth to 500KHz. Additionally, the maximum CMRR (>120dB) is extended to higher frequencies (Figure 8). Other "error producing" input referred parameters of the HA-5147 such as noise, V_{OS}, I_{bias}, V_{OS} drift and temperature coefficients have been minimized, thus maximizing the capabilities of this application.

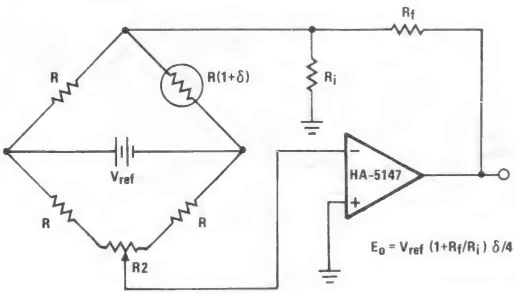


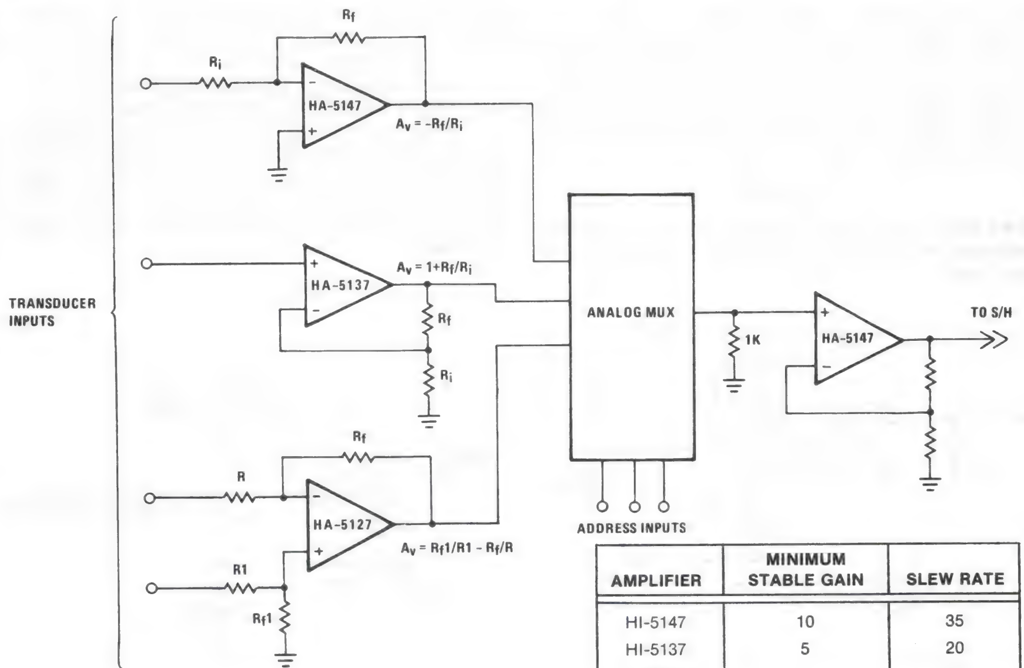
FIGURE 9. LOW LEVEL BRIDGE AMPLIFIER

Very small bridge signals are sensed and amplified accurately when using the precision performance of the HA-5147

Another circuit requiring very accurate amplification of its signal is the transducer bridge amplifier (Figure 9). The HA-5147, shown in an inverting bridge amplifier configuration, is recommended when it is necessary to detect very small bridge level signals. Its high open loop gain (>120dB), low noise, and excellent values for V_{OS}, V_{OS} drift, and bias current provide exceptional sensitivity to the smallest transducer variations. Full scale calibration of this circuit is made possible by placing a small valued potentiometer in series with R_i. Nulling is accomplished with R2.

The high slew rate (37V/μs) and the excellent output current drive (±20mA min.) make HA-5147 highly suitable as an input output buffer amplifier for analog multiplexers (Figure 10). The precision input characteristics of the HA-5147 help simplify system "error budgets" while its speed and drive capabilities provide fast charging of the multiplexer's output capacitance. This eliminates any increased multiplexer acquisition time, which can be induced by more limited amplifiers. The HA-5147 accurately transfers information to the next stage while effectively reducing any loading effects on the multiplexer's output.

Staying within the realm of signal processing, another standard and much used circuit configuration can be enhanced by the speed and precision of the HA-5147. A precision threshold detector (Figure 11) requires low noise, low and stable offset voltage, high open loop gain, and high speed. These requirements are met by the HA-5147, while adding excellent CMRR and PSRR to the list. The standard variations of this circuit can easily be implemented using the HA-5147. For example, hysteresis can be generated by adding R1 to provide a small amount of positive feedback. The circuit becomes a pulse width modulator if V_{ref} and the input signal are left to vary. Although the output drive capability of this device is excellent, the optional buffering circuit may be used to drive heavier loads while preventing loading effects on the amplifier.



AMPLIFIER	MINIMUM STABLE GAIN	SLEW RATE
HI-5147	10	35
HI-5137	5	20
HI-5127	1	10

FIGURE 10. HIGH SPEED INPUT/OUTPUT ANALOG MULTIPLEXER BUFFERING

Reduced "error" budgets and higher speeds of operation are easily achieved when the combined speed and precision of the HA-51X7 are used in these buffer amplifier applications.

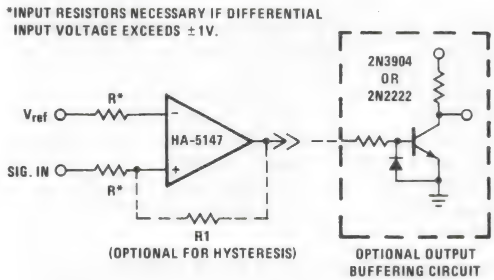


FIGURE 11. PRECISION THRESHOLD DETECTOR

This device can be used to increase response times while maintaining precise detection.

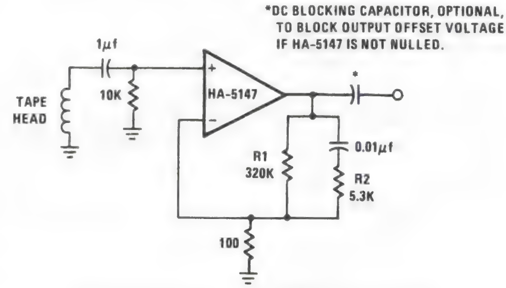


FIGURE 13. PROFESSIONAL AUDIO NAB TAPE PLAYBACK PREAMPLIFIERS

This NAB tape playback preamplifier fully utilizes the speed, bandwidth, and noise features of the HA-5147

Engineers working with professional audio designs will find the HA-5147 highly desirable for many of their applications. With its exceptional noise characteristics (Figure 5), wide power bandwidth (500KHz), and modest power consumption (85mW), this device can be used as a high quality audio preamplifier or as an intermediate stage gain block. A circuit similar to that in Figure 3b can be incorporated into studio or stage monitors.

The audio preamplifier of Figure 3b has a limited output current range. The audio power amplifier in Figure 12 overcomes this limitation and can provide an even greater boost to the HA-5147. Q1 and Q2 are a complementary pair arranged in a push pull manner, with R1 and R2 providing the necessary drive current. The maximum output voltage corresponds to the minimum output current since

$$(15\text{-}V_{be}\text{-}V_O)/R1$$

is the drive current to the transistors. D1 and D2 insure the proper biasing of the transistors as well as a clean crossover from Q1 to Q2.

An audio circuit which can make maximum use of the speed, bandwidth, and low noise of the HA-5147 is the NAB tape playback preamplifier (Figure 13). This circuit is configured to provide low frequency boost to 50Hz, flat response to 3KHz, and high frequency attenuation above 3KHz. Compensation for variations in tape and tape head performance can be achieved by trimming R1 and R2.

Signal generation applications will also find this high precision device useful. As an astable multivibrator (Figure 14) the power bandwidth of the HA-5147 extends the circuit's frequency range to approximately 500KHz. R_t can be made adjustable to vary the frequency if desired. Any timing errors due to V_{OS} or I_{bias} have been minimized by the precision characteristics of the HA-5147. D1 and D2, if used, should be matched to prevent additional timing errors. These clamping diodes may be omitted by tying R_t and the positive feedback resistor Rf directly to the output.

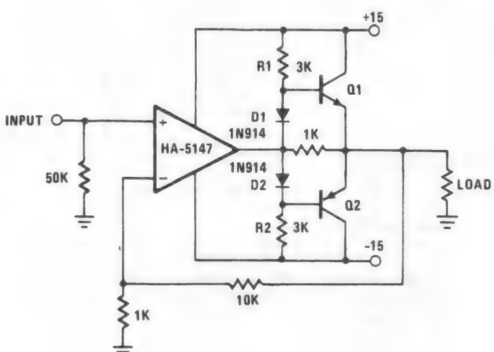


FIGURE 12. HIGH POWER AMPLIFIER

The additional drive capability of the power transistors allows the HA-5147 to drive very heavy loads.

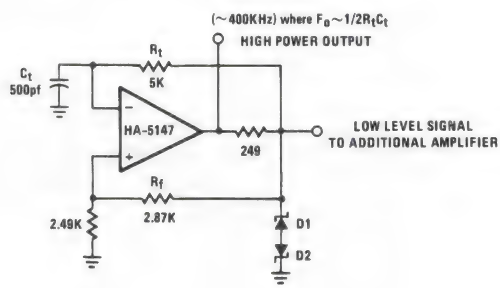
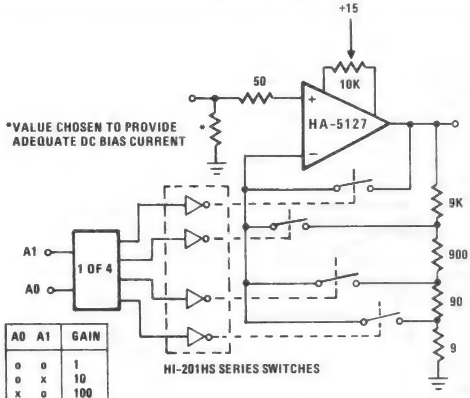


FIGURE 14. ASTABLE MULTIVIBRATOR

Higher frequencies of operation and reduced timing errors make the HA-5147 an attractive building block in signal generation applications.



A0	A1	GAIN
o	o	1
o	x	10
x	o	100
x	x	1000

FIGURE 15. PROGRAMMABLE AMPLIFIER

Variable gain of 1, 10, 100, 1000 is achieved by selecting the proper amount of feedback with the use of analog switches.

Often a circuit will be called upon to perform several functions. In these situations the variable gain configuration of Figure 15 may be quite useful. This programmable gain stage depends on CMOS analog switches to alter the amount of feedback and thereby the gain of the stage. Placement of the switching elements inside the relatively low current area of the feedback loop, minimizes the effects of bias currents and switch resistance on the calculated gain of the stage. Voltage spikes may occur during the switching process, resulting in temporarily reduced gain because of the make-before-break operation of the switches. This can be minimized by providing a separate voltage divider network for each level of gain.

Many signal processing applications depend on low noise characteristics for their operation. One such application involves logrithmic amplifiers. The input sensitivity range is governed by the system noise in such a circuit. The HA-5147, with its low noise characteristics, can extend the basic sensitivity of the common logrithmic amplifier (Figure 16). The circuit uses a matched pair of transistors to offset the effects of temperature and quiescent currents. The final expression for V_{out} reduces to ....

$$V_{out} = -0.026(1 + R_5/R_6)\ln[20V_{in}/V_{ref}]$$

or using the schematic values ...

$$V_{out} = -\ln[2V_{in}]$$

R6 should be temperature dependent if the expression for V_{out} is to hold over an extended temperature range. The overall sensitivity is from a few millivolts to about twice V_{ref}.

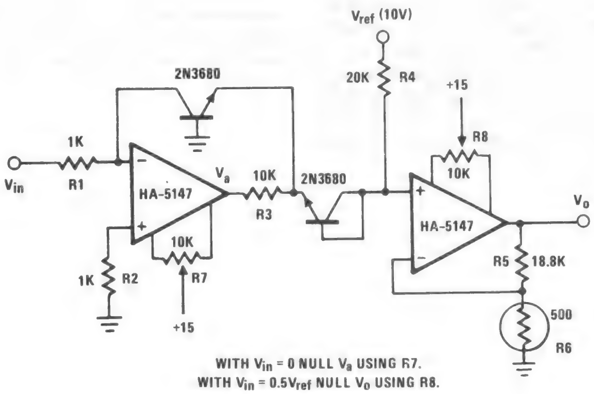


FIGURE 16. LOGRITHMIC AMPLIFIER

The matched pair of transistors makes this a very temperature stable logrithmic amplifier.

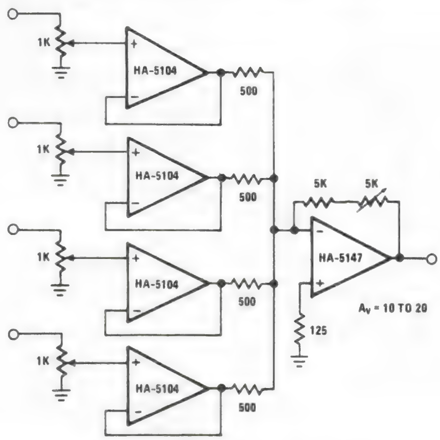


FIGURE 17. INPUT BUFFERED MIXER

Several signals can be combined using this circuit with a minimum of channel cross-talk.

A high signal to noise ratio is important in signal construction and combination. The HA-5147 aids in lowering overall system noise and thereby raises system sensitivity. The signal combination circuit in Figure 17 incorporates input buffering with several other features to form a relatively efficient mixer stage.

The potentiometer used for each channel allows for both variable input levels as well as a constant impedance for the driving source. The buffers serve mainly to prevent reverse cross-talk back through the resistor network. This allows for the combination of varying strength signals without reverse contamination. The gain of the final stage is set at a minimum of 10 and can be adjusted to as much as 20. This allows a great deal of flexibility in combining a vast array of input signals.

References

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Fitchen, F.C. and Motchenbacker, C.D. Low Noise Electronic Design, New York: John Wiley and Sons, 1973.

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APP NOTE

FOR YOUR INFORMATION

No. 554

Harris Analog

LOW NOISE FAMILY HA-5101/02/04/11/12/14

by Alan Wayne Hansford

The HA-510X/511X series is comprised of six separate products designed to meet a wide range of needs. This is accomplished, in part, by offering the HA-5101, with 10V/μs, the HA-5102/04, each with 3V/μs slew rate, the HA-5111 with 50V/μs, and the HA-5112/14, each with 20V/μs slew rate.

HA-5101	Single Amplifier	10V/μs	Unity Gain Stable
HA-5102	Dual Amplifier	3V/μs	Unity Gain Stable
HA-5104	Quad Amplifier	3V/μs	Unity Gain Stable
HA-5111	Single Amplifier	50V/μs	Gains 10 or more
HA-5112	Dual Amplifier	20V/μs	Gains 10 or more
HA-5114	Quad Amplifier	20V/μs	Gains 10 or more

The entire series shares similar design. The noise voltage and noise current will therefore be the same across the series. With a very low noise input stage at just $4.0nV/\sqrt{Hz}$ @ 1KHz, the HA-510X/511X is an excellent choice in applications where a high signal-to-noise ratio is critical, as in professional audio circuits and transducer monitors.

In addition to identical noise performance within the series, the HA-510X/511X all share common DC specifications with 0.5mV of offset voltage and 130nA of bias current. The high open loop gain, 250KV/V, together with the choice of compensation levels, will allow the HA-510X/511X series to meet a wide range of requirements.

Low Noise Design

Since the HA-510X/511X is a very low noise operational amplifier, low noise design techniques must be used to make the most of this feature. There are two primary means of keeping noise down, one requires the amplifier inputs to look into low source resistances and the other requires bandwidth limiting by filtering. A short outline of noise prediction will be presented here to support these concepts.

Noise can be divided into several categories, which include thermal noise (white noise) and flicker noise (pink noise or1/f noise). The feedback components are strongly dominated by thermal noise making thermal noise the most important of these from a system design standpoint (an exception to this are high gain DC amplifiers which require low 1/f noise as measured by the "lower 1/f noise corner"). Flicker noise is more a function of the amplifier construction quality, and system design variations are less effective in reducing this type of noise.

Noise is usually rated in one of two ways. The first is RMS voltage or current (a measure of peak-to-peak noise in a given bandwidth) and the second is by noise density spectrum in $V/\sqrt{Hz}$ and $A/\sqrt{Hz}$ (a measure of the spectral content of the noise in the frequency domain). The two rating schemes are related, with RMS noise levels generated from the integration of the noise density spectrum over a desired frequency bandwidth.

As an illustration of noise prediction, the noise density for the standard inverting amplifier configuration (Figure 1a) will be determined. The total noise is derived from the combination of several noise sources, only three of which are of any significance. These are the amplifier's noise voltage, the thermal noise of the feedback components, and the noise generated by the current noise of the amplifier within the feedback components.

The total noise is defined as the square root of the sum of the squares of the individual noise terms.

$$E_n = G\sqrt{(E_{amp})^2 + (E_{\substack{\text{feedback}\\\text{network}}})^2 + (E_{\substack{\text{current noise in}\\\text{feedback network}}})^2}$$

E_n = total noise

G = gain of stage

E_{amp} = amplifier noise voltage........$4.0nV/\sqrt{Hz}$ @ f > 1KHz

$$E_{\substack{\text{feedback}\\\text{network}}} = \sqrt{4KTR_{eq}} \qquad \text{where... } K = 1.381E\text{-}23,\ T = 300,\ R_{eq} = R \,||\, R_f$$

$$E_{\substack{\text{current noise in}\\\text{feedback network}}} = I_{noise} R_{eq}$$

$I_{noise} = 0.56pA/\sqrt{Hz}$ @ f > 1KHz

or more specifically . . .

$$E_n = G\sqrt{(E_{amp})^2 + R_{eq}4KT + (I_{noise} R_{eq})^2}$$

10 APPLICATION NOTES

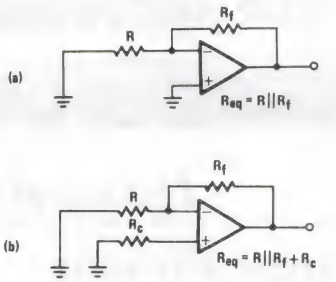


FIGURE 1.

A reasonable estimate of noise levels can be generated with these two basic amplifier circuits.

Both the amplifier noise voltage and noise current are constant above 1KHz and rise slightly for lower frequencies (Figure 2). The resistor thermal noise is derived from the parallel combination of the feedback network (R_{eq}) and several constants (4KT). The third noise term again uses the equivalent resistance of the feedback network (R_{eq}) as well as the current noise generated at the input terminals of the amplifier.

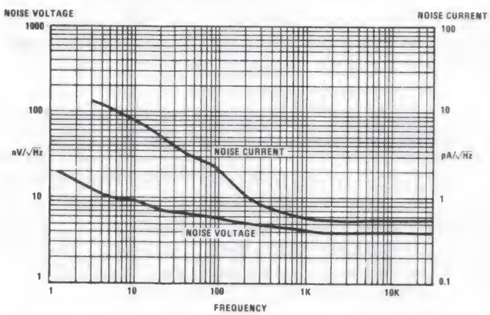


FIGURE 2.

Noise current and voltage for HA-510X/511X.

It should be evident from the above formula that extremely large values of R_{eq} (especially over 10Kohm) will dominate the noise density while low values for R_{eq} will yield to the amplifier's own noise characteristics. Note the asyptotic convergence of the noise voltages in Figures 3a-3c at low values of R_{eq}.

A second circuit (Figure 1b) balances the effects of input bias currents by placing a resistor R_C, equal to R_{eq}, between the non-inverting input and ground. While reducing DC errors, this configuration adds two additional terms to the noise formula.

$$E_n = G\sqrt{(E_{amp})^2 + R_{eq}4KT + (I_{noise}\,R_{eq})^2 + R_C\,4KT + (I_{noise}\,R_C)^2}$$

The original contributors to output noise remain as before and the additional terms represent the thermal contribution by R_C and the associated amplifier current noise seen through that resistor. To optimize DC design, $R_{in} \,||\, R_f = R_{eq} = R_C$, therefore the noise density equation reduces to ...

$$E_n = G\sqrt{(E_{amp})^2 + 2R_{eq}4KT + 2(I_{noise}\,R_{eq})^2}$$

Again the relationship between large values of R_{eq} and a high noise density spectrum remains.

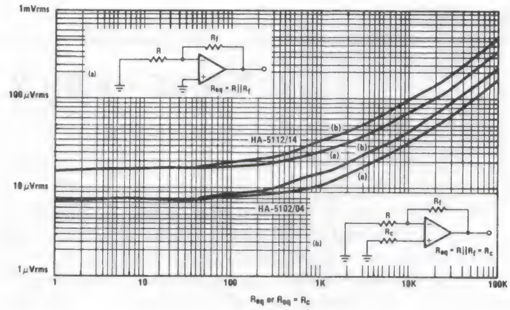


FIGURE 3a. PREDICTED NOISE

Predicted RMS noise at output for bandwidth of 0.1Hz-50KHz for HA-510X and 0.1Hz-250KHz for HA-511X.

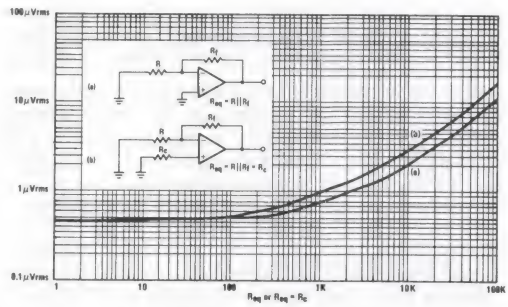


FIGURE 3b. PREDICTED NOISE

Predicted RMS noise at output for bandwidth of 20Hz-20KHz for HA-510X/511X.

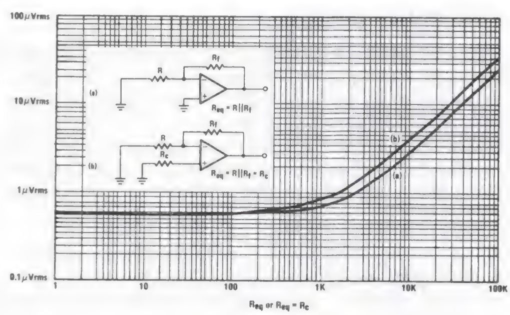


FIGURE 3c. PREDICTED NOISE

Predicted RMS noise at output for bandwidth of 20Hz-100Hz for HA-510X/511X.

RMS noise is derived in part as the integral of the noise density spectrum over a given bandwidth. Below is the complete expression...

$$E_{rms} \text{ (from } f_0 \text{ to } f_1) = \sqrt{\int_{f_0}^{f_1} E_{\substack{\text{noise}\\ \text{density}\\ \text{spectrum}}}^{2}\, df}$$

The strict integration assuming E_n is constant works well for f_0 above ≈1KHz. Both the amplifier's noise voltage and the noise current increase for frequencies below 1KHz. This makes for difficult integration since complicated expressions for I_{noise} and E_{amp} must be generated. To avoid this problem, graphical integration techniques or sampled methods can be used with great success.

The curves in Figures 3a-3c illustrate the relationship between the RMS noise and R_{eq} for both amplifier designs. It should be apparent from the predicted RMS noise curves that increased bandwidth causes an increase in noise voltage. An interesting effect of this relationship is that only absolute bandwidth (f_1-f_0) is important. The general frequencies of interest (if they are above 1KHz) are irrelevant. More simply, 100Hz of bandwidth near 10KHz contains as much noise as 100Hz of bandwidth near 1MHz. This implies that bandwidth should be restricted with appropriate high and low pass filtering, if the lowest noise voltages are to be attained.

From the previous discussion, it is apparent that low noise designs require low resistor values. This is not to say that high gain should be avoided, just that low input and source resistance values are required for low noise operation. Closer examination of the RMS noise formula will also show that limiting bandwidth, with filtering, will also reduce noise levels. Additionally, metal film and wirewound resistors have lower excess noise (a component of resistor noise in addition to thermal noise) than carbon resistors and are therefore preferred.

Applications

Electronic scales have come into wide use and the HA-510X, as a very low noise device, can improve such designs. One circuit (Figure 4) uses a strain gauge sensing element as part of a resistive Wien-bridge. An auto-zero circuit is also incorporated into this design by including a sample-and-hold network.

The bridge signal drives the inverting input of a differentially-configured HA-5102. The non-inverting input is driven by the other half of the HA-5102 used as a buffer for the holding capacitor, C_h. This second amplifier and its capacitor C_h form the sampling circuit used for automatic output zeroing. The 20Kohm resistor between the holding capacitor C_h and the input terminal, reduces the drain from the bias currents. A second resistor R_9 is used in the feedback loop to balance the effect of R_8. If R_7 is approximately equal to the resistance of the strain gauge, the input signal from the bridge can be roughly nulled with R_6.

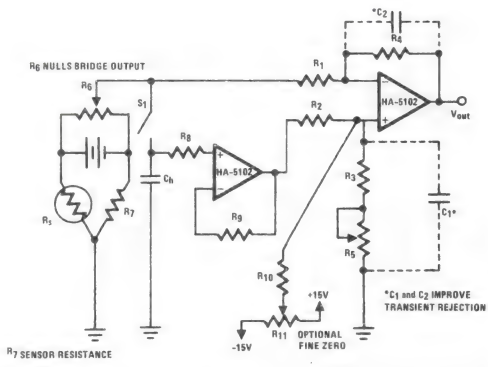


FIGURE 4.

Auto-zeroing scale circuit uses a strain gauge/bridge arrangement to improve sensitivity.

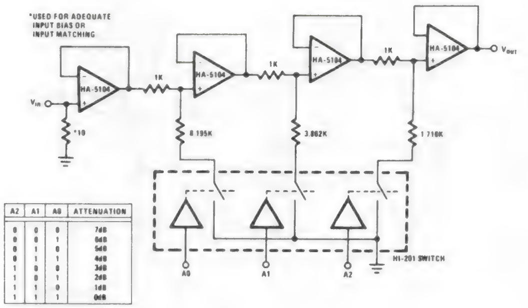
With very close matching of the ratio R_4/R_1 to R_3/R_2, the output offset can be nulled by closing S_1. This will charge C_h and provide a 0 volt difference to the inputs of the second amplifier, which results in a 0 volt output. In this manner, the output of the strain gauge can be indirectly zeroed. R_{10} and potentiometer R_{11} provide an additional mechanism for fine tuning V_{out}, but they may also increase offset voltage away from the zero point. C_1 and C_2 reduce the circuit's susceptibility to noise and transients.

The rise of digital equipment and computers, has created an entire realm of signal processing equipment. In most cases the computer requires elaborate circuitry to bridge over into the analog domain. The digitally programmable attenuator (Figure 5) is a rather simple circuit that still allows a great deal of control of analog signals.

The first stage is a simple buffer used to isolate the signal source from the attenuator stages to follow. Each of the subsequent stages is preceded by a voltage divider formed by two resistors and CMOS switch. Provided that the CMOS switch for each stage is "closed", the drive signal will be attenuated according to the basic voltage divider relationship at each stage. In the event a switch is "open" nearly all of the signal strength will be passed to the next stage through the 1K resistor. The amplifiers act as buffers for the divider networks and reduce interaction between stages. Eight levels of attenuation are possible with the circuit as illustrated in Figure 5, but more stages could be added. Each divider network must be closely matched to the resistor ratios shown or the level of attenuation will not match the levels in the logic chart.

Audio Applications

The HA-510X/511X series lends itself to audio designs. This is due in large part to the low noise characteristics of the series. With 4.0nV/$\sqrt{Hz}$ @ 1KHz, very low noise designs can be realized with little effort. This allows more attention to be placed on the quality of the designs.



A2	A1	A0	ATTENUATION
0	0	0	7dB
0	0	1	6dB
0	1	0	5dB
0	1	1	4dB
1	0	0	3dB
1	0	1	2dB
1	1	0	1dB
1	1	1	0dB

FIGURE 5.
Several resistors may be combined to obtain the precise resistor values used in this precision attenuator or a potentiometer may prove adequate.

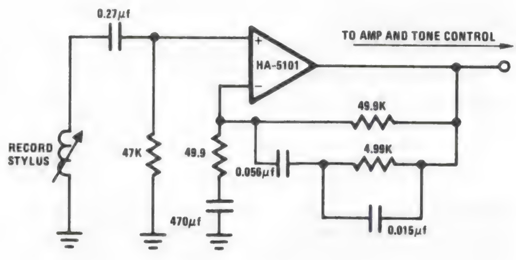


FIGURE 7.
The RIAA amplifier provides industry standard signal correction for vinyl record recordings.

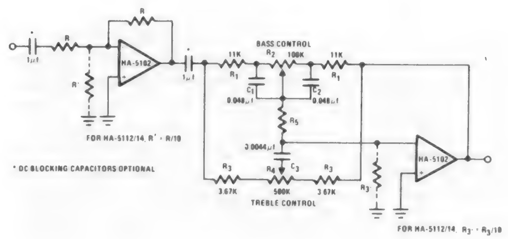


FIGURE 6.
The tone correction circuit requires a low impedance driving source, yet it provides a great deal of control over the output waveform.

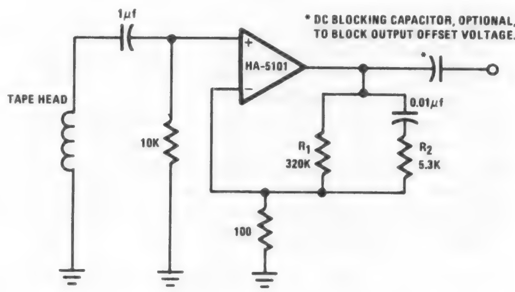


FIGURE 8. PROFESSIONAL AUDIO NAB TAPE PLAYBACK PREAMPLIFIER
This NAB tape playback preamplifier fully utilizes the speed, bandwidth, and noise features of the HA-5101.

The following group of designs point to some of the applications in which the HA-510X/511X series can improve performance without major circuit alterations. They depend, in part, on the $> \pm 20V/\mu s$ slew rate of the HA-511X, which will allow a small signal to be passed without distortion up to 12MHz. The bandwidth of these devices is more than adequate for audio use. The HA-510X will pass a full 10V signal out to 200KHz without distortion and at unity gain. Many other uses for these devices exist. The audio applications simply suggest the more likely uses for the series.

Tone correction of an audio signal is an application that relies on both the low distortion and the low noise of the HA-5102. The Baxandal-type circuit in Figure 6 uses input buffering because of the relatively low input impedance of the RC networks. The output stage is basically a summation amplifier with the high frequency contribution varied by the treble control and the low frequency by the bass control. The component values given in Figure 6 allow ±12dB of gain over the audio range.

One of the more common audio applications is signal correction for recording and playback. Several standard circuits are available and the HA-5101 should prove an excellent centerpiece for these. One such circuit is the RIAA preamplifier used to match the frequency characteristics of vinyl records and phonograph cartridges.

The RIAA circuit essentially provides low frequency boost below 318Hz and high frequency attenuation above 3150Hz. Recent modifications to the response standard include a 31.5Hz peak gain region to reduce DC oriented distortion from external vibration. The circuit in Figure 7 provides the desired response.

The NAB (magnetic tape standard) amplifier circuits are also well suited for use with the HA-5101 (Figure 8). The NAB preamplifier is configured to provide low frequency boost to 50Hz, flat response to 3KHz, and high frequency attenuation above 3KHz. Compensation for variations in tape and tape head performance can be achieved by trimming R_1 and R_2.

The low noise characteristics of the HA-510X family lead to low system noise and improved signal to noise ratios. This has become increasingly more important as the

various recording mediums have progressed to the point of near perfection, at least so far as the ear is concerned.

At the other end of the audio spectrum, opposite the playback arena, is initial sound generation and the microphone. The HA-5104/14 is a very practical choice for a dynamic microphone preamplifier (Figure 9). The relatively simple design allows for DC coupling of both input and output.

The microphone sees an input impedance equal to $R_1 + R_2$ (2Kohm). The input impedance of the amplifier group is not matched to the 600ohm impedance of the microphone. This is because the instrumentation amplifier does not rely on input power, but rather input voltage alone for its driving source. In many cases the frequency range of the microphone will be extended with the reduced loading.

R_5, R_6, and R_7 provide stable DC gain in conjunction with R_3 and R_4, which form the DC feedback network around the first two amplifiers. R_7 also controls the DC offset at the output. R_8, R_9, and C_3 provide the proper AC gain above 0.6Hz. R_{14} is tuned for maximum CMRR by matching the feedback element ratios of the third amplifier $[R_{11}/R_{10} = (R_{13} + R_{14})/R_{12}]$. With a total gain of 4dB, the 2mV microphone signal is increased to the standard $1V_{rms}$ output.

The optional output stage provides a 600ohm matched output impedance to maximize the power transfer to the next stage. The HA-5104 and the HA-5114 will both function well in this circuit. There will, however, be an extra unused amplifier. To avoid this unused amplifier the tone correction circuit in Figure 6 is recommended for use with the fourth amplifier. If the HA-5114 is used, the DC gain resistors R' and R3' in Figure 6 must be used with the tone correction circuit to insured proper DC stability.

One of the most useful circuits in audio filtering is the Biquad. This universal filter offers low pass, high pass, band pass, band elimination, and all pass functions. The HA-5104 is an excellent choice for the four amplifier Biquad circuit in Figure 10. This is due in large part to the low noise and high slew rate characteristics of the HA-5104, both of which reduce distortion effects.

The Biquad consists of two successive integration stages followed by an inverting stage. The entire group has a feedback loop from the front to the back consisting of R_1 which is chiefly responsible for controlling the center frequency, ω_0. The first stage of integration is termed a "poor" integrator because of R_2 which limits the range of integration. R_2 and C form the time constant of the first stage integrator with R_3 influencing the gain (H) almost directly. The band pass function is taken after the first stage with the low pass function taken after the third stage. The remaining filter operations are generated by various combination of the three stages.

The Biquad is "orthogonally" tuned, meaning that ω_0, Q, and gain (H) can all be independently adjusted. The component values in Figure 10 will allow ω_0 to range from 40Hz to 20KHz. The other component values give an adequate range of operation to allow for virtually universal filtering in the audio region. ω_0, Q, and gain (H) can all be independently adjusted by adjusting R_1 - R_3 respectively and in succession.

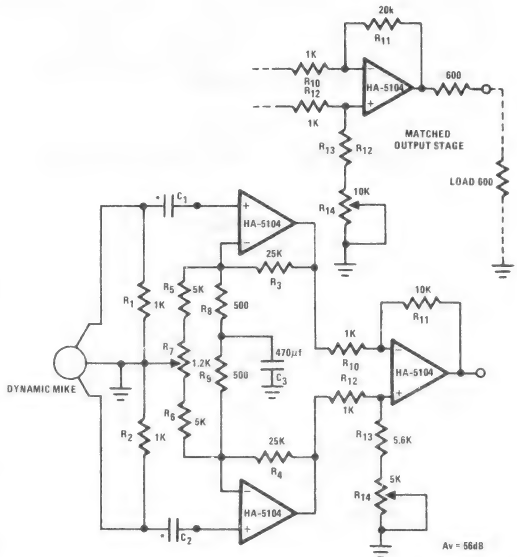
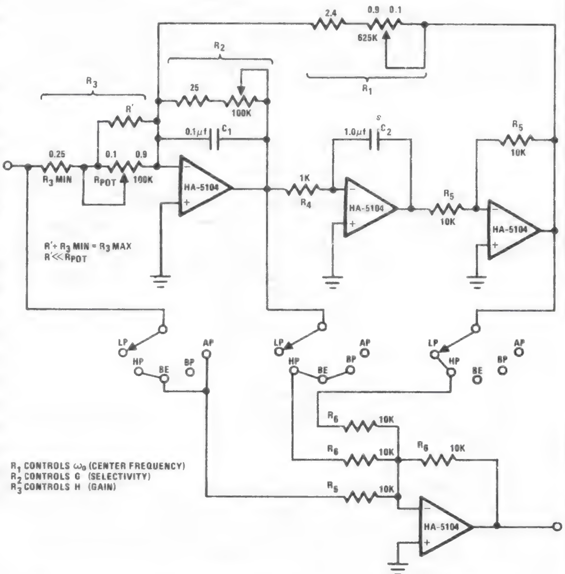


FIGURE 9.
The dynamic microphone preamplifier does not use a transformer which reduces both complexity and cost.



The biquad offers a universal filter with ω_0, Q, and gain "orthogonally" tuned.

The standard Biquad circuit in Figure 10 uses three stages of inverting amplifiers. This produces negative feedback for stability (any odd number of stages would produce the same effect). There, however, is no restriction such that only inverting stages must be used. The standard Biquad of Figure 10 has been altered in Figure 11 by combining the function of the last two stages into one non-inverting integrator. This reduces the number of amplifiers required for the band pass function to just two. The bandpass transfer function is of course altered to reflect the consolidation of the last two stages and is as follows...

$$\frac{V3}{V1} = \frac{-R_1R_2R_3Cs}{(R_1R_2R_3R_4CC)s^2 + (R_1R_2R_3R_4C)s + 2R_2R_3}$$

$$= \frac{-(1/R_3C)s}{s^2 + (1/R_2C)s + 2/R_1R_4CC}$$

$$= \frac{+H\omega_o^2}{s^2 + (\omega_o/Q)s + \omega_o^2}$$

therefore....

$$\omega_o = \sqrt{2/R_1R_4CC}$$

$$Q = \sqrt{2R_2^2/R_1R_4}$$

$$H = -R_1R_4C/2R_3 \qquad \text{if } C_1 = C_2 = C$$

The two amplifier Biquad bandpass filter constructed around the HA-5102 can easily be incorporated into a ten band graphic equalizer. By restricting gain to ±12dB and requiring Q = 1.7, a very usable design can be generated. See Figure 12.

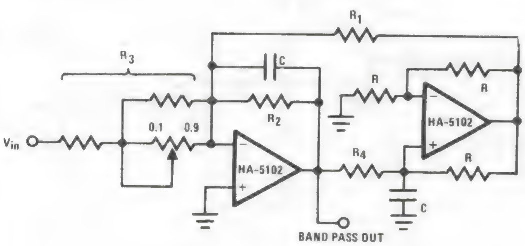


FIGURE 11.
The two amplifier biquad forms an economical band pass filter, which in this case is oriented towards a ten band equalizer.

A high signal to noise ratio is important in signal construction applications. The low noise aspect of the HA-5104 aids in lowering the system noise and thereby raises the system sensitivity. The signal combination circuit in Figure 13 incorporates input buffering with several other features to form a relatively efficient mixer stage.

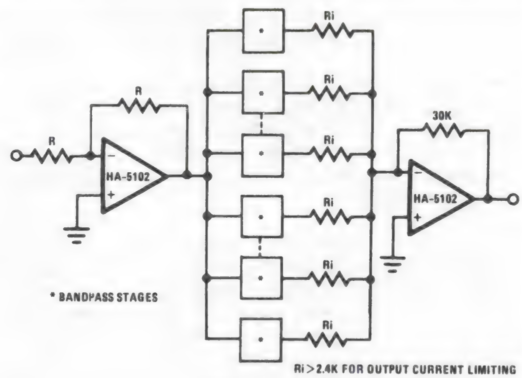


FIGURE 12.
The bandpass stages can be incorporated into a multiple band equalizer.

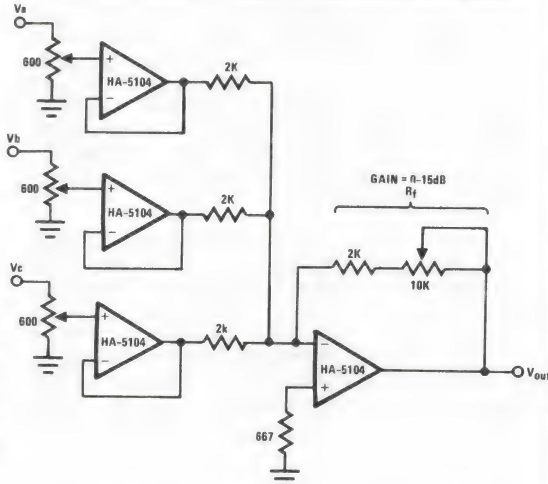


FIGURE 13.
The 600 ohm input impedance provides for proper audio level signal mixing using the HA-5104.

The circuit in Figure 13 uses buffer stages to prevent channel crosstalk back through the mixer resistor network. The potentiometers used for each stage allow for convenient signal strength adjustment while maintaining input impedance matching at the 600ohm audio standard. The feedback resistor R_f will permit the output signal gain to be as high as 15dB. The circuit in Figure 14 illustrates some of the other possible buffer combinations. These include a differential input stage, a voltage follower as well as both non-inverting and inverting stages. The allowable resistor ratios and recommended device types are also included. One restriction applies to this type of mixer network which is Rg >2.4Kohm. This limits the worst case output current for each of the input buffers to less than 10mA.

The bulk of the HA-5102/04/12/14 series applications have involved audio uses. This does not represent the full range of application of the series. In general, most

common amplifier applications, excluding video, could benefit from the group. The goal here was to introduce the designer to some of the more common and well know designs using the series, in hope of triggering interest for more extensive uses.

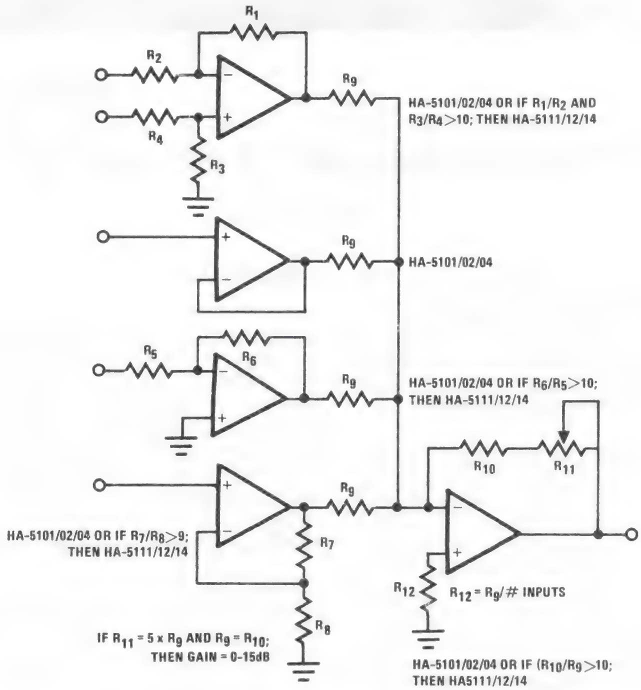


FIGURE 14.
Universal mixer stage combines the more useable configurations of the HA-510X/511X family to meet most signal construction needs.

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APP NOTE

FOR YOUR INFORMATION

No. 555

Harris Analog

ULTRA LOW BIAS AMPLIFIER, HA-5180

by Alan Wayne Hansford

Most amplifiers depend on the voltage at the inputs to determine the output voltage, and require a parasitic input bias current for proper operation. Typically these currents are in the μA range, but they needn't be so large. A very few devices fall into the ultra low bias current group which ranges from fA levels to a few pA. The HA-5180 is one of the few, with only 250fA of Bias current.

DC offset errors are created at the output of most amplifiers from the interaction of input bias currents with circuit resistances. If bias currents are significantly reduced, as with the HA-5180, the DC errors are also significantly reduced. This implies that with very low bias currents, larger resistances can be used without creating a DC error that exceeds normal bias current/resistance combinations. A great many high source impedance applications are only practical with some means of bias reduction, typically FET buffering. The ultra-low bias amplifiers, like the HA-5180, eliminate the need for FET buffering with its FET input stage. This makes the HA-5180 particularly well suited for atomic particle detectors and precision sampling circuits, to name two.

The outstanding features of the HA-5180 do not end simply at input bias current, but combine to form a very usable device. The Common Mode Rejection Ratio (CMRR) and Power Supply Rejection Ratio (PSRR) are both examples of this. The rejection of a common signal appearing at both input terminals of the device is 105dB (CMRR) and the rejection of power supply fluctuations is 110dB (PSRR). The open loop gain is a very respectable 1000KV/V. All of these outstanding features reflect the quality built into the HA-5180.

Given the type of device and the primary emphasis on low input bias currents, the HA-5180 has several other points worthy of praise. The basic speed of the device with a 2MHz bandwidth and a 7V/μSec slew rate, is above average and noteworthy for any amplifier. This becomes even more apparent in light of the low supply current (0.8mA). The relationship between supply current and speed usually implies that a high speed device requires a high supply current. Yet, the design of the HA-5180 has judiciously metered its use of available supply current to optimize speed at gains as low as unity.

Building Tips

The HA-5180 was designed with high performance in mind as indicated by its parameter list. The design enhancements did not stop at the drawing board however, and have been brought into the user's control. The most interesting development is the case connection to pin 8 of the can. By grounding the can through pin 8, a high level of shielding may be easily implemented. The effects of shielding should be further increased by using a grounding plane under the HA-5180. Both of these techniques will also improve the heat transfer away from the chip and package to extend the operational safety margins.

The remarkably low input bias currents are extremely important to many applications. They, in spite of their merit, can not stand alone in every circuit design. For this reason the voltage offset pins were included in the design of the HA-5180. With pins 1 and 5 (Figure 1), the offset voltage can be reduced below the very acceptable value of 100μV, establishing an amplifier with nearly ideal characteristics.

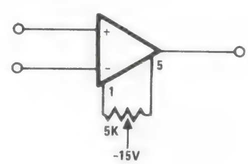


FIGURE 1.
Nulling the HA-5180s offset adjust to 0 volts brings it closer to the "ideal".

Low Noise Design

Since the HA-5180 is a moderately low noise operational amplifier, low noise design techniques must be used to make the most of this feature. There are two primary means of keeping noise down, one requires the amplifier inputs to look into low source resistances and the other requires bandwidth limiting by filtering. A short outline of noise prediction will be presented here to support these concepts.

Noise can be divided into several categories, which include thermal noise (white noise) and flicker noise (pink noise or 1/f noise). The feedback components are strongly dominated by thermal noise making thermal noise the most important of these from a system design standpoint (an exception to this are high gain DC amplifiers which require low 1/f noise as measured by the lower "1/f noise corner"). Flicker noise is more a function of the amplifier construction quality, and system design variations are less effective in reducing this type of noise.

Noise is usually rated in one of two ways. The first is RMS voltage or current (a measure of peak-to-peak noise in a given bandwidth) and the second is by noise density spectrum in $V/\sqrt{Hz}$ and $A/\sqrt{Hz}$ (a measure of the spectral content of the noise in the frequency domain). The two rating schemes are related, with RMS noise levels generated from the integration of the noise density spectrum over a desired frequency bandwidth.

As an illustration of noise prediction, the noise density for the standard inverting amplifier configuration (Figure 2a) will be determined. The total noise is derived from the combination of several noise sources, only three of which are of any significance. These are the amplifier's noise voltage, the thermal noise of the feedback components, and the noise generated by the current noise of the amplifier within the feedback components.

The total noise is defined as the square root of the sum of the squares of the individual noise terms.

$$E_n = G\sqrt{(E_{amp})^2 + (E_{\substack{\text{feedback}\\ \text{network}}})^2 + (E_{\substack{\text{current noise in}\\ \text{feedback network}}})^2}$$

E_n = total noise
G = gain of stage
E_{amp} = amplifier noise voltage.........$70nV/\sqrt{Hz}$ @ $f > 1KHz$

$$E_{\substack{\text{feedback}\\ \text{network}}} = \sqrt{4KTR_{eq}} \quad \text{where...} \quad K = 1.381E\text{-}23,\; T = 300,\; R_{eq} = R\,||\,R_f$$

$$E_{\substack{\text{current noise in}\\ \text{feedback network}}} = I_{noise}R_{eq}$$

$$I_{noise} = 0.01pA/\sqrt{Hz} \text{ @ } f > 1KHz$$

or more specifically . . .

$$E_n = G\sqrt{(E_{amp})^2 + R_{eq}4KT + (I_{noise}R_{eq})^2}$$

Both the amplifier noise voltage and noise current are constant above 1KHz and rise slightly for lower frequencies (Figure 3). The resistor thermal noise is derived from the parallel combination of the feedback network (R_{eq}) and several constants (4KT). The third noise term again uses the equivalent resistance of the feedback network (R_{eq}) as well as the current noise generated at the input terminals of the amplifier.

It should be evident from the above formula that extremely large values of R_{eq} (usually over 10Kohm, but

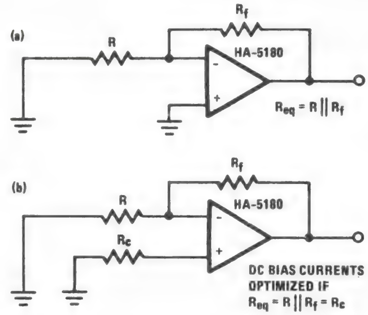


FIGURE 2. NOISE PREDICTION CIRCUITS

A reasonable estimate of noise levels can be generated with these two basic amplifier circuits.

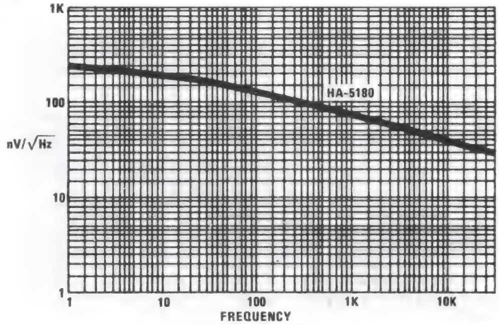


FIGURE 3. NOISE VOLTAGE

Due to the extremely low noise currents, only the voltage noise generates a significant contribution.

1Megohm for the HA-5180) will dominate the noise density while low values for R_{eq} will yield to the amplifier's own noise characteristics. Note the asyptotic con vergence of the noise voltages in Figures 4a-4c at low values of R_{eq}.

A second circuit (Figure 2b) balances the effects of input bias currents by placing a resistor R_C, equal to R_{eq}, between the non-inverting input and ground. While reducing DC errors, this configuration adds two additional terms to the noise formula.

$$E_n = G\sqrt{(E_{amp})^2 + R_{eq}4KT + (I_{noise}R_{eq})^2 + R_C\,4KT + (I_{noise}R_C)^2}$$

The original contributors to output noise remain as before and the additional terms represent the thermal contribution by R_C and the associated amplifier current noise seen through that resistor. To optimize DC design, $R_{in}\,||\,R_f = R_{eq} = R_C$, therefore the noise density equation reduces to ...

$$E_n = G\sqrt{(E_{amp})^2 + 2R_{eq}4KT + 2(I_{noise}R_{eq})^2}$$

Again the relationship between large values of R_{eq} and a high noise density spectrum remains.

RMS noise is derived in part as the integral of the noise density spectrum over a given bandwidth. Below is the complete expression...

$$E_{rms} \text{ (from } f_0 \text{ to } f_1) = \sqrt{\int_{f_0}^{f_1} E_{\substack{\text{noise}\\\text{density}\\\text{spectrum}}}^{\,2}\, df}$$

The strict integration assuming E_n is constant works well for f_0 above ≈1KHz. Both the amplifier's noise voltage and the noise current increase for frequencies below 1KHz. This makes for difficult integration since complicated expressions for I_{noise} and E_{amp} must be generated. To avoid this problem, graphical integration techniques or sampled methods can be used with great success.

The curves in Figures 4a-4c illustrate the relationship between the RMS noise and R_{eq} for both amplifier designs. It should be apparent from the predicted RMS noise curves that increased bandwidth causes an increase in noise voltage. An interesting effect of this relationship is that only absolute bandwidth (f_1-f_0) is important. The general frequencies of interest (if they are above 1KHz) are irrelevant. More simply, 100Hz of bandwidth near 10KHz contains as much noise as 100Hz of bandwidth near 1MHz. This implies that bandwidth should be restricted with appropriate high and low pass filtering, if the lowest noise voltages are to be attained.

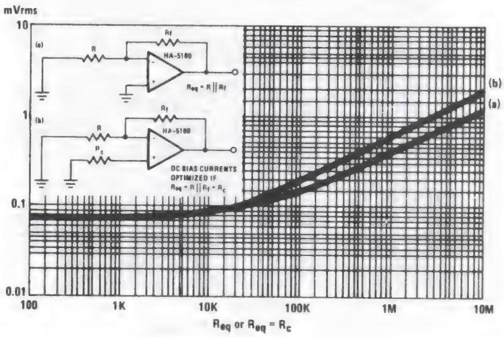


FIGURE 4a. PREDICTED NOISE

Predicted RMS noise at output of HA-5180 for a bandwidth of 0.1Hz-110KHz.

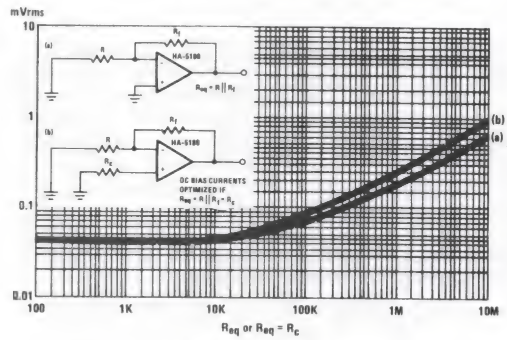


FIGURE 4b. PREDICTED NOISE

Predicted RMS noise at output of HA-5180 for a bandwidth of 20Hz-20KHz.

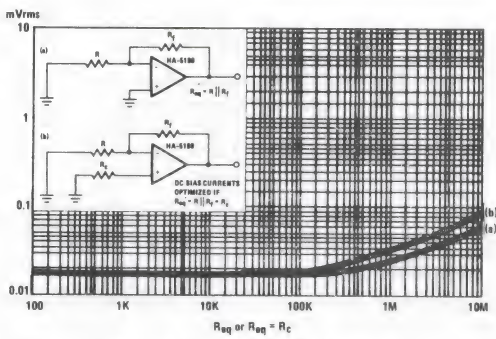
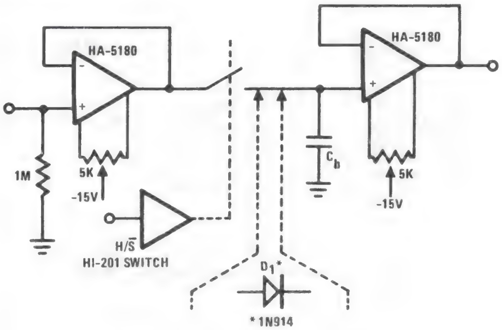


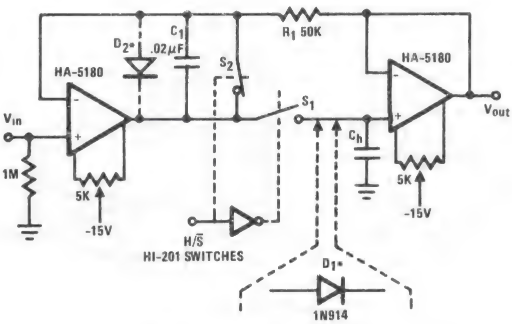
FIGURE 4c. PREDICTED NOISE

Predicted RMS noise at output of HA-5180 for a bandwidth of 20Hz-100Hz.



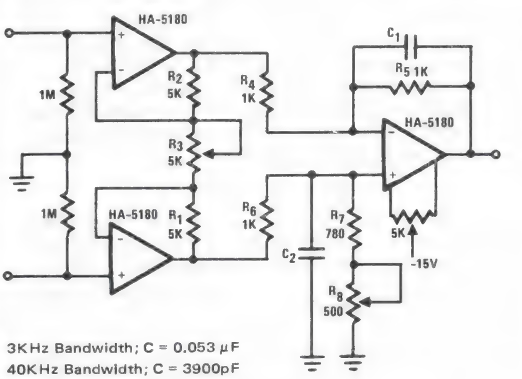
*Diode used for S/H peak detector

FIGURE 5a.
"Fast" sample-and-hold must be nulled using the offset potentiometers but offers very short aquisition times.



*Diodes used for S/H peak detector

FIGURE 5b.
"Precision" sample-and-hold is an excellent use of the HA-5180, but, because of the extended feedback, has greater overshoot.



3KHz Bandwidth; C = 0.053 μF
40KHz Bandwidth; C = 3900pF

FIGURE 6.
The standard three amplifier instrumentation configuration gives a multimeter preamplifier extremely high input impedance.

From the previous discussion, it is apparent that low noise designs require low resistor values. This is not to say that high gain should be avoided, just that low input and source resistance values are required for low noise operation. Closer examination of the RMS noise formula will also show that limiting bandwith, with filtering, will also reduce noise levels. Additionally, metal film and wirewound resistors have lower excess noise (a component of resistor noise in addition to thermal noise) than carbon resistors and are therefore preferred.

Applications

One of the most critical applications, relative to input bias currents, is the sample-and-hold. The HA-5180 requires such a low input bias current (250fA) that the drain on holding capacitors is all but eliminated. Figure 5 illustrates both a "precision" sample-and-hold as well as a "fast" sample-and-hold. Both circuits buffer the input voltage and the sampled voltage on C_h.

The "precision" circuit achieves a lower error voltage by closing the feedback loop around both amplifiers. This adds a delay to the feedback signal and increases the overshoot. The DC error voltages are reduced in this configuration and can be reduced further with the V_{OS} offset nulling potentiometers, hence the term "precision". C_1 improves transient response while R_1 provides isolation of the input and the output during the hold cycle. S_1 determines whether the holding capacitor C_h follows the input voltage or holds a previous value. The necessary feedback to the input buffer is provided by S_2 during the hold operation. D_1 converts the sample-and-hold into a peak voltage sample-and-hold. D_2 reduces the reverse saturation of the input buffer when used in the peak mode.

The "fast" sample-and-hold incorporates feedback around each amplifier separately. This makes for a much faster response, but does tend to increase DC error voltages. The effects of DC offset can be minimized with the V_{OS} offset nulling potentiometers. As with the precision sample-and-hold, S_1 controls the charging and holding operation of the holding capacitor C_h. D_1, as before, converts the circuit into a peak voltage sample-and-hold.

Like the sample-and-hold, the differential instrumentation amplifier relies on extremely high input impedance for effective operation. The HA-5180 with its JFET input stage, performs well as a multimeter preamplifier (Figure 6). The standard three amplifier configuration is used with very close matching of the resistor ratios R_5/R_4 and $(R_7 + R_8)/R6$, to insure high common mode rejection (CMRR). The gain is controlled through R_3 and is equal to $2R_1/R_3$. Additional gain can be had by increasing the ratios R_5/R_4 and $(R_7 + R_8)/R_6$.

The capacitors C_1 and C_2 improve the AC response by limiting the effects of transients and noise. Two suggested values are given for maximum transient suppression at frequencies of interest. Some of the faster

DVM's are operating at a peak sampling frequency of 3KHz, hence the 4KHz low pass time constant. The 40KHz low pass time constant for AC voltage ranges is an arbitrary choice, but should be chosen to match the bandwidth of the other components in the system. C_1 and C_2 may however, reduce CMRR for AC signals if not closely matched. Input impedances have also been added to provide adequate DC bias currents for the HA-5180 when open circuited.

Sensors And Transducers

Most passive transducers and sensors vary in resistance relative to light, sound, pressure, etc. Often the average resistance of the transducer is quite large. This presents a problem in the choice of an amplifier, since bias currents are typically high enough to create a significant error voltage ($V_{error} = I_{bias}\ R$). Extremely low input bias currents of the HA-5180 minimize this effect for the most part and allow for more conventional transducer and sensor circuits.

The circuit in Figure 7 uses a light sensitive cadmium sulfide cell to form a crude light level detecton module. If R, the sensor matching resistor, is equal to the "dark" resistance of the cadimum sulfide cell, the amplifier output will range from 0 volts to ≈12 volts as the light level ranges from "dark" to "bright". The circuit in Figure 8 operates in a similar manner but use the standard non-inverting configuration instead of the voltage follower configuration. This allows for variable gain. Although the "dark" resistance of the cadmium sulfide cell is only ≈7Kohms, the principles of operation apply to other types of detectors which require the high input impedance of the HA-5180 for reasonable linearity and useability.

An example of a high resistive value sensor that depends heavily on high amplifier input impedance is the pH probe and Detector, with the average probe resistance on the order of 100Megohms. The circuits in Figures 7 and 8 may still be used with this type of transducer, but a bridge circuit may prove more appropriate (Figure 9). The greatest sensitivity is achieved if R_1 is approximately equal to the probe resistance. The circuit can be "zeroed" with R_2 while the full scale voltage is controlled by R_5. The correlation between pH and output voltage may not be linear, which would necessitate a shaping circuit. A calibration scheme, using solutions of known pH, may prove adequate and more reliabile over a period of time due to probe variance.

The general schematic could be applied to strain gauges or any other type of resistive sensor. The key is the extremely low input bias current required by the HA-5180, which allows higher value resistances to be used without producing significant error voltages. This leads to more conventional designs with less exotic circuitry.

Along the same lines as the pH meter and light level detector, is the photo-diode current to voltage converter (Figure 10). One common use of this type of device is as a light to voltage converter for densitometers. This circuit depends on the light level/current relationship of a photo-

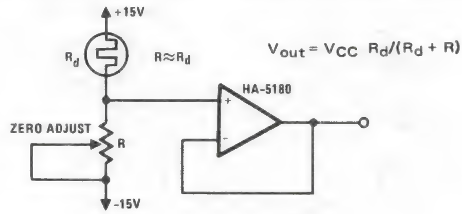


FIGURE 7.
Cadmium Sulfide cells control two light detection circuits.

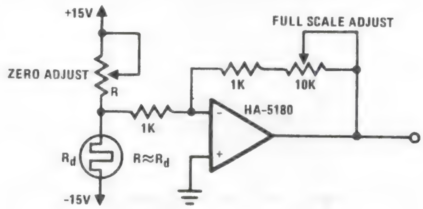
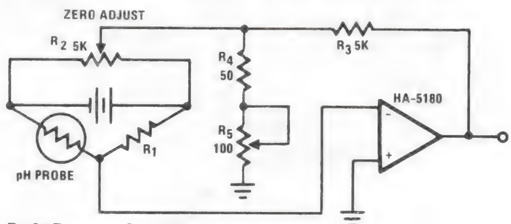


FIGURE 8.
Cadmium Sulfide cells control two light detection circuits.



$R_1 \approx R_{PROBE} \approx 100$Megohm

FIGURE 9.
Another popular sensor circuit is the bridge network. The pH probe can be replaced with nearly any resistive sensor.

diode. Since the diode will only pass as much current as the light level will allow, the diode becomes a light controlled current sink. A current source is summed along with the photo-diode current, and a difference current appears at the input of the HA-5180. Relying on ideal amplifier input impedance, which is nearly the case with the HA-5180, all of the difference current is applied to R_f. The output is then defined as . . .

$$V_{out} = (I_{ref} - I_d)R_f$$

Several current sources may be used. The simplest is a resistor with $I = (V_{CC} - V_{be})R$. A more accurate current source is the two transistor current mirror, where $I = (V_{CC} - V_{be})/R_{ref}$ (Figure 10). Since the controlling component, R_{ref}, is not in the current path for I, a more accurate summation at the amplifier input terminal can take place. The stage can be zeroed with R or R_{ref} as the case may be. The nulling potentiometer will provide the fine zero.

The precision integrator is a classic circuit which can also benefit from the JFET inputs of the HA-5180. The traditional relationship between C and R holds very well in one

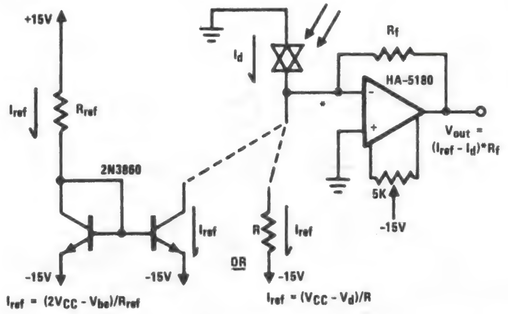


FIGURE 10.

The low bias currents of the HA-5180 provide a nearly ideal summing point (*) for the circuit currents in this photo-diode current to voltage converter.

design (Figure 11), since the drain on C by the amplifier is so small. A second HA-5180 has been incorporated into this design to allow a threshold voltage to be adjusted. The threshold voltage is set while present at the input with S_1 and S_2 closed. S_1 is opened before S_2, then S_3 is closed momentarily to reset the output voltage. The stage will then take the time integral of the input signal relative to the threshold voltage. R_2 provides stable gain during the threshold setting procedure. The nulling potentiometer reduces the effects of V_{OS}.

The precision integrator can be converted into a precision timer with a few modifications. The reset switch used to discharge the capacitor C is used as the timer on reset switch. The output will be proportional to the elapse time as long as the input voltage is constant and not equal to the threshold voltage. If the timer needs a hold function, a switch must be inserted to isolate the capacitor C from the resistor R.

Many signal processing applications depend on low amplifier bias currents for their operation. One such design involves logarithmic amplifiers (Figure 12). The input sensitivity is governed by the system bias currents in such a circuit. The HA-5180, with its low input bias currents, can extend the sensitivity of the logarithmic current to voltage converter. The specific application may well be an atomic particle counter in which the current from the detector is converted into a voltage. For the design in Figure 12 the output voltage is defined as ...

$$V_o = -V_t(R_3 + R_4)/R_3 \ln[I_{in}/I_{ref}]; \text{ where } V_t = 0.0259V.$$

Using the schematic values, the expression reduces to .....

$$V_o = -\ln[2000 I_{in}]$$

This is a typical matched transistor pair logarithmic amplifier. The matching removes a constant from the output expression and improves temperature stability. The temperature stability will be even greater if R_t varies inversely with temperature.

The input range of this circuit can be extended by using another HA-5180 as a current preamplifier to the logarithmic converter, as shown in Figure 12.

The HA-5180 is an extremely powerful building block. The sample-and-hold and the precision integrator are examples of the low drain placed on circuit capacitors by the bias currents. The bias currents themselves are nearly low enough to class the HA-5180 as an "ideal amplifier" in that respect. The transducer applications illustrate the HA-5180's merit in this area. The list of applications and uses could continue on, but the material presented should allude to the general applications and uses of the HA-5180.

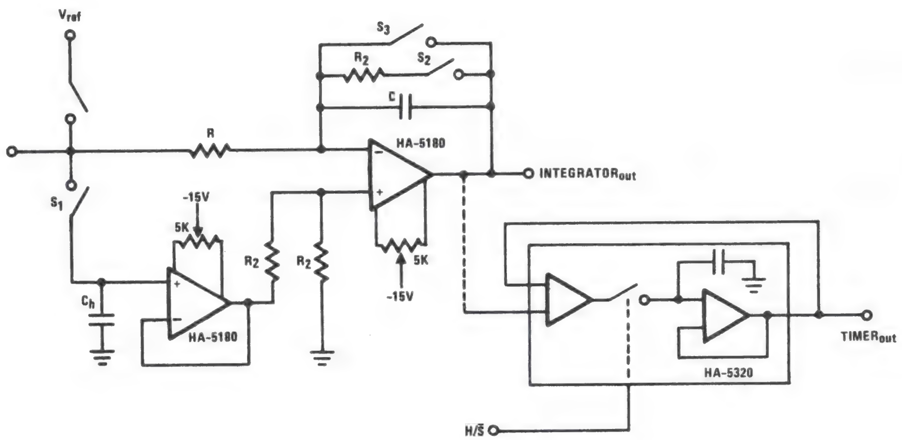


FIGURE 11.

S_1 and S_2 when closed, provide a threshold settling for this precision integrator while S_3 allows the output to be reset.

10

APPLICATION NOTES

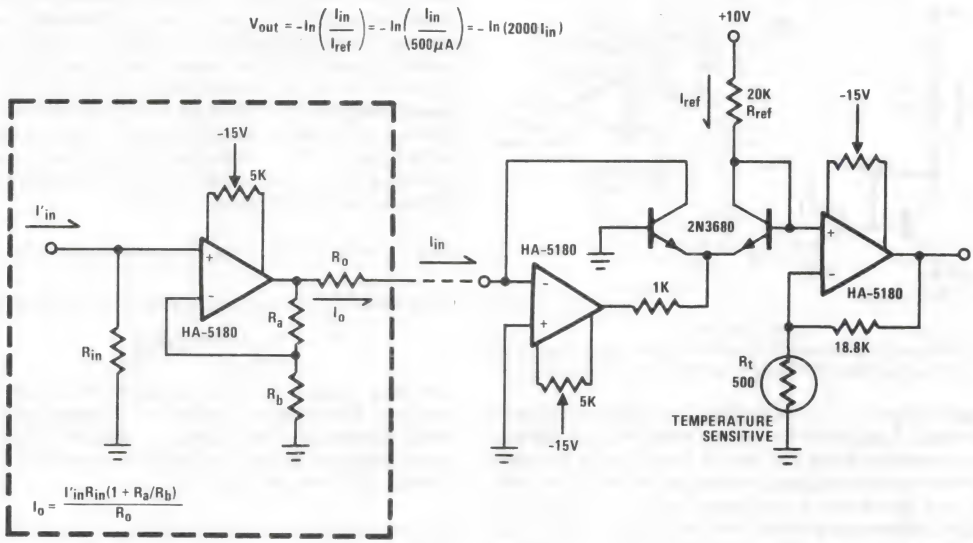


FIGURE 12

Logarithmic current to voltage converter depends on the low bias currents of the HA-5180 for accuracy.

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APP NOTE
FOR YOUR INFORMATION

No. 556

Harris Analog

THERMAL SAFE-OPERATING-AREAS FOR HIGH CURRENT OP AMPS

By: Brian Mathews

Many new Harris op amps can supply large amounts of output sink or source current. While this is a useful feature, it must be used carefully to avoid damaging or degrading the reliability of the device.

Output current contributes to the total amount of power dissipated within the amplifier according to the following formula:

TOTAL POWER = SUPPLY POWER + OUTPUT POWER

$P_{TOTAL} = [I_{CC} \times (V^+ - V^-)] + [|I_{OUT}| \times |(V_{CC} - V_{OUT})|]$

I_{CC} is the quiescent supply current and $(V^+ - V^-)$ is the total supply voltage. I_{OUT} is the amount of current flowing into or out of the output terminal and $(V_{CC} - V_{OUT})$ is the voltage across the op amp's output device.

Power dissipation generates heat and is related to temperature in the following way:

$$\text{POWER DISSIPATION} = \frac{\text{TEMPERATURE DIFFERENCE}}{\text{THERMAL RESISTANCE}}$$

The temperature difference we are interested in is the difference between the junction temperature of the circuit (T_J) and the ambient temperature (T_A). Thermal resistance is a measure of the heat conductivity of the integrated circuit, the mounting medium and the package. Different packages and die mounts have different thermal resistances measured in degrees Centigrade of temperature rise per watt of power dissipated (°C/W). Typically, integrated circuits will have two thermal resistances, θ_{ja} and θ_{jc}. θ_{ja} is the thermal resistance from the semiconductor junction to ambient air. θ_{jc} is from junction to case only. This is useful if a heat sink is used. If so, then the total thermal resistance is the sum of junction-to-case, case-to-sink and sink-to-air. Thus, for no sink, the equation is:

$$P = \frac{T_J - T_A}{\theta_{ja}}$$

Harris maintains an absolute maximum rating on junction temperature or power dissipation on all op amps. The maximum junction temperature for most Harris op amps is +175°C although some have been designed for and specified at a T_J maximum of +200°C.

We can now see that maximum allowable power dissipation depends on the ambient temperature and the thermal resistance of the package. For example, given that ambient temperature and maximum junction temperature are +25°C and +175°C respectively, assuming a thermal resistance of +100°C/W, the maximum allowable power dissipation would be:

$$P_{MAX} = \frac{175 - 25}{100} = 1.5W$$

Applying this to our output power equation we can determine the maximum allowable output current.

Assuming: $V^+ = +15V$, $V^- = -15V$, $I_{CC} = 10mA$, $V_{OUT} = \pm 5V$

recall that

$P_{TOTAL} = [I_{CC} \times (V^+ - V^-)] + [|I_{OUT}| \times (|V_{CC} - V_{OUT}|)]$

$1.5W = [(10 \times 10^{-3}) \times (30)] + [I_{OUT} \times (10)]$

I_{OUT} MAX = 0.120 = 120mA

Thus, although this device might have a rated maximum output current of 200mA, that amount of current would cause the junction temperature to exceed the absolute maximum, with the given conditions, $T_A = +25°C$, $V_{OUT} = 5V$, etc.

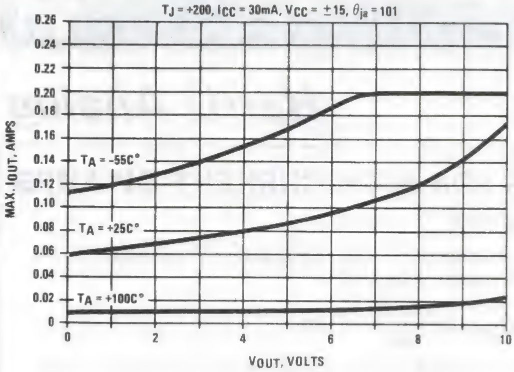
A collection of curves is included which represent graphically the maximum allowable output current over a range of output voltages. Only one quadrant is shown since it is symmetrical with respect to both axes. The graphs are entitled SOA for Safe-Operating-Area since the device can safely be operated within these boundaries. Each graph shows maximum output current for three different temperatures. The title lines indicate part type, package type, maximum T_J, assumed I_{CC} and V_{CC} levels and the package thermal resistance from junction to ambient temperature.

As long as voltage and current Maximum Limits are observed, then second breakdown effects will not be a factor in this analysis. Second breakdown must be considered for transient conditions exceeding the normal limits. This type of operation will be covered in a future report.

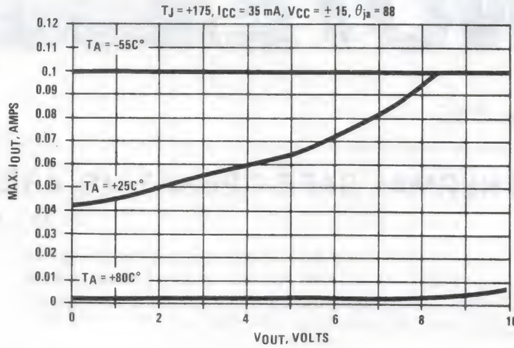
The graphs show how the output current capability is severely limited at elevated ambient temperatures. Several things can be done to help regain some of the output drive. Package choice can make a great deal of difference, be sure that the thermal implications of the package chosen are understood. Voltage supply levels are sometimes variable. Some devices, like the HA-5002, are specified at lower supply voltages. Other amplifiers may not meet all specifications but will operate with acceptable performance at reduced supply levels which will reduce quiescent power dissipation allowing greater output current levels.

DC SOA Graphs

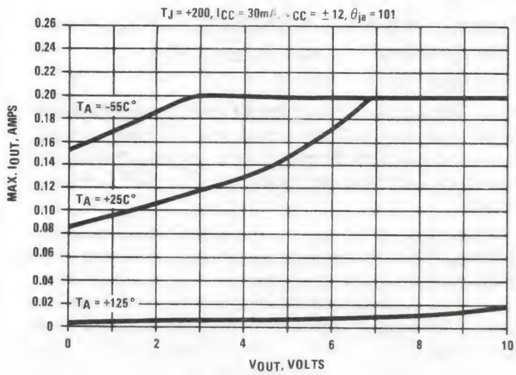
HA-5033 SOA, TO-8, NO SINK



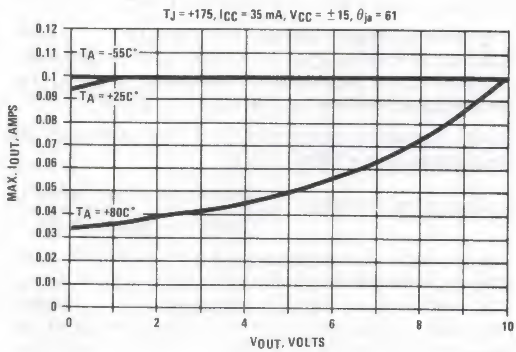
HA-2542 SOA, CERDIP, NO SINK



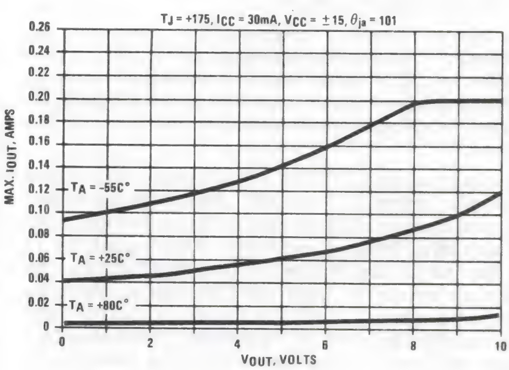
HA-5033 SOA, TO-8, NO SINK



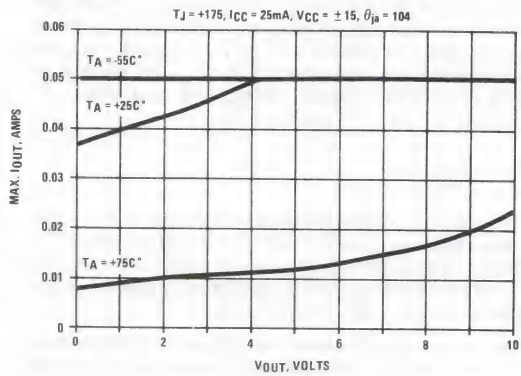
HA-2542 SOA, TO-8, NO SINK



HA-5033 SOA, TO-8, NO SINK

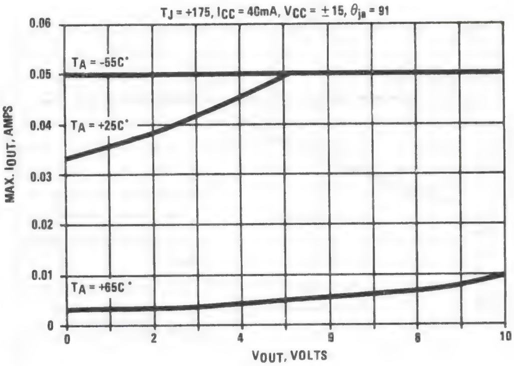


HA-2539/40 SOA, CERDIP, NO SINK

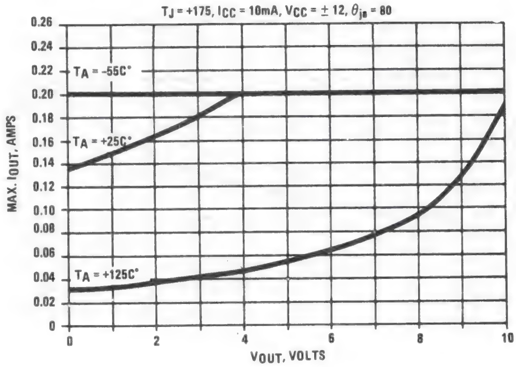


DC SOA Graphs

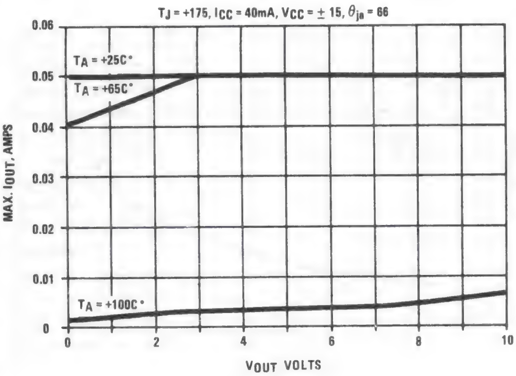
HA-2541 SOA, CERDIP, NO SINK



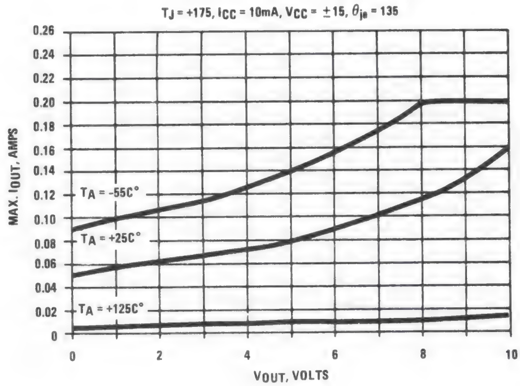
HA-5002 SOA, PLASTIC DIP, NO SINK



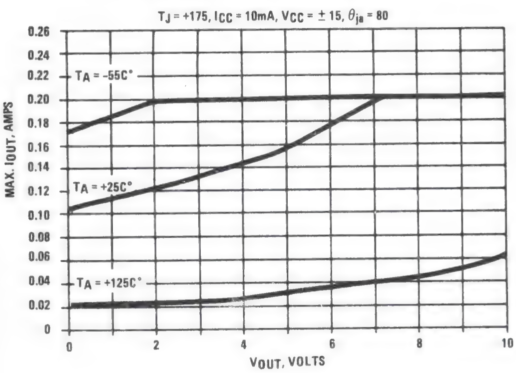
HA-2541 SOA, TO-8, NO SINK



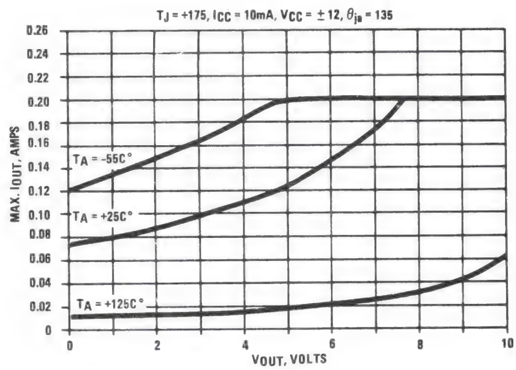
HA-5002 SOA, TO-99, NO SINK



HA-5002 SOA, PLASTIC DIP, NO SINK

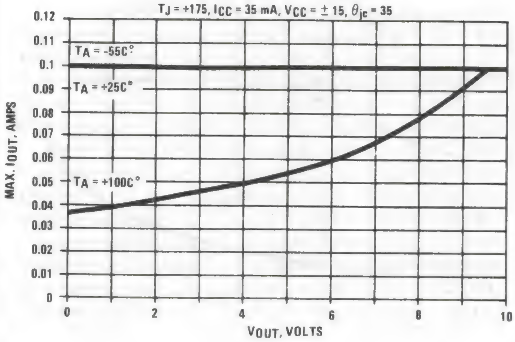


HA-5002 SOA, TO-99, NO SINK

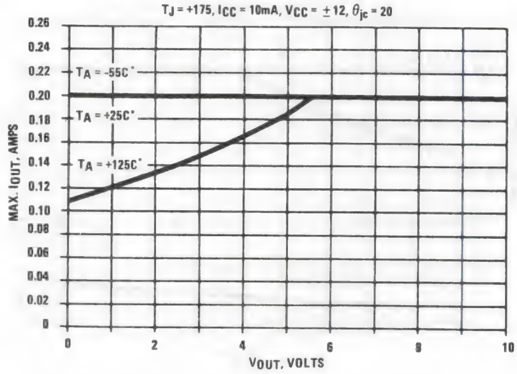


SOA Graphs With Heat Sink

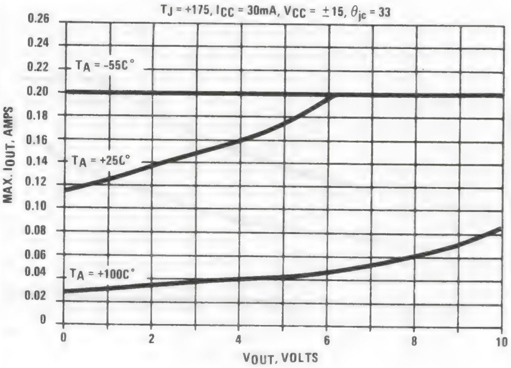
HA-2542, DIP, AAVID 5802 θ_{sa} = 15



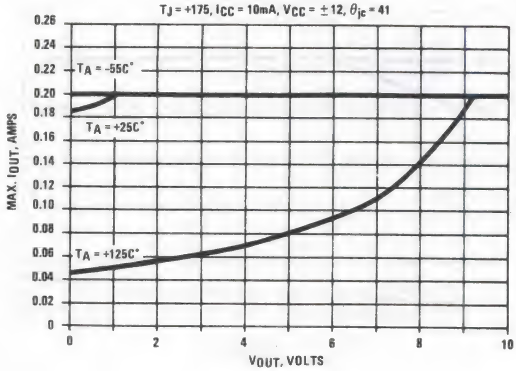
HA-5002, PLASTIC DIP, AAVID 5801 θ_{sa} = 12



HA-5033, TO-8, AAVID 5792 θ_{sa} = 25



HA-5002, TO-99, THERMALLOY 2227 θ_{sa} = 21



If package and supply voltage selection still do not allow enough current then a heat sink will be necessary. The thermal equation when a sink is used is:

$$P = \frac{T_J - T_A}{\theta_{jc} + \theta_{cs} + \theta_{sa}}$$

θ_{jc} is given in the device data sheet, θ_{cs} is from case to sink and is usually very small (one or less), and θ_{sa} is from sink to ambient and is given by the heat sink manufacturer.

Some representative curves are shown for some different types of heat sinks with different Harris part types.

Only DC steady-state conditions have been examined. AC and transient situations are not as straight forward.

The simplest way to handle the AC case is to utilize conservation of power. Thus, the output stage power drawn from the supplies is equal to the power in the load plus the power dissipated in the amplifier's output:

$$P_{SUPPLY} = P_{DISS} + P_{LOAD}$$

This discussion will assume a sine-wave output with peak voltage and current; V_P and I_P, and a resistive load, R_L.

The average power drawn from the supplies is:

$$P_{SUPPLY} = 2V_{CC}\ I_{CAVG}$$

Where I_{CAVG} is the average collector current in the output device. After calculating this current the following is obtained [1]:

$$P_{SUPPLY} = 2V_{CC} \frac{V_P}{\pi R_L}$$

The average power in the load is half the product of peak voltage and current, referred to voltage alone:

$$P_{LOAD} = \frac{V_P^2}{2R_L}$$

Thus the average power dissipated in the device's output is:

$$P_{DISS} = P_{SUPPLY} - P_{LOAD}$$

$$P_{DISS} = \frac{2V_{CC}V_P}{\pi R_L} - \frac{V_P^2}{2 R_L}$$

This figure, added to the quiescent device dissipation, should be used to determine the thermal operating conditions when the output is a sine-wave and the load is resistive. For complex waveforms or reactive loads a thorough analysis should be performed on the particular application. This obviously cannot be done in this article.

For transient conditions, thermal capacitance and second breakdown must be considered. When power is supplied by an amplifier, the junction temperature does not rise instantaneously. The different elements in the thermal path all have thermal capacitance in addition to thermal resistance. Thus, the thermal transient response is determined by a time constant which is the product of thermal resistance and capacitance. Thermal capacitance is a material dependent value and will be covered thoroughly in a follow-up article along with second breakdown. Suffice to say that most packages have thermal time constants on the order of hundreds of milliseconds so that power pulses of short duration should not raise the junction temperature appreciably. Again, transient thermal characteristics will be covered in another article.

The graphs shown here are only general guidelines. The equations are included so that specific applications can be analyzed and thermal requirements can be determined. Methods have been shown for calculating total power dissipation, maximum allowable power dissipation, and average AC power dissipation with respect to output current and voltage, ambient temperature, junction temperature and thermal resistance. Thus, Harris high output devices can be used with confidence if these techniques are used.

Bibliography:

1. Antognetti, (Ed.): "Power Integrated Circuits," New York: McGraw-Hill, 1986.

2. Gray, P. and Meyer, R.: "Analysis and Design of Analog Integrated Circuits," New York: Wiley, 1977.

Heat Sink Manufacturers:

AAVID Engineering, Inc.
One Kool Path
Box 400
Laconia, NH 03247
(603) 524-4443

Thermalloy, Inc.
P.O. Box 810839
2021 West Valley View Lane
Dallas, TX 75381-0839
(214) 243-4321

APP NOTE

FOR YOUR INFORMATION

No. 557

Harris Analog

RECOMMENDED TEST PROCEDURES FOR ANALOG SWITCHES

By: Brian Mathews

Introduction

The following text describes the basic test procedures that can be used for most Harris CMOS switches. Various test conditions are used with the various switches. Table 1 has been included to help define the specific test setups to be used with each variety of switch. One additional note, all schematics assume an open switch for high logic inputs.

DC Switch Parameters

Analog Signal Range ($+V_S$) and ($-V_S$)

The analog signal range is the maximum input signal level which can be switched to the output with minimal distortion. For supply voltages lower than nominal, the analog signal range should be restricted to the voltage span between the supplies. Note that other parameters, such as "ON" resistance and leakage currents, are guaranteed over a smaller input range and tend to degrade toward the analog limits ($+V_S$ and $-V_S$). Harris switches can tolerate the positive analog signal limit ($+V_S$) applied to one side of a switch cell while the negative analog signal limit ($-V_S$) is applied to the other side (the switch must be open to avoid excessive currents).

The analog signal range is measured (Figure 1) by increasing an input waveform until the output shows evidence of distortion or the maximum analog level is reached (as stated in the maximum ratings section of the data sheet).

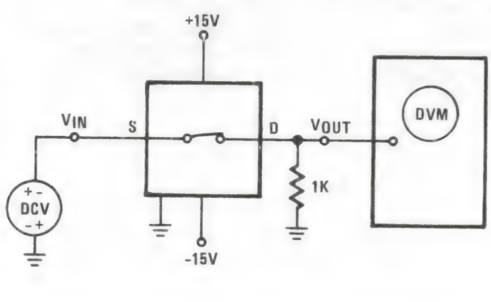
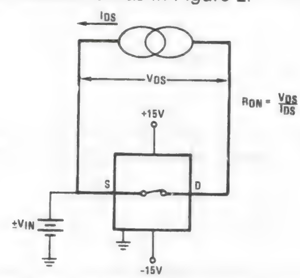


FIGURE 1. SUGGESTED CIRCUIT TO DETERMINE ANALOG SIGNAL RANGE

R_{ON}, ON Resistance (R_{DS})

"ON" resistance is the effective series on-switch resistance measured from input to output under specified conditions. Note that R_{ON} typically changes with temperature (highest at high temperature), and to a lesser degree with signal voltage and current.

R_{ON} is calculated from the voltage drop across a switch with a known current flow as in Figure 2.



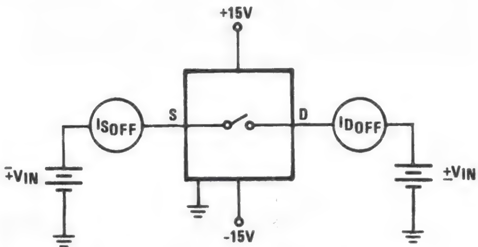
See Table 1 for Specific Test Conditions

FIGURE 2. "ON" RESISTANCE TEST CIRCUIT

$I_{S(OFF)}$, $I_{D(OFF)}$, $I_{D(ON)}$: Leakage Currents

Harris prefers to guarantee only worst case high temperature leakage currents because the room temperature picoampere levels are virtually impossible to measure repeatedly on currently available automated test equipment. Even under laboratory conditions, fixture and test equipment leakage currents may frequently exceed the device leakage currents. Since the leakage currents tend to double for every 10°C increase in temperature, it is reasonable to assume that the +25°C value is about 1/1000 the +125°C value; however, in some cases there may be ohmic leakage paths, such as across the package, which would tend to make the +25°C reading slightly higher than expected.

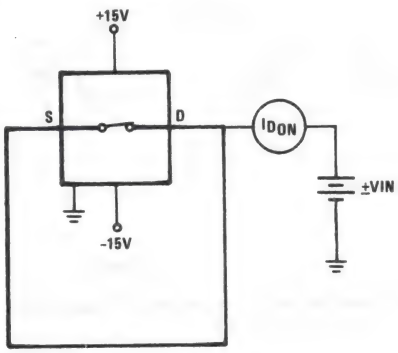
$I_{S(OFF)}$, measured directly with the circuit in Figure 3, consist largely of the diode leakage current from the source-body junction. $I_{D(OFF)}$, also measured directly with the circuit in Figure 3, is largely due to the diode leakage current in the drain-body junction.



See Table 1 for Specific Test Conditions

FIGURE 3. OFF LEAKAGE CURRENT TEST CIRCUIT

"ON" leakage current ($I_{D(ON)}$) is the current flowing through both the source-body and drain-body junctions of a closed switch. $I_{D(ON)}$ tends to have the most noticeable effect since it creates an offset voltage across the switch equal to $I_{D(ON)}$*R_{ON}. $I_{D(ON)}$ is measured directly with the circuit in Figure 4.



See Table 1 for Specific Test Conditions

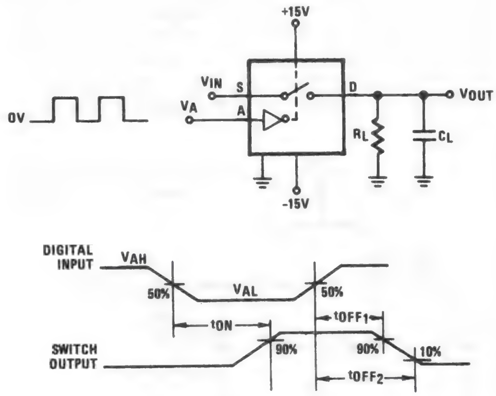
FIGURE 4. "ON" LEAKAGE CURRENT TEST CIRCUIT

Dynamic Switch Parameters

T_{ON}, T_{OFF}: Access Time

Switch "Turn On" time T_{ON} is the time required to activate an "OFF" switch to an "ON" state. T_{ON} is measured from the 50% point of the logic transition to the 90% point of the output transition (Figure 5).

Switch "Turn Off" time T_{OFF} is the time required to deactivate an "ON" switch to an "OFF" state. T_{OFF} is measured from the 50% point of the logic transition to the 10% point of the output transition (Figure 5).



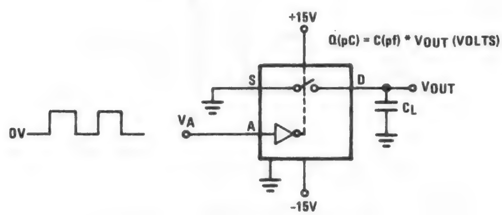
See Table 1 for Specific Test Conditions

FIGURE 5. "TURN ON" AND "TURN OFF" DELAY TEST CIRCUIT AND WAVEFORMS

Charge Injection

Cycling a switch "ON" or "OFF" results in a small amount of charge being injected into the analog signal path. This charge injection is generated through the capacitive coupling between the digital control lines and the analog outputs. The ensuing voltage spikes create an acquisition interval during which the output level is invalid even when little or no steady state level change is involved. The total net energy (charge injection) coupled onto the analog lines is especially critical when switching voltage to a capacitor since the injection charge will change the capacitor voltage at the instant of switching.

Charge injection, measured in pico-coulombs, is measured with the aid of the circuit in Figure 6.

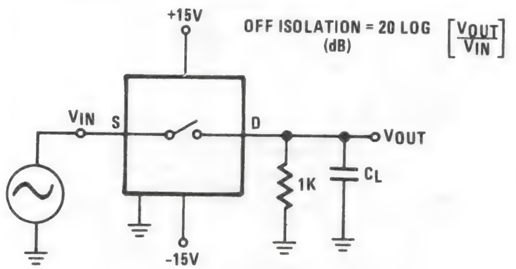


See Table 1 for Specific Test Conditions

FIGURE 6. CHARGE INJECTION TEST CIRCUIT

Off Isolation

Off Isolation is the degree of attenuation seen at the output of an "Open" switch when a high frequency signal is applied to the input. This feedthrough occurs through the source-body and drain-body capacitances and has a greater effect at higher frequencies. Off isolation is usually specified in decibels where Off Isolation = 20Log (V_{OUT}/V_{IN}), see Figure 7. The isolation generally decreases by 10dB/decade with increasing frequency.

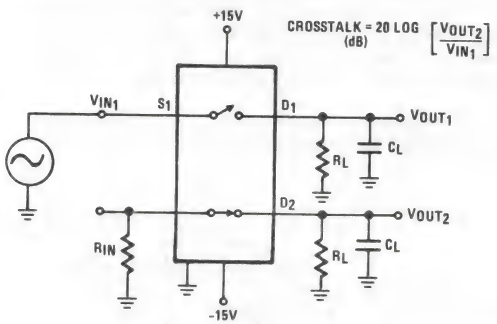


See Table 1 for Specific Test Conditions

FIGURE 7. OFF ISOLATION TEST CIRCUIT

Crosstalk

Crosstalk is the amount of signal cross coupling from an "OFF" analog input to the output of another "ON" channel output. Crosstalk is usually measured in decibles where: Crosstalk = 20Log(V_{OUT2}/V_{OUT1}), see Figure 8.

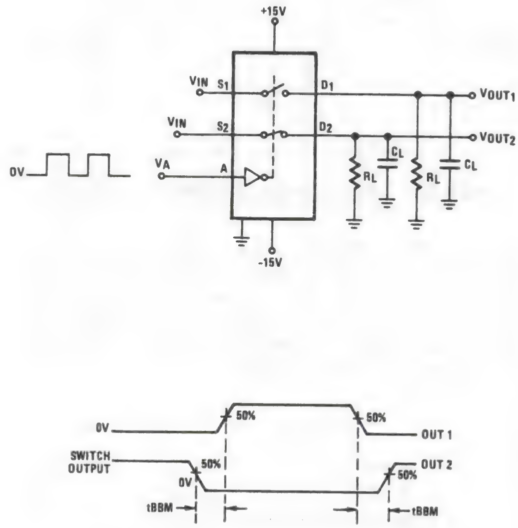


See Table 1 for Specific Test Conditions

FIGURE 8. GENERAL CROSSTALK TEST CIRCUIT

Break-Before-Make-Delay $T_{(OPEN)}$

The break-before-make-delay $T_{(OPEN)}$ is the elapsed time between the "Turn Off" of one switch and the corresponding "Turn On" of another for a common change in logic states (Figure 9). The delay measurement is taken at the 50% levels of the output transitions. The $T_{(OPEN)}$ delay prevents the switches from being simultaneously close during switching transitions.



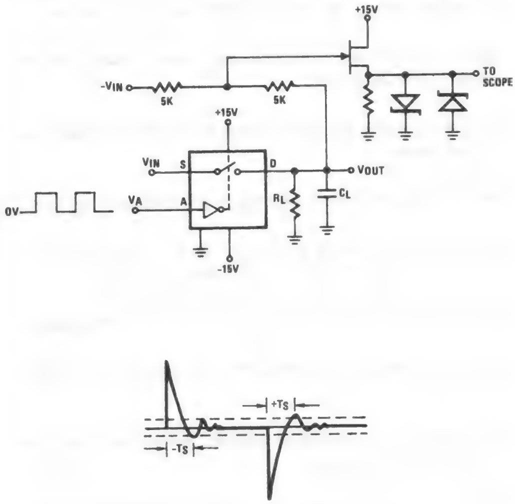
See Table 1 for Specific Test Conditions

FIGURE 9. BREAK-BEFORE-MAKE-DELAY TEST CIRCUIT AND WAVEFORMS

Settling Time

Settling time is the time required for the switch output to settle within a given percentage of the final value following a change in the digital input level. Usually the worst-case settling time occurs when the switch is required to slew across its full dynamic range (generally a 0V to +10V transition). This is known as full-scale settling time.

The settling time circuit is Figure 10, employs two resistors to generate an error voltage equal to the output error. A FET is used to buffer the summing junction from the oscilloscope probe capacitance.



Settling Time (T_S) is measured using a high speed recovery oscilloscope to display the error voltage V_E.

See Table 1 for Specific Test Conditions

FIGURE 10. SETTLING TIME TEST CIRCUIT AND WAVEFORM

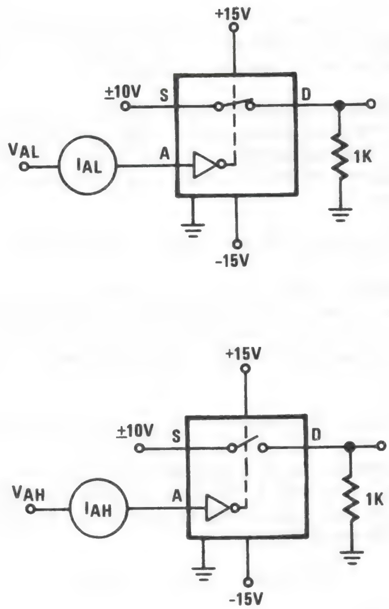
Switch Logic Parameters

Input Thresholds V_{AL} and V_{AH}

The input thresholds are the digital input upper and lower limits at which proper switching action is guaranteed to take place. The input low threshold V_{AL} is the maximum allowable voltage that can be applied to the digital input and still be recognized as a logic low ("0") input. The input high threshold V_{AH} is the minimum allowable voltage that can be applied to the digital input and still be recognized as a logic high ("1") input. All other parameters will be valid if the logic inputs are either below V_{AL} or above V_{AH}.

Input Leakage Current (I_{AL}, I_{AH})

Input leakage current is the bias current flowing either into or out of the digital input terminal. Input leakage current high (I_{AH}) is the current flowing while the digital input is in the high state ($\geq V_{AH}$), while input leakage current low (I_{AL}) is the current flowing when the digital input is in the low state ($\leq V_{AL}$). Input leakage currents are measured directly using the circuits in Figure 11.



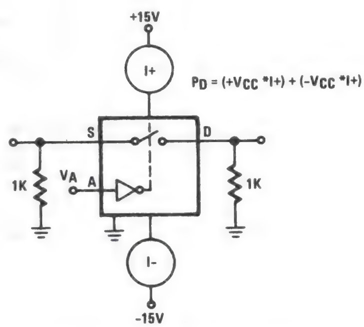
See Table 1 for Specific Test Conditions

FIGURE 11. INPUT LEAKAGE CURRENT TEST CIRCUITS

Static and Package Related Switch Parameters

P_D Power Dissipation: I+, I-

Quiesent power dissipation $P_D = (+V_{CC}*I+) + (-V_{CC}*I-)$ (Figure 12). P_D may be specified with the switch in either a cycling or a steady state condition. Note that, as with all CMOS devices, power dissipation increases with switching frequency.



See Table 1 for Specific Test Conditions

FIGURE 12. SUPPLY CURRENT TEST CIRCUIT

Switch Capacitance $C_{S(OFF)}$, $C_{D(OFF)}$, $C_{D(ON)}$, C_A

The various switch capacitances are stated as typical values. These values are given by design and are not subject to production testing (Figure 13).

Capacitance Source-Off $C_{S(OFF)}$ is the capacitance with respect to ground seen at the analog input with the switch open. This capacitance is the sum of the source capacitance of the N-channel and P-channel switching devices.

$$C_{S(OFF)} = C_{SGP1} + C_{SBP1} + C_{SGN} + C_{SBN}$$

Capacitance Drain-Off $C_{D(OFF)}$ is the capacitance with respect to ground seen at the output terminal with the switch open. This capacitance is the sum of the drain capacitance of the N-channel and P-channel switching devices.

$$C_{D(OFF)} = C_{DGP1} + C_{DBP1} + C_{DGN} + C_{DBN}$$

Capacitance Drain-On $C_{D(ON)}$ is the capacitance with respect to ground at the drain with the switch closed. Generally $C_{D(ON)}$ is the total of the source-off and drain-off capacitances.

$$C_{D(ON)} = C_{D(OFF)} + C_{S(OFF)}$$

Input to output capacitance $C_{DS(OFF)}$ is the capacitance between the analog input and output with the switch open.

Digital input capacitance C_A is the capacitance with respect to ground at the digital input. C_A chiefly affects propagation delays when the switch is driven by CMOS logic.

Switch Test Fixture Design Rules

The high performance characteristics of Harris switches require high quality test fixtures for accurate characterization. The following design rules should eliminate most sources of error and provide highly accurate results.

- Decoupling capacitors should be placed as close to the supply pins as possible.
- A ground plane should be used to minimize distributed capacitance.
- All grounds should terminate at a single point ground.
- All sensitive analog lines should be routed between ground traces and kept away from digital lines.
- Analog and digital lines should cross at right angles.
- All unused logic pins should be connected to either V_{AL} or V_{AH}.
- All unused analog pins should be connected to ground through a 1K resistor.
- Teflon sockets should be used to minimize socket capacitance.

Acknowledgement

This Application Note is the combined result of the work of various laboratory technical staff, most notably Robert C. Junkins.

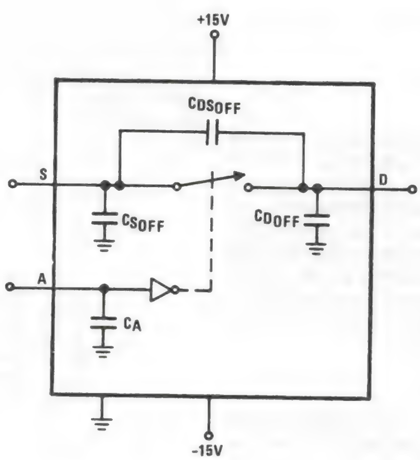


FIGURE 13. EQUIVALENT SWITCH CIRCUIT INCLUDING CAPACITANCES

TABLE 1.

	LOGIC LEVELS	LOGIC REFERENCE	R_{ON}	I_S, I_D	T_{ON}, T_{OFF}	CHARGE INJECTION	CROSSTALK	OFF ISOLATION	SETTLING TIME	BREAK-BEFORE-MAKE	I_{AL}, I_{AH}	POWER DISSIPATION
HI-200	V_{AL} = 0.8V V_{AH} = 2.4V	V_{REF} OPEN	V_{IN} = +10V I_{DS} = 1mA	V_{IN} = +14V	V_{IN} = +10V R_L = 1K C_L = 35pF V_A = 0V, 4V			V_{IN} = 3Vrms f = 100KHz R_L = 1K C_L = 10pF V_A = 5V, 0V		V_{AL} = 0V V_{AH} = 4V	V_{AL}min = 0V V_{AH}max = 5V	V_A = 0V or V_A = 3V
HI-201	V_{AL} = 0.8V V_{AH} = 2.4V	V_{REF} OPEN	V_{IN} = +10V I_{DS} = 1mA	V_{IN} = +14V	V_{IN} = +10V V_A = 0V, 4V			V_{IN} = 3Vrms f = 100KHz R_L = 1K C_L = 10pF V_A = 5V, 0V		V_{AL} = 0V V_{AH} = 4V	V_{AL}min = 0V V_{AH}max = 5V	V_A = 0V or V_A = 3V
HI-201HS	V_{AL} = 0.8V V_{AH} = 3.0V		V_{IN} = +10V I_{DS} = 1mA	V_{IN} = +14V	V_{IN} = +10V R_L = 1K C_L = 35pF V_A = 3V, 0V	C = 1000pF	V_{IN} = 3Vrms f = 100KHz R_L = 1K V_A = 3V, 0V R_{IN} = 1K	V_{IN} = 3Vrms f = 100KHz R_L = 1K C_L = 10pF V_A = 3V, 0V	V_{IN} = +10V R_L = 1K C_L = 35pF V_A = 3V, 0V		V_{AL}min = 0V V_{AH}max = 5V	V_A = 0V or V_A = 3V
HI-300 Thru HI-303	V_{AL} = 0.8V V_{AH} = 4.0V		V_{IN} = +10V I_{DS} = 10mA	V_{IN} = +14V	V_{IN} = +3V R_L = 300 C_L = 33pF V_A = 4V, 0V	C = 10000pF V_A = 5.0V		V_{IN} = 1Vrms f = 500KHz R_L = 1K C_L = 15pF		V_{AL} = 0V V_{AH} = 5V R_L = 300 C_L = 33pF V_{IN} = +3V	V_{AL}min = 0V V_{AH}max = 5V	V_A = 0.8V or V_A = 4.0V
HI-304 Thru HI-307	V_{AL} = 3.5V V_{AH} = 11.0V		V_{IN} = +10V I_{DS} = 10mA	V_{IN} = +14V	V_{IN} = +3V R_L = 300 C_L = 33pF V_A = 15V, 0V	C = 10000pF V_A = 15V		V_{IN} = 1Vrms f = 500KHz R_L = 1K C_L = 15pF		V_{AL} = 0V V_{AH} = 15V R_L = 300 C_L = 33pF V_{IN} = +3V	V_{AL}min = 0V V_{AH}max = 15V	V_A = 0V or V_A = 15V
HI-381 Thru HI-390	V_{AL} = 0.8V V_{AH} = 4.0V		V_{IN} = +10V I_{DS} = 10mA	V_{IN} = +14V	V_{IN} = +3V R_L = 300 C_L = 33pF V_A = 5V, 0V	C = 10000pF V_A = 5.0V		V_{IN} = 1Vrms f = 500KHz R_L = 1K C_L = 15pF		V_{AL} = 0V V_{AH} = 5V R_L = 300 C_L = 33pF V_{IN} = +3V	V_{AL}min = 0V V_{AH}max = 5V	V_A = 0.8V or V_A = 4.0V
HI-5040 Thru HI-5051	V_{AL} = 0.8V V_{AH} = 3.0V	V_L = 5V V_R = 0V	V_{IN} = +10V I_{DS} = 1mA	V_{IN} = +10V	V_{IN} = +10V R_L = 1K	C = 10000pF	V_{IN} = 2Vp-p f = 100KHz R_L = 100 C_L = 5pF R_{IN} = 0	V_{IN} = 2Vp-p f = 100KHz R_L = 100 C_L = 15pF			V_{AL}min = 0V V_{AH}max = 5V	V_A = 0V or V_A = 3.0V

No. 607

Harris Analog

DELTA MODULATION FOR VOICE TRANSMISSION

By Don Jones

Introduction To Deltamod

Delta modulation has evolved into a simple, efficient method of digitizing voice for secure, reliable communications and for voice I/O in data processing.

To illustrate basic principles, a very simple delta modulator and demodulator are illustrated in Figure 1. The modulator is a sampled data system employing a negative feedback loop. A comparator senses whether or not the instantaneous level of the analog voice input is greater or less than the feedback signal. The comparator output is clocked by a flip-flop to form a continuous NRZ digital data stream. This digital data is also integrated and fed back to the comparator. The feedback system is such that the integrator ramps up and down to produce a rough approximation of the input waveform. An identical integrator in the demodulator produces the same waveform, which when filtered, reproduces the voice.

One can see that the digital data 0's and 1's are commands to the integrators to "go up" or "go down" respectively. Another way of looking at it is that the digital data stream also has analog significance; it approximates the differential of the voice, since analog integration of the data reproduces the voice.

Note that the integrator output never stands still; it always travels either up or down by a fixed amount in any clock period. Because of its fixed integrator output slope, the simple delta modulator is less than ideal for encoding human voice which may have a wide dynamic amplitude range.

The integrator cannot track large, high frequency signals with its fixed slope. Fortunately, human speech has statistically smaller amplitudes at higher frequencies, therefore an integrator time constant of about 1 millisecond will satisfactorily reproduce voice in a 3kHz bandwidth.

A more serious limitation is that voice amplitude changes which are less than the height of the integrator ramp during one clock period cannot be resolved. So dynamic range is proportional to clock frequency, and satisfactory range cannot be obtained at desirable low clock rates.

A means of effectively increasing dynamic range is called "companding" (compressing-expanding); where at the modulator, small signals are given higher relative gain, and an inverse characteristic is produced at the demodulator.

The CVSD: A popular effective scheme for companded delta modulation is known as CVSD (continuously variable slope deltamod) shown in Figure 2. Additional digital logic, a second integrator, and an analog multiplier are added to the simple modulator.

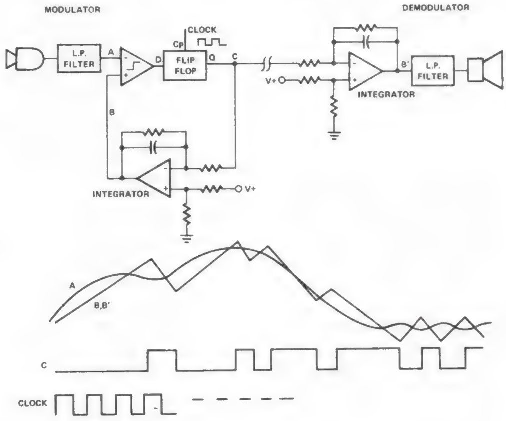
Under small input signal conditions, the second integrator (known as the syllabic filter) has no input, and circuit function is identical to the simple modulator, except that the multiplier is biased to output quite small ramp amplitudes giving good resolution to the small signals.

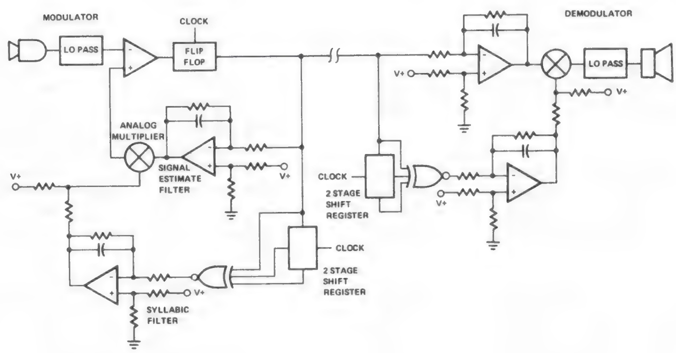
A larger signal input is characterized by consecutive strings of 1's or 0's in the data as the integrator attempts to track the input. The logic input to the syllabic filter actuates whenever 3 or more consecutive 0's or 1's are present in the data. When this happens, the syllabic filter output starts to build up, increasing the multiplier gain, passing larger amplitude ramps to the comparator, enabling the system to track the larger signal. Up to a limit, the more consecutive 1's or 0's generated, the larger the ramp amplitude. Since the larger signals increase the negative feedback of the modulator and the forward gain of the demodulator, companding takes place. By listening tests, the syllabic filter time constant of 4 to 10 milliseconds is generally considered optimum.

An outstanding characteristic of CVSD is its ability, with fairly simple circuitry, to transmit intelligible voice at relatively low data rates. Companded PCM, for telephone quality transmission, requires about 64K bits/sec data rate per channel. CVSD produces equal quality at 32K bits/sec. (However, at this rate it does not handle tone signals or phase encoded modern transmissions as well.)

CVSD is useful at even lower data rates. At 16K bits/sec the reconstructed voice is remarkably natural, but has a slightly "Fuzzy Edge". At 9.6K bits/sec intelligibility is still excellent, although the sound

is reminiscent of a damaged loudspeaker. Of course, very sophisticated speech compression techniques have been used to transmit speech at even lower data rates; but CVSD is an excellent compromise between circuit simplicity and bandwidth economy.





The Digital CVSD

Delta modulated data is in a form which can be digitally filtered with fairly simple circuitry. A compatible CVSD can be made using digital integrators and multipliers driving a digital-to-analog converter. The block diagram of the Harris HC-55564 monolithic CVSD is shown in Figure 3.

The CMOS digital circuit functions of Figure 3 closely parallel the equivalent analog function in Figure 2. The filters are single pole recursive types using shift registers with feedback. A digital multiplier feeds a 10 bit R-2R DAC which reconstructs the voice waveform. The DAC output is in steps, rather than ramps.

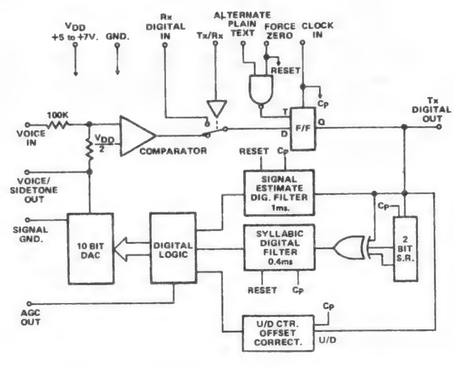


Figure 3 – HC-55564 CVSD Functional Diagram

The digital CVSD has a number of advantages over its analog counterpart, and has desirable features which would otherwise require additional circuitry:

1) The all CMOS device requires only 1mA current from a single +4.5V to +7V supply.

2) No bulky external precision resistors or capacitors are required for the integrators; time constants of the digital filters are set by the clock frequency and do not drift with time or temperature.

3) For best intelligibility and freedom from listener fatigue, it is important that the recovered audio is quiet during the pauses between spoken words. During quiet periods, an alternate "1", "0" pattern should be encoded, which when decoded and filtered will be inaudible. Achieving this in the analog CVSD requires that up and down ramp slopes are precisely equal and that offsets in the comparator and amplifiers are adjusted to zero. Improper adjustment or excessive component drift can result in noisy oscillations. In the digital design, comparator offset and drift are adjusted by a long up-down counter summed to the DAC to insure that over a period of time equal numbers of 1's and 0's are generated.

   An added feature is automatic quieting, where if the DAC input would be less than 2 LSB's the quieting pattern is generated instead. This has proven to aid intelligibility.

4) To prevent momentary overload when beginning to encode or decode, it is desirable to initialize the integrators. In the analog CVSD, external analog switches would be required to discharge the capacitors.

   In the digital CVSD, the filters are reset by momentarily putting the "Force Zero" pin low. At the same time, a quieting pattern is generated without affecting internal encoding by putting the "Alternate Plain Text" pin low.

5) In some analog CVSD designs, transient noise will be generated during recovery from a low frequency overdriven input condition. The digital CVSD has a clipped output with instant recovery, when overdriven.

6) Half-duplex operation (using the same device, switching between the encode and decode functions) requires external circuits with the analog CVSD, while the digital type is switched internally by a logic input.

Applications Of Delta Modulation

1) **Telecommunications:** Digitized signals are easily routed and multiplexed with low cost digital gates. Voice channels may be easily added to existing multiplexed digital data transmission systems. The digital signals are much more immune to crosstalk and noise when transmitted over long distances by wire, R.F., or optical paths. CVSD has better intelligibility than PCM when random bit errors are introduced during transmission.

2) **Secure Communications:** Digital data can be quite securely encrypted using fairly simple standard hardware (Figure 4a). Scrambled speech for audio channels may also be accomplished by encoding into a shift register, then selecting different segments of the shifted data in pseudo-random fashion and decoding it (Figure 4b).

3) **Audio Delay Lines:** Although charge-coupled deviced (CCD) will perform this function, they are still expensive and choice of configurations is quite limited. Also, there is a practical limit to the number of CCD stages, since each introduces a slight degradation to the signal.

   As shown in Figure 5, the delay line consists of a CVSD modulator, a shift register and a demodulator. Delay is proportional to the number of register stages divided by the clock frequency. This can be used in speech scrambling, as explained above, echo supression in PA systems; special echo effects; music enhancement or synthesis; and recursive or nonrecursive filtering.

4) **Voice I/O:** Digitized speech can be entered into a computer for storage, voice identification, or word recognition. Words stored in ROM's, disc memory, etc. can be used for voice output. CVSD, since it can operate at low data rates, is more efficient in storage requirements than PCM or other A to D conversions. Also, the data is in a useful form for filtering or other processing.

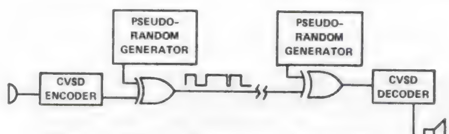


Figure 4a – Digital Transmission Encription

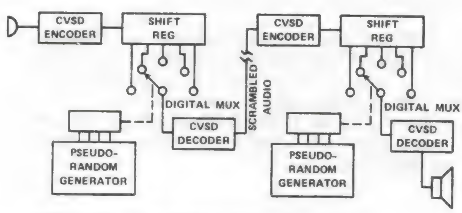


Figure 4b – Voice Transmission Scrambling

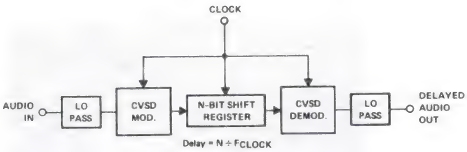


Figure 5 – Audio Delay Line

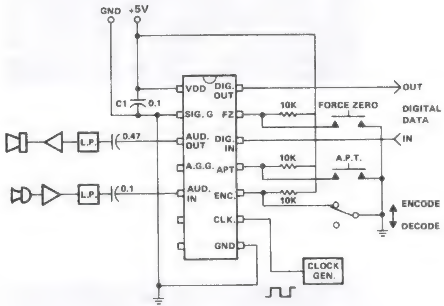


Figure 6 – CVSD Hookup for Evaluation

Figure 6 illustrates a simple evaluation breadboard circuit for the HC-55564. A single device is sufficient to evaluate sound quality, etc. since, when encoding, the feedback signal at pin 3 is identical to the decoded signal from a receiver. The following are some pointers for using the devices:

1) Power supply decoupling is essential with the capacitor (C1 in Figure 6) located close to the I.C.

2) Power to the I.C. must be present before the audio input, the clock, or other digital inputs are applied. Failure to observe this may result in a latchup condition, which is usually not destructive and may be removed by cycling the supply off, then on.

3) Signal ground (pin 2) should be externally connected to pin 8 and power ground. It is recommended for noise-free operation that the audio input and output ground returns connect directly to pin 2 and to no other grounds in the system. Pins 6 and 7 must be open circuited.

4) Digital inputs and outputs are similar to and compatible with standard CMOS logic circuits using the same supply voltage. The illustrated 10K pullup resistors are necessary only with mechanical switches, and are not necessary when driving these pins with CMOS. Unused digital inputs should be tied to the appropriate supply rail for the desired operation. TTL output, however, will require pullup resistors (about 1K) to obtain the required CMOS input levels. Pins 4 and 14 will drive CMOS logic, or each can drive one low power TTL input.

5) Capacitor coupling is recommended for the audio in and out (pins 3 and 5) as each pin is internally biased to about 1/2 the supply voltage.

6) The AGC output (pin 4) is a digital output, whose duty cycle is dependent on the average audio level. This may be externally integrated to drive an AGC preamplifier; or it could be used (through a buffer gate) to drive an LED indicator to indicate proper speaking volume.

7) To prevent generation of alias frequencies, the input filter should reduce the audio amplitude at frequencies greater than half the clock rate to less than 12 millivolts peak-to-peak.

8) The PCM Filter shown in the data sheet lends itself well as a cost-effective input/output filter to the CVSD.

9) A suggested receiver clock circuit is a free running multivibrator, synchronized at each transition of the incoming data. Any synch errors occurring during reception of long strings of zeros or ones will have negligible effect on the decoded voice.

Figures 7 though 11 illustrate some typical audio output (before filtering) and digital output waveforms. To make the scope picture stationary, the audio input generator was synchronized with a submultiple of the clock frequency.

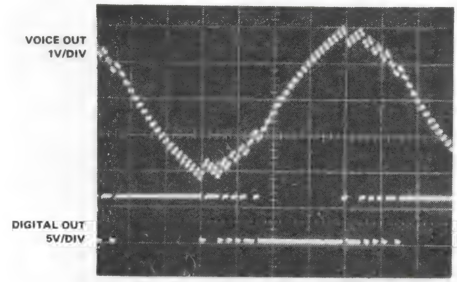
Figure 7 shows the results of a large low frequency sine wave. The somewhat jagged peaks are typical of all CVSD systems. Note that the digital output is continuous "ones" while the waveform is slewing down and continuous "zeros" while slewing up.

Figure 8 shows the excellent recovery from overdriven conditions at low frequency. Some analog type CVSD's have trouble recovering from this condition.

As mentioned previously, CVSD's cannot handle large signals at high frequencies (but these are not generally present in the human voice). Figure 9 shows this limitation where the voice output is slewing at its maximum rate, but cannot catch up with the input. At reduced amplitudes, however, the same signal can be reproduced. as shown in Figure 10.

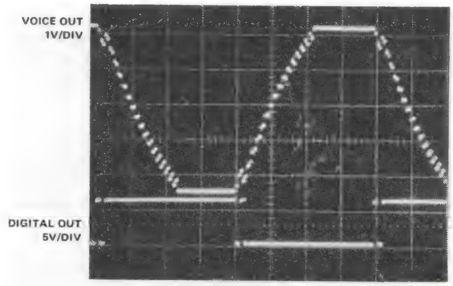
The transfer function curve on the data sheet shows that at 16kHz clock rate, a 1.2V RMS signal can be tracked up to 500Hz. With a 32kHz clock, the same curves may be used but with each of the indicated frequencies doubled. Likewise, each of the SNR figures shown on the data sheet will be 6dB better with a 32kHz clock.

Figure 11 shows the 10 millivolt voice output waveform at 1/2 the clock rate, when there is no audio input. After filtering, this signal is inaudible.



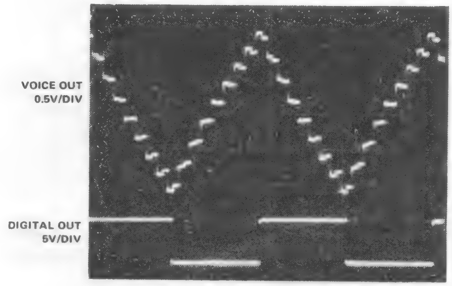
0.5ms/DIV.
VOICE IN = 250Hz, 4V P-P SINE WAVE
CLOCK = 16kHz

Figure 7 — CVSD Large Signal Sine Wave Reconstruction



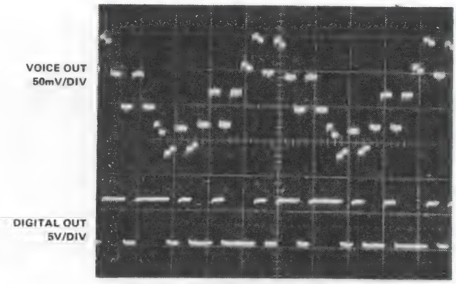
0.5ms/DIV.
VOICE IN = 250Hz, 6V P-P SINE WAVE
CLOCK = 16kHz

Figure 8 — CVSD Large Signal, Low Frequency Clipped Waveform



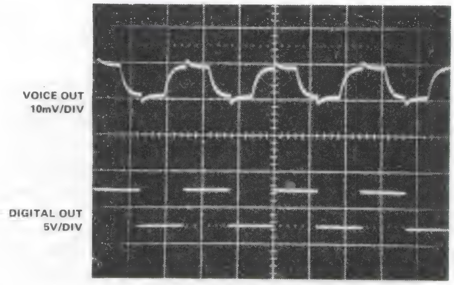
0.2ms/DIV.
VOICE IN = 1kHz, 6V P-P SINE WAVE
CLOCK = 16kHz

Figure 9 — CVSD Large Signal, High Frequency Slew Limiting



0.2ms/DIV.
VOICE IN = 1kHz, 0.15V P-P SINE WAVE
CLOCK = 16kHz

Figure 10 — CVSD Small Signal Sine Wave Reconstruction



50 μs/DIV.
VOICE IN = 0
CLOCK = 16kHz

Figure 11 — CVSD Zero Signal Idle Pattern

ANALOG

Appendices 11

PAGE

CMOS Digital Products

CMOS Microprocessors

80C286 .... Static 16-Bit Microprocessor
80C86 .... Static 16-Bit Microprocessor
80C88 .... Static 8/16-Bit Microprocessor
RTX 2000 .... Static 16-Bit Microntroller

CMOS Peripherals

82C37A .... High Performance Programmable DMA Controller
82C54 .... Programmable Interval Timer
82C55A .... Programmable Peripheral Interface
82C59A .... Priority Interrupt Controller
82C82 .... Octal Latching Bus Driver
82C83H .... Octal Latching Inverting Bus Driver
82C284 .... Clock Generator Driver
82C84A .... Clock Generator Driver
82C85 .... Static Clock Controller/Generator
82C86H .... Octal Bus Transceiver
82C87H .... Octal Bus Transceiver (Inverting)
82C288 .... Bus Controller
82C88 .... Bus Controller
82C89 .... Bus Arbiter

Data Communications

HD-6408 .... Asynchronous Serial Manchester Adapter
HD-6409 .... Manchester Encoder-Decoder
HD-15530 .... Manchester Encoder-Decoder
HD-15531 .... Manchester Encoder-Decoder
HD-4702 .... Programmable Bit Rate Generator
HD-6402 .... Universal Asynchronous Receiver Transmitter
82C50A .... Asynchronous Communications Element
82C52 .... Serial Controller Interval Timer
HD-6406 .... Programmable Asynchronous Communication Interface

CMOS Memory

HM-6504 .... 4K x 1 Synchronous RAM
HM-6508 .... 1K x 1 Sychronous RAM
HM-6514 .... 1K x 4 Synchronous RAM
HM-6516 .... 2K x 8 Synchronous RAM
HM-65162 .... 2K x 8 Asynchronous RAM
HM-6518 .... 1K x 1 Synchronous RAM
HM-65262 .... 16K x 1 Asynchronous RAM
HM-6551 .... 256 x 4 Synchronous RAM
HM-6561 .... 256 x 4 Synchronous RAM
HM-6564 .... 64K Synchronous RAM Module
HM-65642 .... 8K x 8 Asynchronous RAM
HM-6617 .... 2K x 8 Fuse Link PROM
HM-6642 .... 512 x 8 Fuse Link PROM
HM-8808/08A .... 8K x 8 Asynchronous RAM Module
HM-8816H .... 16K 8 Asynchronous RAM Module
HM-8832 .... 32K x 8 Asynchronous RAM Module
HM-92560 .... 256K Synchronous RAM Module
HM-92570 .... 256K Buffered Synchronous RAM Module
HM-91M2 .... 1M-Bit Asynchronous RAM Module

CMOS Multipliers

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HMU-17 .... 16 x 16-Bit Parallel Multiplier
HMU-18 .... 16 x 16-Bit Parallel Multiplier

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HS-6551RH	256 x 4 CMOS Static RAM (Synchronous)	Rad Hard
HS-6504RH	4K x 1 CMOS Static RAM (Synchronous)	Rad Hard
HS-6514RH	1K x 4 CMOS Static RAM (Synchronous)	Rad Hard
HS-65142RH	1K x 4 CMOS Static RAM (Asynchronous)	Rad Hard
HS-65C162RH HS-65T162RH	2K x 8 CMOS Static RAM (Asynchronous)	Rad Hard
HS-65C262RH HS-65T262RH	16K x 1 CMOS Static RAM (Asynchronous)	Rad Hard
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HS-76161RH	2K x 8 Bipolar PROM (Synchronous)	Rad Hard

Quad Power Strobe

HS-6600RH	Quad Power Strobe	Rad Hard

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HS-80C85RH	8-Bit CMOS Microprocessor	Rad Hard
HS-3374RH	CMOS/TTL Bidirectional Level Shifter	Rad Hard
HS-54C138RH	3-Line to 8-Line CMOS Decoder/Demultiplexer	Rad Hard
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HS-82C08RH	8-Bit CMOS Bus Transceiver	Rad Hard
HS-82C12RH	8-Bit CMOS I/O Port	Rad Hard
HS-83C55RH	2K x 8 CMOS ROM with I/O Ports	Rad Hard

80C86 16-BIT MICROPROCESSOR FAMILY

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HS-3560RH	High Speed Latching Comparator	Rad Hard
HS-3761RH	Regulating Pulse Width Modulator	Rad Hard

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HS-508ARH	8 Channel CMOS Analog Multiplexer	Rad Hard
HS-1840RH	16 Channel CMOS Analog Multiplexer	Rad Hard
HS-302/303/306/ 307/384/390RH	CMOS Analog Switches	Rad Hard

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HMF-0301	125mW Power GaAs FET-Packaged
HMF-0302	125mW Power GaAs FET-Flange
HMF-0310	High Gain GaAs FET-Chip
HMF-0314	High Gain Low Noise GaAs FET-Package
HMF-0330	High Gain Low Current GaAs FET
HMF-0600	250mW Power GaAs FET-Chip
HMF-0602	250mW Power GaAs FET-Flange
HMF-0610	High Gain Power GaAs FET-Chip
HMF-0620	High Gain Power GaAs FET-Chip
HMF-1200	500mW Power GaAs FET-Chip
HMF-1202	500mW Power GaAs FET-Flange
HMF-1210	High Gain Power GaAs FET
HMF-2400	1W Power GaAs FET-Chip
HMF-2402	1W Power GaAs FET-Flange

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HMM-10610	2-6 GHz MMIC Amplifier
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HMM-11820	Low Current 6-18 GHz MMIC Amplifier
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- ☐ Telecom (SLIC, Filters, etc.)
- ☐ Voice/Digital-Digital/ Voice Converters
- ☐ Speech

CUSTOM ICs

- ☐ Radiation Hardened
- ☐ Gate Arrays, Rad Hard-Digital Bipolar/CMOS
- ☐ Custom Design, CMOS
- ☐ Custom Design, Digital Bipolar
- ☐ Custom Design, Linear
- ☐ Custom Design, GaAs
- ☐ GaAs Standard Cell

DIGITAL ICs

- ☐ Microprocessors/ Peripherals, CMOS
- ☐ Data Communication Circuits, CMOS
- ☐ Memory, CMOS RAM
- ☐ Memory, High Density Modules
- ☐ Programmable Logic, CMOS
- ☐ Standard Cell, CMOS

MICROWAVE PRODUCTS

- ☐ Microwave GaAs FETs
- ☐ Microwave GaAs ICs
- ☐ GaAs MMICs

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